Aperture Time, Aperture Jitter, Aperture Delay Time—Removing the Confusion

by Walt Kester

INTRODUCTION

Perhaps the most misunderstood and misused ADC and sample-and-hold (or track-and-hold) specifications are those that include the word *aperture*. A simple model is shown in Figure 1, and the most essential dynamic property of a SHA is its ability to disconnect quickly the hold capacitor from the input buffer amplifier. Historically, the short (but non-zero) interval required for this action is called *aperture time (or sampling aperture)*, t_a. The actual value of the voltage that is held at the end of this interval is a function of both the input signal slew rate and the errors introduced by the switching operation itself. Figure 1 shows what happens when the hold command is applied with an input signal of two arbitrary slopes labeled as 1 and 2. For clarity, the sample-to-hold pedestal and switching transients are ignored. The value that is finally held is a delayed version of the input signal, averaged over the aperture time of the switch. The first-order model assumes that the final value of the voltage on the hold capacitor is approximately equal to the average value of the signal applied to the switch over the interval during which the switch changes from a low to high impedance (t_a).

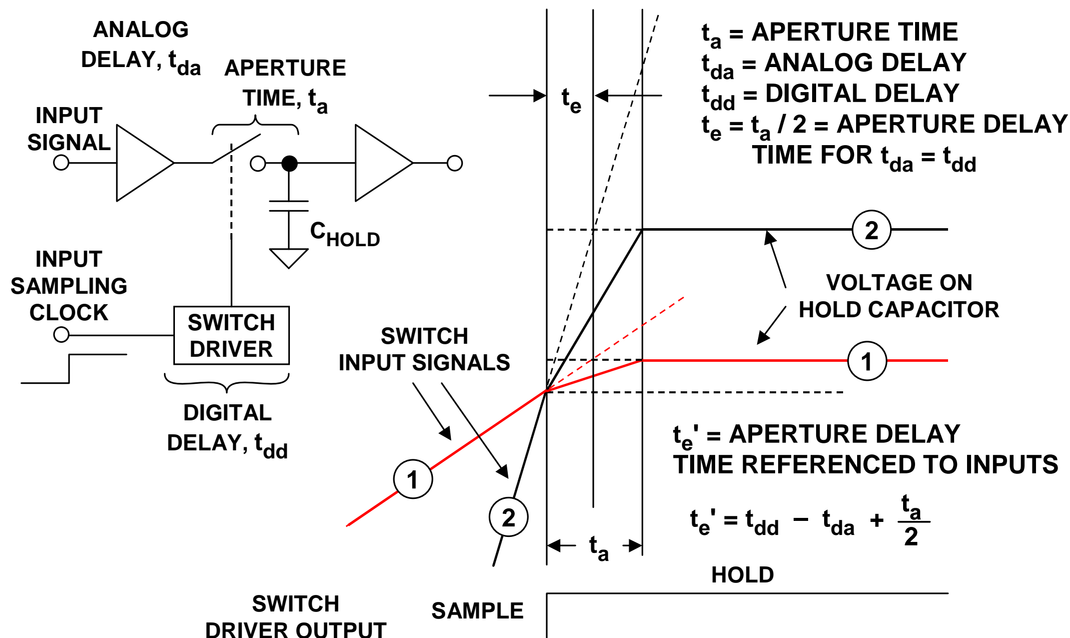


Figure 1: Sample-and-Hold Waveforms and Definitions

The model shows that the finite time required for the switch to open (t_a) is equivalent to introducing a small delay t_e in the sampling clock driving the SHA. This delay is constant, and can be either positive or negative. The diagram shows that the same value of t_e works for the two signals, even though the slopes are different. This delay is called *effective aperture delay time*, *aperture delay time*, or simply *aperture delay*, t_e.

In an ADC, the aperture delay time is referenced to the input of the converter, and the effects of the analog propagation delay through the input buffer, t_{da}, and the digital delay through the switch driver, t_{dd}, must be considered. Referenced to the ADC inputs, aperture time, t_e', is defined as the time difference between the analog propagation delay of the front-end buffer, t_{da}, and the switch driver digital delay, t_{dd}, plus one-half the aperture time, $t_a/2$.

The effective aperture delay time is usually positive, but may be negative if the sum of one-half the aperture time, $t_a/2$, and the switch driver digital delay, t_{dd}, is less than the propagation delay through the input buffer, t_{da}. The aperture delay specification thus establishes when the input signal is actually sampled with respect to the sampling clock edge.

Aperture delay time can be measured by applying a bipolar sinewave signal to the ADC and adjusting the synchronous sampling clock delay such that the output of the ADC is mid-scale (corresponding to the zero-crossing of the sinewave). The relative delay between the input sampling clock edge and the actual zero-crossing of the input sinewave is the aperture delay time as shown in Figure 2.

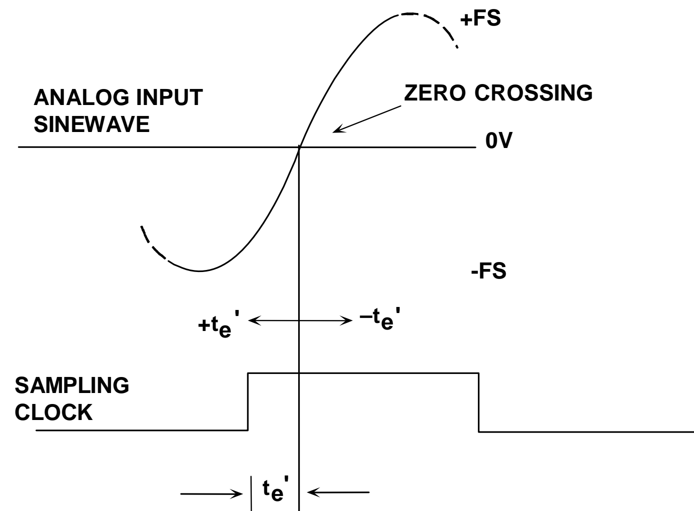


Figure 2: Effective Aperture Delay Time Measured with Respect to ADC Input

Aperture delay produces no errors (assuming it is relatively short with respect to the hold time), but acts as a fixed delay in either the sampling clock input or the analog input (depending on its sign). However, in "interleaved" ADCs, simultaneous sampling applications, or in direct I/Q demodulation, where two or more ADCs must be well matched; variations in the aperture delay between converters can produce errors on fast slewing signals. In these applications, the aperture delay mismatches must be removed by properly adjusting the phases of the individual sampling clocks to the various ADCs.

If, however, there is *sample-to-sample* variation in aperture delay (*aperture jitter*), then a corresponding voltage error is produced as shown in Figure 3. This sample-to-sample variation in the instant the switch opens is called *aperture uncertainty*, or *aperture jitter* and is usually measured in rms picoseconds.

The amplitude of the associated output error is related to the rate-of-change of the analog input. For any given value of aperture jitter, the aperture jitter error increases as the input dv/dt increases. The effects of phase jitter on the external sampling clock (or the analog input for that matter) produce exactly the same type of error. For this reason, the total amount of jitter is the root-sum-square of the external sampling clock jitter and the ADC aperture jitter.

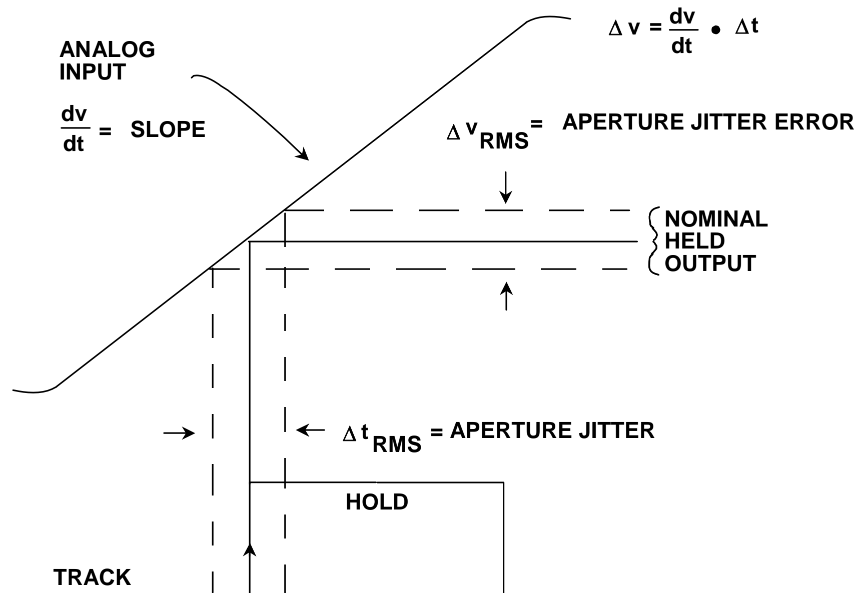


Figure 3: Effects of Aperture Jitter and Sampling Clock Jitter

EFFECT OF APERTURE JITTER AND SAMPLING CLOCK JITTER ON ADC SIGNAL-TO-NOISE RATIO (SNR)

The effects of aperture and sampling clock jitter on an ideal ADCs SNR can be predicted by the following simple analysis. Assume an input signal given by

$$v(t) = V_O \sin 2\pi ft. \qquad \text{Eq. 1}$$

The rate of change of this signal is given by:

$$\frac{dv}{dt} = 2\pi f\ V_O \cos 2\pi ft\ . \qquad \text{Eq. 2}$$

The rms value of dv/dt can be obtained by dividing the amplitude, $2\pi fV_O$, by $\sqrt{2}$:

$$\left.\frac{dv}{dt}\right|_{rms} = \frac{2\pi fV_O}{\sqrt{2}}\ . \qquad \text{Eq. 3}$$

Now let Δv_{rms} = the rms voltage error and Δt = the rms aperture jitter t_j, and substitute these values into Eq. 3:

$$\frac{\Delta v_{rms}}{t_j} = \frac{2\pi fV_O}{\sqrt{2}}\ . \qquad \text{Eq. 4}$$

Solving Eq. 4 for Δv_{rms}:

$$\Delta v_{rms} = \frac{2\pi fV_O t_j}{\sqrt{2}}\ . \qquad \text{Eq. 5}$$

The rms value of the full-scale input sinewave is $V_O/\sqrt{2}$, therefore the rms signal to rms noise ratio (expressed in dB) is given by

$$SNR = 20\log_{10}\left[\frac{V_O/\sqrt{2}}{\Delta v_{rms}}\right] = 20\log_{10}\left[\frac{V_O/\sqrt{2}}{2\pi fV_O t_j/\sqrt{2}}\right] = 20\log_{10}\left[\frac{1}{2\pi f\ t_j}\right]. \qquad \text{Eq. 6}$$

This equation assumes an infinite resolution ADC where aperture jitter is the only factor in determining the SNR. This equation is plotted in Figure 4 and shows the serious effects of aperture and sampling clock jitter on SNR and ENOB, especially at higher input/output frequencies. For instance, in order to achieve 14-bit SNR performance when sampling a 100-MHz IF signal, the aperture jitter must be less than 0.1 ps. ADCs are currently available with typical aperture jitter specifications of 60-fs rms (AD9445 14-bits @ 125 MSPS and AD9446 16-bits @ 100 MSPS). Extreme care must be taken to minimize phase noise in the sampling/reconstruction clock so as not to degrade the inherent performance of the ADC itself.

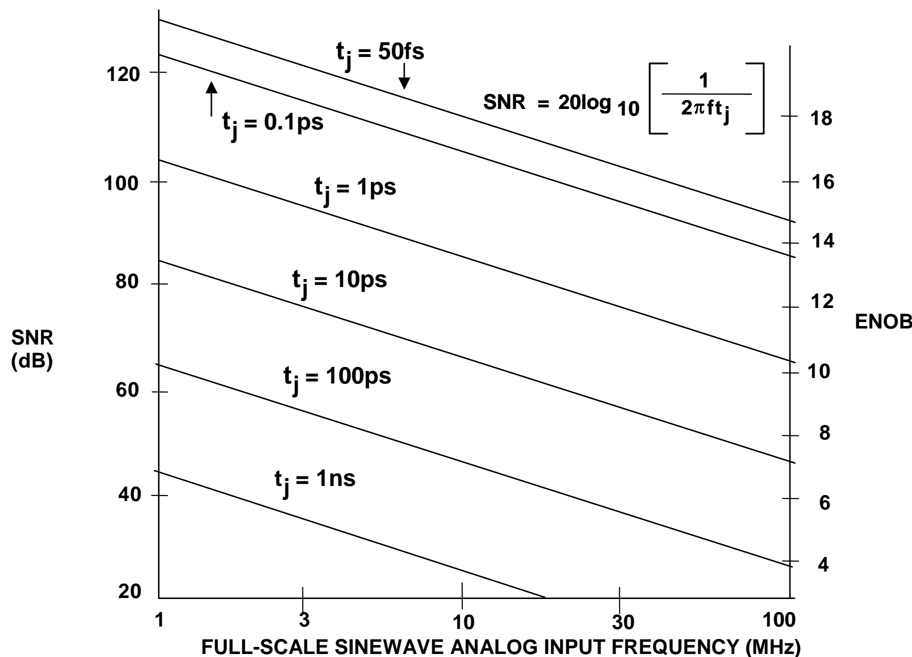


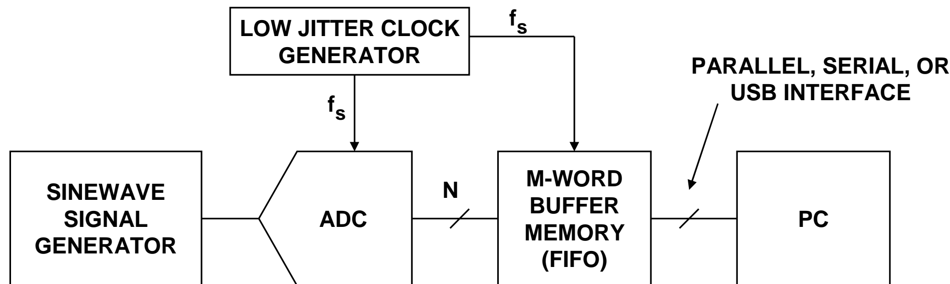
Figure 4: Theoretical Data Converter SNR and ENOB Due to Jitter vs. Fullscale Sinewave Input Frequency

This care must extend to all aspects of the clock signal: the oscillator itself (for example, a 555 timer is absolutely inadequate, but even a quartz crystal oscillator can give problems if it uses an active device which shares a chip with noisy logic); the transmission path (these clocks are very vulnerable to interference of all sorts), and phase noise introduced in the ADC or DAC. As discussed, a very common source of phase noise in converter circuitry is aperture jitter in the integral sample-and-hold (SHA) circuitry, however the total rms jitter will be composed of a number of components—the actual SHA aperture jitter often being the least of them.

Before the 1980s, most sampling ADCs were generally built from a separate SHA and ADC. Interface design was complex, and accurately predicting the performance of the combination was difficult. Today, almost all sampled data systems use *sampling* ADCs which contain an integral SHA. The aperture jitter of the SHA may not be specified as such, but this is not a cause of concern if the SNR or ENOB is clearly specified over frequency, since a guarantee of a specific SNR at a specific input frequency is an implicit guarantee of an adequate aperture jitter specification.

MEASURING ADC APERTURE JITTER USING FFT TECHNIQUES

The FFT test routine for measuring ADC SNR, SFDR, etc., is an excellent indirect method for measuring aperture jitter. The caveat in this test is that the measurement includes the jitter of the sampling clock generator as well as the ADC internal aperture jitter. Therefore, a generator should be selected with an rms jitter specification which is several times less than the specified aperture jitter of the ADC under test, since individual jitter components combine on an rss basis. The basic test setup for the aperture jitter test is shown in Figure 5 along with the key calculations.



- SNR FOR LOW FREQUENCY FS INPUT = SNRL
- SNR FOR HIGH FREQUENCY FS INPUT = SNRH (FREQUENCY = f)
- $\text{SNRA} = 20\log_{10}\left[\frac{1}{2\pi f t_a}\right]$
- $t_a = \frac{1}{2\pi f}\sqrt{\left[10^{-\text{SNRH}/20}\right]^2 - \left[10^{-\text{SNRL}/20}\right]^2}$
- INCLUDES JITTER OF CLOCK GENERATOR

Figure 5: Measuring Aperture Jitter Based on Degradation in SNR at High Frequencies

There are two SNR measurements required, and both utilize a full-scale input sinewave having a frequency f_L and f_H. The first measurement, SNRL, is made at a relatively low frequency, f_L, where the noise is primarily the combination of the ADC input-referred noise and the quantization noise. It should be possible to vary the low input frequency quite a bit and still measure the same SNR value. The sampling frequency is generally set for the maximum allowable. The second measurement, SNRH, is made using a high frequency input, f_H, where the effects of aperture jitter on the ADC SNR are noticeable. Depending on the ADC, this frequency may be as high as $f_s/2$. We have shown that relationship between the signal-to-noise ratio due to aperture jitter alone is given by:

$$\text{SNRA} = 20\log_{10}\left[\frac{1}{2\pi f_H t_a}\right], \qquad \text{Eq. 7}$$

where SNRA is the SNR (dB) due to aperture jitter, and f_H is the input frequency.

Solving for t_a:

$$t_a = \frac{1}{2\pi f_H} \cdot \frac{1}{10^{SNRA/20}} . \qquad \text{Eq. 8}$$

The next step is to calculate SNRA based on SNRH and SNRL. Since the SNRs are in dB, they must first be converted to ratios, and their reciprocals can then be combined on an rss basis:

$$\left(\frac{1}{10^{SNRH/20}}\right)^2 = \left(\frac{1}{10^{SNRL/20}}\right)^2 + \left(\frac{1}{10^{SNRA/20}}\right)^2 . \qquad \text{Eq. 9}$$

Re-arranging Eq. 9:

$$\left(\frac{1}{10^{SNRA/20}}\right) = \sqrt{\left(\frac{1}{10^{SNRH/20}}\right)^2 - \left(\frac{1}{10^{SNRL/20}}\right)^2} . \qquad \text{Eq. 10}$$

Substituting Eq. 10 into Eq. 8:

$$t_a = \frac{1}{2\pi f_H} \cdot \sqrt{\left(\frac{1}{10^{SNRH/20}}\right)^2 - \left(\frac{1}{10^{SNRL/20}}\right)^2} . \qquad \text{Eq. 11}$$

SUMMARY

It should be emphasized that all the measurements required for this test use SNR and not SINAD (signal-to-noise and distortion). It is extremely important that the 2nd, 3rd, 4th, 5th, and 6th harmonics (as well as the dc components) be removed when making the SNR calculation from the FFT output. Otherwise, the measurement will not give an accurate measure of aperture jitter.

As a final note, measuring rms aperture jitter less than 10-ps rms is extremely difficult, simply because of unwanted jitter which may occur on the input signal or the ADC sampling clock, or layout-induced jitter and noise. Obtaining this level of accuracy requires frequency synthesizers with extremely low jitter, as well as detailed attention to layout, signal routing, grounding, and decoupling.

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