ANALOG DEVICES

Applications Engineering Notebook

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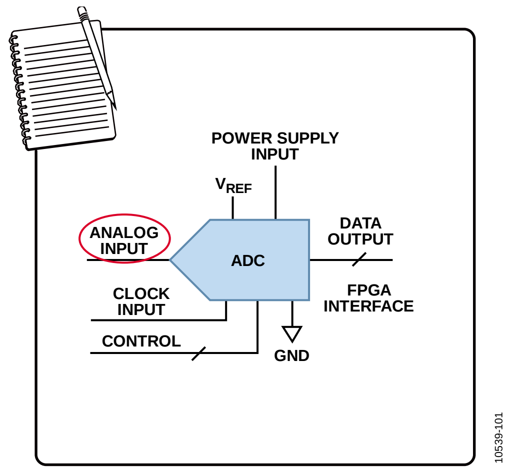
High Speed ADC Analog Input Interface Considerations

by the Applications Engineering Group
Analog Devices, Inc.

IN THIS NOTEBOOK

Since designing a system that uses a high speed analog-to-digital converter (ADC) is challenging, this notebook provides an overview of the basic design considerations.



The Applications Engineering Notebook Educational Series

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REVISION HISTORY

4/12—Rev. 0 to Rev. A

Changes to Figure 26 14

2/12—Revision 0: Initial Version

BASIC INPUT INTERFACE CONSIDERATIONS

Designing a system that uses high speed analog-to-digital converters (ADCs) with high input frequencies can be a challenging task. The six main criteria for ADC input interface design are the input impedance, input drive, bandwidth, pass-band flatness, noise, and distortion.

INPUT IMPEDANCE

Input impedance is the characteristic impedance of the design. The ADC's internal input impedance depends upon the type of ADC architecture; it is provided by the ADC vendor in the data sheet or on the product page. The voltage standing wave ratio (VWSR), which is closely related to the input impedance, measures the amount of power that is reflected into the load over the bandwidth of interest. It is important because it sets the input drive level required to achieve the ADC's full-scale input. Maximum power transfer occurs when the source impedance is equal to the load impedance.

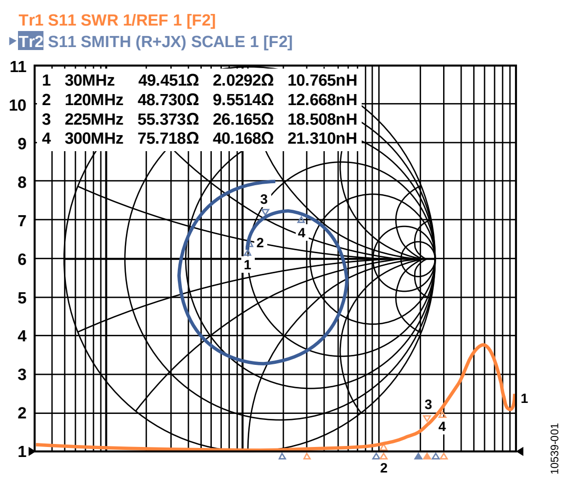

Figure 1. Input Z/VWSR on a Network Analyzer

Figure 1 shows an example plot of input impedance and VSWR taken from a front-end network using a network analyzer. Input impedance is the characteristic impedance of the design. In most cases, it is 50 Ω; however, a design can require a different impedance.

VSWR is a unitless parameter that can be used to understand how much power is being reflected into the load over the bandwidth of interest. It is important because it sets the input drive level required to achieve the ADC's full-scale input. Note that, as frequency is increased, driving the ADC input to full scale requires more drive power or gain.

INPUT DRIVE

Input drive is a function of the bandwidth specification and sets the system gain needed for a particular application. The input drive level should be established before the front-end design is started and depends on the front-end components chosen, such as the filter, transformer, and amplifier.

BANDWIDTH AND PASS-BAND FLATNESS

Bandwidth is the range of frequencies to be used in the system. Pass-band flatness is the amount of fluctuation within a specified bandwidth. This fluctuation could be due to ripple effects or simply a slow roll-off characteristic of a Butterworth filter. Pass-band flatness is usually less than 1 dB and is critical for setting the overall system gain.

NOISE

Signal-to-noise ratio (SNR) and distortion requirements are usually established early in the design process since they help determine the ADC selection. The amount of noise the converter sees relative to its own noise is defined as the SNR. SNR is a function of the bandwidth, signal quality (jitter), and gain. Increasing the gain increases the noise components that are associated with it as well.

DISTORTION

Distortion is measured by the spurious-free dynamic range (SFDR), the ratio of the rms full scale to the rms value of the peak spurious spectral component. SFDR is controlled primarily by two factors. The first factor is the linearity of the front-end balance quality, which is primarily a function of the second harmonic distortion. The second is the gain and the input match required. A higher gain requirement increases matching difficulty. A higher gain requirement also increases nonlinearity by pushing the headroom of the devices inside the ADC as well as nonlinearity from the external passives as more power runs through them. This effect is generally seen as a third harmonic.

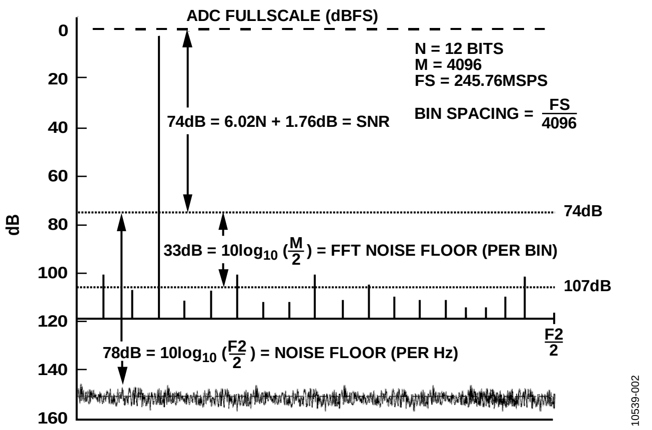

Figure 2. Noise Floor for an Ideal 12-Bit ADC Using 4096-Point FFT

Figure 2 shows the output of a 4096-point FFT for an ideal 12-bit ADC and some of its basic computations. The theoretical SNR is 74 dB. This noise is spread over the entire Nyquist bandwidth. The FFT adds process gain because it looks at small "bins" which have a width equal to the sampling frequency divided by the number of points in the FFT. In the case of a 4096-point FFT, the process gain is 33 dB. This works like narrowing the bandwidth of an analog spectrum analyzer.

The actual FFT noise floor is equal to the SNR plus the process gain as shown in Figure 2. The FFT noise floor for the conditions above is equal to 74 + 33 = 107 dBFS. In some systems, the results of several individual FFTs are averaged. This does not lower the FFT noise floor, but simply reduces the variations in the amplitudes of the noise components.

TYPES OF INPUT ARCHITECTURE

There are two types of ADC architectures to choose from, buffered and unbuffered.

CHARACTERISTICS OF BUFFERED AND UNBUFFERED ARCHITECTURE

The basic characteristics of the buffered architecture are

- Highly linear buffer, but requires more power
- Easier to design input network to interface high impedance buffer since it provides a fixed input termination resistance
- Buffer provides isolation between sample capacitors and input network resulting in reduced charge injection transients

The basic characteristics of the unbuffered architecture are

- Input impedance set by switched-capacitor design
- Lower power
- Input impedance varies over time (sample clock – track and hold)
- Charge injection from sample capacitors reflects back onto input network

UNBUFFERED ADCS

The switched capacitor ADC (see Figure 3) is one type of unbuffered ADC. Unbuffered ADCs usually dissipate much less power than buffered ADCs because the external front-end design connects directly to the internal sample-and-hold (SHA) network of the ADC.

There are two drawbacks associated with this approach. The first is that the input impedance is time and mode varying. The second is a charge injection that reflects back onto ADC's analog inputs, which may cause filter settling issues.

The input impedance for an unbuffered ADC changes as the analog input frequency changes, and as the SHA changes from sample mode to hold mode. The goal is to match the input to the ADC sample mode, as shown in Figure 4.

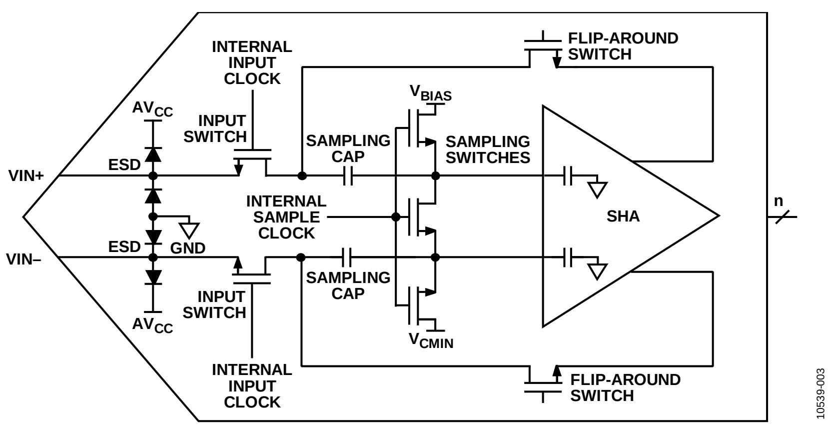

Figure 3. Switched Capacitor ADC

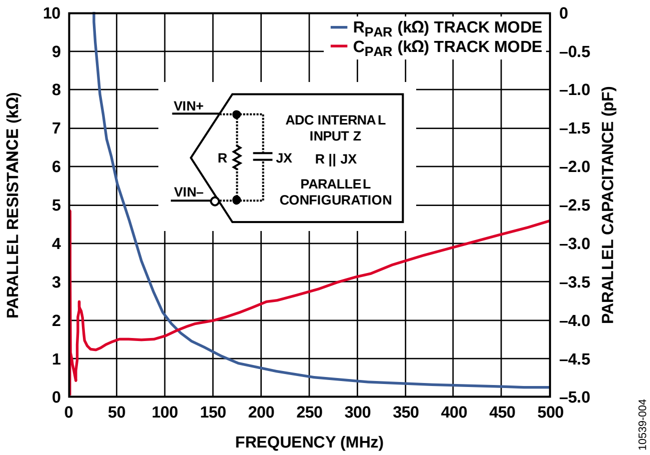

Figure 4. Input Impedance as a Function of Mode and Frequency

The real part of the input impedance (blue line) is in the several kilohms range at lower frequencies in the baseband range and rolls off to less than 2 kΩ above 200 MHz. The imaginary or capacitive part of the input impedance (red line) starts out as a fairly high capacitive load and tapers off to 2 pF at high frequencies. This makes the input structure more challenging to design, especially at frequencies greater than 100 MHz.

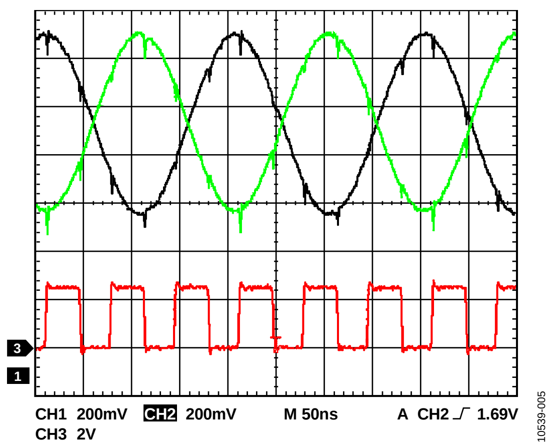

Figure 5. Typical Single-Ended Input Transients

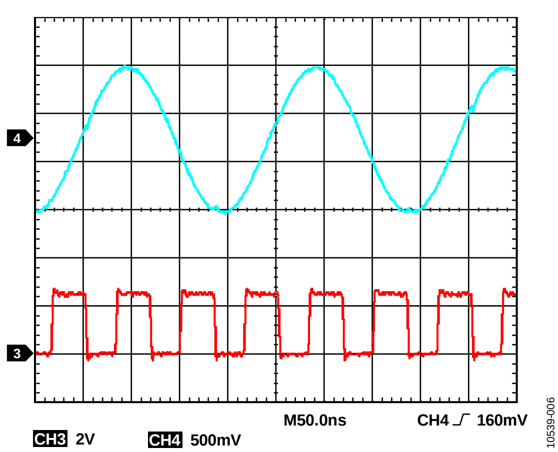

Figure 6. Typical Differential Input Transients

How can an ADC sample a corrupted signal, such as the one shown in Figure 5, and achieve good performance? Looking at the ADC inputs differentially in Figure 6, the input signal appears much cleaner. The corrupt signal glitches are gone. Common-mode rejection is inherent in differential signaling. This cancels out any noise, whether it is from the supply, digital injection, or charge injection.

Another way to view the unbuffered ADC's glitches is in the time domain using a spectrum analyzer to measure the noise coming back onto the analog inputs. This illustrates the effect of the switched capacitor ADC structure on the analog inputs.

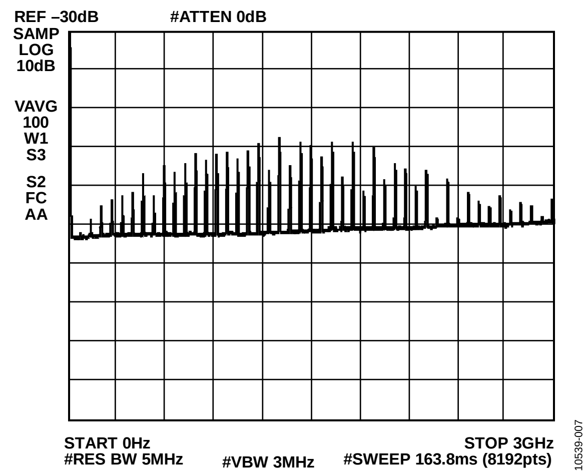

Figure 7. Spectrum Analyzer Measurement at the Analog Inputs with No Input Match Applied

Figure 7 shows that harmonics, noise, and other spurious content of the clock feed through in the spectrum above 3 GHz.

Matching the ADC input to reduce the clock feedthrough typically improves most of the harmonics by more than 10 dB.

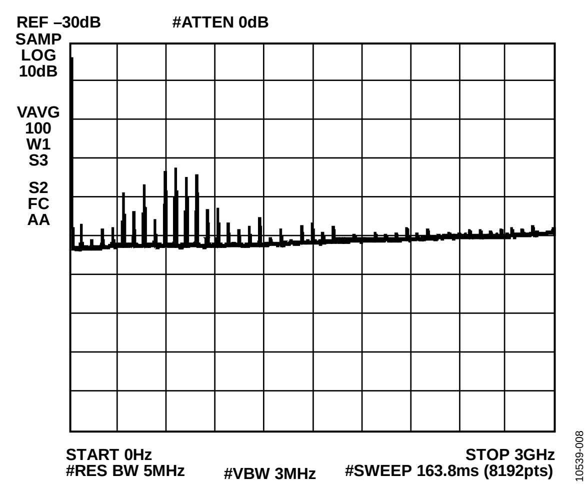

Figure 8. Spectrum Analyzer Measurement at the Analog Input with an Input Match Applied using a Low-Q Inductors or Ferrite Beads

This was accomplished in Figure 8 by adding a low-Q inductor or ferrite bead in series with each leg on the analog input. This is one way to reduce the amount of noise coming onto the analog input when needed.

BUFFERED ADCS

The buffered input ADC (see Figure 9) is simpler to use because the input impedance is fixed. Switching transients are significantly reduced due to an isolation buffer that suppresses the charge injection spikes. The buffer is made up of an internal bipolar junction transistor stage, which has a fixed input termination.

Unlike switched capacitor ADCs, this termination does not vary with the analog input frequency and selection of the proper drive circuit is therefore simplified. The downside of the buffered input stage is that the ADC dissipates more power. However, since it is specifically designed to be very linear and have low noise, the constant input impedance is over the entire specified bandwidth of the ADC.

When designing an antialiasing filter (AAF), keep in mind that too many components can cause mismatch tolerance, which in turn leads to even-order distortions. All inductors are not created equally—they can respond very differently. Inexpensive, low quality inductors usually do not work well. In addition, it is sometimes difficult to get a good solder connection on an inductor, resulting in distortion. Make sure the stop-band region in an AAF is specified as flat because broadband noise can still fold back in-band (see Figure 10).

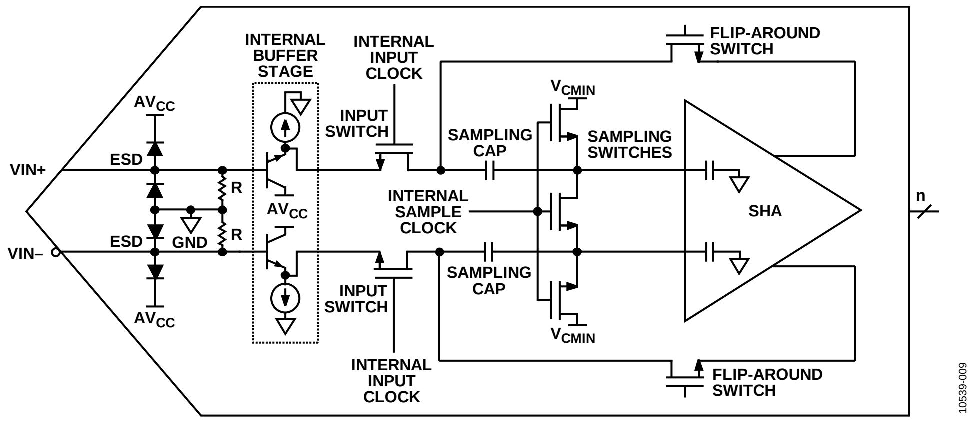

Figure 9. Buffered Input ADC

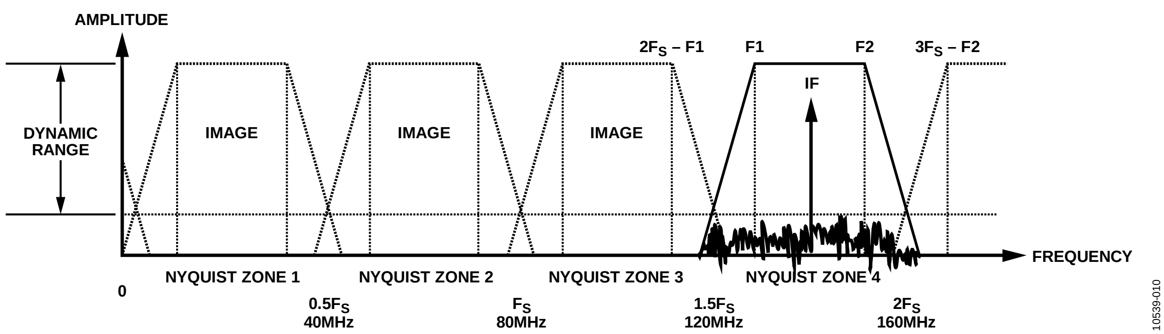

Figure 10. Antialiasing Filter

Most converters have wide analog input bandwidths. Dynamic range is degraded due to aliasing if no AAF is used. The AAF should be designed to match or slightly exceed the target signal bandwidth. The order and type of filter designed depends on desired stop-band rejection and pass-band ripple. The AAF should have sufficient stop-band rejection over the entire ADC's bandwidth.

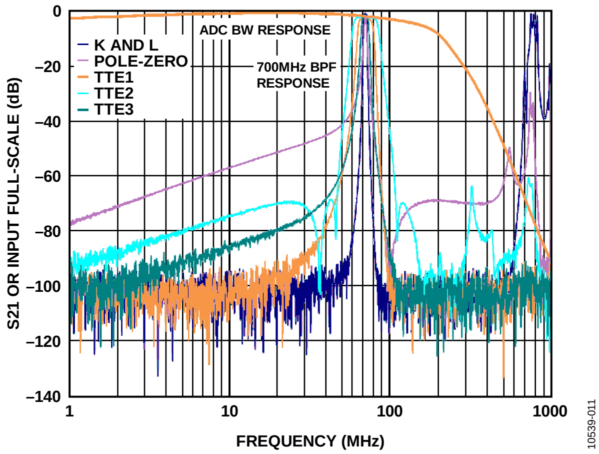

Figure 11. AAF Response vs. ADC Bandwidth Response

Figure 11 illustrates the importance of stop-band rejection in an AAF design. Note that the converter bandwidth, indicated by the red curve, is much larger than the frequency band to be sampled. Noise and spurs can fold back into the in-band frequencies being sampled because of this. Note the light blue and pink curves where the filter response comes up into the stop-band rejection region. Also, note the dark green or orange curves where the stop-band rejection is held constant throughout.

TRANSFORMER-COUPLED FRONT ENDS

As a rule, transformer-coupled front ends drive higher intermediate frequencies without significant loss, have wider bandwidths, consume less power, and provide inherent ac coupling. Multiturn ratio transformers also provide noise-free gain. On the other hand, designing transformer-coupled front ends with higher impedance/turn ratios can be difficult because they result in less bandwidth, degraded amplitude, phase imbalance, and sometimes degraded pass-band ripple.

When transformers are used in ADC front ends, keep in mind that no two transformers are created equal—even if their data sheets look the same. For example, a 1:1 impedance ratio does not mean that the secondary termination is 50 Ω. Either use the return loss from the data sheet or measure it using an ENA. The bandwidth on a transformer data sheet should typically be cut in half because transformers are usually measured under ideal conditions using PCB extraction techniques. Transformers with a gain greater than 1:1 Z ratio have an even lower bandwidth and are more difficult to work with. At frequencies above 150 MHz, HD2 begins to rise due to the inherent phase imbalance of the transformer. To address this issue, use two transformers or use a better one.

MODELING TRANSFORMERS

Modeling transformers can be difficult. Transformers have many different characteristics, such as voltage gain and impedance ratio, bandwidth and insertion loss, magnitude and phase imbalance, and return loss. Transformer characteristics change as the frequency changes.

An example of a starting point in modeling a transformer for ADC applications is shown in Figure 13. However, each of the parameters changes depending on the transformer chosen. In addition, while transformer models provide a good understanding of bandwidth and impedance over frequency, there is really no good way to measure linearity other than testing the transformer in the system itself.

TRANSFORMER BASICS

The turns ratio, current ratio, impedance ratio, and signal gain are all characteristics of a transformer.

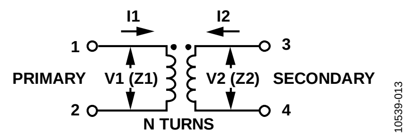

Figure 12. Transformer Basics

The turns ratio *n* defines the ratio of the primary to the secondary voltages.

Turns ratio

$n = N1/N2$

The impedance ratio is the square of the turns ratio.

Impedance ratio

$n^2 = Z1/Z2$

The current ratio is inversely related to the turns ratio.

The signal gain is related to the impedance ratio.

$20 \log (V2/V1) = 10 \log (Z2/Z1)$

A transformer with a voltage gain of 3 dB would have a 1:2 impedance ratio. This is good since data converters are voltage devices. Voltage gain is noise-free!

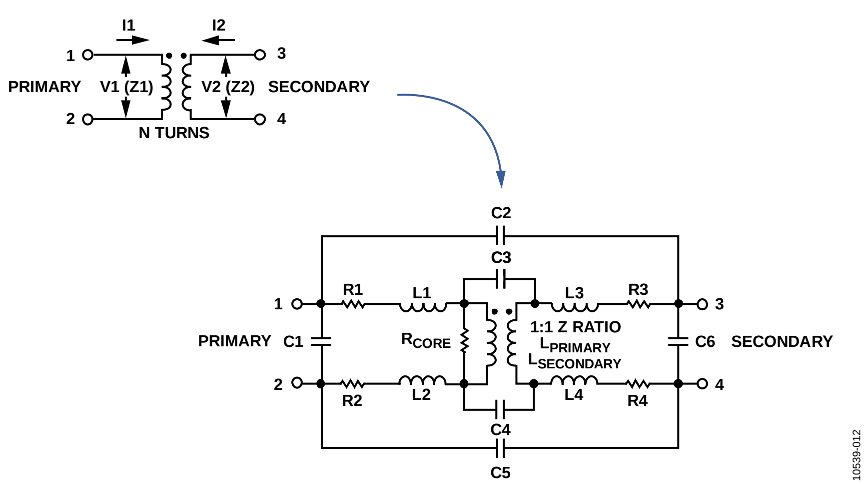

Figure 13. Modeling Transformers

UNDERSTANDING TRANSFORMER PERFORMANCE

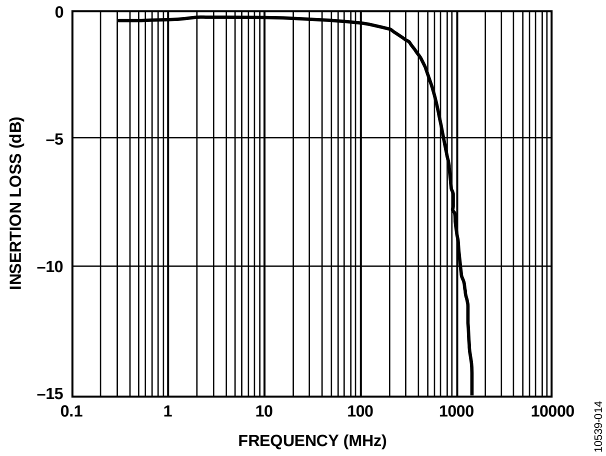

Figure 14. Insertion Loss vs. Frequency

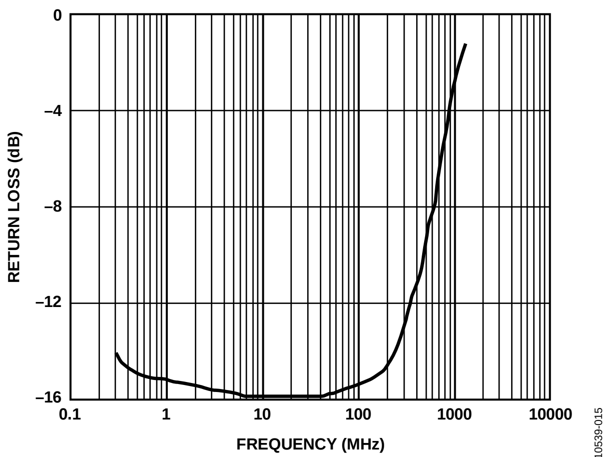

Figure 15. Return Loss vs. Frequency

A transformer can be viewed simplistically as a pass-band filter. This characteristic allows you to determine the loss of the transformer over a specified frequency.

The insertion loss is the most common measurement specification found in a data sheet, but it is not the only consideration.

Return loss is the effective impedance as seen by the primary when the secondary is terminated. For example, if you have an ideal 1:2 impedance transformer, you would expect a 50 Ω impedance reflected onto the primary when the secondary is terminated with 100 Ω. However, this is not always true. The reflected impedance on the primary is dependent on the frequency. In general, as the impedance ratio goes up, so does the variability of the return loss.

AMPLITUDE AND PHASE IMBALANCE

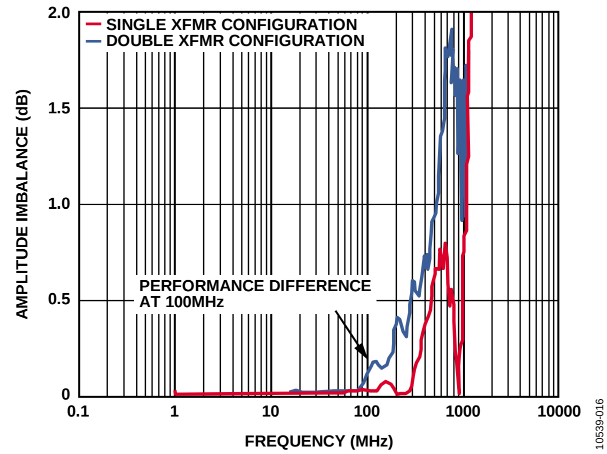

Figure 16. Amplitude Imbalance vs. Frequency

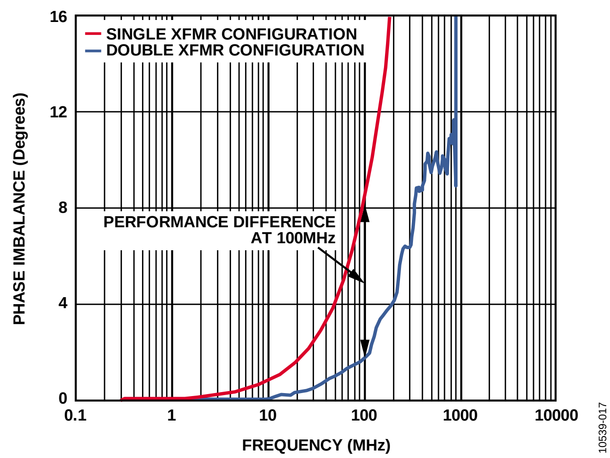

Figure 17. Phase Imbalance vs. Frequency

Amplitude and phase imbalance are critical performance characteristics when using a transformer. These two specifications give the designer a perspective on how much nonlinearity to expect when a design requires very high IF frequencies above 100 MHz. As the frequency increases, the nonlinearity of the transformer also increases. Phase imbalance usually dominates, which translates to even-order distortions, or increased second harmonics. The red curves show a single transformer and the blue curves show a double transformer configuration.

The best way to select a transformer for your design is to collect all of the specifications described in this notebook. Most manufacturers have this data available, even it is not specifically stated on their data sheets. Alternatively, you can measure transformer performance using a network analyzer.

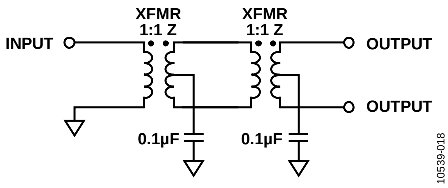

Figure 18. Two Transformer Configuration

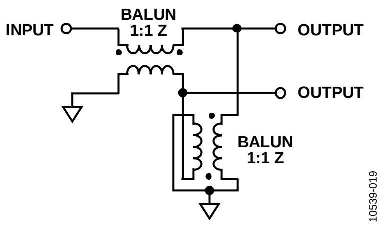

Figure 19. Two Balun Configuration

By adding a second transformer, the first transformer's core current is redistributed in an effort to rebalance the parasitic capacitance that couples across the primary and secondary. This minimizes the phase imbalance presented to the ADC, which looks like second-order harmonic distortion.

A double transformer configuration is generally used in high frequency applications when the input frequencies are above 100 MHz. Depending on the input frequency, one may want to consider using a double balun configuration since balun transformers are generally specified for much higher bandwidths. An alternative to using a double transformer configuration is to choose a better performing transformer.

ACTIVE-COUPLED FRONT-END NETWORKS

Most active-coupled front-end networks use an amplifier.

Consider the following when selecting an amplifier for both ac and dc coupled applications:

- Common-mode issues, working down at 1 VCM
- Supply issues, (What is the input range? What is the output range?)
- Some amps only can be used for ac coupling
- Put series R's on the outputs to keep the amplifier stable (5 Ω to 10 Ω)
- Follow the layout guidelines for the data sheet: remove ground on the second layer to keep the output C low and also to avoid oscillations
- Follow data sheet recommended output load. Sometimes this load value is a fixed resistor, not a product of the network impedance.
- For current feedback amps, it very important to read the data sheets. The recommended feedback resistor is specified in the data sheet. This value determines the stability of the amplifier.

DIFFERENTIAL SIGNALING EXAMPLE

The example in Figure 20 provides an overall view of differential signaling. A common question is: how can a 1.8 V ADC sample a 2 V p-p sine wave signal? The example shows how this can be accomplished through differential signaling. Note the importance of the common-mode voltage (CMV) of the converter's analog inputs. In order to sample the signal correctly and accurately, the CMV must be present and robust.

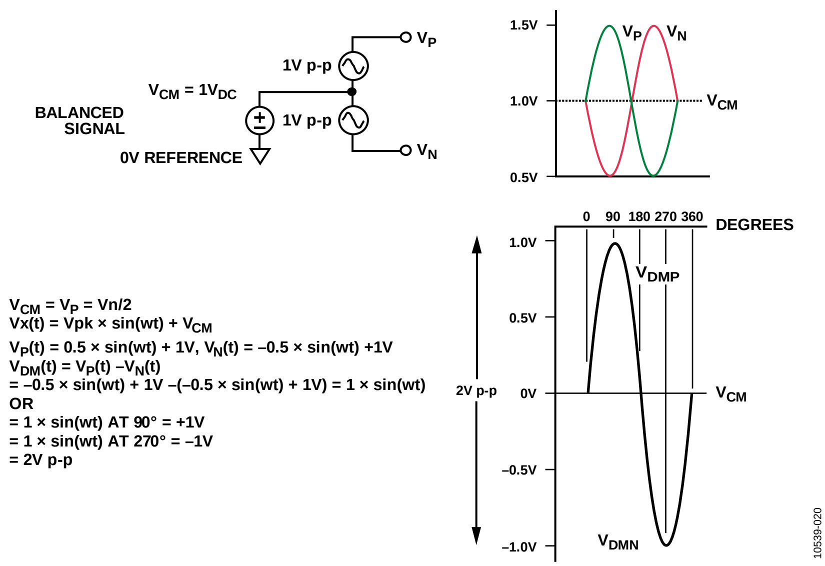

Figure 20. Example of Differential and Common-Mode Signals

FREQUENCY AND TIME DOMAIN PERFORMANCE EXAMPLES

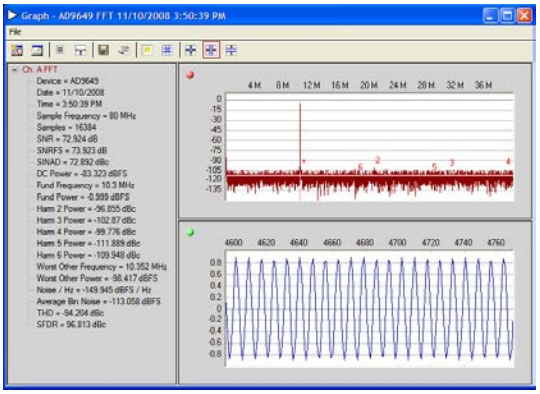

Figure 21. AD9649 FFT/TD Typical Performance

Figure 21 shows a typical example of frequency and time domain performance when the correct input signal is applied. Note the flat noise floor and good SNR and SFDR performance.

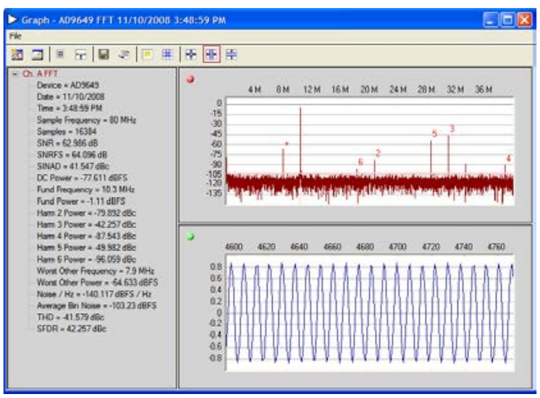

Figure 22. AD9649 FFT/TD with Common-Mode Voltage on Both Analog Inputs Unbiased/Floating

When the correct signal amplitude is applied, but the common-mode voltage is floating at the ADC's analog input pins, distortion can occur. Note the difference in SNR and SFDR performance in Figure 22 as well as Figure 21. The input signal is floating around its 1 V signal swing, clipping either in a positive or negative manner.

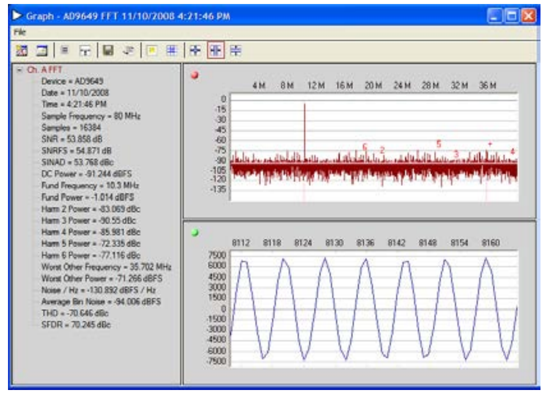

Figure 23. AD9649 FFT with Common-Mode Voltage on Both Analog Inputs Too High (>+0.9 V)

When the correct signal amplitude is applied, but the common-mode voltage is too high for the ADCs analog input pins (in this case >0.9 V), distortion can occur. Note the difference in SNR and SFDR performance in Figure 23 compared to the baseline performance seen in Figure 21. Even though the input signal is fine, the CMV is above where is should be, forcing the signal to clip in either a positive or negative manner.

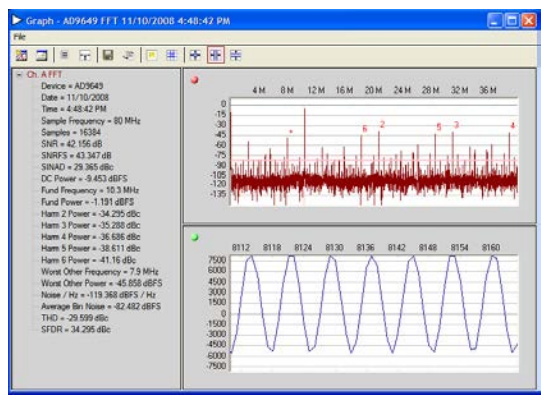

Figure 24. AD9649 FFT with Common-Mode Voltage on Both Analog Inputs Mismatched

In Figure 24, the correct signal amplitude is applied, but both the common-mode voltages are mismatched for ADC's analog input pins (in this case, both are not 0.9 V), resulting in distortion and offset. Note the difference in SNR and SFDR performance compared to the baseline performance in Figure 21. In this case, the CMVs are above or below their nominal values, forcing the signal to clip in either a positive or negative manner. Also, notice how the signal is offset rather than centered in the time domain plot.

ANTIALIASING FILTER CONSIDERATIONS

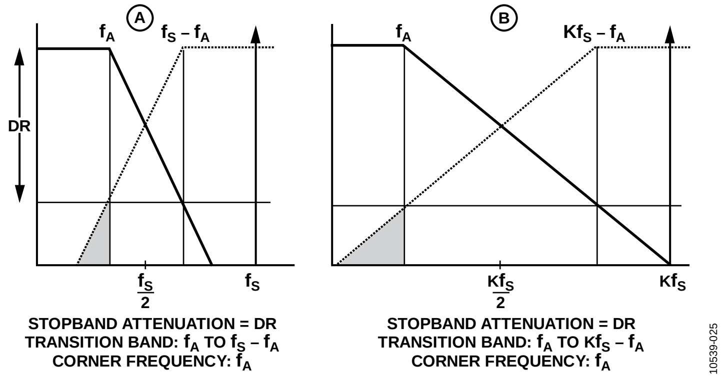

Figure 25. Oversampling Relaxes Requirements on Baseband Antialiasing Filter

Figure 25 illustrates the requirements for an antialiasing filter for a baseband signal with a maximum frequency f_a, given a desired dynamic range of DR. This is a worst-case condition, because it assumes that full-scale signals can occur outside the bandwidth of interest, which is rarely the case. However, it is a good starting point.

The dotted regions indicate where the dynamic range can be limited by signals outside the bandwidth of interest. The requirements on the filter can be quite severe, especially if F_s is not much greater than $2f_a$, as shown in (A) in Figure 25.

As an example, CD audio is sampled at 44.1 kSPS. The maximum bandwidth of audio is 20 kHz. In this case, $f_s - f_a =$ 24.1 kHz. Achieving a stop-band attenuation of 60 dB, for example, in the transition band between 20 kHz and 24.1 kHz is nearly impossible, especially when linear phase is required, as it is in audio.

Therefore, many systems rely on oversampling as shown in Figure 25 (B) to relax the requirements on the analog anti-aliasing filter. Sigma-delta converters are a good example of oversampling. Outputs of DACs are filtered with so-called "anti-imaging" filters that serve essentially the same purpose as the antialiasing filter in front-end of an ADC.

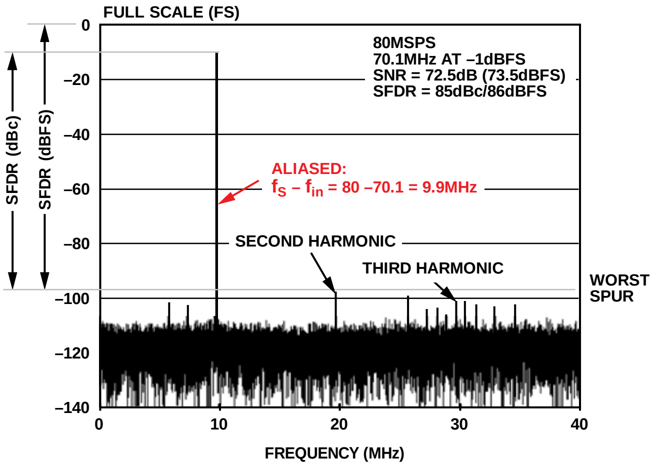

Figure 26. AD9644 14-Bit, 80 MSPS ADC SFDR for 70.1 MHz Input

Figure 26 shows a 70.1 MHz signal sampled at 80 MSPS by the AD9644. Note that in the FFT spectrum, the 70.1 MHz signal actually appears at 80 – 70.1 = 9.9 MHz because of aliasing. In this case, the SFDR is approximately 85 dBc or 86 dBFS. dBc refers to the measurement relative to the carrier signal while dBFS refers to the measurement relative to the carrier signal at full scale or 0 dBFS.

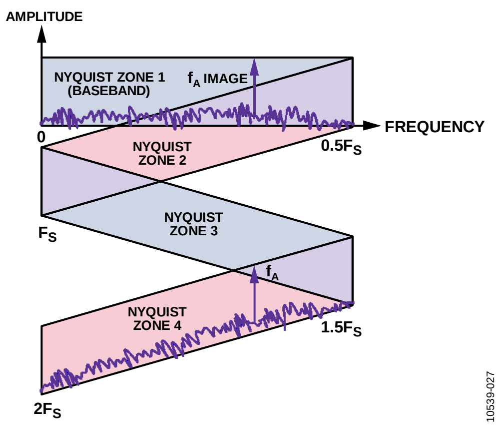

Figure 27. Undersampled Analog Signal f_a Sampled at F_s has Images (Aliases) at $|\pm KFs \pm f_a|$, K = 1, 2, 3, . . .

In Figure 27, Nyquist zones are depicted to show how IF signals fold back to baseband. IF signals are considered to be in any Nyquist zone above the first, where the first Nyquist zone or Fs/2 is considered baseband.

CONSIDERATIONS

Key characteristics of amplifier driven front-ends are as follows:

- May preserve the dc content of the signal
- Provide isolation between previous stage and ADC on the order of ~40 dB to 60 dB
- Easier to work with when gain is required and they are not as gain-bandwidth dependent
- Have inherent noise that gets gained up along with signal
- Less ripple through the pass band
- May convert single-ended signals to differential
- Bandwidth is typically lower than transformers, but is increasing over time

Key points to consider when deciding whether to use a passive (transformer or balun) or active (amplifier) ADC front-end analog input are as follows:

For amplifier driven input

- AC or DC coupled
- Provides good isolation
- Gain settings may be controlled remotely
- Limits ADC performance, that is, degrades SNR

For transformer driven input

- AC coupled only
- Provides poor isolation
- Fixed gain
- Does not limit ADC performance, that is, no degradation in SNR

USEFUL DATA CONVERTER FORMULAS

Noise Floor (–dB) = 6.02 × *n* + 1.76 + 10 × log (*N*/2)

Assume coherent sampling and no windowing (see Table 1).

Noise Floor (–dB) = 6.02 ×*n* + 10 × log (3 × *N*/(*p* × *ENBW*))

Assume noncoherent sampling and no windowing.

Table 1.

FFT Points	12-Bit	14-Bit	16-Bit
1024	101	113	125
2048	104	116	128
4096	107	119	131
8192	110	122	134
16384	113	125	137
32768	116	128	140
SNR (dB)	74.0	86.0	98.1

EFFECTIVE NUMBER OF BITS (ENOB)

ENOB (BITS) = (*SINAD* – 1.76 + 20 × (*FSR*/*ActualFSR*))/6.02

SIGNAL-TO-NOISE RATIO AND DISTORTION (SINAD)

SINAD (*dB*) = -20 × log (*sqrt*(10(–*SNR W/O DIST*/10) + 10(*THD*/10)))

TOTAL HARMONIC DISTORTION (THD)

THD (–*dB*) = 20 × log (*sqrt*((10(–*2ND HAR*/20))2 + (10(–*3RD HAR*/20))2 +… (10(–*6TH HAR*/20))2)

THEORETICAL SIGNAL-TO-NOISE RATIO (SNR)

RMS Signal = (*FSR*/2)/*sqrt*(2)

RMS Noise = *Qn* = *q*/*sqrt(12)*

SNR (dB) = *rms Signal*/*rms Noise* = 20 × log(2(*n*-1) × *sqrt*(6)) = 6.02 × *n* + 1.76

DEFINITIONS/TERMS

Fs = Sampling rate (Hz)

Fin = Input signal frequency (Hz)

FSR = Full scale range (V)

n = Number of bits

q = LSB size

Qn = Quantization noise

LSB = Least significant bit = *FSR*/2*n*

N = Number of FFT points

ENBW = Equivalent noise bandwidth of window function (for example: Four-term Blackman-Harris window, ENBW = 2)

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