ANALOG DEVICES

Applications Engineering Notebook
MT-200

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Minimizing Jitter in ADC Clock Interfaces

by the Applications Engineering Group
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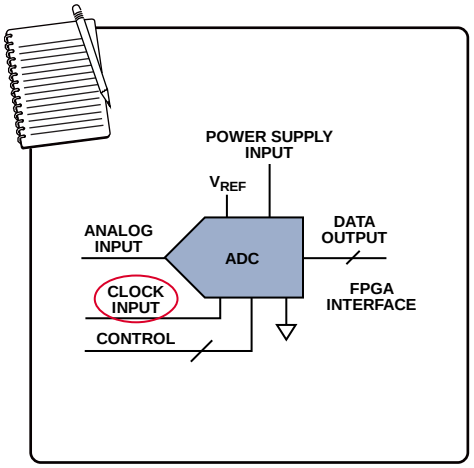
IN THIS NOTEBOOK

Since jitter around the threshold region of a clock interface can corrupt the dynamic performance of an analog-to-digital converter (ADC), this notebook provides an overview of clocking considerations and jitter-reduction techniques.



The Applications Engineering Notebook Educational Series

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REVISION HISTORY

1/12—Revision 0: Initial Version

CLOCK INPUT NOISE

Jitter around the threshold region of the clock interface can corrupt the timing of an analog-to-digital converter (ADC). For example, jitter can cause the ADC to capture a sample at the wrong time, resulting in false sampling of the analog input and reducing the signal to noise (SNR) ratio of the device. A reduction in jitter can be achieved in a number of different ways, including improving the clock source, filtering, frequency division, and clock circuit hardware. This document provides suggestions on how to improve the clock system to achieve the best possible performance from an ADC.

Noise in the circuit between the clock and ADC is the root cause of clock jitter. Random jitter is caused by random noise, which is distinguished by its unbounded character and follows statistical distributions. Major random noise sources include

- Thermal (Johnson or Nyquist) noise is caused by Brownian motion of the charge carriers.
- Shot noise is related to the dc current flow across a potential barrier that is not continuous and smooth, but instead is the result of pulses of current caused by the individual flow of carriers.
- Flicker noise occurs when a dc current is flowing. It is caused by traps in semiconductors that hold carriers that would normally constitute a dc current flow for a short period before releasing them.
- Burst, or popcorn, noise is caused by contamination and crystal lattice dislocation at the surface of the silicon that captures and releases carriers in a random manner.

Deterministic jitter is caused by interference that shifts the threshold in certain ways that are usually bounded by nature.

There are three ways to view the noise in a clock signal:

- Time domain
- Frequency domain
- Phase domain

TIME DOMAIN VIEW

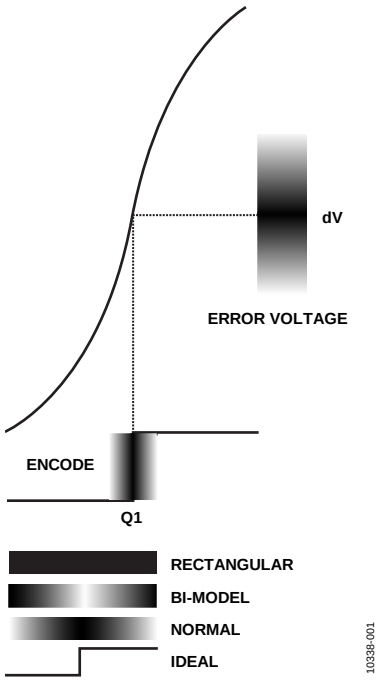

Figure 1. Time Domain View of Jitter

Clock jitter is the sample-to-sample variation of the encode clock which includes both external and internal jitter. Full-scale SNR is jitter limited by

$$SNR_{jitter} = 20\log(\frac{S_{rms}}{N_{rms}}) = 20\log(\frac{1}{2\pi f_{ana\log} t_{jitter}})$$

For example, at 1 Ghz with 100 FS rms jitter, the SNR is 64 dB.

Viewed in the time domain, variation of the encode edge in the x-axis direction causes a y-axis error with a magnitude dependent on the rise time of the edge. Aperture jitter produces errors in the ADC output as shown in Figure 2. The jitter can occur internally in the ADC or externally in the sampling clock or interface circuitry.

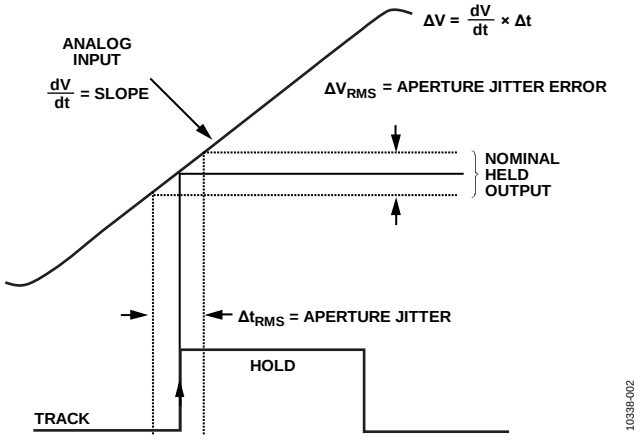

Figure 2. Effects of Aperture Jitter and Sampling Clock Jitter

Figure 3 shows the effects of jitter on SNR. Five traces are shown in Figure 3, each representing a different value of jitter. The x-axis is full-scale analog input frequency, and the y-axis is the SNR due to the jitter as opposed to the total ADC SNR. Jitter on a clock is defined from the f_{START} and f_{STOP} offset frequency. For example, a clock may have 200 fsec of jitter integrated from 1 kHz to fs/2 and 170 fsec of jitter integrated from 10 kHz to fs/2. The integration range is dependent upon the end application.

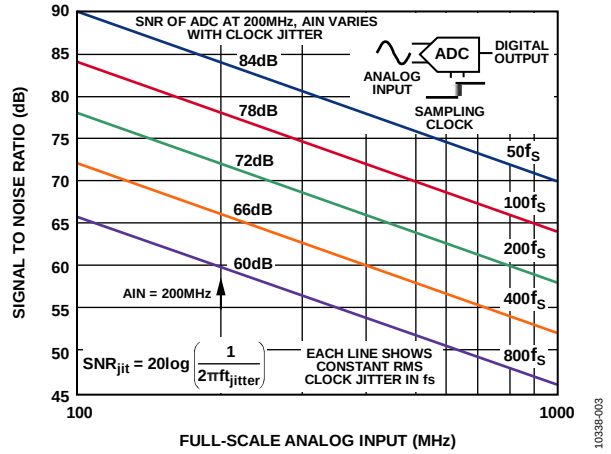

Figure 3. As Analog Signal Increases, Clock Jitter Increases SNR

The jitter-based SNR and the effective number of bits (ENOB) are related by the equation: SNR = 6.02 N + 1.76 dB where N = ENOB. For full-scale 100 MHz input, 14-bit ENOB requires that the rms jitter be no greater than 0.125 ps or 125 fs. The equation assumes an ADC of infinite resolution where the only error is noise produced by the clock jitter.

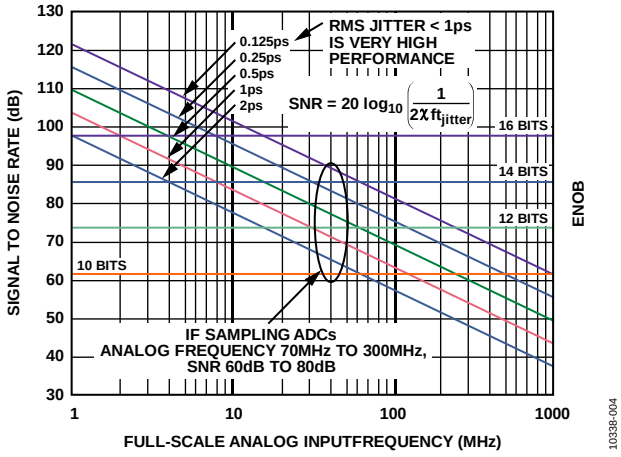

Figure 4. Theoretical SNR and ENOB Due Jitter as a Function of Full-Scale Sinewave Analog Input Frequency

Effect of Slew Rate

Increasing the slew rate of the clock edge reduces the effects of noise and jitter by leaving the circuit less exposed. On the other hand, a faster slew rate increases the difficulty of circuit design, may cause electromagnetic interference (EMI) issues and may cause interference in other circuits. Note that an oscilloscope with very low input capacitance is needed to accurately measure the slew rate. Figure 5 shows how increasing the slew rate reduces jitter because only noises in the threshold range contribute to jitter.

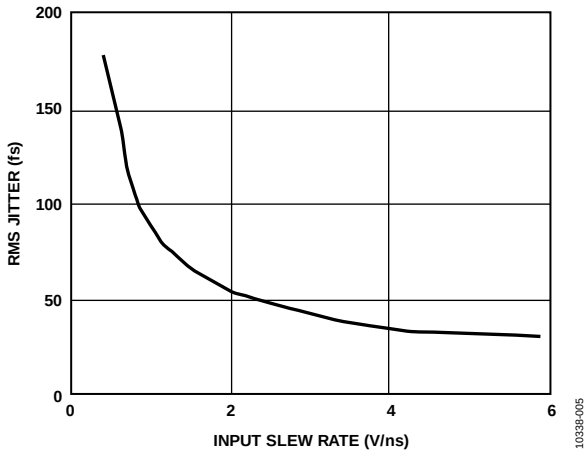

Figure 5. Increasing Slew Rate Reduces Jitter

FREQUENCY DOMAIN VIEW

Close-in noise occurs in the region between the center frequency of the sample clock to a single sideband (SSB) offset equal to half the signal bandwidth. Wideband noise extends from the SSB offset to ½ the bandwidth of the clock receiver.

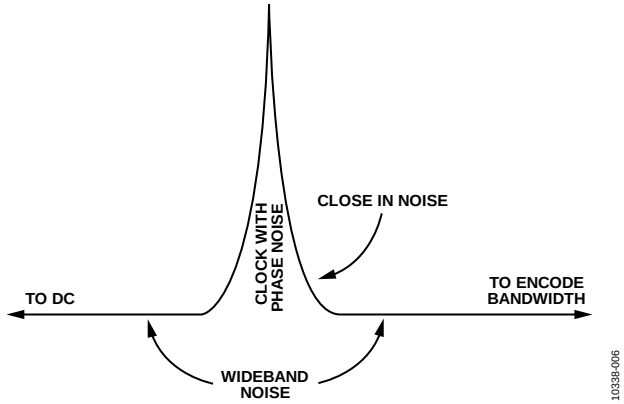

Figure 6. Frequency Domain View

Multiplication in time is convolution in the frequency domain. Therefore, any skirt on the clock is applied to the digitized signal. This increases the EVM of the signal and degrades overall performance. The amount convolved onto the sample signal depends on the relationship of the analog frequency to the sample frequency.

$$SampledOutput = ClockSignal + 20\log(\frac{f_{signal}}{f_{clock}})$$

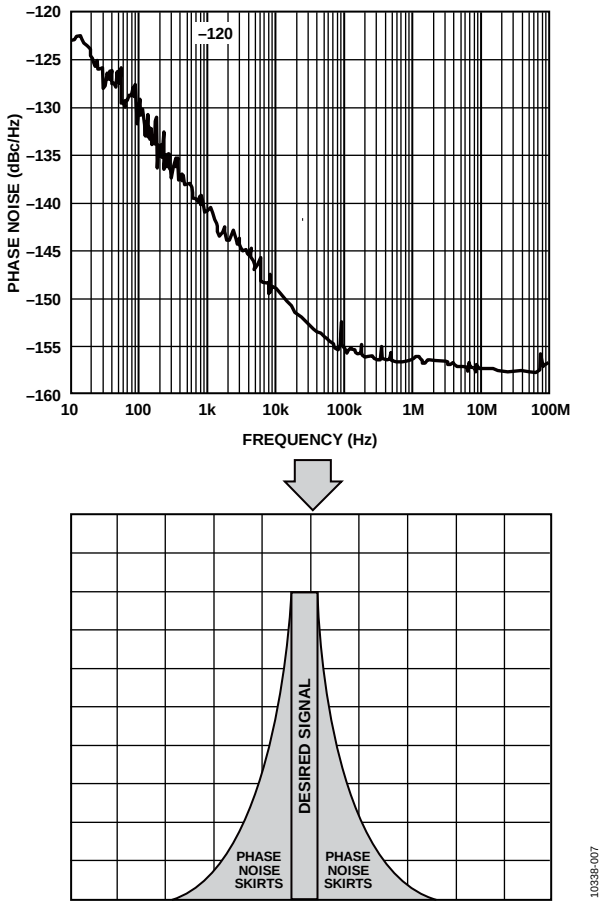

Figure 7. The Noise Convolved onto the Sampled Signal Depends on the Relationship of the Analog Frequency to the Sample Frequency

PHASE DOMAIN VIEW

Phase noise is cause by variations in the time period between each clock cycle. The end result is that the clock signal varies around a fundamental frequency. This spread of frequencies will degrade the ADC's SNR.

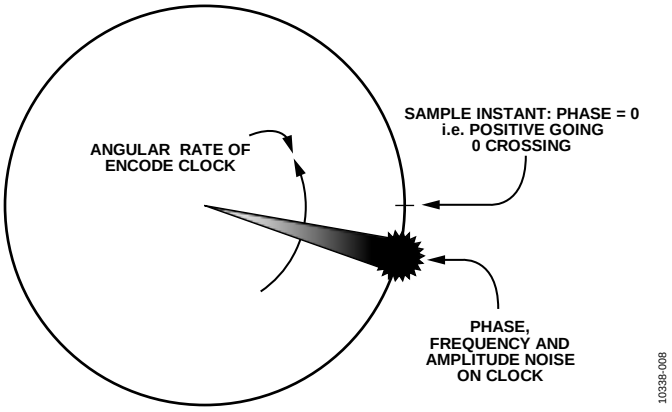

Figure 8. Phase Domain View of Jitter

In the example shown below, a spur is added to a 78 MHz clock at level of −66 dBc and is used to control an ADC sampling a 30.62 MHz analog signal.

The spur is at −74.1 dBc as determined by the following equation:

$$-66 + 20\log(\frac{30.62}{78}) = -74.1 dBc$$

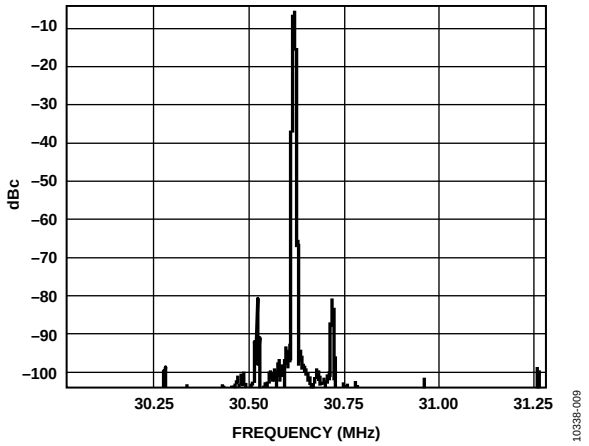

Figure 9. 30.62 MHz Signal when Sampled with a Noisy Clock

Clock designers typically provide a phase noise, but not a jitter specification. The phase noise specification can be converted to jitter by first determining the noise on the clock and then comparing noise to the main clock component using small angle math.

The phase noise power is integrated by calculating the gray area in Figure 10.

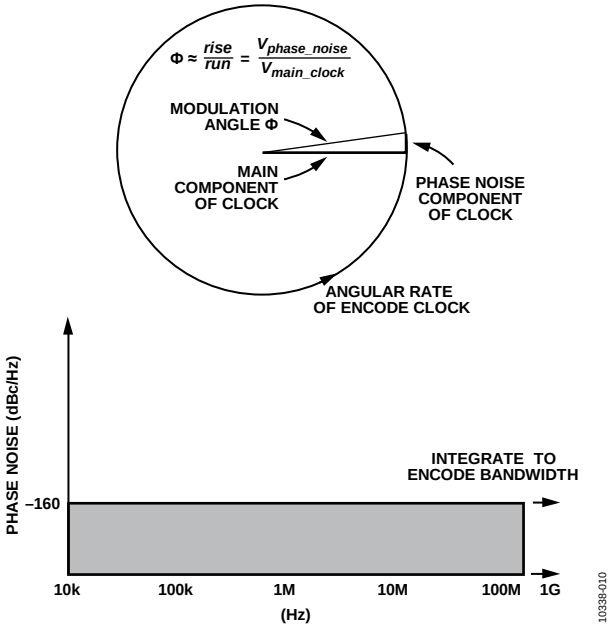

Figure 10. Integrating the Noise from Close-In to the Clock Out to the Bandwidth of the Encode

The height is −160 dBc and the width is 10 KHz to 245.76 MHz. Therefore, $10\times\log(245.7e^6 - 10e^3)$ = 83.9 dB and −160 + 83.9 dB = 76.1 dBc of integrated noise.

$$P_{Noise} = -160\,dBc/Hz + 10\log(245.76\times10^{6} - 10.0\times10^{3} = -76.1\,dBc$$

$$Jitter_{phase} \cong \sqrt{2\times10^{P_{Noise}/10=}} = \sqrt{2\times10^{-76.1/10}} = 2.217\times10^{-4}\,radians\ for\ small\ angles$$

$$Jitter = \frac{Jitter_{Phase}}{2\pi f_{Osc}} = \frac{2.217\times10^{-4}}{2\pi\times245.76\times10^{6}} = .1435\,pS$$

At different offsets from the carrier, the slope of the noise can be different. For example, the A1 region is typically 1/f noise while the A4 region is considered broadband noise.

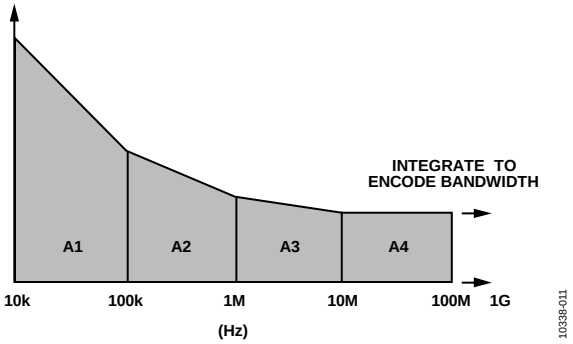

Figure 11. Case Where Noise Varies Across Frequency Range

A = Area = integrated phase noise power (dBc).

The jitter can be determined by integrating the noise from close-in to the clock out to the bandwidth of the encode. The frequency range must be broken down into smaller bands and added together to get the total.

A = 10 log10 (A1 + A2 + A3 + A4)

$$\text{Rms phase jitter (radians)} \approx \sqrt{2\times10^{\frac{A}{10}}}$$

$$\text{Rms jitter (seconds)} \approx \frac{\sqrt{2\times10^{\frac{A}{10}}}}{2\pi f_{Osc}}$$

f_{Osc} = oscillator frequency

10 k to 100 k

(−133.5 + −141.6) = −137.5

2 + 10 × log(90 k)=−87.9 dBc

100 k to 1 M

(−141.5 + −147.8) = −144.7

2 + 10 × log(900 k)=−85.2 dBc

10 M to 40 M

(−161.7 + −162.5) = −162.1

2 + 10 × log(30 M)=-87.3 dBc

RSS

10^(−87.9/10)+10^(−85.2/10)+10^(−87.3/10) = −81.7 dBc

PNoise = −81.7 dBc

$$Jitter_{phase} \cong \sqrt{2\times10^{P_{Noise}/10=}} = \sqrt{2\times10^{-81.7/10}} =$$

$1.163\times10^{-4}\,radians$

for small angles

$$Jitter = \frac{Jitter_{Phase}}{2\pi f_{Osc}} = \frac{1.163\times10^{-4}}{2\pi\times12288\times10^{6}} = .151\,fS$$

The calculated value is close to the measured value of 158 fS.

SOLUTIONS FOR CLOCKING CONVERTERS

A phase locked loop (PLL) can be used to lock the reference clock output to the desired frequency. Figure 12 shows a reference clock with high noise at a bandwidth of about 100 kHz. The green and two blue traces are noise sources in an AD9516 clock generator. The red trace is the noise of the external reference feeding the AD9516. The brown trace is the total noise of the AD9516. The graph shows that the dirty reference clock is the reason for the noise problem.

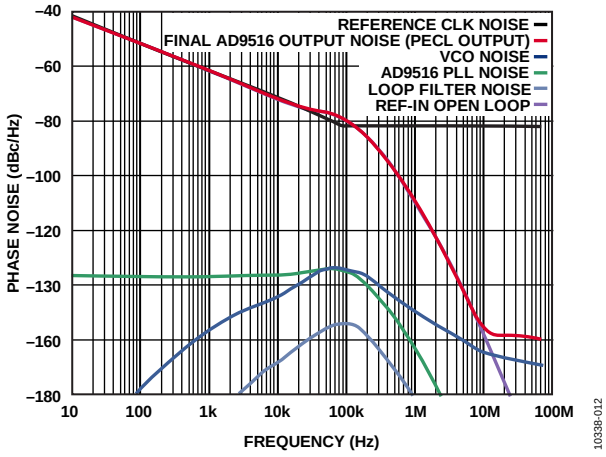

Figure 12. Jitter Caused by Dirty Reference Clock

In this example, a PLL is used to filter the output of the reference clock. The PLL bandwidth is set to 30 Hz and a good quality VCXO is used. The PLL removes the unwanted jitter from the recovered system clock as shown in Figure 13.

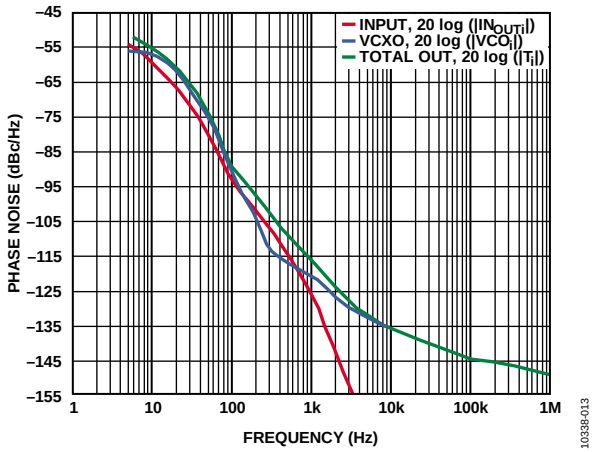

Figure 13. PLL Removes Unwanted Jitter

In this example, an ADF4002 is used as the PLL to clean the recovered input reference clock. The AD9516 clock generator is then used to produce multiple clocks.

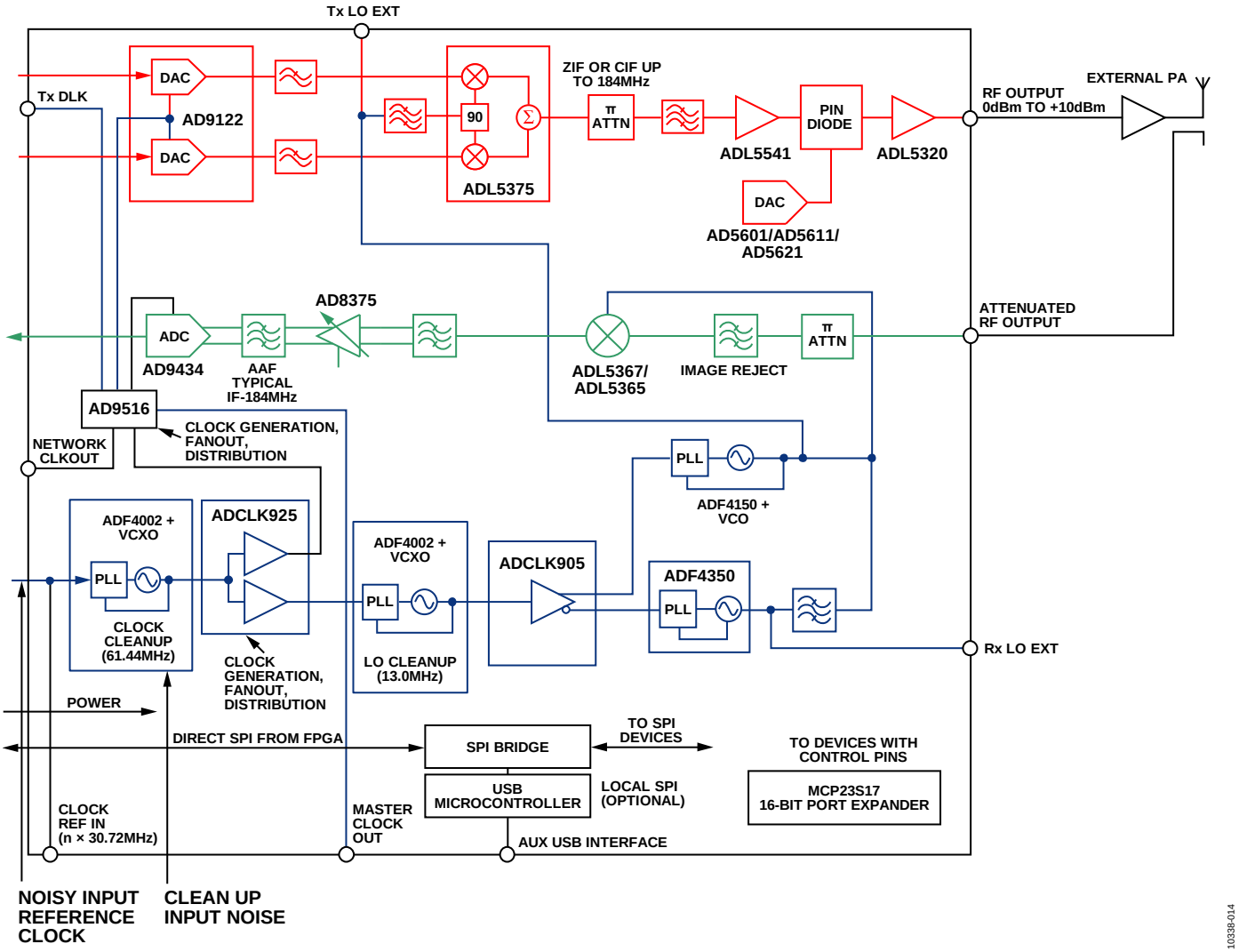

Figure 14.

The AD9523, AD9524, and AD9523-1 clock generators integrate the functions of jitter clean and clock generation/distribution into a single device. The AD9524 device has seven outputs while the AD9523 and AD9523-1 have 15 outputs.

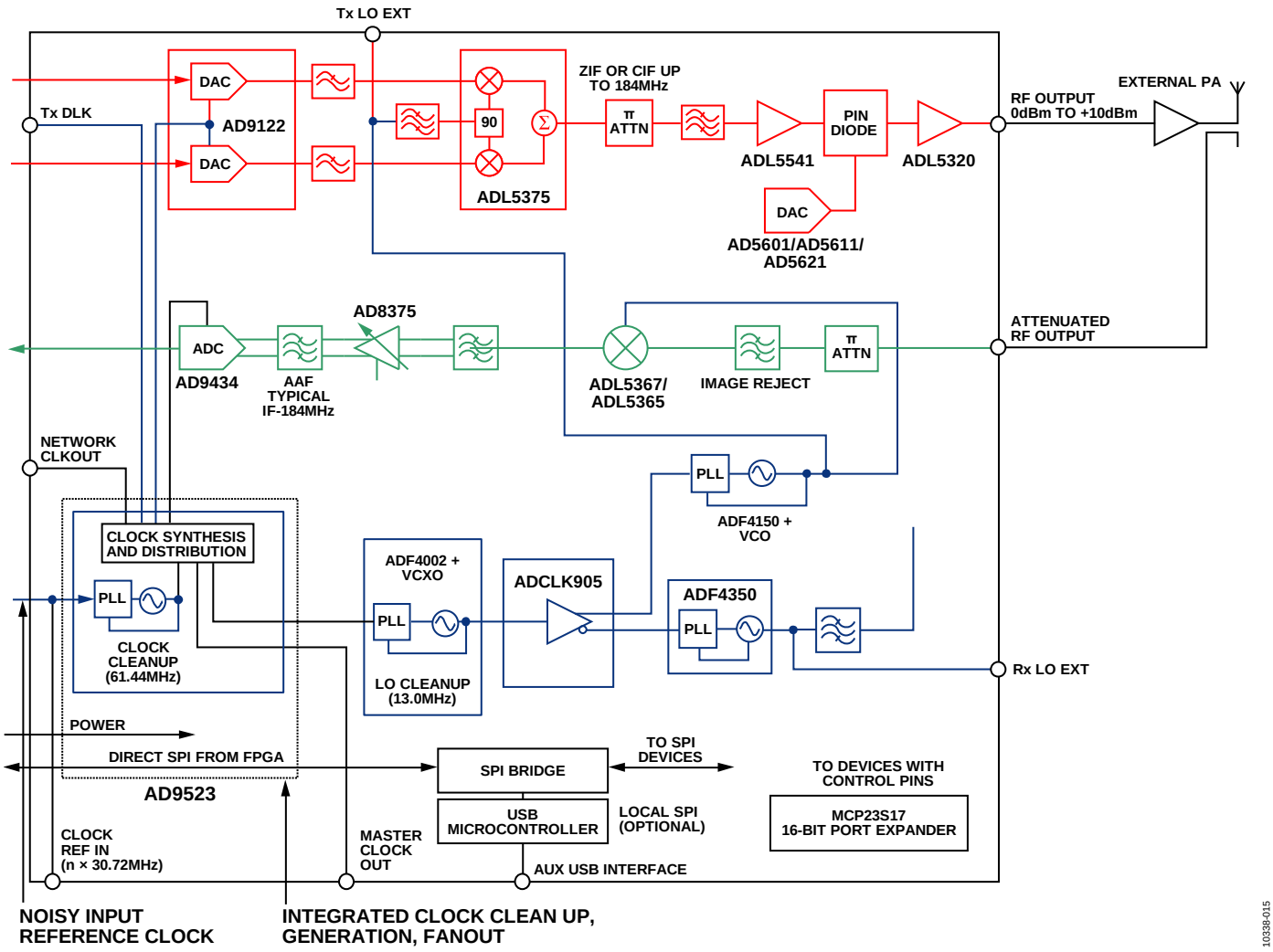

Figure 15.

The driver design of the Analog Devices AD9523, AD9524, and AD9523-1 offer multimode output which means that it's possible to use a common 100 Ω differential resistor and change a register value to change from LVPECL, LVDS, and HSTL signal formats. Each signal format has advantages and disadvantages as shown in the charts below. All signal formats have different voltage swings. Select the format with best swing for the application but remember that a lower swing uses less power.

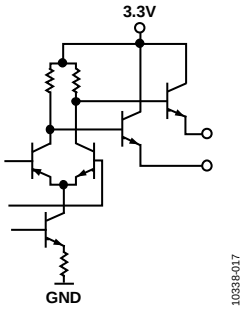

Figure 16.

Table 1. LVPECL Signal Format Pros and Cons

Pros	Cons
quasidifferential	high power
high slew rates	requires a bipolar device that is not available on CMOS processes
can accept near/far termination	
fanout capability	
relatively quiet such that it doesn't corrupt other signals easily	

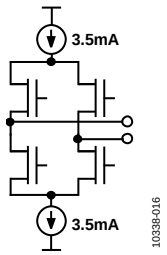

Figure 17.

Table 2. LVDS Signal Format Pros and Cons

Pros	Cons
true differential	low signaling (±0.4 V) often does not yield highest slew
some variants can accept near/far termination	care needs to be taken to insure aggressor signals equally couple to differential LVDS lines
quiet such that it doesn't corrupt other signals easily	
low power rates at receiver resulting in higher noise than LVPECL	

Table 3. CML Signal Format Pros and Cons

Pros	Cons
true differential	common mode voltage near ground or V_{CC}
high slew rate	
particularly suitable for the most demanding applications	
quiet	