Intentionally Nonlinear DACs

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INTRODUCTION

Usually, we have emphasized the importance of maintaining good differential and integral linearity in data converters. However, there are situations where ADCs and DACs which have been made intentionally nonlinear (but maintaining good differential linearity) are useful, especially when processing signals having a wide dynamic range.

TELECOMMUNICATIONS APPLICATIONS OF NON-LINEAR DACs AND ADCs

One of the earliest uses of nonlinear data converters was in the digitization of voiceband signals for pulse code modulation (PCM) systems. Major contributions were made at Bell Labs during the development of the T1 carrier system. The motive for the nonlinear ADCs and DACs was to reduce the total number of bits (and therefore the serial transmission rate) required to digitize voice channels. Straight linear encoding of a voice channel required 11- or 12-bits and a sampling rate of 8 kSPS. In the 1960s Bell Labs determined that 7-bit nonlinear encoding was sufficient; and later in the 1970s they went to 8-bit nonlinear encoding for better performance (References 1-6).

The nonlinear transfer function allocates more quantization levels out of the total range for small signals and fewer for large amplitude signals. In effect, this reduces the quantization noise associated with small signals (where it is most noticeable) and increases the quantization noise for larger signals (where it is less noticeable). The term "companding" is generally used to describe this form of encoding.

The logarithmic transfer function chosen is referred to as the "Bell µ-255" standard, or simply "µ-law." A similar standard developed in Europe is referred to as "A-law." The Bell µ-law allows a dynamic range of about 4000:1 using 8 bits, whereas an 8-bit linear data converter provides a range of only 256:1.

The first generation channel bank (D1) generated the logarithmic transfer function using temperature controlled resistor-diode networks for "compressors" ahead of a 7-bit linear ADC in the transmitter. Corresponding resistor-diode "expandors" having an inverse transfer function followed the 7-bit linear DAC in the receiver. The next generation D2 channel banks used nonlinear ADCs and DACs to accomplish the compression/expansion functions in a much more reliable and cost-effective manner, and eliminated the need for the temperature-controlled diode networks.

In his 1953 classic paper, B. D. Smith proposed that the transfer function of a successive approximation ADC utilizing a nonlinear internal DAC in the feedback path would be the inverse transfer function of the DAC (Reference 7). The same basic DAC could therefore be used in the ADC and also for the reconstruction DAC. Later in the 1960s and early 1970s, nonlinear ADC and DAC technology using piecewise linear approximations of the desired transfer function allowed low cost, high volume implementations (References 1-6). These nonlinear 8-bit, 8-kSPS data converters became popular telecommunications building blocks.

The nonlinear transfer function of the 8-bit DAC is first divided into 16 segments (chords) of different slopes—the slopes are determined by the desired nonlinear transfer function. The 4 MSBs determine the segment containing the desired data point, and the individual segment is further subdivided into 16 equal quantization levels by the 4 LSBs of the 8-bit word. This is shown in Figure 1 for a 6-bit DAC, where the first 3 bits identify one of the 8 possible chords, and each chord is further subdivided into 8 equal levels defined by the 3 LSBs. The 3 MSBs are generated using a nonlinear string DAC, and the 3 LSBs are generated using a 3-bit binary R-2R DAC.

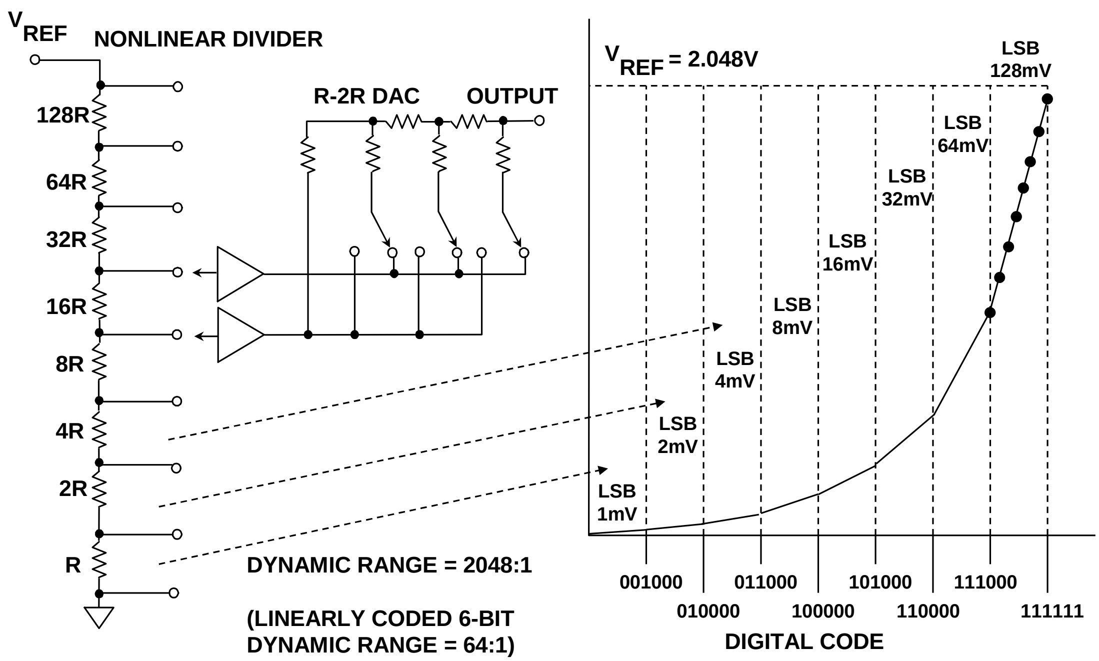

Figure 1: Nonlinear 6-Bit Segmented DAC

In 1982, Analog Devices introduced the LOGDAC® AD7111 monolithic multiplying DAC featuring wide dynamic range using a logarithmic transfer function. The basic DAC in the LOGDAC is a linear 17-bit current-mode "inverted" R-2R DAC preceded by an 8-bit input decoder (see Figure 2). The LOGDAC can attenuate an analog input signal, V_{IN}, over the range 0 dB to 88.5 dB in 0.375 dB steps. The degree of attenuation across the DAC is determined by an nonlinear-coded 8-bit word applied to the onboard decode logic. This 8-bit word is mapped into the appropriate 17-bit word, which is then applied to a 17-bit R-2R ladder. A functional diagram of the LOGDAC is shown in Figure 2. In addition to providing the logarithmic transfer function, the LOGDAC also acts as a full four-quadrant multiplying DAC.

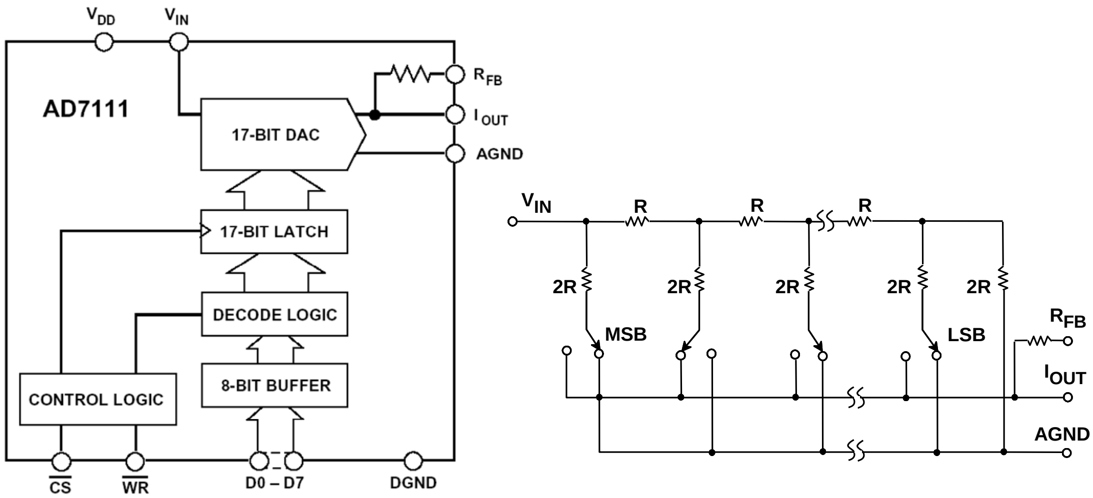

Figure 2: AD7111 LOGDAC® (Released 1982)

With the introduction of high resolution linear ADCs and DACs, the method used in the LOGDAC® is widely used today to implement various nonlinear transfer functions such as the µ-law and A-law companding functions required for telecommunications and other applications. Figure 3 shows a general block diagram of the modern approach.

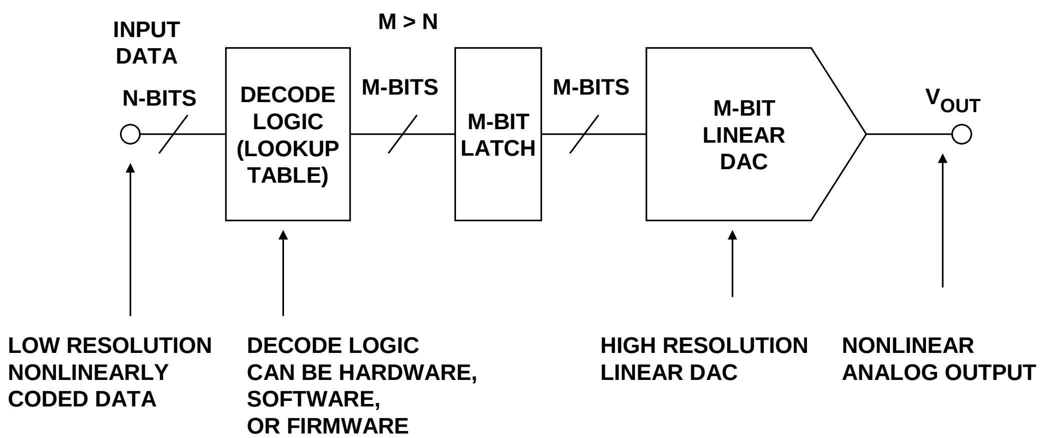

Figure 3: General Nonlinear DAC

The µ-law or A-law companded input data is mapped into data points on the transfer function of a high resolution DAC. This mapping can be easily accomplished by a simple lookup table in either hardware, software, or firmware. A similar nonlinear ADC can be constructed by digitizing the analog input signal using a high resolution ADC and mapping the data points into a shorter word using the appropriate transfer function. A big advantage of this method is that the transfer curve does not have to be approximated with straight line segments as in the earlier method, thereby providing more accuracy.

REFERENCES

1. B. Smith, "Instantaneous Companding of Quantized Signals, *Bell System Technical Journal*, Vol. 36, May 1957, pp. 653-709. *(one of the first papers written about using nonlinear coding techniques for speech signals in PCM).*

2. H. Kaneko and T. Sekimoto, "Logarithmic PCM Encoding Without Diode Compandor," *IEEE Transactions on Communications Systems*, Vol. 11, No. 3, September 1963, pp. 296-307. *(describes several methods for nonlinear encoding speech directly without the need for diode compandors).*

3. C. L. Dammann, "An Approach to Logarithmic Coders and Decoders," *NEREM Record*, Boston MA, November 2-4, 1966, pp. 196-197. *(more discussions on nonlinear coders and decoders for PCM).*

4. H. Kaneko, "A Unified Formulation of Segment Companding Laws and Synthesis of Codecs and Digital Compandors," *Bell System Technical Journal*, Vol. 49, September 1970, pp. 1555-1558. *(discusses the piecewise linear approximation to the logarithmic transfer companding function).*

5. M. R. Aaron and H. Kaneko, "Synthesis of Digital Attenuators for Segment Companded PCM Codes," *Transactions on Communications Technology*, COM-19, December 1971, pp. 1076-1087. *(more on nonlinear coding).*

6. C. L. Dammann, L. D. McDaniel, and C. L. Maddox, "D2 Channel Bank: Multiplexing and Coding," *Bell System Technical Journal*, Vol. 51, October 1972, pp. 1675-1699. *(still more on nonlinear coding).*

7. B. D. Smith, "Coding by Feedback Methods," *Proceedings of the I. R. E.*, Vol. 41, August 1953, pp. 1053-1058. *(Smith uses an internal binary weighted DAC and also points out that a non-linear transfer function can be achieved by using a DAC with non-uniform bit weights, a technique which is widely used in today's voiceband ADCs with built-in companding. He was also one of the first to propose using an R/2R ladder network within the DAC core).*

8. Walt Kester, *Analog-Digital Conversion*, Analog Devices, 2004, ISBN 0-916550-27-3, Chapter 3. Also available as *The Data Conversion Handbook,* Elsevier/Newnes, 2005, ISBN 0-7506-7841-0, Chapter 3.