# Chapter II

# Scott connected transformers, the representation of angles in digital form, logic inputs and outputs

## INTRODUCTION

Before proceeding to describe the operation and application of Synchro/Resolver to Digital and Digital to Synchro/Resolver converters, it is worth while touching briefly upon three subjects which are particularly relevant when discussing these products.

## SCOTT CONNECTED TRANSFORMERS

Modern synchro to digital converters (SDC's) and digital to synchro converters (DSC's) deal internally with signals in resolver format. For this reason it is necessary to convert synchro input signals into resolver form for SDC's and to convert the internal resolver format signals into synchro format in the case of DSC's. These conversions are generally carried out by the use of interconnected transformers known as Scott Connected or Scott T transformers. (In the case of the input transformers in a resolver to digital converter and the output transformers in a digital to resolver converter, they do not need to be Scott connected and usually consist of completely separate isolation transformers for sine and cosine channels).

### Synchro to resolver format Scott connected transformers

A pair of Scott T transformers connected to perform a synchro to resolver format conversion is shown in Fig. 2-1.
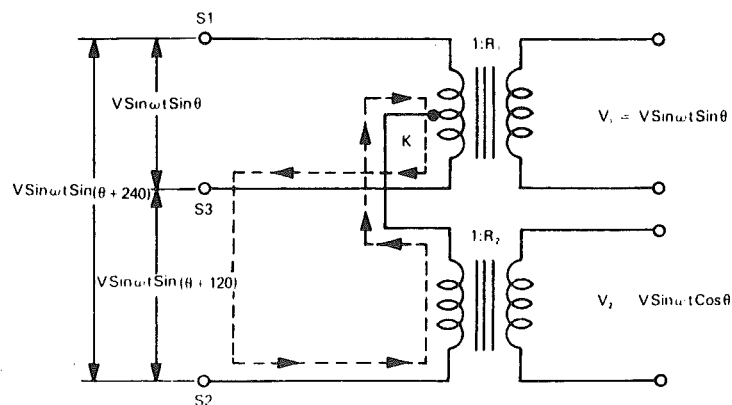


Fig. 2-1 Scott connected transformer pair. Synchro to resolver.

As can be seen in the diagram, the synchro format voltages are applied to S1, S2 and S3 of the Scott connected pair and the resolver format output voltages are produced on the two secondary windings. In most practical situations the transformers will also be used to scale the voltages between input and output as well as performing the conversion from synchro to resolver format. This is simply accomplished by increasing the turns on one side or other of

each transformer. However in this case we will consider that the transformation ratio of the Scott T pair is 1:1, ie. the line to line resolver format output voltage will have the same maximum value as the line to line synchro format input voltages.

Referring to Fig. 2-1, the tapped transformer is often known as the "Main transformer" and the untapped one is known as the "Teaser transformer".

With synchro format input signals, viz.

$$V_{S1-S3} = V \sin \omega t \sin \theta$$

$$V_{S3-S2} = V \sin \omega t \sin (\theta + 120°)$$

$$V_{S2-S1} = V \sin \omega t \sin (\theta + 240°)$$

the output resolver format signals will be:

$$V_1 = V \sin \omega t \sin \theta$$

$$V_2 = V \sin \omega t \cos \theta$$

In a Scott connected pair, it can be shown that the ratio of turns between primary and secondary is 1:1 for the main transformer and $1:2/\sqrt{3}$ for the teaser. This is assuming that the input maximum voltage equals the output maximum voltage as stated above. It can also be shown that the main transformer is tapped at its midpoint, ie. the tapping point $K = 0.5$. These postulations can be proven as follows:

Let $1:R_1$ be the turns ratio on the main transformer and $1:R_2$ on the teaser.

The primary voltage on the main transformer is:

$$V \sin \omega t \sin \theta$$

Therefore the voltage on the secondary is:

$$V R_1 \sin \omega t \sin \theta$$

However, we want to show that:

$$V_1 = V \sin \omega t \sin \theta$$

Therefore

$$\underline{\underline{R_1 = 1}}$$

Concerning $V_2$ we have:

$$V_2 = V R_2 [\sin \omega t \sin (\theta + 120°) + K \sin \omega t \sin \theta]$$

which is obtained by adding the voltages around the arrowed path and multiplying by the ratio $R_2$.

Taking $\sin \omega t$ outside gives:

$$V_2 = V R_2 \sin \omega t [\sin (\theta + 120°) + K \sin \theta]$$

However:

$$V_2 = V \sin \omega t \cos \theta$$

which is the resolver format voltage required on $V_2$

Therefore:

$$V \sin \omega t \cos \theta = V R_2 \sin \omega t [\sin (\theta + 120°) + K \sin \theta]$$

Cancelling out $V \sin \omega t$ gives:

$$\cos \theta = R_2 [\sin (\theta + 120°) + K \sin \theta] \dots\dots\dots\dots\dots\dots\dots (1)$$

This must hold for all values of $\theta$, therefore putting $\theta = 0°$ gives:

$$1 = R_2 \cos 30°$$

Therefore

$$\underline{\underline{R_2 = 1/\cos 30° = \frac{2}{\sqrt{3}}}}$$

Putting $\theta = 90°$ into equation (1) gives:

$$0 = \frac{2}{\sqrt{3}} [-\text{Sin } 30° + K]$$

or

$$\frac{2}{\sqrt{3}} \cdot \frac{1}{2} = \frac{2}{\sqrt{3}} \cdot K$$

or

$$\underline{K = 0.5}$$

### Resolver to synchro format Scott connected transformers

Fig. 2-2 shows the resolver to synchro Scott connected transformer arrangement. By the reciprocal theorem, the arrangement is simply the inverse of the synchro to resolver case, the main transformer having a ratio of 1:1 and the teaser a step down ratio of $2/\sqrt{3}:1$. These ratios give the same maximum line to line voltage as the maximum line to line input voltage. As was mentioned earlier, generally both transformer ratios will be scaled in proportion to provide either a step up or a step down ratio as required. Scott transformers are precision components: the design criteria will be influenced by the requirement for the exact ratios.
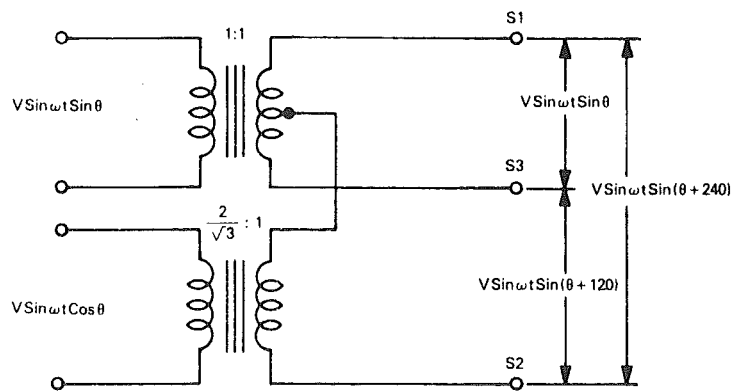


Fig. 2-2 Scott connected transformer pair. Resolver to synchro.

### The reflected resistance in the Scott connected output transformers of Digital to synchro converters

To avoid the spurious generation of quadrature signals (signals of the same fundamental frequency but with a 90° phase shift) in the output transformers of Digital to synchro converters, it is important that the inductive and resistive output impedances of the Scott connected pair of transformers should be equal in each of the three output wires S1, S2 and S3. By choosing suitable wire gauges, the secondary resistance can be made equal. The question arises about the primary resistance when reflected to the secondary side. The primary turns are equal and for similar wire gauges the primary resistances will be equal and by design the output impedances of the driving amplifiers can be made equal. The question is, do these equal primary resistances give rise to equivalent equal resistances in the three secondary wires?

Fig. 2-3 shows the resistance on the primary side and Fig. 2-4 shows the resistances in the secondary side due to the primary resistance.

The resistance between $S_1$ and $S_3$ will be $R_p . N^2$

Therefore $R_1 = R_2 = R_p . \dfrac{N^2}{2}$

The resistance between $S_1$ and CT will be $R_p . \left(\dfrac{N}{2}\right)^2$ where CT = Midpoint Tap

Therefore the resistance in series with the CT will have to be negative and equal to
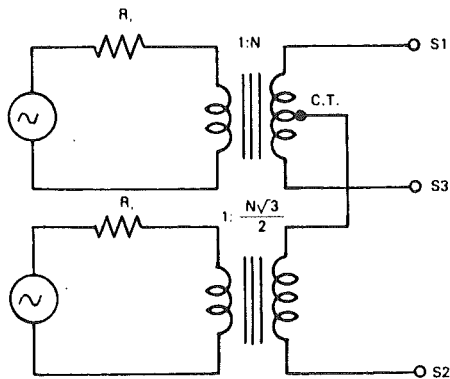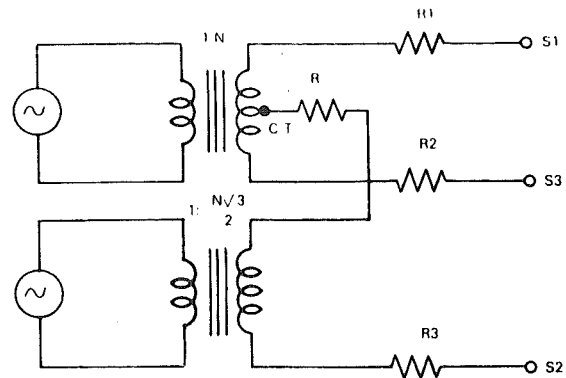
$$- R_p . \frac{N^2}{4}$$

Fig. 2-3                    Fig. 2-4

The resistance $R_3$ is equal to $R_p \cdot \dfrac{3}{4} \cdot N^2$

Checking the resistances between $S_1$, $S_2$ and $S_3$ we have:

$$S_1 \text{ to } S_3 = R_p \cdot N^2$$

$$S_1 \text{ to } S_2 = R_p \cdot \frac{N^2}{2} - R_p \cdot \frac{N^2}{4} + R_p \cdot \frac{3}{4} \cdot N^2 = R_p \cdot N^2$$

$$S_3 \text{ to } S_2 = R_p \cdot \frac{N^2}{2} - R_p \cdot \frac{N^2}{4} + R_p \cdot \frac{3}{4} \cdot N^2 = R_p \cdot N^2$$

Therefore the answer to the question is that if the primary resistances are equal, they give rise to equal equivalent resistances on the secondary side. The necessary balancing of the resistances to reduce to a minimum the introduction of quadrature signals can therefore be carried out by resistive balancing of the secondary windings only. (See Section on quadrature errors in DSC's in Chapter 4.)

### The use of Scott connected transformers as the input to synchro to digital converters

When used as the input transformers in synchro to digital converters, the input impedance of the amplifiers at the converter side of the input Scott connected pair of transformers is very high, so high in fact that it does not contribute in any significant way to the loading on the input signal lines. The loading on the lines is determined by the primary reactances and resistances in series. The primary reactance is very high compared with the resistance, it is so high in fact that when the Scott connected transformers are driven from the low output impedances from Control Transmitters that a considerable out of balance is required before any significant errors occur. The point being made however is that in this case if we are to seek balanced loading on the lines it is the primary inductances and not the resistances of the windings which is the dominating factor. To provide some figures a low voltage CX size 11 could have an output $Z_{SS}$ of $9 + j3$ ohms ($Z_{SS}$ is Z stator, rotor shorted) or an output $Z_{SO}$ of $8 + j45$ $Z_{SO}$ is (Z stator rotor open). (Which of these impedances is relevant will depend on whether the rotor is voltage or current driven.) If we take the worst case of $Z_{SO}$ of $8 + j45$ this corresponds to a $Z_{LL}$ of $10.7 + j60$. ($Z_{LL} = 4/3\ Z_{SO}$). This impedance must be compared with 20 K ohms which is a typical low voltage line to line impedance.

The line to line impedances which are of the order of 20 K ohms (nearly purely reactive) must be balanced to give the required accuracy when driven from sources of between 10 and

60 ohms line to line. The balance required is on the inductances of the synchro input to the Scott connected transformers. Fig. 2-5 shows the arrangement which gives this inductive balance.
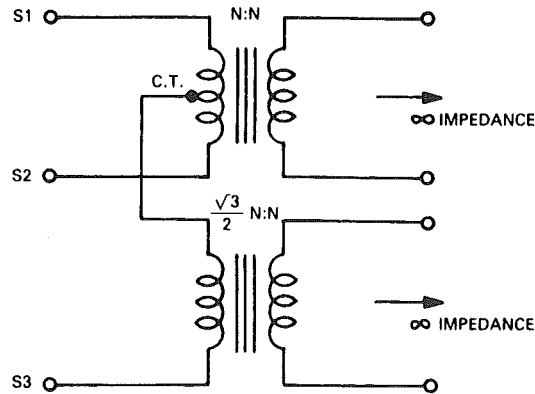


**Fig. 2-5** Scott connected transformers with balanced inductances.

Inductance between $S_1$, $S_2$ = $KN^2$

Inductance between $S_2$, $S_3$ = $K(1/2 \times N)^2 + K(\sqrt{3}/2 \times N)^2$
$$= KN^2$$

Inductance between $S_1$, $S_3$ = $K(1/2 \times N)^2 + K(\sqrt{3}/2 \times N)^2$
$$= KN^2$$

The inductive balances depend upon the same core size and material being used for each transformer (the same K for each transformer). Since the same core sizes are required identical transformers can be used with tappings on the primary for the CT and the $\sqrt{3}/2$ point. With this arrangement the resistances are not balanced (they could be by using differing wire gauges) but since their effect is negligible it is of no consequence.

## Electronic Scott T transformers

It is possible to carry out these Synchro to resolver format conversions and vice versa without the use of transformers at all. This is done by operational amplifiers and is often referred to as an Electronic Scott T. However, the need in synchro systems for a high voltage common mode rejection makes the transformer method preferable and in some cases, for example in aircraft systems, mandatory.

None of the products discussed in this book use electronic Scott T's.

## THE REPRESENTATION OF ANGLES IN DIGITAL FORM

### Binary coding

There are many possible methods of representing angular information in digital form. By far the most common, and that used in all of the binary input and output products discussed in this book is natural binary coding. In this system of coding, the Most Significant Bit (MSB) represents 180°, while the next represents 90°, the next 45° and so on. The value of the Least Significant Bit (LSB) will depend on the number of bits in the digital word (word length). Word lengths used will depend on the accuracy and the resolution required and in the case of SDC's and DSC's will usually lie in the range of 10 to 20 bits.

The digital word is usually represented in positive logic where a '1' state indicates that the particular bit is included in the word and a '0' state indicates that it is not.

An example of an angle represented in natural binary coding is 257.96° which would be represented in a 12 bit word as follows:

101101110111
|                    |
MSB            LSB

Fig. 2-6 shows the bit weights for words up to 20 bits in length.

| Bit no. | Angle in degrees/decimal | Angle in | | |
|---------|--------------------------|---------|-----------|-----------|
| | | Degrees | Arc. Mins. | Arc. Secs. |
| 1 MSB | 180.00000 | 180 | 0 | 0.0 |
| 2 | 90.00000 | 90 | 0 | 0.0 |
| 3 | 45.00000 | 45 | 0 | 0.0 |
| 4 | 22.50000 | 22 | 30 | 0.0 |
| 5 | 11.25000 | 11 | 15 | 0.0 |
| 6 | 5.62500 | 5 | 37 | 30.0 |
| 7 | 2.81250 | 2 | 48 | 45.0 |
| 8 | 1.40625 | 1 | 24 | 22.5 |
| 9 | 0.70313 | 0 | 42 | 11.3 |
| 10 | 0.35156 | 0 | 21 | 5.6 |
| 11 | 0.17578 | 0 | 10 | 32.8 |
| 12 | 0.08790 | 0 | 5 | 16.4 |
| 13 | 0.04395 | 0 | 2 | 38.2 |
| 14 | 0.02197 | 0 | 1 | 19.1 |
| 15 | 0.01099 | 0 | 0 | 39.6 |
| 16 | 0.00549 | 0 | 0 | 19.8 |
| 17 | 0.00275 | 0 | 0 | 9.9 |
| 18 | 0.00137 | 0 | 0 | 4.9 |
| 19 | 0.00069 | 0 | 0 | 2.5 |
| 20 | 0.00034 | 0 | 0 | 1.2 |

**Fig. 2-6** Bit weighting in natural binary for word lengths up to 20 bits.

## B.C.D. Binary coded decimal

When angles have to be displayed in digital form, it is often convenient to have the input to the display in Binary coded decimal format.

The B.C.D. coding for angles is as for other B.C.D. codes where each decimal digit is formed from a group of four binary coded bits. The groups of four binary digits represent the following angular ranges:

0.00° to 0.09° in 0.01° increments

0.0° to 0.9° in 0.1° increments

0.0° to 9.0° in 1° increments

00° to 90° in 10° increments

000° to 300° in 100° increments

Note that in a system requiring a full scale output of 0° to 359.99°, only 2 bits are required in the 100° group. In a system requiring 0° to ±180°, only 1 bit (the 100° bit) is required in the 100° group, the second bit in this group is generally used as the sign bit.

The advantage of the B.C.D. method of coding for display purposes is that the seven segment decoders that go with the displays each only require inputs from four binary bits.

When the output from a synchro to digital converter is required both for computation and for display, it is usual to use an SDC giving a binary output followed by a Binary to B.C.D. converter for producing the display data. When the data is used only for display purposes, Synchro to digital converters are available which give the B.C.D. data directly.

An example of an angle represented in Binary coded decimal form is 276.4° which would be:

|      | 10   | 0111 | 0110 | .   | 0100 |   |
|------|------|------|------|-----|------|---|
| (    | 2    | 7    | 6    | .   | 4    | ) |

### Machine tool scaling (4000 counts)

Machine tool control applications sometimes demand that a full revolution of 360° is represented by 4000 counts. The requirement stems from the fact that the inputs are usually in inches or metric units and divisions of the basic unit into 4000 parts (divisions of 2000 and 1000 are automatically achieved) leads to more easily interpreted sub units.

When the output scaling is in 4000 counts per revolution, the output is often used in serial form with an additional pulse once per revolution for setting the datum point. In addition to the serial output, a level is provided which indicates the direction of rotation. Since the applications of this type of converter are such that many revolutions are often used to represent the movement involved, external counters are used which count the pulses within the 360° as well as the total number of revolutions.

### Military scales (6400 counts)

In some military applications, particularly those involving artillery, it has been found convenient to use the scale of 6400 counts representing 360°. As a consequence of this, Synchro to digital converters are available where the output has a full scale value of 6400 or 6400.0 represented in Binary coded decimal.

### Degrees and Arc. Minutes

It is sometimes necessary to display an angle in degrees and arc. minutes instead of degrees and fractions of a degree. This is done with a B.C.D. representation in a similar way to the degrees and fractions method. For example, 276° 45′ would be:

|      | 10   | 0111 | 0110 | 0100 | 0101 |   |
|------|------|------|------|------|------|---|
| (    | 2    | 7    | 6°   | 4    | 5′   | ) |

Various products are available to perform the binary to Degree and arc. minute B.C.D. conversion.

## LOGIC INPUTS AND OUTPUTS

### Logic types

The products discussed in this book use three main digital input/output types, namely Standard TTL, Low power Schottky TTL (L.S.) and Buffered three-state. The loading details given in the data sheets are given in terms of how many TTL loads the devices are capable of driving in the case of outputs and how many TTL loads they present in the case of inputs.

Because different rules apply to each type of digital output as far as interfacing is concerned, a list of the output devices used internally in each product featuring a digital output is given below. When considering the interfacing and lead length limitations, the information below should be used in conjunction with the data in the appropriate data sheet. It should also be remembered that in most cases a certain amount of the logic output device drive capability is used internally by the converter.

*Standard TTL*

| Product  | Output logic device type          |
|----------|-----------------------------------|
| SBCD1752 | MM5331 (Monolithic Memories Inc)  |
| SBCD1753 | MM5331 (Monolithic Memories Inc)  |
| SBCD1756 | MM5331 (Monolithic Memories Inc)  |
| SBCD1757 | MM5331 (Monolithic Memories Inc)  |
| SDC1602  | 54193                             |
| SDC1603  | 54193                             |
| SDC1604  | 54193                             |

| Product | Output logic device type |
|---------|--------------------------|
| SDC1700 | 54LS191 |
| SDC1702 | 54LS191 |
| SDC1704 | 54LS191 |
| TSL1612 | 54LS83 |

In these devices it is suggested that the user incorporates adequate signal transmission techniques to retain the noise immunity performance of the low power Schottky family.

## Buffered Three-state

| Product | Output logic device type |
|---------|--------------------------|
| SDC1725 | 54LS374 and 54LS173 |
| SDC1726 | 54LS374 and 54LS173 |
| SDC1741 | 54LS374 and 54LS173 |
| SDC1742 | 54LS374 and 54LS173 |

These devices, being Three-state possess the added advantage of buffered outputs.

In interfacing all three categories of products described above over long distances, the use of Schmitt trigger devices, such as the LS132, is advocated at the receiving end.

Note that all the devices mentioned above are used by the extended (military) temperature range products.

## Interfacing TTL outputs with CMOS devices

As inputs, CMOS logic levels are as below:

Logic '1' state $\qquad$ greater than $0.7\ V_{DD}$

Logic '0' state $\qquad$ less than $0.3\ V_{DD}$

where $V_{DD}$ is the highest rail voltage applied to the CMOS device.

When it is required to interface TTL outputs into CMOS devices, an amplification of the logic state changes will be required. A suitable device for doing this is the SN5406, of which one sixth can be used per bit.
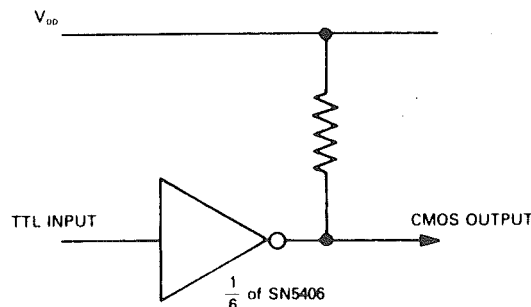
This is shown in Fig. 2-7.



**Fig. 2-7** Interfacing a TTL device to a CMOS device.

Other alternative circuits can be found in chapter 5, vol. 3 of 'Semiconductor Circuit Design' published by Texas Instruments Inc.

# SYNCHRO AND RESOLVER CONNECTION CONVENTIONS

## Introduction

Synchro control transmitters and control transformers each have five wires connected to them. ie. S1, S2, S3, R1 and R2. Concerning the possible permutations of the ways that the wires may be connected, there are two ways that the reference can be connected and for each of these there are six ways that the three signal wires may be connected.

In the case of resolvers, there are S1, S2, S3, and S4 together with R2(R1) and R4(R3). (ie. most resolvers have two rotor windings.) Concerning the number of ways of connecting these there are two ways for the reference and for each of these there are two ways for S1 and S3 and for each of these there are two ways for S2 and S4. ie. there are eight permutations after the three pairs of wires have been sorted out.

Below are definitions which are adopted for the voltages between S1, S2, S3 and S4 and the reference for synchro and resolver use which should remove some of the possible alternatives.

### Synchro definitions

Fig. 2-8 shows how the voltages between the various pairs of wires vary with the output angle of a Singer Gertsch Synchro/Resolver Standard. The positions of the suffixes in the equations is important. A way of defining the voltages which makes the meaning of the suffixes clear is:

If S1 is connected to R2 and both are connected to a dual trace oscilloscope common and S3 is displayed on one trace with R1 displayed on the other trace, the carrier voltages will be in time phase in the first angular quadrant.



$$E\,(S1\,S3) = KE\,(R2\,R1)\,\sin\theta$$
$$E\,(S3\,S2) = KE\,(R2\,R1)\,\sin\,(\theta + 120°)$$
$$E\,(S2\,S1) = KE\,(R2\,R1)\,\sin\,(\theta + 240°)$$

WHERE $R1 = R_{Hi}$  $R2 = R_{Lo}$  ON CONVERTERS

OUTPUTS AS A FUNCTION OF INCREASING ANGLE (FROM ELECTRICAL ZERO) FROM A SINGER GERTSCH DECADE SYNCHRO/RESOLVER STANDARD

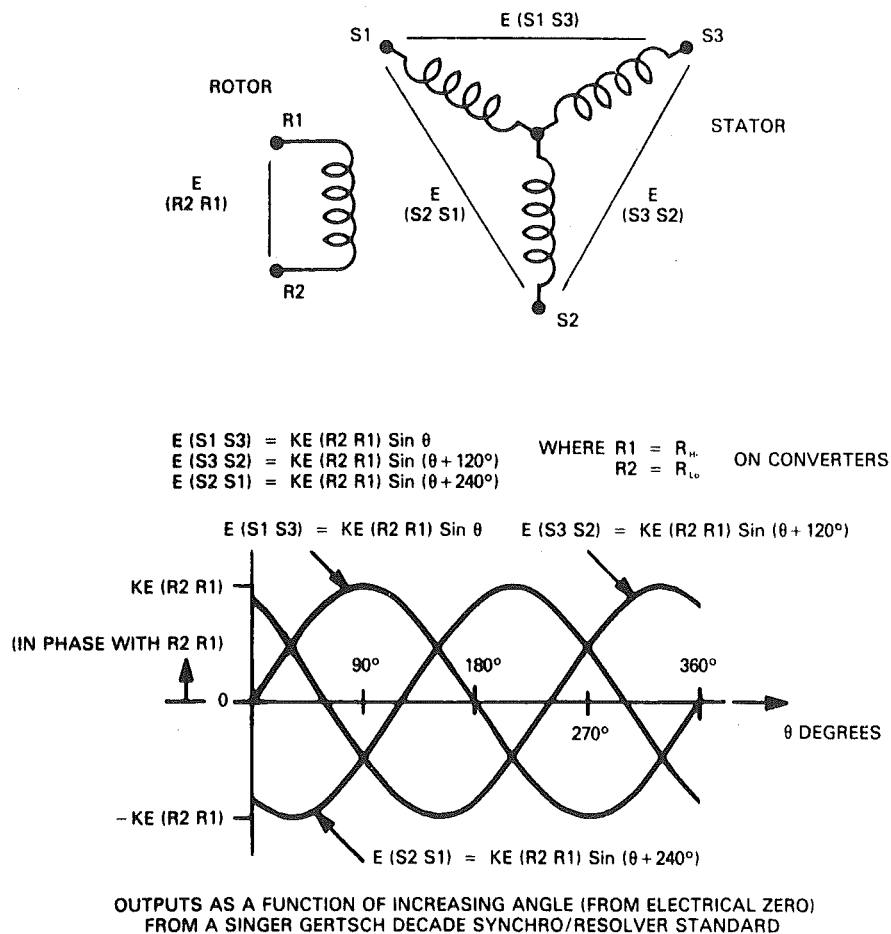**Fig. 2-8** Synchro connection convention.

Fig. 2-9 shows how resolver voltages vary with the output angle of a Singer Gertsch Decade Synchro/Resolver Standard. An alternative way of stating the resolver voltage convention is:

If S3, S4 and R4(R3) are connected together and to a dual trace oscilloscope common, then S2(S1) is in phase with R2(R1) and S1(S4) is 180° out of phase with R2(R1) in the first angular quadrant.

Fig. 2-10 shows the relationship between the voltages on the resolver to digital converters and the synchro to digital converters relative to the Singer Gertsch Decade Synchro/Resolver standard, model DSRS 5DR. All the converters discussed in this book are calibrated using this type of instrument.
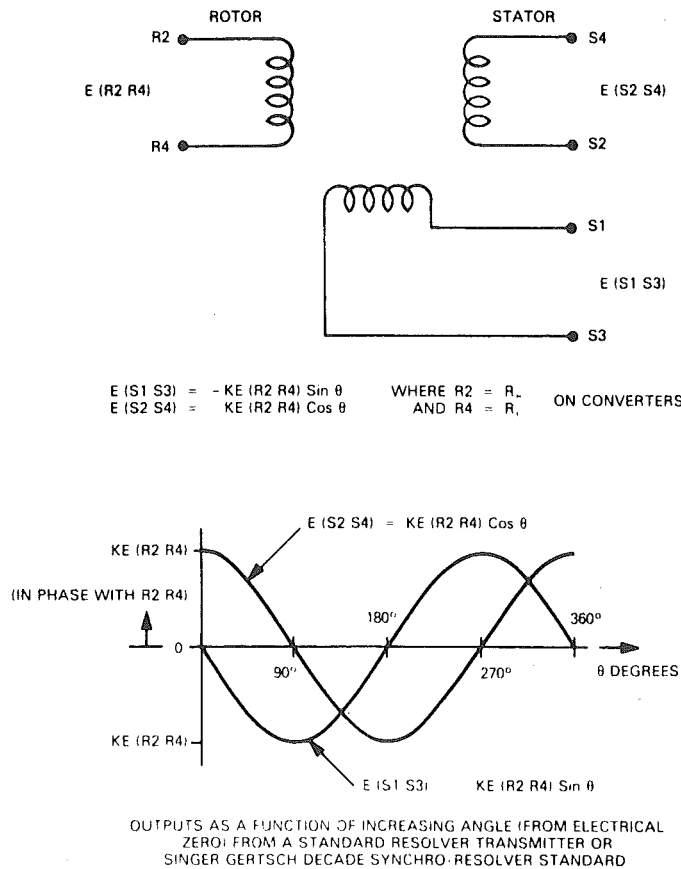


$$E\,(S1\,S3)\;=\;-KE\,(R2\,R4)\,\text{Sin}\,\theta$$
$$E\,(S2\,S4)\;=\;KE\,(R2\,R4)\,\text{Cos}\,\theta$$

WHERE R2 = R$_-$
AND R4 = R$_,$   ON CONVERTERS

OUTPUTS AS A FUNCTION OF INCREASING ANGLE (FROM ELECTRICAL ZERO) FROM A STANDARD RESOLVER TRANSMITTER OR SINGER GERTSCH DECADE SYNCHRO-RESOLVER STANDARD

**Fig. 2-9** Resolver connection convention.

| STANDARD | R2 (R1) RESOLVER I/P | R4 (R3) RESOLVER I/P | S1 (S4) SIN θ | S2 (S1) COS θ | S3 (S2) SIN θ | S4 (S3) COS θ |
|---|---|---|---|---|---|---|
| R/D CONVERTER | $R_{Hi}$ | $R_{Lo}$ | S1 | S2 | S3 | S4 |

RESOLVER CONNECTIONS

| STANDARD | R1 SYNCHRO I/P | R2 SYNCHRO I/P | S1 SYNCHRO O/P | S2 SYNCHRO O/P | S3 SYNCHRO O/P |
|---|---|---|---|---|---|
| S/D CONVERTER | $R_{Hi}$ | $R_{Lo}$ | S1 | S2 | S3 |

SYNCHRO CONNECTIONS

**Fig. 2-10** Singer Gertsch Decade Synchro/Resolver standard, Model DSRS 5DR Connections.