Chapter III

MONOLITHIC INSTRUMENTATION AMPLIFIERS

ADVANTAGES OVER OP AMP IN-AMPS

Monolithic IC instrumentation amplifiers were developed to satisfy the demand for in-amps that would be easier to apply. These circuits incorporate variations in the 3-op amp and 2-op amp in-amp circuits previously described, while providing laser-trimmed resistors and other benefits of monolithic IC technology. Since both active and passive components are now within the same die, they can be closely matched—this will ensure that the device provides a high CMR. In addition, these components will stay matched over temperature, ensuring excellent performance over a wide temperature range. IC technologies such as laser wafer trimming allow monolithic integrated circuits to be tuned up to very high accuracy and provide low cost, high volume manufacturing. An additional advantage of monolithic devices is that they are available in very small, very low cost SOIC, MSOP, or LFCSP

(chip scale) packages designed for use in high volume production. Table 3-1 provides a quick performance summary of Analog Devices in-amps.

Which to Use—an In-Amp or a Diff Amp?

Although instrumentation amplifiers and difference amplifiers share many properties, the first step in the design process should be which type of amplifier to use.

A difference amplifier is basically an op amp subtractor, typically using high value input resistors. The resistors provide protection by limiting the amplifier's input current. They also reduce the input common-mode and differential voltage to a range that can be handled by the internal subtractor amplifier. In general, difference amplifiers should be used in applications where the common-mode voltage or voltage transients may exceed the supply voltage.

Table 3-1. Latest Generation Analog Devices In-Amps Summarized[1]

Product	Features	Power Supply Current Typ	–3 dB BW Typ (G = 10)	CMR G = 10 (dB) Min	Input Offset Voltage Max	V_{OS} Drift (µV/°C) Max	RTI Noise[2] (nV/$\sqrt{Hz}$) (G = 10)	Input Bias Current (nA) Max
AD8221	Precision, high BW	0.9 mA	560 kHz	100[3]	60 µV	0.4	11 max	1.5
AD620	General-purpose	0.9 mA	800 kHz	95[3]	125 µV	1	16 max	2
AD8225	Precision gain = 5	1.1 mA	900 kHz[4]	83[4,5]	150 µV	0.3	45 typ[4]	1.2
AD8220	R-R, JFET input	750 µA	1500 kHz	100	250 µV	5	17 typ	10 pA
AD8222	Dual, precision, high BW	1.8 mA	750 kHz	100[3]	120 µV	0.4	11 max	2
AD8230	R-R, zero drift	2.7 mA	2 kHz	110	10 µV	10	240 typ	1
AD8250	High BW, programmable gain	3.5 mA	3.5 MHz	100	100 µV	1	13 typ	15
AD8251	High BW, programmable gain	3.5 mA	3.5 MHz	100	100 µV	1	13 typ	15
AD8553	Auto-zero with shutdown	1.1 mA	1 kHz	100	20 µV	0.1	150 typ	1
AD8555	Zero drift dig prog	2.0 mA	700 kHz[6]	80[6]	10 µV	0.07	32 typ	22
AD8556	Dig prog IA with filters	2.0 mA	700 kHz[6]	80[6]	10 µV	0.07	32 typ	54
AD622	Low cost	0.9 mA	800 kHz	86[3]	125 µV	1	14 typ	5
AD621	Precise gain	0.9 mA	800 kHz	93[3]	250 µV[7]	2.5[7]	17 max[7]	2
AD623	Low cost, S.S.	375 µA	800 kHz	90[3]	200 µV	2	35 typ	25
AD627	Micropower, S.S.	60 µA	80 kHz	100	250 µV	3	42 typ	10

NOTES

S.S. = single supply.

[1]Refer to ADI website at www.analog.com for latest products and specifications.

[2]At 1 kHz. RTI noise = $\sqrt{((e_{ni})^2 + (e_{no/G})^2)}$.

[3]For dc to 60 Hz, 1 kΩ source imbalance.

[4]Operating at a gain of 5.

[5]For 10 kHz, 1 kΩ source imbalance.

[6]Operating at a gain of 70.

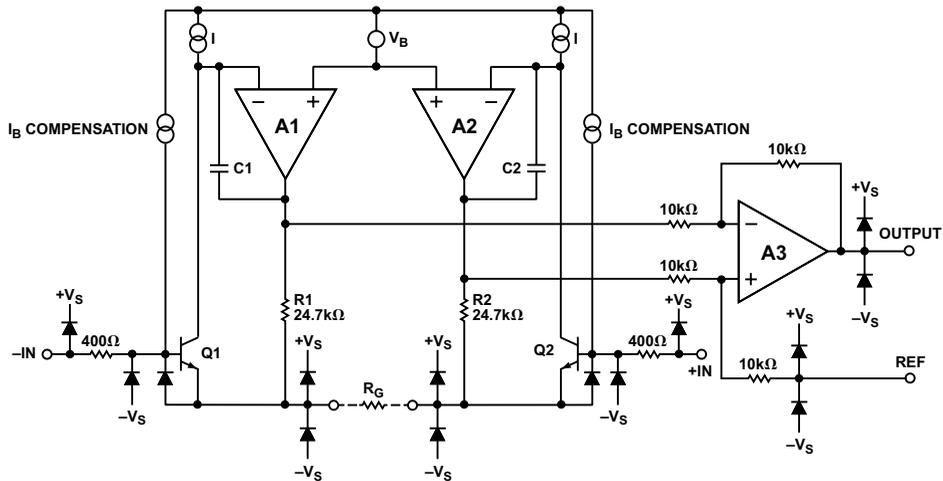[7]Referred to input (RTI).

Figure 3-1. AD8221 simplified schematic.

In contrast, an instrumentation amplifier is most commonly an op amp subtractor with two input buffer amplifiers (these increase the input Z and thus reduce loading of the input source). An in-amp should be used when the total input common-mode voltage plus the input differential voltage, including transients, is less than the supply voltage. In-amps are also needed in applications where the highest accuracy, best signal-to-noise ratio, and lowest input bias current are essential.

MONOLITHIC IN-AMP DESIGN—THE INSIDE STORY

High Performance In-Amps

Analog Devices introduced the first high performance monolithic instrumentation amplifier, the **AD520**, in 1971.

In 2003, the **AD8221** was introduced. This in-amp is in a tiny MSOP package and offers increased CMR at higher bandwidths than other competing in-amps. It also has improved ac and dc specifications over the industry-standard **AD620** series in-amps.

The AD8221 is a monolithic instrumentation amplifier based on the classic 3-op amp topology (Figure 3-1). Input transistors Q1 and Q2 are biased at a constant current so that any differential input signal will force the output voltages of A1 and A2 to be equal. A signal applied to the input creates a current through R_G, R1, and R2 such that the outputs of A1 and A2 deliver the correct voltage. Topologically, Q1, A1, R1 and Q2, A2, R2 can be viewed as precision current feedback amplifiers. The amplified differential and common-mode signals are applied to a difference amplifier, A3, which rejects the common-mode voltage, but processes the differential voltage. The difference amplifier has a low output offset voltage as well as low output offset voltage drift. Laser-trimmed resistors allow for a highly accurate in-amp with gain error typically less than 20 ppm and CMRR that exceeds 90 dB (G = 1).

Using superbeta input transistors and an I_B compensation scheme, the AD8221 offers extremely high input impedance, low I_B, low I_{OS}, low I_B drift, low input bias current noise, and extremely low voltage noise of 8 nV/√Hz.

The transfer function of the AD8221 is

$$G = \frac{49.4\,k\Omega}{R_G} + 1$$

$$R_G = \frac{49.4\,k\Omega}{G - 1}$$

Care was taken to ensure that a user could easily and accurately set the gain using a single external standard value resistor.

Since the input amplifiers employ a current feedback architecture, the AD8221's gain bandwidth product increases with gain, resulting in a system that does not suffer from the expected bandwidth loss of voltage feedback architectures at higher gains.

In order to maintain precision even at low input levels, special care was taken with the AD8221's design and layout, resulting in an in-amp whose performance satisfies even the most demanding applications (see Figures 3-3 and 3-4).

A unique pinout enables the AD8221 to meet an unparalleled CMRR specification of 80 dB at 10 kHz (G = 1) and 110 dB at 1 kHz (G = 1000). The balanced pinout, shown in Figure 3-2, reduces the parasitics that had, in the past, adversely affected CMR performance. In addition, the new pinout simplifies board layout because associated traces are grouped. For example, the gain setting resistor pins are adjacent to the inputs, and the reference pin is next to the output.
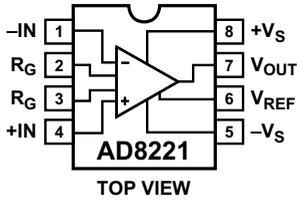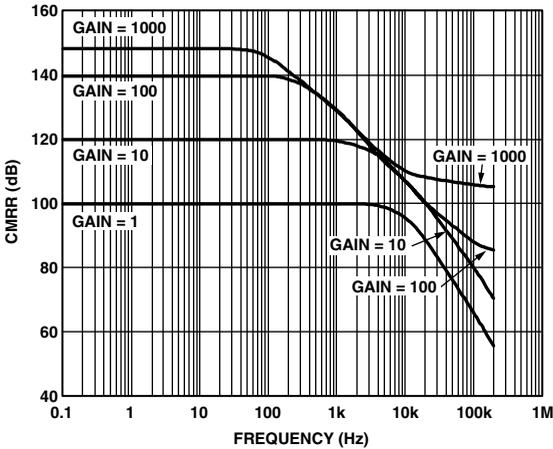

Figure 3-2. AD8221 pinout.

Figure 3-3. CMRR vs. frequency (RTI) of the AD8221.
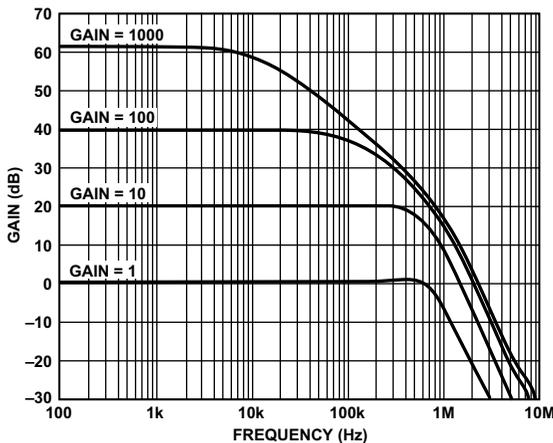
Figure 3-4. AD8221 closed-loop gain vs. frequency.

The **AD8222** (Figure 3-5) is a dual version of the AD8221 in-amp, with similar performance and specifications. Its small size allows more amplifiers per PC board. In addition, the AD8222 is the first in-amp to be specified for differential output performance. It is available in a 4 mm × 4 mm, 16-lead LFCSP package.
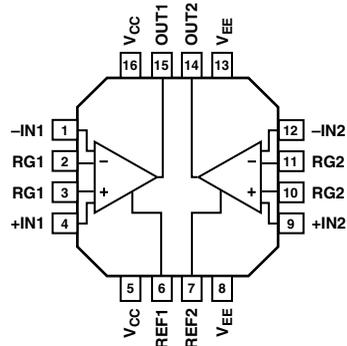
Figure 3-5. AD8222 connection diagram.

For many years, the **AD620** has been the industry-standard, high performance, low cost in-amp. The AD620 is a complete monolithic instrumentation amplifier offered in both 8-lead DIP and SOIC packages. The user can program any desired gain from 1 to 1000 using a single external resistor. By design, the required resistor values for gains of 10 and 100 are standard 1% metal film resistor values.
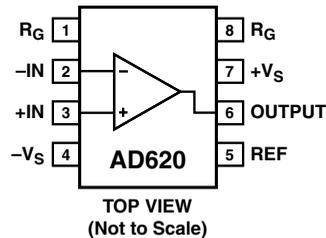

Figure 3-6. AD620 pin configuration.

The AD620 (see Figure 3-7) is a second-generation version of the classic **AD524** in-amp and embodies a modification of its 3-op amp circuit. Laser trimming of on-chip thin film resistors, R1 and R2, allows the user to accurately set the gain to 100 within ±0.3% max error, using only one external resistor. Monolithic construction and laser wafer trimming allow the tight matching and tracking of circuit components.

A preamp section comprised of Q1 and Q2 provides additional gain up front. Feedback through the Q1-A1-R1 loop and the Q2-A2-R2 loop maintains a constant collector current through the input devices Q1 and Q2,
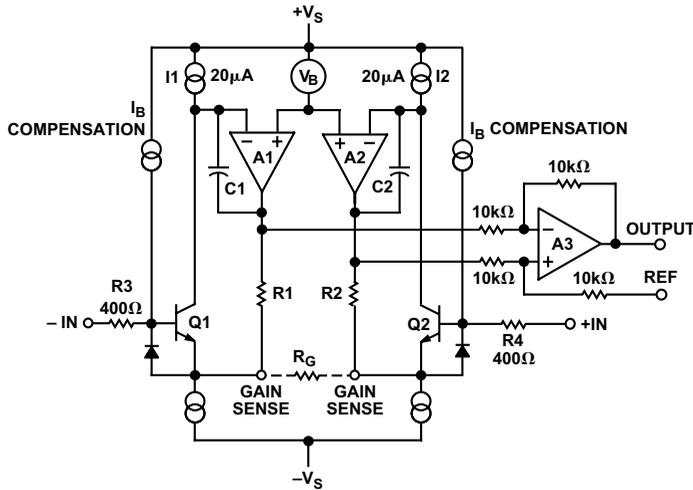
Figure 3-7. A simplified schematic of the AD620.

thereby impressing the input voltage across the external gain setting resistor, R_G. This creates a differential gain from the inputs to the A1/A2 outputs given by $G = (R1 + R2)/R_G + 1$. The unity-gain subtractor, A3, removes any common-mode signal, yielding a single-ended output referred to the REF pin potential.

The value of R_G also determines the transconductance of the preamp stage. As R_G is reduced for larger gains, the transconductance increases asymptotically to that of the input transistors. This has important advantages: First, the open-loop gain is boosted for increasing programmed gain, thus reducing gain related errors. Second, the gain bandwidth product (determined by C1, C2, and the preamp transconductance) increases with programmed gain, thus optimizing the amplifier's frequency response. Figure 3-8 shows the AD620's closed-loop gain vs. frequency.

The AD620 also has superior CMR over a wide frequency range, as shown in Figure 3-9.

Figure 3-9. AD620 CMR vs. frequency.

Figure 3-8. AD620 closed-loop gain vs. frequency.
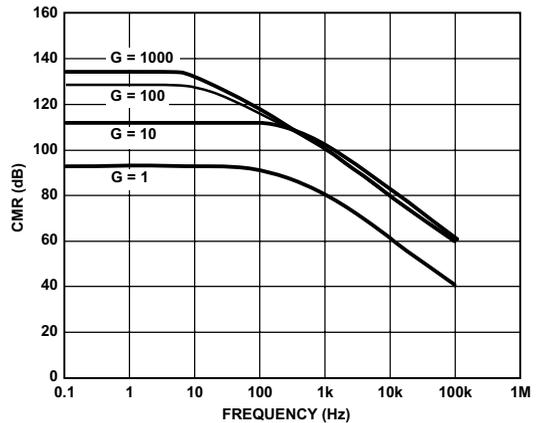
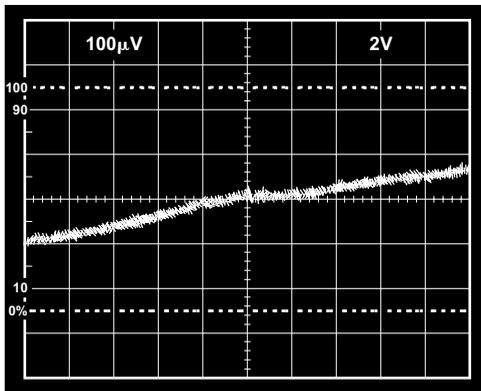Figures 3-10 and 3-11 show the AD620's gain nonlinearity and small signal pulse response.

Figure 3-10. AD620 gain nonlinearity
(G = 100, R_L = 10 kΩ, vertical scale: 100 μV =
10 ppm, horizontal scale: 2 V/div).

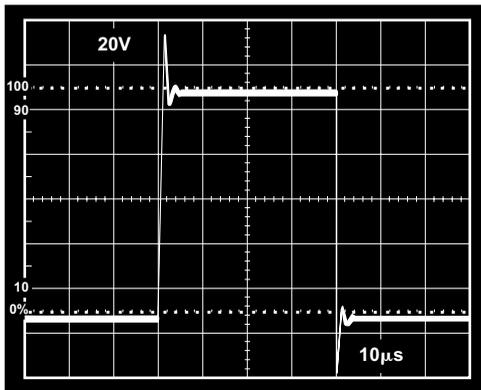
Figure 3-11. Small signal pulse response of
the AD620 (G = 10, R_L= 2 kΩ, C_L = 100 pF).

Finally, the input voltage noise is reduced to a value of 9 nV/√Hz, determined mainly by the collector current and base resistance of the input devices.

The internal gain resistors, R1 and R2, are trimmed to an absolute value of 24.7 kΩ, allowing the gain to be programmed accurately with a single external resistor. The gain equation is then

$$G = \frac{49.4\,\text{k}\Omega}{R_G} + 1$$

So that

$$R_G = \frac{49.4\,\text{k}\Omega}{G - 1}$$

Where resistor R_G is in kΩ.

The value of 24.7 kΩ was chosen so that standard 1% resistor values could be used to set the most popular gains.

Low Cost In-Amps
The **AD622** is a low cost version of the AD620 (see Figure 3-6). The AD622 uses streamlined production methods to provide most of the performance of the AD620 at lower cost.

Figures 3-12, 3-13, and 3-14 show the AD622's CMR vs. frequency, gain nonlinearity, and closed-loop gain vs. frequency.
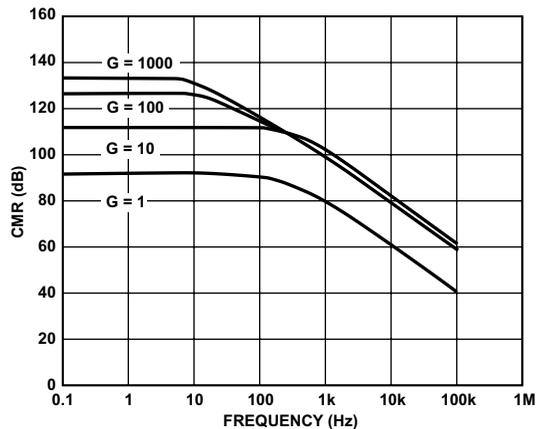

Figure 3-12. AD622 CMR vs. frequency
((RTI) 0 to 1 kΩ source imbalance).

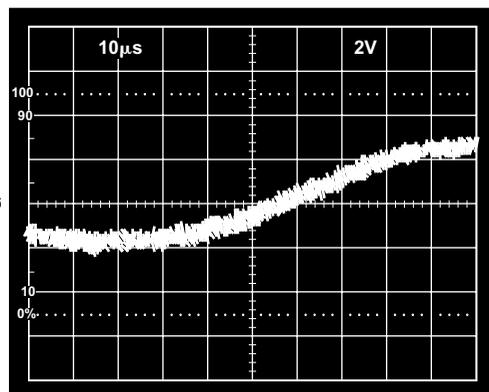Figure 3-13. AD622 Gain nonlinearity
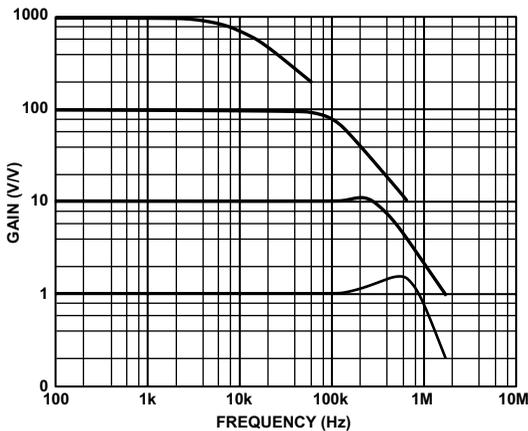(G = 1, R_L = 10 kΩ, vertical scale: 20 μV = 2 ppm).

Figure 3-14. AD622 closed-loop
gain vs. frequency.

Pin-Programmable, Precise Gain In-Amps

The **AD621** is similar to the AD620, except that for gains of 10 and 100 the gain setting resistors are on the die—no external resistors are used. A single external jumper (between Pins 1 and 8) is all that is needed to select a gain of 100. For a gain of 10, leave Pin 1 and Pin 8 open. This provides excellent gain stability over temperature, as the on-chip gain resistor tracks the TC of the feedback resistor. Figure 3-15 is a simplified schematic of the AD621. With a max total gain error of 0.15% and ±5 ppm/°C gain drift, the AD621 has much greater built-in accuracy than the AD620.

The AD621 may also be operated at gains between 10 and 100 by using an external gain resistor, although gain error and gain drift over temperature will be degraded. Using external resistors, device gain is equal to
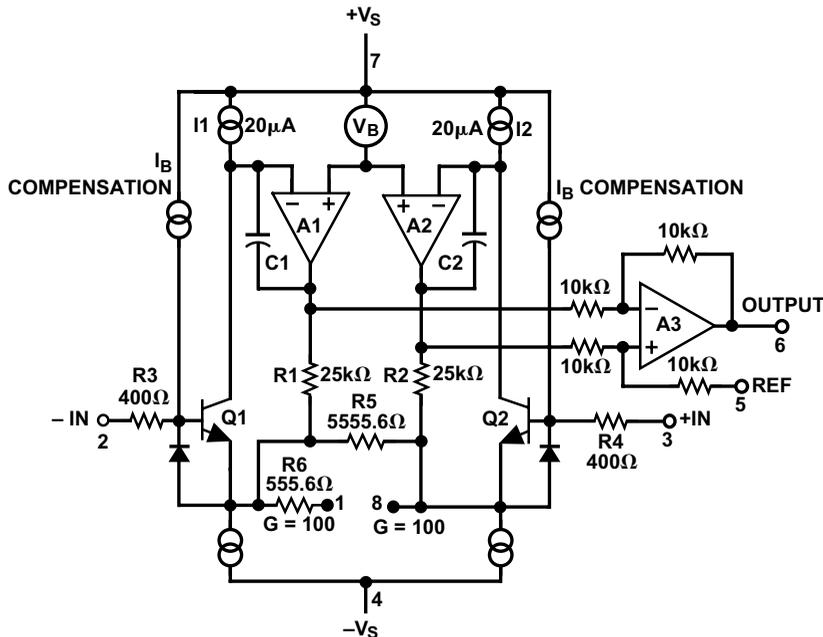
$$G = (R1 + R2)/R_G + 1$$

Figure 3-15. A simplified schematic of the AD621.

Figures 3-16 and 3-17 show the AD621's CMR vs. frequency and closed-loop gain vs. frequency.
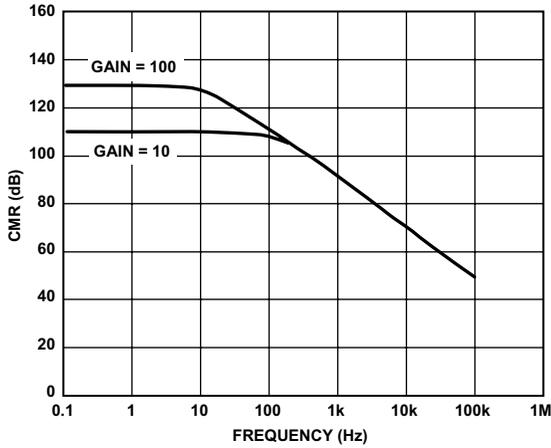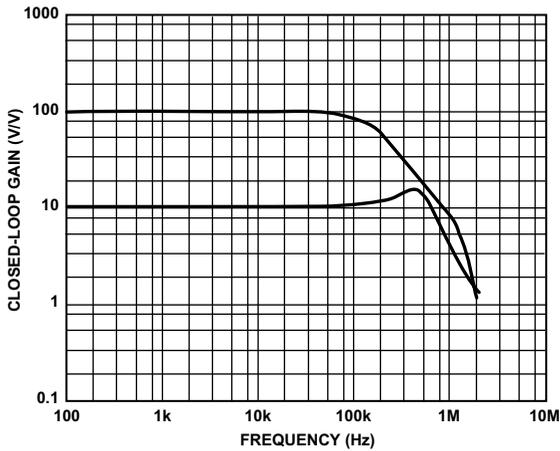
Figures 3-18 and 3-19 show the AD621's gain nonlinearity and small signal pulse response.

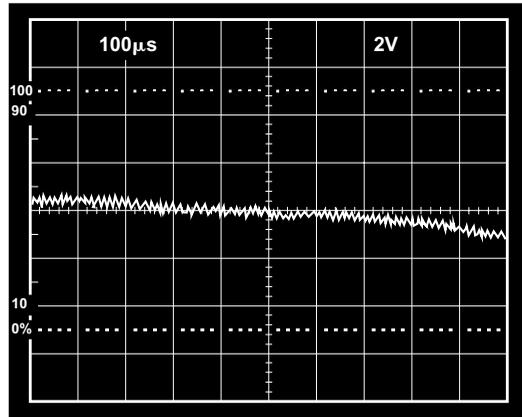Figure 3-16. AD621 CMR vs. frequency.

Figure 3-18. AD621 gain nonlinearity ($G = 10$, $R_L = 10$ kΩ, vertical scale: 100 μV/div = 100 ppm/div, horizontal scale 2 V/div).

Figure 3-17. AD621 closed-loop gain vs. frequency.
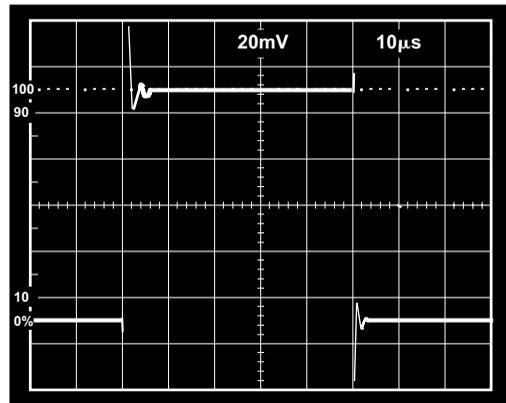

Figure 3-19. Small signal pulse response of the AD621 ($G = 10$, $R_L = 2$ kΩ, $C_L = 100$ pF).
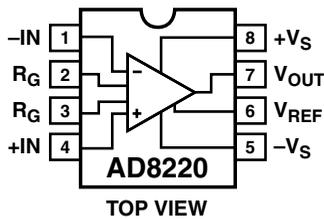
Figure 3-20. AD8220 connection diagram.

The **AD8220** is a FET input, gain-programmable, high performance instrumentation amplifier with a max input bias current of 10 pA. It also features excellent high frequency common-mode rejection (see Figure 3-20). The AD8220 maintains a minimum CMRR of 70 dB up to 20 kHz, at G = 1. The combination of extremely high input impedance and high CMRR over frequency makes the AD8220 useful in applications such as patient monitoring. In these applications, input impedance is high and high frequency interference must be rejected.

The rail-to-rail output, low power consumption and small MSOP/CSP package make this precision instrumentation amplifier attractive for use in multi-channel applications.
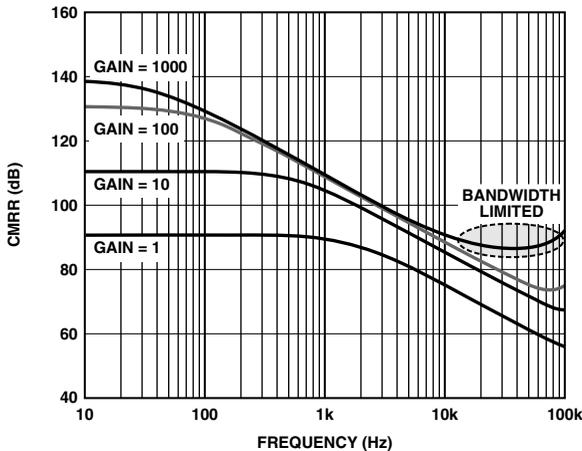

Figure 3-21. Typical AD8220 CMRR vs. frequency.

A single resistor sets the gain from 1 to 1000. The AD8220 operates on both single and dual supplies and is well-suited for applications where input voltages close to those of the supply are encountered. In addition, its rail-to-rail output stage allows for maximum dynamic range, when constrained by low single-supply voltages.

Auto-Zeroing Instrumentation Amplifiers
Auto-zeroing is a dynamic offset and drift cancellation technique that reduces input referred voltage offset to the μV level, and voltage offset drift to the nV/°C level.

The **AD8230** (Figure 3-22) is an instrumentation amplifier that utilizes an auto-zeroing topology and combines it with high common-mode signal rejection.
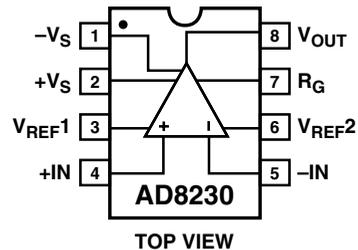

Figure 3-22. AD8230 connection diagram.

The internal signal path consists of an active differential sample-and-hold stage (preamp), followed by a differential amplifier (gain amp). Both amplifiers implement auto-zeroing to minimize offset and drift. A fully differential topology increases the immunity of the signals to parasitic noise and temperature effects. Amplifier gain is set by two external resistors for convenient TC matching. The AD8230 can accept input common-mode voltages within and including the supply voltages ($\pm 5\,V$).

The signal sampling rate is controlled by an on-chip, 10 kHz oscillator and logic to derive the required nonoverlapping clock phases. For simplification of the functional description, two sequential clock phases, A and B, will be used to distinguish the order of internal operation as depicted in Figures 3-23 and 3-24, respectively.

During Phase A, the sampling capacitors are connected to the input signals at the common-mode potential. The input signal's difference voltage, V_{DIFF}, is stored across the sampling capacitors, C_{SAMPLE}. The common-mode potential of the input affects C_{SAMPLE} insofar as the sampling capacitors are at a different common-mode potential than the preamp. During this period, the gain amp is disconnected from the preamp so that its output remains at the level set by the previously sampled input signal, held on C_{HOLD} in Figure 3-23.

In Phase B, upon sampling the analog input signals, the input common-mode component is removed. The common-mode output of the preamp is held at the reference potential, V_{REF}. When the bottom plates of the sampling capacitors connect to the output of the preamp, the input signal common-mode voltage is pulled to the amplifier's common-mode voltage, V_{REF}. In this manner, the sampling capacitors are brought to the same common-mode voltage as the preamp. The remaining differential signal is presented to the gain amp, refreshing the hold capacitors' signal potentials, as shown in Figure 3-24.

Figures 3-25 through 3-28 show the internal workings of the AD8230 in depth. As noted, both the preamp and gain amp auto-zero. The preamp auto-zeroes during phase A, shown in Figure 3-25, while the sampling caps are connected to the signal source. By connecting the
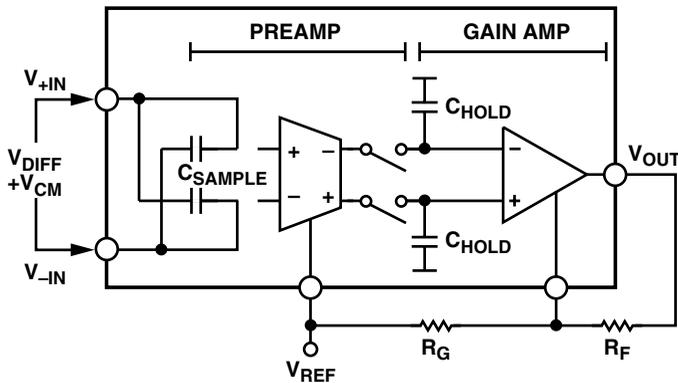

Figure 3-23. The AD8230 in Phase A sampling phase. The differential component of the input signal is stored on sampling capacitors, C_{SAMPLE}. The gain amp conditions the signal stored on the hold capacitors, C_{HOLD}. Gain is set with the R_G and R_F resistors.
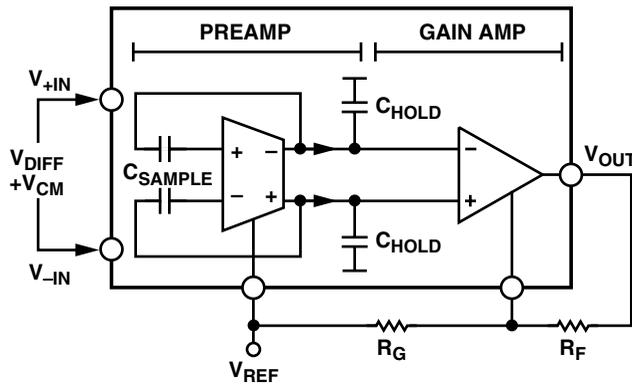

Figure 3-24. In Phase B, the differential signal is transferred to the hold capacitors, refreshing the value stored on C_{HOLD}. The gain amp continues to condition the signal stored on the hold capacitors, C_{HOLD}.

preamp differential inputs together, the resulting output referred offset is connected to an auxiliary input port to the preamp. Negative feedback operation forces a canceling potential at the auxiliary port, which is subsequently held on a storage capacitor, C_{P_HOLD}.

While in Phase A, the gain amp shown in Figure 3-26 reads the previously sampled signal held on the holding capacitors, C_{HOLD}. The gain amp implements feedforward offset compensation to allow for transparent nulling of

the main amp and a continuous output signal. A differential signal regimen is maintained throughout the main amp and feedforward nulling amp by utilizing a double differential input topology. The nulling amp compares the input of the two differential signals. As a result, the offset error is fed into the null port of the main amp, V_{NULL}, and stored on C_{M_HOLD}. This operation effectively forces the differential input potentials at both the signal and feedback ports of the main amp to be equal. This is the requirement for zero offset.
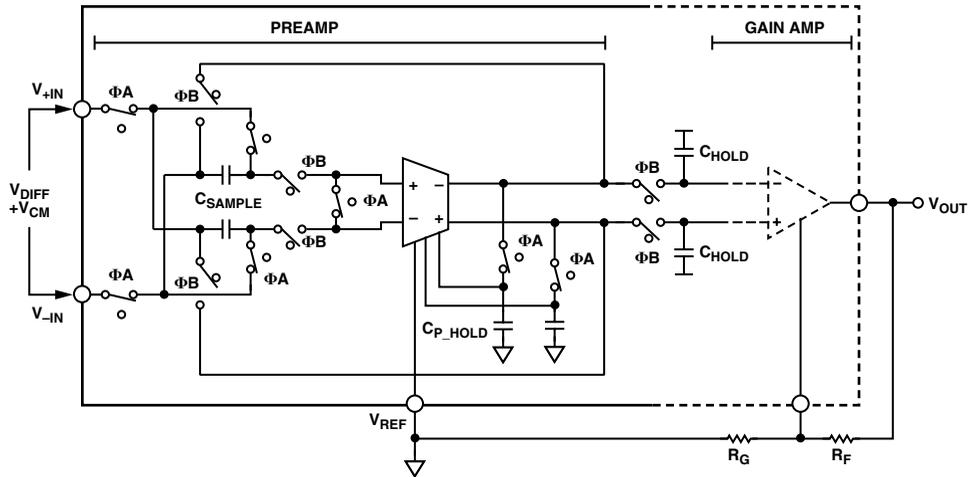

Figure 3-25. Detailed schematic of the preamp during Phase A. The differential signal is stored on the sampling capacitors. Concurrently, the preamp nulls its own offset and stores the correction voltage on its hold capacitors, C_{P_HOLD}.
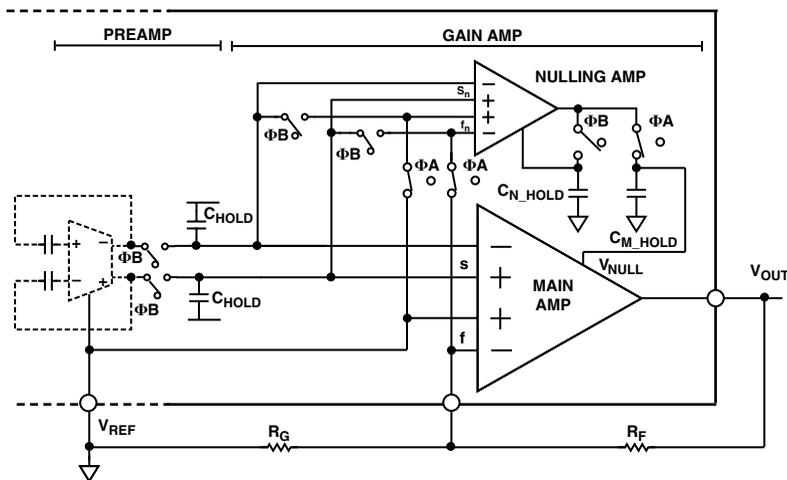

Figure 3-26. Detailed schematic of the gain amp during Phase A. The main amp conditions the signal held on the hold capacitors, C_{HOLD}. The nulling amplifier forces the inputs of the main amp to be equal by injecting a correction voltage into the V_{NULL} port, removing the offset of the main amp. The correction voltage is stored on C_{M_HOLD}.

During Phase B, the inputs of the preamp are no longer shorted, and the sampling capacitors are connected to the input and output of the preamp as shown in Figure 3-27. The preamp, having been auto-zeroed in Phase A, has minimal offset. When the sampling capacitors are connected to the preamp, the common mode of the sampling capacitors is brought to V_{REF}. The preamp outputs the difference signal onto the hold capacitors, C_{HOLD}.

The main amp continues to output the gained difference signal, shown in Figure 3-28. Its offset is kept to a minimum by using the nulling amp's correction potential stored on C_{M_HOLD} from the previous phase. During this phase, the nulling amp compares its two differential inputs and corrects its own offset by driving a correction voltage into its nulling port and, ultimately, onto C_{N_HOLD}. In this fashion, the nulling amp reduces its own offset in Phase B before it corrects for the main amp's offset in the next phase, Phase A.
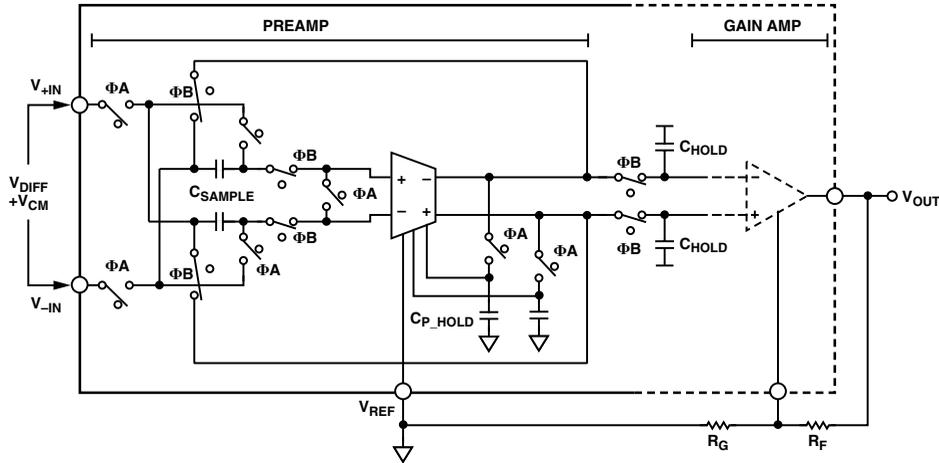

Figure 3-27. Detailed schematic of the preamp during Phase B. The preamp's offset remains low because it was corrected in the previous phase. The sampling capacitors connect to the input and output of the preamp, and the difference voltage is passed onto the holding capacitors, C_{HOLD}.
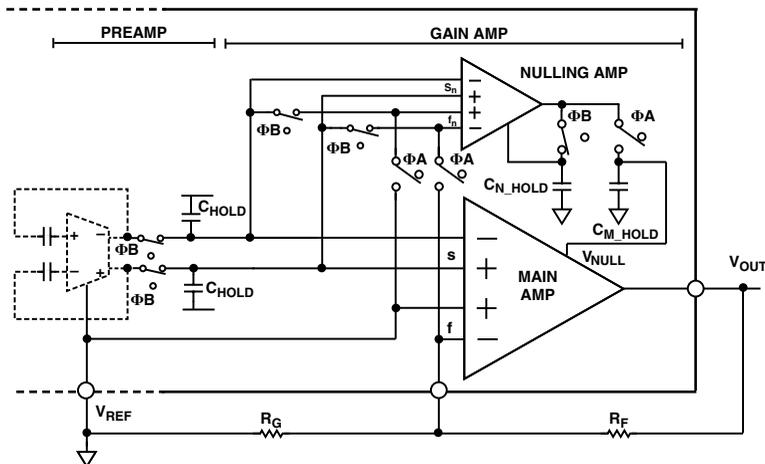

Figure 3-28. Detailed schematic of the gain amp during Phase B. The nulling amplifier nulls its own offset by injecting a correction voltage into its own auxiliary port and storing it on C_{N_HOLD}. The main amplifier continues to condition the differential signal held on C_{HOLD}, yet maintains minimal offset because its offset was corrected in the previous phase.

Two external resistors set the gain of the AD8230. The gain is expressed in the following function:
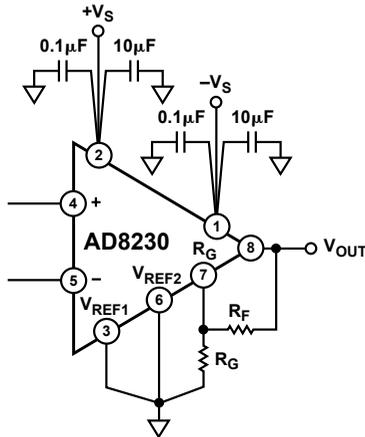
$$Gain = 2\left(1 + \frac{R_F}{R_G}\right)$$

Figure 3-29. Gain setting.

Table 3-2. Gains Using Standard 1% Resistors

Gain	R_F	R_G	Actual Gain
2	0 Ω (short)	None	2
10	8.06 kΩ	2 kΩ	10
50	12.1 kΩ	499 Ω	50.5
100	9.76 kΩ	200 Ω	99.6
200	10 kΩ	100 Ω	202
500	49.9 kΩ	200 Ω	501
1000	100 kΩ	200 Ω	1002

Figure 3-29 and Table 3-2 provide an example of some gain settings. As Table 3-2 shows, the AD8230 accepts a wide range of resistor values. Since the instrumentation ampmlifier has finite driving capability, ensure that the output load in parallel with the sum of the gain setting resistors is greater than 2 kΩ.

$$R_L \| (R_F + R_G) > 2 \text{ k}\Omega$$

Offset voltage drift at high temperature can be minimized by keeping the value of the feedback resistor, R_F, small. This is due to the junction leakage current on the R_G pin, Pin 7.

Figure 3-30 shows the AD8230's common-mode rejection vs. frequency. Figure 3-31 is a plot of AD8230's gain flatness vs. frequency at a gain of 10.
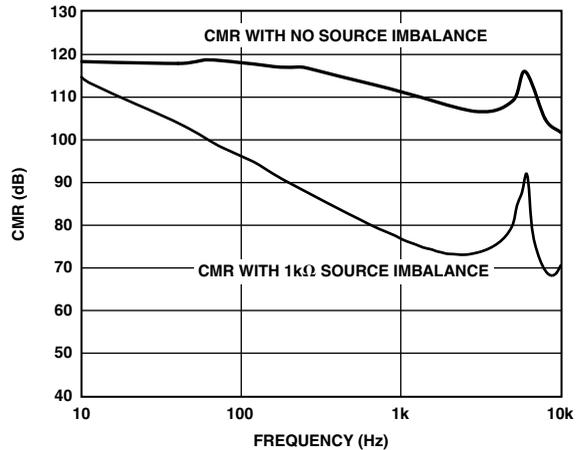

Figure 3-30. Common-mode rejection vs. frequency.
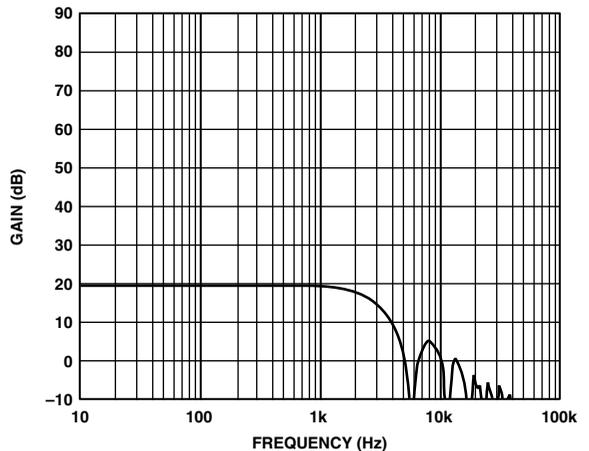

Figure 3-31. Gain vs. frequency, G = 10.

The **AD8553** is a precision current-mode auto-zero instrumentation amplifier capable of single-supply operation. The current-mode correction topology results in excellent accuracy, without the need for trimmed resistors on the die.
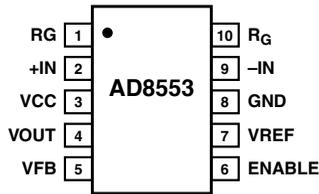
Figure 3-32. AD8553 connection diagram.

Figure 3-32 is the AD8553 connection diagram while Figure 3-33 shows a simplified schematic illustrating the basic operation of the AD8553 (without correction). The circuit consists of a voltage-to-current amplifier (M1 to M6), followed by a current-to-voltage amplifier (R2 and A1). Application of a differential input voltage forces a current through external resistor R1, resulting in conversion of the input voltage to a signal current. Transistors M3 to M6 transfer twice this signal current to the inverting input of the op amp A1. Amplifier A1 and external resistor R2 form a current-to-voltage converter to produce a rail-to-rail output voltage at VOUT.

Op amp A1 is a high precision auto-zero amplifier. This amplifier preserves the performance of the autocorrection current-mode amplifier topology while offering the user a true voltage-in, voltage-out instrumentation amplifier. Offset errors are corrected internally.

An external reference voltage is applied to the noninverting input of A1 for output-offset adjustment. Because the AD8553 is essentially a *chopper* in-amp, some type of low-pass filtering of the ouput is usually required. External capacitor C2 is used to filter out high frequency noise.

The pinout of the AD8553 allows the user to access the signal current from the output of the voltage-to-current converter (Pin 5). The user can choose to use the AD8553 as a current-output device instead of a voltage-output device.

The **AD8555** is a zero-drift, sensor signal amplifier with digitally programmable gain and output offset. Designed to easily and accurately convert variable pressure sensor and strain bridge outputs to a well-defined output voltage range, the AD8555 also accurately amplifies many other differential or single-ended sensor outputs.

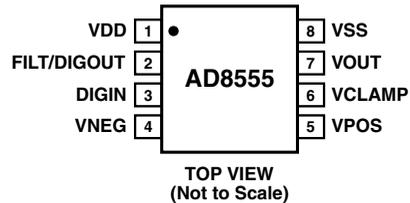Figure 3-34 shows the pinout and Figure 3-35 the simplified schematic.

Figure 3-34. AD8555 connection diagram.

The AD8555 (and **AD8556**) use both auto-zeroing and "chopping" techniques to maintin zero drift. A1, A2, R1, R2, R3, P1, and P2 form the first gain stage of the differential amplifier. A1 and A2 are auto-zeroed op amps that minimize input offset errors. P1 and P2 are digital potentiometers, guaranteed to be monotonic. Programming P1 and P2 allows the first stage gain to be varied from 4.0 to 6.4 with 7-bit resolution, giving a fine gain adjustment resolution of 0.37%. R1, R2, R3, P1, and P2 each have a similar temperature coefficient, so the first stage gain temperature coefficient is lower than 100 ppm/°C.
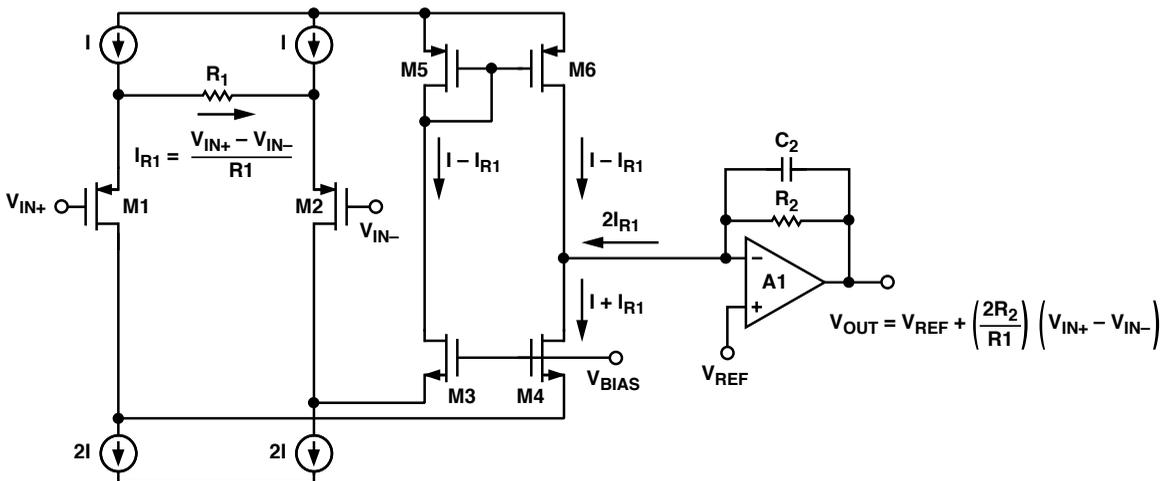

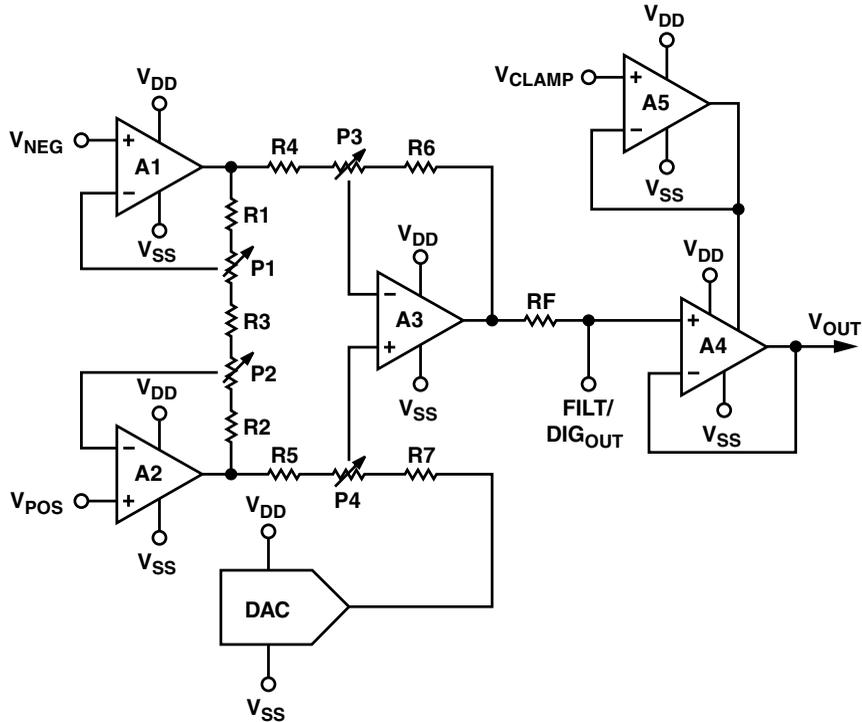*Figure 3-33. AD8553 simplified schematic.*

Figure 3-35. AD8555 simplified schematic.

A3, R4, R5, R6, R7, P3, and P4 form the second gain stage of the differential amplifier. A3 is also an auto-zeroed op amp that minimizes input offset errors. P3 and P4 are digital potentiometers, allowing the second stage gain to be varied from 17.5 to 200 in eight steps; they allow the gain to be varied over a wide range. R4, R5, R6, R7, P3, and P4 each have a similar temperature coefficient, so the second stage gain temperature coefficient is lower than 100 ppm/°C.

A5 implements a voltage buffer, which provides the positive supply to the amplifier output buffer A4. Its function is to limit V_{OUT} to a maximum value, useful for driving analog-to-digital converters (ADC) operating on supply voltages lower than V_{DD}. The input to A5, V_{CLAMP}, has a very high input resistance. It should be connected to a known voltage and not left floating. However, the high input impedance allows the clamp voltage to be set using a high impedance source (e.g., a potential divider). If the maximum value of V_{OUT} does not need to be limited, V_{CLAMP} should be connected to V_{DD}.

A4 implements a rail-to-rail input and output unity-gain voltage buffer. The output stage of A4 is supplied from a buffered version of V_{CLAMP} instead of V_{DD}, allowing the positive swing to be limited. The maximum output current is limited between 5 to 10 mA.

An 8-bit digital-to-analog converter (DAC) is used to generate a variable offset for the amplifier output. This DAC is guaranteed to be monotonic. To preserve the ratiometric nature of the input signal, the DAC references are driven from V_{SS} and V_{DD}, and the DAC output can swing from V_{SS} (Code 0) to V_{DD} (Code 255). The 8-bit resolution is equivalent to 0.39% of the difference between V_{DD} and V_{SS} (e.g., 19.5 mV with a 5 V supply). The DAC output voltage (V_{DAC}) is given approximately by

$$V_{DAC} \approx \left(\frac{Code + 0.5}{256} \right) \left(V_{DD} - V_{SS} \right) + V_{SS}$$

The temperature coefficient of V_{DAC} is lower than 200 ppm/°C.

The amplifier output voltage (V_{OUT}) is given by

$$V_{OUT} = GAIN\left(V_{POS} - V_{NEG}\right) + V_{DAC}$$

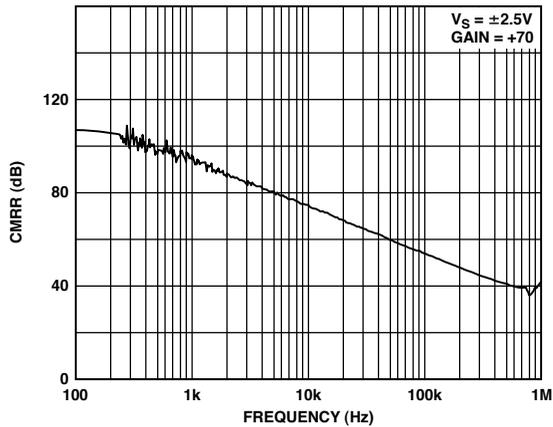where GAIN is the product of the first and second stage gains.

Figure 3-36. AD8555 CMRR vs. frequency.

Figures 3-36 and 3-37 show the AD8555's CMRR vs. frequency and its closed-loop gain vs. frequency.

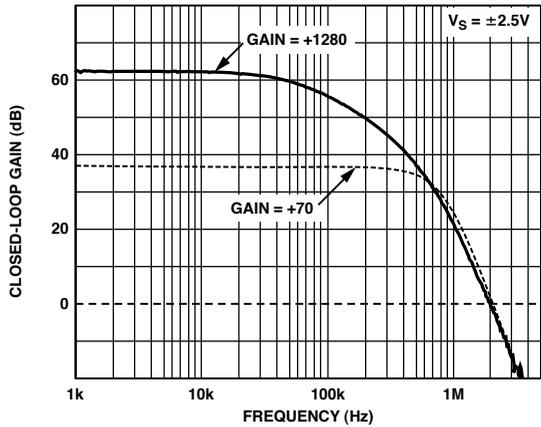See the AD8555 product data sheet for more details.

Figure 3-37. AD8555 closed-loop gain vs. frequency measured at output pin.

The **AD8556** is essentially the same product as the AD8555, except that the former includes internal RFI filtering. The block diagram for the AD8556 is shown in Figure 3-38. For theory of operation, refer to the previous section that covers the AD8555.
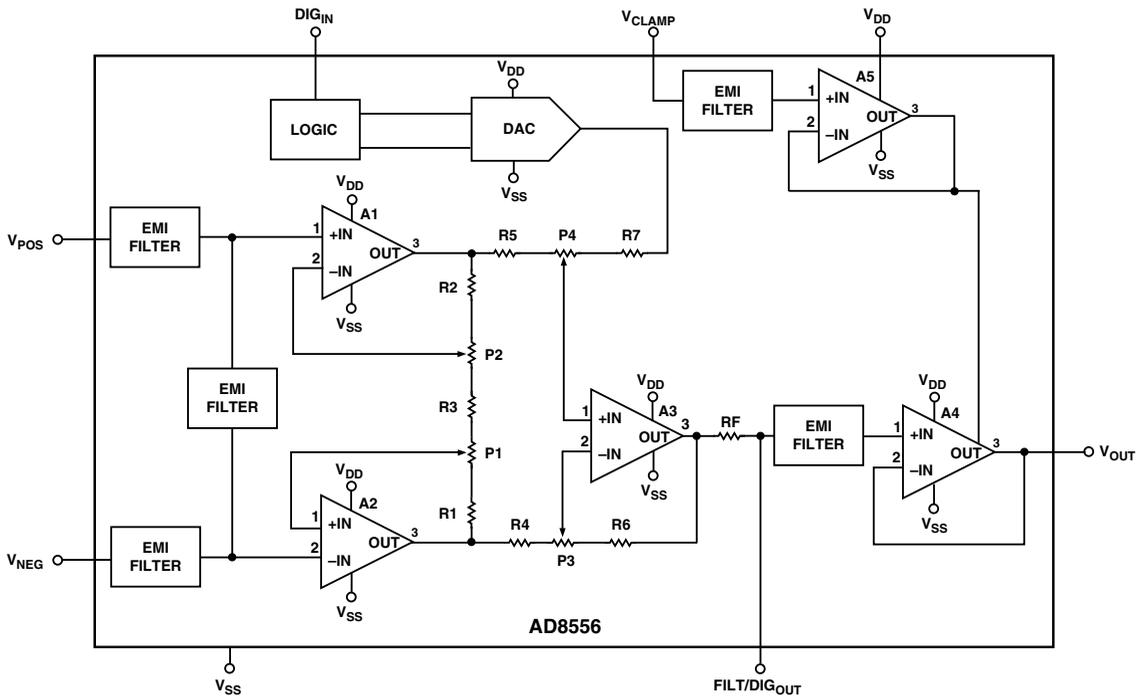

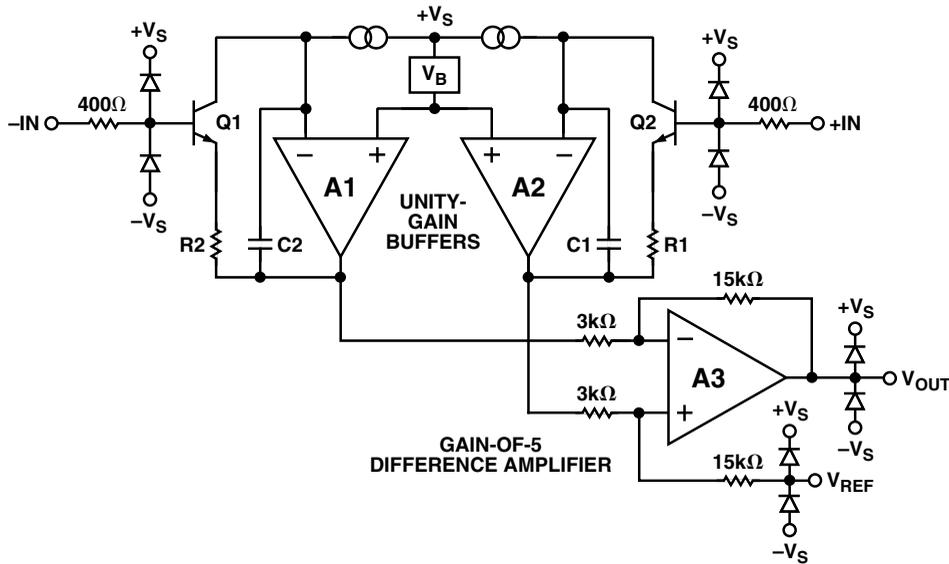Figure 3-38. AD8556 block diagram showing EMI/RFI built-in filters.

Figure 3-39. AD8225 simplified schematic.

Fixed Gain (Low Drift) In-Amps

The **AD8225** is a precision, gain-of-5, monolithic in-amp. Figure 3-39 shows that it is a 3-op amp instrumentation amplifier. The unity-gain input buffers consist of superbeta NPN transistors Q1 and Q2 and op amps A1 and A2. These transistors are compensated so that their input bias currents are extremely low, typically 100 pA or less. As a result, current noise is also low, only 50 fA/$\sqrt{\text{Hz}}$. The input buffers drive a gain-of-5 difference amplifier. Because the 3 kΩ and 15 kΩ resistors are ratio matched, gain stability is better than 5 ppm/$^\circ$C over the rated temperature range.

The AD8225 has a wide gain bandwidth product, resulting from its being compensated for a fixed gain of 5, as opposed to the usual unity-gain compensation of variable gain in-amps. High frequency performance is also enhanced by the innovative pinout of the AD8225. Since Pin 1 and Pin 8 are uncommitted, Pin 1 may be connected to Pin 4. Since Pin 4 is also ac common, the stray capacitance at Pins 2 and 3 is balanced.

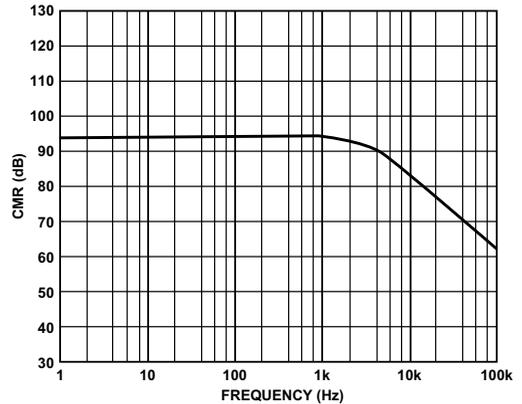Figure 3-40 shows the AD8225's CMR vs. frequency while Figure 3-41 shows its gain nonlinearity.
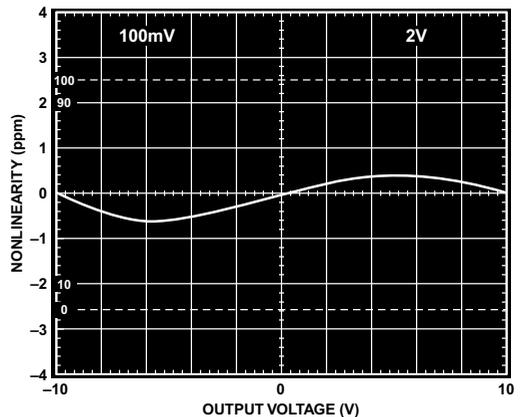

Figure 3-40. AD8225 CMR vs. frequency.

Figure 3-41. AD8225 gain nonlinearity.

3-16

**Monolithic In-Amps Optimized for
Single-Supply Operation**

Single-supply in-amps have special design problems that need to be addressed. The input stage must be able to amplify signals that are at ground potential (or very close to ground), and the output stage needs to be able to swing to within a few millivolts of ground or the supply rail. Low power supply current is also important. And, when operating from low power supply voltages, the in-amp needs to have an adequate gain bandwidth product, low offset voltage drift, and good CMR vs. gain and frequency.

The **AD623** is an instrumentation amplifier based on the 3-op amp in-amp circuit, modified to ensure operation on either single- or dual-power supplies, even at common-mode voltages at, or even below, the negative supply rail (or below *ground* in single-supply operation). Other features include rail-to-rail output voltage swing, low supply current, MSOP packaging, low input and output voltage offset, microvolt/dc offset level drift, high common-mode rejection, and only one external resistor to set the gain.

As shown in Figure 3-42, the input signal is applied to PNP transistors acting as voltage buffers and dc level shifters. A resistor trimmed to within 0.1% of 50 kΩ in each amplifier's (A1 and A2) feedback path ensures accurate gain programmability.

The differential output is

$$\left(V_O = 1 + \frac{100\,\text{k}\Omega}{R_G}\right)V_C$$

where R_G is in kΩ.

The differential voltage is then converted to a single-ended voltage using the output difference amplifier, which also rejects any common-mode signal at the output of the input amplifiers.

Since all the amplifiers can swing to either supply rail, as well as have their common-mode range extended to below the negative supply rail, the range over which the AD623 can operate is further enhanced.

Note that the base currents of Q1 and Q2 flow directly *out* of the input terminals, unlike dual-supply, input-current-compensated in-amps such as the AD620. Since the inputs (i.e., the bases of Q1 and Q2) can operate at ground (i.e., 0 V or, more correctly, 200 mV below ground), it is not possible to provide input current compensation for the AD623. However, the input bias current of the AD623 is still very small: only 25 nA max.

The output voltage at Pin 6 is measured with respect to the *reference* potential at Pin 5. The impedance of the reference pin is 100 kΩ. Internal ESD clamping diodes allow the input, reference, output, and gain terminals of the AD623 to safely withstand overvoltages of 0.3 V above or below the supplies. This is true for all gains, and with power on or off. This last case is particularly important, since the signal source and the in-amp may be powered separately. If the overvoltage is expected to exceed this value, the current through these diodes should be limited to 10 mA, using external current limiting resistors (see Input Protection Basics for ADI In-Amps section in Chapter 5). The value of these resistors is defined by the in-amp's noise level, the supply voltage, and the required overvoltage protection needed.

The bandwidth of the AD623 is reduced as the gain is increased since A1 and A2 are voltage feedback op amps. However, even at higher gains, the AD623 still has enough bandwidth for many applications.
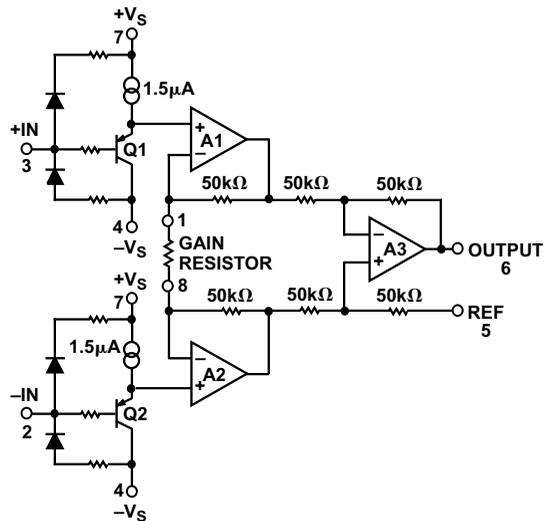

Figure 3-42. AD623 simplified schematic.

The AD623's gain is resistor-programmed by R_G or more precisely by whatever impedance appears between Pins 1 and 8. Figure 3-43 shows the gain vs. frequency of the AD623. The AD623 is laser-trimmed to achieve accurate gains using 0.1% to 1% tolerance resistors.
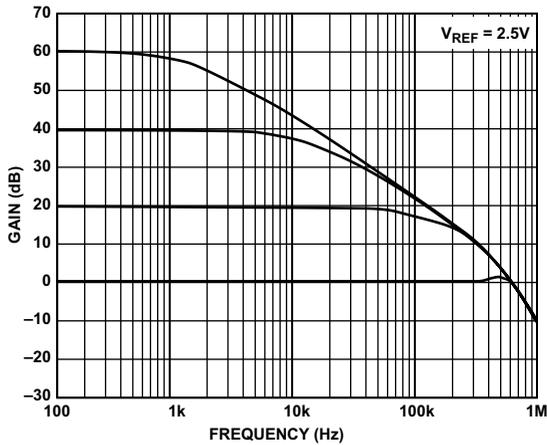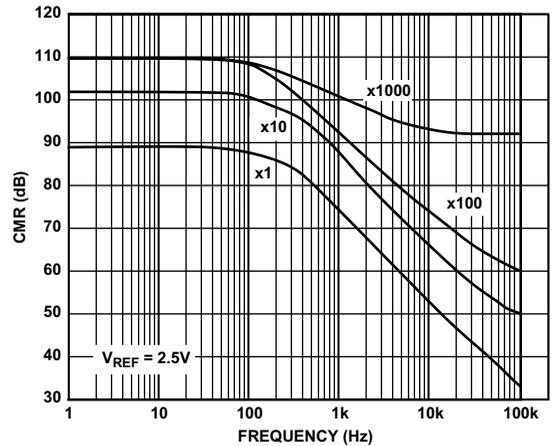
Figure 3-43. AD623 closed-loop gain
vs. frequency.

Table 3-3. Required Value of Gain Resistor

Desired Gain	1% Std. Value of R_G (Ω)	Calculated Gain Using 1% Resistors
2	100 k	2
5	24.9 k	5.02
10	11 k	10.09
20	5.23 k	20.12
33	3.09 k	33.36
40	2.55 k	40.21
50	2.05 k	49.78
65	1.58 k	64.29
100	1.02 k	99.04
200	499	201.4
500	200	501
1000	100	1001

Table 3-3 shows required values of R_G for various gains. Note that for $G = 1$, the R_G terminals are unconnected ($R_G = \infty$). For any arbitrary gain, R_G can be calculated using the formula

$$R_G = 100 \text{ k}\Omega/(G - 1)$$

Figure 3-44 shows the AD623's CMR vs. frequency. Note that the CMR increases with gain up to a gain of 100 and that CMR also remains high over frequency, up to 200 Hz. This ensures the attenuation of power line common-mode signals (and their harmonics).
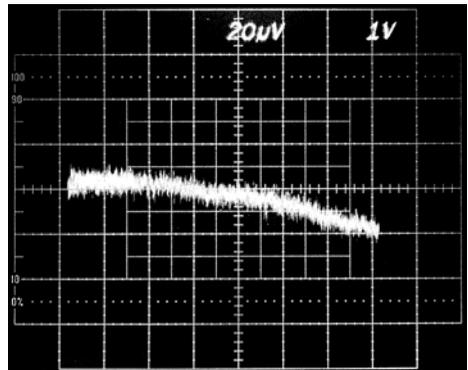

Figure 3-44. AD623 CMR vs. frequency ($V_S = \pm 5\,V$).

Figure 3-45 shows the gain nonlinearity of the AD623.

Figure 3-45. AD623 gain nonlinearity
($G = -10$, 50 ppm/div).

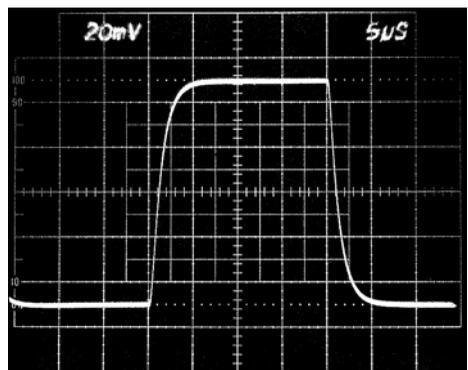Figure 3-46 shows the small signal pulse response of the AD623.

Figure 3-46. AD623 small signal pulse response
($G = 10$, $R_L = 10$ kΩ, $C_L = 100$ pF).

3-18

Low Power, Single-Supply In-Amps

The **AD627** is a single-supply, micropower instrumentation amplifier that can be configured for gains between 5 and 1000 using just a single external resistor. It provides a rail-to-rail output voltage swing using a single 3 V to 30 V power supply. With a quiescent supply current of only 60 µA (typical), its total power consumption is less than 180 µW, operating from a 3 V supply.

Figure 3-47 is a simplified schematic of the AD627. The AD627 is a true instrumentation amplifier built using two feedback loops. Its general properties are similar to those of the classic 2-op amp instrumentation amplifier configuration and can be regarded as such, but internally the details are somewhat different. The AD627 uses a modified current feedback scheme, which, coupled with interstage feedforward frequency compensation, results in a much better CMRR at frequencies above dc (notably the line frequency of 50 Hz to 60 Hz) than might otherwise be expected of a low power instrumentation amplifier.

As shown in Figure 3-47, A1 completes a feedback loop, which, in conjunction with V1 and R5, forces a constant collector current in Q1. Assume for the moment that the gain-setting resistor (R_G) is not present. Resistors R2 and R1 complete the loop and force the output of A1 to be equal to the voltage on the inverting terminal with a gain of (almost exactly) 1.25. A nearly identical feedback loop completed by A2 forces a current in Q2, which is substantially identical to that in Q1, and A2 also provides the output voltage. When both loops are balanced, the gain from the noninverting terminal to V_{OUT} is equal to 5, whereas the gain from the output of A1 to V_{OUT} is equal to –4. The inverting terminal gain of A1

(1.25), times the gain of A2 (–4), makes the gain from the inverting and noninverting terminals equal.

The differential mode gain is equal to 1 + R4/R3, nominally 5, and is factory trimmed to 0.01% final accuracy (AD627B typ). Adding an external gain setting resistor (R_G) increases the gain by an amount equal to (R4 + R1)/R_G. The gain of the AD627 is given by the following equation:

$$G = 5 + \left(\frac{200 \,\text{k}\Omega}{R_G} \right)$$

Laser trims are performed on resistors R1 through R4 to ensure that their values are as close as possible to the absolute values in the gain equation. This ensures low gain error and high common-mode rejection at all practical gains.

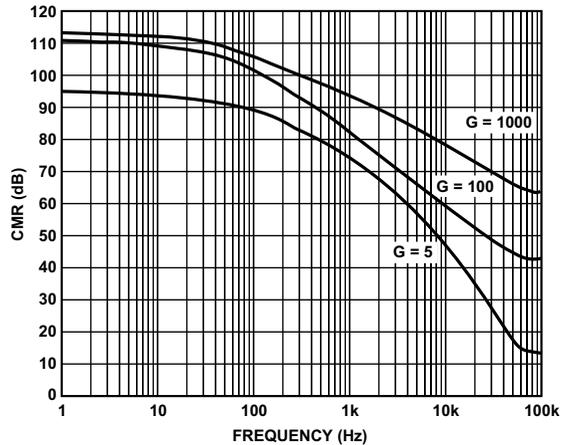Figure 3-48 shows the AD627's CMR vs. frequency.

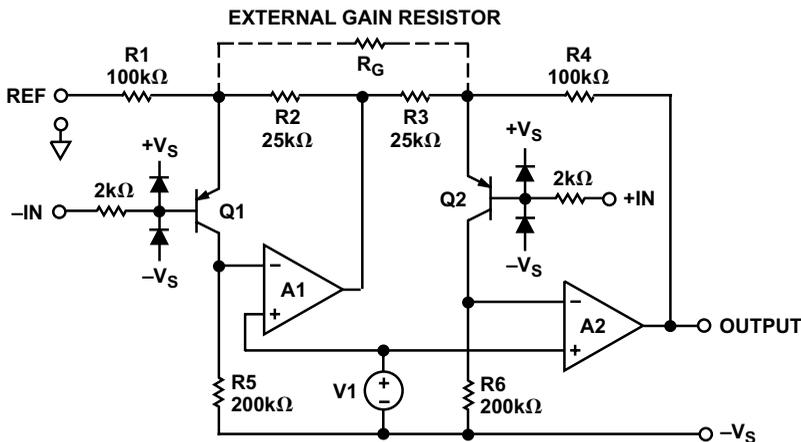
Figure 3-48. AD627 CMR vs. frequency.

Figure 3-47. AD627 simplified schematic.

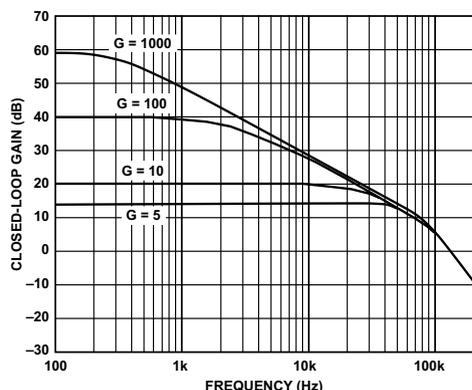Figures 3-49 and 3-50 show the AD627's gain vs. frequency and gain nonlinearity.
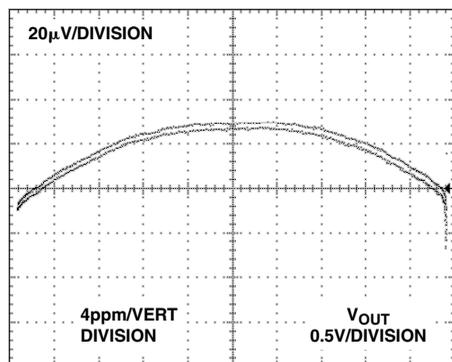

Figure 3-49. AD627 closed-loop gain vs. frequency.

Figure 3-50. AD627 gain nonlinearity ($V_S = \pm 2.5$ V, G = 5, 4 ppm/vertical division).

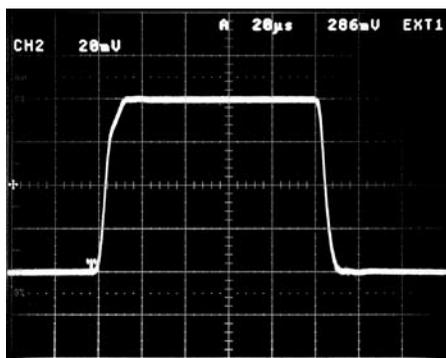The AD627 also has excellent dynamic response, as shown in Figure 3-51.

Figure 3-51. Small signal pulse response of the AD627 ($V_S = \pm 5$ V, G = +10, $R_L = 20$ kΩ, $C_L = 50$ pF, 20 μs/horizontal division, 20 mV/vertical division).

Gain-Programmable In-Amps

The **AD8250** and **AD8251** (Figure 3-52) are digitally gain-programmable instrumentation amplifiers that have high (GΩ) input impedances and low distortion, making them suitable for sensor interfacing and driving high sample rate analog-to-digital converters. The two products are nearly identical, except for their gain ranges. The AD8250 has programmable gains of 1, 2, 5, and 10, while the AD8251 has a range of 1, 2, 4, and 8 (for binary applications). Both products have high bandwidths of 10 MHz, low distortion, and a settling time of 0.5 μs to 0.01%. Input offset drift and gain drift are only 1 μV/°C and 10 ppm/°C, respectively. In addition to their wide input common-voltage range, they boast a high common-mode rejection of 80 dB at G = 1 from dc to 100 kHz. The combination of precision dc performance coupled with high speed capabilities makes the AD8250 and AD8251 excellent candidates for data acquisition and medical applications. Furthermore, these monolithic solutions simplify design and manufacturing, while boosting their performance, by maintaining a tight match of internal resistors and amplifiers.
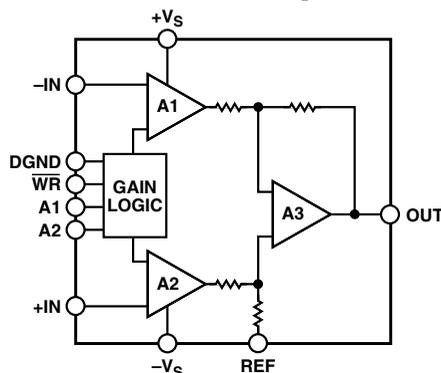

Figure 3-52. AD8250 and AD8251 simplified schematic.

The AD8250 and AD8251 user interfaces are comprised of a parallel port that allows users to set the gain in one of three different ways (Figure 3-52). A 2-bit word sent to A1 and A2 via a bus may be latched using the CLK input. An alternative is to set the gain within 1 μs by using the gain port in transparent mode. The last method is to strap A1 and A2 to a high or low voltage potential, permanently setting the gain.

The AD8250 and AD8251 are available in a 10-lead MSOP package and are specified over the –40°C to +125°C temperature range, making them an excellent solution for applications where size and packing density are important considerations. To simplify matters, their pinout was chosen to optimize layout and increase ac performance.