IV Log Circuit Applications

Chapter 1

In Chapter 3-1, the design and testing of logarithmic devices have been discussed and explained in some detail. This chapter will consider the various tradeoffs a designer is confronted with when applying a log device with a predetermined reference. The specifications of log modules, which were listed in Chapter 3-1, will be discussed in greater depth here, in the context of the manner in which they affect performance in an application.

SELECTING THE APPROPRIATE LOG DEVICE

There are many options available to the designer. These range from performing one's own design – from the ground up – using the most appropriate approach (linear approximations, diodes, monolithic-dual transistors, or other components characterized by logarithmic transfer characteristics) to purchasing one of the several types of log module available on the market today. Available standard devices, with guaranteed performance, range from modules containing a simple transistor-pair packaged with a temperature-compensating resistor network to complete log-amplifiers containing op amps, a reference-current source, and all the necessary temperature- and frequency-compensating components.

THE BASIC LOGARITHMIC ELEMENT

The simplest module available for temperature-compensated log circuits is the basic log element. A schematic of the Analog Devices Model 751 is shown in Figure 1.

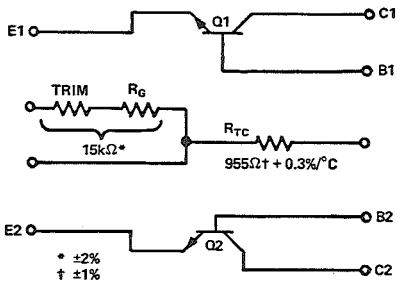


Figure 1. Schematic diagram of 751N basic log element

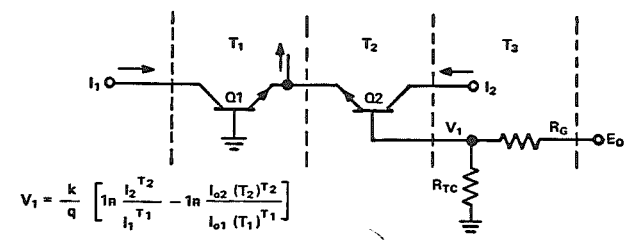
At first glance, one may think that this is too trivial a module to consider for purchase; it contains only two transistors and three resistors. Superficially, this is true, but it is also true (though less obvious) that an essential characteristic of such a device is its isothermal environment. Also, despite the many advantages of monolithic dual transistors, a matched discrete-transistor pair is better-suited to the purpose of the device. Since the log element is the heart of a circuit that provides a logarithmic output, a thorough understanding of these two points is essential to successful design.

The transistors used in Model 751 are discrete transistors especially selected for log characteristics and carefully matched. There is a subtle, but important, advantage for discrete transistors: the combination of base spreading resistance and contact resistance, which can be lumped together and considered as a small resistor in series with the emitter, is the major cause of log conformity error at current levels from 100μA to 1mA. The discrete transistors used in the 751 have a much lower value of series resistance, hence three to ten times better performance at these levels (without compensation circuitry) than do available high-β monolithic pairs.

In order to capitalize on this advantage (as well as the temperature-tracking capability of matched transistors), it is imperative that the two transistors be located in an isothermal environment. At constant current, the V_{be} of a transistor has a temperature-coefficient of approximately -2mV/°C. If the junctions are

allowed to be as little as 0.5°C apart, the corresponding voltage difference is 1mV, which corresponds to an input-current change of *4%* (If $1mV = kT/q\ \ln(1+\lambda) = 26mV\ \ln(1+\lambda)$, then $\lambda = 0.04$). If errors from this source are to be held at less than 0.5%, the junctions must be held within 130μV, or 0.06°C, under all conditions of ambient or internally-generated temperature change.

To obtain an isothermal environment, conductive epoxy and "heat clips" are used, and particular attention is paid to the layout. This environment is also essentially isothermal as regards the temperature-compensating resistor. To appreciate this advantage, one need only consider the effect of a small amount of air circulation over similar components sitting on an open circuit board. Although the compensation resistor may be precisely trimmed to eliminate the temperature-dependence of the scale factor, its effect can be nullified (and even detrimental) for differences greater than 1°C. These points are illustrated in Figure 2.



$$V_1 = \frac{k}{q}\left[\ln\frac{I_2^{T_2}}{I_1^{T_1}} - \ln\frac{I_{o2}(T_2)^{T_2}}{I_{o1}(T_1)^{T_1}}\right]$$

IF $T_2 = T_1 = T$
AND $I_{o1}(T) = I_{o2}(T)$

$$V_1 = \frac{kT}{q}\left[\ln\frac{I_2}{I_1}\right]$$

$$E_O = \left[1+\frac{R_G}{R_{TC}}\right]\frac{kT}{q}\ln\frac{I_2}{I_1}$$

Q1 AND Q2 ARE SELECTED FOR EQUAL REVERSE-SATURATION CURRENTS AT A GIVEN TEMPERATURE. THIS MATCH HOLDS WELL FOR LARGE TEMPERATURE EXCURSIONS, BUT BOTH TRANSISTORS MUST BE AT THE SAME TEMPERATURE. IF $T_1 - T_2 \neq 0$, THE ERROR BETWEEN V_{be1} AND V_{be2} WILL BE APPROXIMATELY -2mV/°C. R_{TC} IS A TEMPERATURE-SENSITIVE RESISTOR WHICH IS TRIMMED TO CANCEL THE EFFECT OF THE kT/q TERM. ITS TEMPERATURE (T_3) MUST BE THE SAME AS THAT OF T_1, T_2, OR THE DESIRED CANCELLATION OF TEMPERATURE EFFECTS CANNOT BE ACHIEVED.

Figure 2. Importance of an isothermal environment for the basic log element.

When to Apply the Basic Log Element

The simplest of all log modules, it contains only the log transistors, calibrated temperature-compensating resistors, and the isothermal environment necessary for reliable and predictable log

operation. By itself, the basic log element can perform no useful function, but when coupled with two or three op amps, a reference-current source, and frequency compensation, a complete log amplifier can be built.

The basic log element should be considered primarily for special-purpose designs, calling for considerable design flexibility, e.g., physical form, current ranges, choice of reference or gains, etc. Though allowing considerable freedom for the circuit designer, it requires the greatest amount of care in the external wiring, circuit layout, and choice of components, to obtain best results.

The designer must take especial pains to obtain the best compromise of speed and dynamic stability. Familiarity with the stability considerations in Chapter 3-1, especially Figures 5 through 7 in that chapter, is essential. The *Log Circuits* Application Note[1] will also be of value.

THE LOG TRANSCONDUCTOR

This term describes a device that combines a log element, reference-current source, op amp for the reference transistor, and the related frequency-compensation components. Figure 3 shows the basic circuitry of a log transconductor (Model 752) and its relationship to the basic log element (751).

Besides offering a completely-tested circuit, the log transconductor eliminates a number of application problems relating to stabilization: it is dynamically stable at all rated levels of input current.

To complete the log amplifier circuit, the designer needs only to provide an external operational amplifier and the two trim

[1]"Design of Temperature-Compensated Log Circuits Employing Transistors and Operational Amplifiers," by W. Borlase and E. David, Analog Devices, Inc., March, 1969.

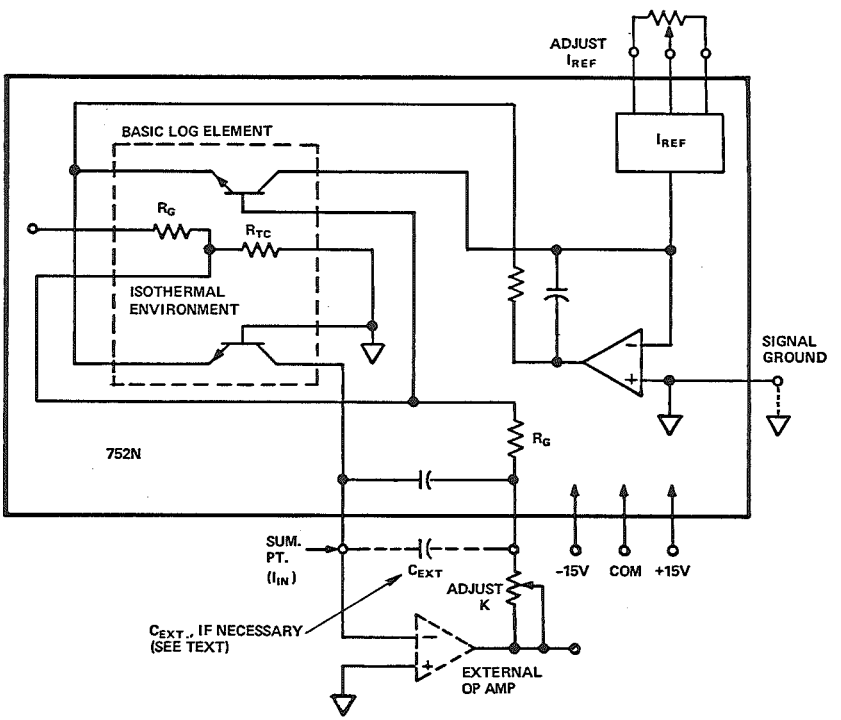


Figure 3. Functional diagram of a log transconductor and its relationship to the basic log element.

adjustments for I_{ref} and the scale factor, K. When currents beyond the specified range of the log transconductor are to be "logged," it may be necessary to add capacitance (10-20pF) in the feedback circuit of the external amplifier (Figure 3) for stability, at the cost of reduced bandwidth.

It should be noted that Figure 3 is a *functional* diagram of the 752 transconductor. For a wholly-packaged circuit, a separate basic log module is not used; in many cases a monolithic dual transistor is used to obtain improved temperature-tracking. To overcome the series-resistance problem mentioned above, a feedback compensation circuit is used internally to reduce the series resistance.

When to Apply the Log Transconductor

Log transconductors are used in preference to basic log modules when it is desired to use an essentially-complete packaged circuit with guaranteed performance instead of a collection of parts; yet, on the other hand, the designer wishes to optimize the price/performance mix by choosing the most appropriate operational amplifier to fit his needs.

The major error terms associated with log amplifier circuits (that are readily controllable) are the offset voltage and bias current of the operational amplifier. By choosing an amplifier to fit a specific application, the designer may, in most cases, effectively eliminate amplifier-caused errors at a given level of voltage or current. For example, when the logarithm of a low-level current is to be computed, the Model 42K amplifier may be used because of its 100fA bias-current specification.

If 100fA is compared to the lowest-level of signal current specified for the 752, 1nA, it can be seen to represent an error of 0.01%. If one starts by choosing this low value of bias current, its contribution to error could be completely ignored, despite the characteristic doubling/10°C of FET-input-amplifier bias current. At 65° C, the bias current would have increased by a factor of $2^4 = 16$, which is still insignificant compared to the other errors.

If the input signal is a voltage, the external op amp would be chosen for minimal offset voltage and drift. For ultimate low-level performance, "spikeless" chopper-stabilized amplifiers are perhaps the best choice; but one should also consider such low-drift chopperless types as the 184L and the AD504M, and especially, the 52K (I_b = 2pA, $\Delta E_{os}/\Delta T = 1\mu V/°C$).

When economy is of prime concern, the log transconductor and a low-cost IC op amp can be the best answer. To achieve good performance when using a low-cost (modest-performance) amplifier, the input signal should be scaled so that its geometric mean falls in the center (i.e., geometric mean) of the range determined by the log transconductor's upper limit and 100X the bias voltage or offset current of the amplifier. With this approach, excellent

results can be obtained over a limited range. Figure 4 shows how the log transconductor is connected with an external op amp. Table 1 provides a brief selection guide.

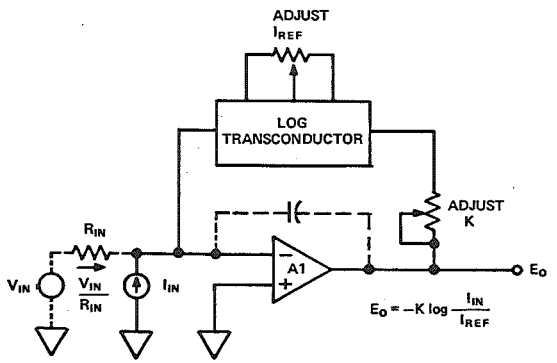


Figure 4. Application of log transconductor. If the input signal is a current, connect it directly to the summing junction, as shown. If the input signal is a voltage, connect it to the summing junction through a resistance as shown by the dashed lines. Note that R_{IN} includes the source resistance of V_{IN}.

TABLE 1. SELECTION CRITERIA FOR A1 (FIGURE 4)

INPUT SIGNAL	SELECT A1 FOR	RECOMMENDED OP-AMP TYPE
VOLTAGE	LOW OFFSET VOLTAGE	CHOPPER (234) CHOPPERLESS LOW-DRIFT (184L, 504M, 52K)
CURRENT	LOW BIAS CURRENT	ELECTROMETER (42K)
VOLTAGE OR CURRENT; LIMITED DYNAMIC RANGE	PRICE-REASONABLE PERFORMANCE	LOW-COST BIPOLAR OR FET, I.C. OR MODULE: AD301A, AD540, MODEL 40, AD308

THE COMPLETE LOG AMPLIFIER

The complete log amplifier contains a log transconductor, all the necessary trim circuitry, and a high-quality FET-input op amp. This is the most convenient type of log module, since the designer has only to connect power (usually ±15V @ ±10mA), input and

output leads. All the necessary frequency-stabilization and trimming have been performed by the manufacturer.

When to Apply the Complete Log Amplifier (and When Not to)

The complete log amplifier is the starting point for all new log-circuit designs. By freeing himself from the problems of designing, building, and trimming a log amplifier, the designer has more time available to deal with the problems involved in the instrument, apparatus, or system that led to the use of a log amplifier.

Performance of the complete log amplifier is adequate to deal with a wide range of input currents and voltages; and the fixed choices of reference (10μA, 100mV) and scale factor (2/3, 1, 2) provide convenient scaling, which can be modified for the system by external gains and biases.

If wider ranges of current or voltage, greatly-different local scaling, or paired operations (such as the use of 752P and 752N in hyperbolic-sine operations), are necessary, then the need for the flexibility inherent in the log transconductor (or basic log devices) will become apparent (see Page 102).

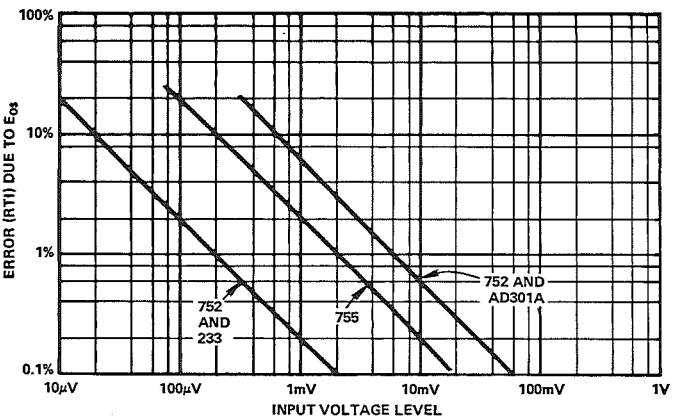


Figure 5. Effect of offset on dynamic range in terms of error vs. input level. Errors are for +2°C temperature change. Greater temperature changes move curves up proportionally (e.g., 755 at 10mV has 0.2% change for 2°, 2% for 20°).

As an aid to determining the performance tradeoffs between the complete log amplifier (755) and the log transconductor-plus-external amplifier, the graphs of Figures 5 and 6 will be found helpful. They show the error as a function of input-voltage and current levels for the 755 and for the 752 with-external-op-amps of several types. The voltage error used in the plots is that caused by a 2°C variation from an initially-zeroed condition. The current error is essentially that caused by the amplifier's bias current.

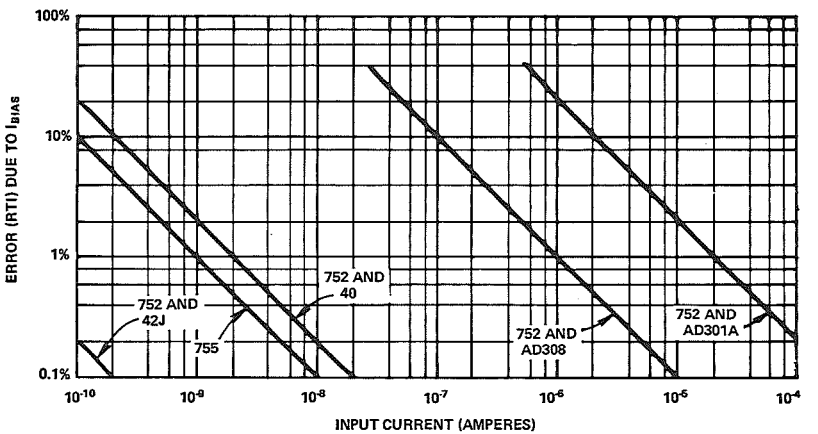


Figure 6. Effect of op-amp bias current on dynamic range in terms of error vs. input level, for various combinations of op amps and log transconductors

Selecting the Best Log Device for the Application

Table 2 provides general guidelines as to the choice of approach. The choice will be determined by the designer's principal objective: best performance, lowest cost, easiest-to-apply.

If cost is the criterion, then the basic log element may be the answer, but the saving is somewhat marginal; the designer must honestly evaluate the cost of designing, assembling, and testing the finished device. If the design is to be used in quantity, costs of drawings, parts inventorying, and production engineering must also be anticipated.

TABLE 2. SUMMARY OF SALIENT FEATURES OF CONSTANT-REFERENCE LOG MODULES (SUMMER, 1973)

Log Module	Description Contents and Applications	Advantages	Disadvantages
Basic Log Element Model 751	2 Matched Log Transistors, Scaling and Temperature-Compensating Resistors. For Special-purpose log. designs	Lowest Cost. Greatest Flexibility	Most Complex to Apply. Requires at least 2 external op amps plus dynamic stabilization in conventional log application.
Log Transconductor Model 752	Basic Log Element, Reference-current source. To optimize operation at low levels	Best performance obtainable through op amp choice	Requires external op amp, gain trim I_{REF} trim
Log Amplifier Model 755	Log Transconductor, FET-Input Op Amp. The initial choice for all fixed-reference log applications.	Easiest to apply. Meets specs with no trimming or external components. Best performance over a wide range.	Op amp is optimized for most (but not all) applications

To optimize performance for a specific application, the log transconductor and a high-performance op amp selected for the application can offer the best performance.

The easiest log module to apply is the complete log amplifier. Except for the extremely low end of the signal range, the log amplifier offers performance equal to or better than that of any of the other choices.

While the generalities given above are helpful in selecting the best log device for the application, the proper choice can be made only when specific information regarding signal level, source impedance, and acceptable error has been developed.

Once this is known, the limitations on dynamic range caused by the input parameters of the op amp associated with the log modules can be determined.

STEP RESPONSE

The dynamic parameters of log modules are highly dependent on signal level, as Chapter 3-1 has demonstrated. Perhaps the most useful parameter to discuss in detail is the step response, since the response to a step of a given magnitude is usually a matter of

prime concern. The time required for the output to change (or "slew") from one level to another is dependent on the magnitudes of the input currents and on the direction, i.e., whether the current is increasing or decreasing.

Slewing rate of a log transistor's base-emitter voltage can be explained in terms of the effects of current level on the transistor's base-charging capacitance (C_b), transconductance (g_m), and incremental space-charge-layer capacitance (C_{je}). Base-charging capacitance, C_b is defined as

$$C_b = \tau_F g_m = \tau_F \frac{q}{kT} |I_c| \tag{1}$$

where τ_F is the average charge-replacement time in the base and I_c is the collector current.

Transconductance, g_m, and – in turn – C_b are proportional to I_c, provided that the base current is much greater than the reverse saturation current. This condition is met for all log modules operated within the specified range.

The capacitance of the transistor hybrid Π model, C_Π, directly controls the common-emitter current gain at high frequencies. It is equivalent to

$$C_\Pi \equiv C_{je} + C_b \tag{2}$$

which, from (1), may be written as

$$C_\Pi \equiv C_{je} + \tau_F \frac{q}{kT} |I_c| \tag{3}$$

The dependence of ω_t, the frequency at which current-gain is unity, on C_Π is

$$\frac{1}{\omega_T} \equiv \frac{C_\Pi + C_\mu}{g_m} \tag{4}$$

where C_μ is the feedback capacitance of the hybrid model.

Substituting (2) and $g_m = \frac{q}{kT} |I_c|$ into (4),

$$\frac{1}{\omega_T} = (C_{je} + \tau_F \frac{q}{kT} |I_c| + C_\mu) \left[\frac{kT}{q|I_c|}\right] \quad (5)$$

$$= \tau_F + (C_{je} + C_\mu) \left[\frac{kT}{q|I_c|}\right] \quad (6)$$

Although base-charging capacitance, C_b, is directly proportional to collector current, its effect on ω_t is nullified by the proportionality of g_m to collector current.

The net effect of these expressions is to show that the admittances of C_{je} and C_μ are controlled by collector current; an increase in collector current results in greater bandwidth and faster slewing rate.

The above discussion relates only to the effect of the signal level on speed through its effect on the parameters of the log transistor. In a practical situation, there are many other factors that influence the speed of response of the circuit. The most important of these factors in log modules are the added feedback capacitance for stabilization, the stray capacitance at the amplifier input, and the bandwidth of the amplifier.

With proper stabilization circuitry, the amplifier and its stabilizing feedback capacitor should restrict speed only at the high end of the allowable input range. Stray capacitances modify the values of C_{je}, C_μ, and τ_F in the expression defining ω_t. The stray capacitance from summing junction to common is a constant that modifies τ_F. Stray capacitance from collector to base is feedback capacitance and affects C_μ.

Table 3 lists response times for steps of differing magnitude and current level for the 755 log amplifier. By comparing them with the equation for the radian period $1/\omega_t$, it is clear that the predicted linear relationship does exist at the lower levels, with a limit determined by the feedback capacitance and strays at the higher levels. In this region (1μA to 1mA), other considerations, such as the bandwidth of the amplifier and the size of the stabilizing capacitor, dominate the response, and further improve-

TABLE 3. RESPONSE TIME (755) FROM 10 TO 90%

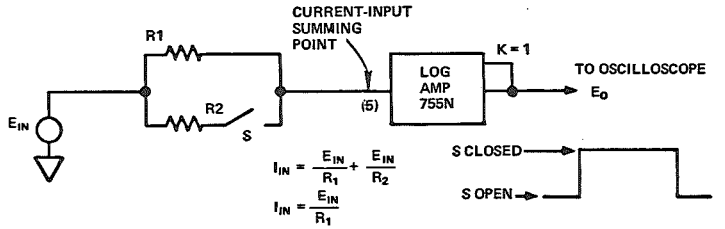
I_{IN} INCREASING		I_{IN} DECREASING	
I_{IN}	TIME	I_{IN}	TIME
1nA → 10nA	1ms	10nA → 1nA	4.5ms
10nA → 100nA	100μs	100nA → 10nA	400μs
100nA → 1μA	7μs	1μA → 100nA	30μs
1μA → 1mA	4μs	1mA → 1μA	7μs

ments in response time become marginal. Even if an external amplifier having near-infinite gain and requiring no stabilization capacitor were used, the improvements in slew rate would be slight. C_{je} and C_{μ} are not quite constant, as assumed, but increase with signal level for currents of 0.1mA and more).

If steps of current are applied to the log module in the direction of increasing magnitude, a faster slew rate will be achieved than for steps in the direction of decreasing magnitude. Since the time to charge or discharge a capacitor is dependent on the available current, it is to be expected that steps which increase quiescent current will have a faster slewing rate and a shorter final exponential "tail." Because of the decreased time constant at high current levels, responses that end at higher levels will be completed faster than those ending at lower levels, even though the latter start faster than the former in traversing a given current range.

For changes over combinations of the ranges listed in Table 3, the response time will be determined by the final value of current. For example, in traversing the entire range of 1nA to 1mA, the total time will be dictated by the final value of 1mA, resulting in a total response time of about 6μs. Conversely, when slewing from 1mA to 1nA, the final value is 1nA, and the total response time will correspond approximately to that for 1nA, or 4.5ms.

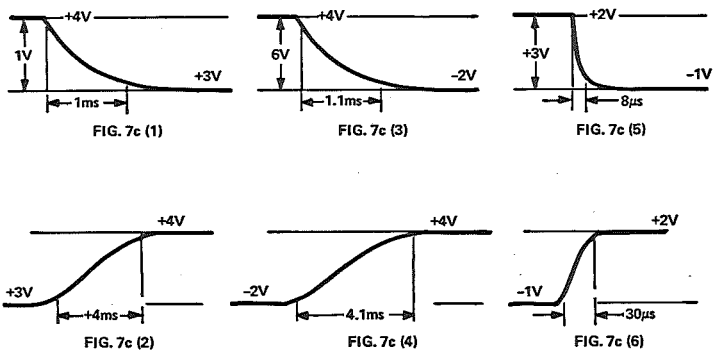
The dependence of slew rate on signal level will cause varying degrees of distortion for input square waves at various signal levels. Shown in Figure 7 are several input signals and the corresponding outputs from the log amplifier. By the choice of V_{IN}, R1, and R2, and the position of electronic switch S1, the various input signals are readily obtainable. Alternatively, the square-wave-plus-bias of Figure 20, Chapter 3-1, may be used.



a) Test setup for measuring response time (10% — 90%)

E_{IN}	R_1	R_2	S Operation	Magnitude Change	Output Waveform Fig. 7c ( )
100mV	100MΩ	11MΩ	CLOSED	1nA → 10nA	7c (1)
100mV	100MΩ	11MΩ	OPEN	10nA → 1nA	7c (2)
100mV	100MΩ	100Ω	CLOSED	1nA → 1mA	7c (3)
100mV	100MΩ	100Ω	OPEN	1mA → 1nA	7c (4)
100mV	1MΩ	1kΩ	CLOSED	0.1μA → 100μA	7c (5)
100mV	1MΩ	1kΩ	OPEN	100μA → 0.1μA	7c (6)

b) Table of input values



c) Responses (10% — 90%)

Figure 7. Response time (10% — 90%) for steps of various magnitudes and polarities

ANOTHER LOOK AT SPECIFICATIONS OF LOG DEVICES

The transfer equation for a log module is

$$E_o = -K \log \frac{I_{IN}}{I_{REF}} \text{ or } -K \log \frac{V_{IN}}{E_{REF}} \quad (7)$$

I_{REF} is a dimensional constant necessitated by the fact that logarithms exist only for pure numbers (the expression log I_{IN} by itself would imply a reference current of 1A). When $I_{IN} = I_{REF}$, the logarithm of the ratio is zero. I_{REF} for practical devices can be chosen as one or the other extreme of the range of I_{IN}, or it may be approximately in the middle of the range (geometric mean). I_{REF} for Model 755 and similar devices is 10μA, which corresponds to 0.1V for E_{REF}, the geometric mean between 1mV and 10V, hence mid-scale. Since the logarithm is real only for positive arguments, the input and reference must be of the same polarity, i.e., if V_{IN} is negative, V_{REF} must also be negative.

The gain, or scale factor, K is also a dimensional constant (volts). The typical log amplifier (755) can be connected for K = 1, K = 2, or K = 2/3. -K = -1 gives an output decrease of 1 volt for each 10X increase in the input ratio. K $\log_{10}$(ratio) can also be interpreted in terms of other logarithmic bases (B), according to the relationship, $E_O = -K' \log_B$ (ratio), where

$$K' = K \log_{10} B \quad (8)$$

For K = 1, BASE (B)	K'
100	2.0
10	1.0
8	0.903
5	0.699
3.16	0.50
e	0.434
2	0.301

K' is the output change corresponding to an input ratio change, B.

The 755 and 752 modules are really families having devices of both polarities. 755N and 752N utilize NPN transistors (751N); 755P and 752P utilize PNP transistors (751P). When used for log operations, the "N" versions accept positive voltage or current, and K is positive (that is, the output becomes less positive or more negative as the input becomes more positive – the characteristic response of any circuit involving an inverting operational amplifier); the P versions accept negative voltage or current for logarithmic operation, and K is negative (that is, the output becomes less negative, or more positive, as the input becomes more negative – again, an inverting response). The output voltage of both devices is plotted against current input (log scale) in Figure 8. All three inherent values of the scale factor, K, are shown.

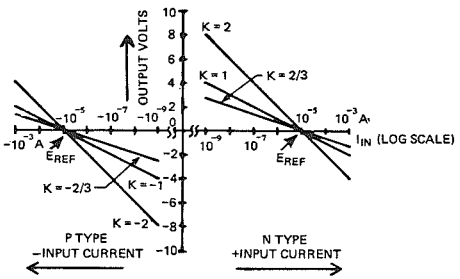


Figure 8. Plot of output voltage vs. input current for model 755

INTERPRETING LOG-DEVICE TERMS

Log Conformity Error: Log conformity error is the difference between the actual output voltage and the output voltage predicted by the log-transfer equation. A plot of output vs. input, when plotted on semilog paper (linear output scale, log input scale), should be a straight line. Any deviation from this straight line is log conformity error; in this sense, it is analogous to linearity error for linear devices. For most log amplifiers, the best

linearity is obtained in the middle 4 decades (10nA to 100μA). In this range, for 755, log-conformity error is ±0.5% referred to the input (RTI) or 2.17mV referred to the output (RTO) for |K| = 1. To obtain best results, the input data, if possible, should be centered within this range.

Log conformity error is the one irreducible error of the log amplifier. It appears as an error in the log operation and cannot be compensated-for with internal circuitry.

Offset Voltage (E_{os}): The offset voltage of the log module is the offset voltage of the internal amplifier. This voltage acts as though it were a small dc offset voltage in series with the input terminals. For voltage-logging operations, best performance is obtained with the offset voltage trimmed.

Since E_{os} appears in series with V_{IN}, the effect of E_{os} depends on the level of V_{IN}. Referred to the input, the error contribution of E_{os} is

$$\% \text{ RTI} = (E_{os}/V_{in})\ 100\% \qquad (9)$$

Determining the output error corresponding to a given RTI error is straightforward. For example, for a RTI error of ½%, (1± 0.005), the respective values of the logarithm are 0.002166 (1.005) and -0.002177 (0.995), or about ±0.0022. Multiplying by K = 1V yields an output error of ±2.2mV for an input error of ±½%.

An alternative metnod of determining RTO errors from RTI (or vice versa) is to use an abbreviated table, such as Table 4,* with linear interpolation, if necessary.

*Note: Table 4 differs from the table in the Specifications section of Chapter 3-1; in the latter table, the errors are based on low-side error (e.g., 1−0.1% → 0.999), hence give greater errors referred to the output. In table 4 on this page, the errors are based on high-side error (1 + 0.1% → 1.001), hence give greater errors referred to the input. While not significantly different, worst-case error computations should take into account the more-important error from the standpoint of the application.

% Error Referred to Input (δ_i)	Millivolt Error Referred to Output (δ_o) K = 1	K = 2	K = 2/3
0.1%	0.43mV	0.87mV	0.29mV
0.5	2.17	4.33	1.44
1.0	4.32	8.64	2.88
3.0	12.84	25.67	8.56
4.0	17.03	34.07	11.36
5.0	21.19	42.38	14.13
10.0	41.39	82.79	27.60

This table gives representative examples of input errors and the corresponding error at the output for common values of K. For a given output error, the input error can be computed by linear interpolation. The curves may also be helpful in obtaining approximate error conversions instantly. Example shown: 2% error ≅ 8.5mV.

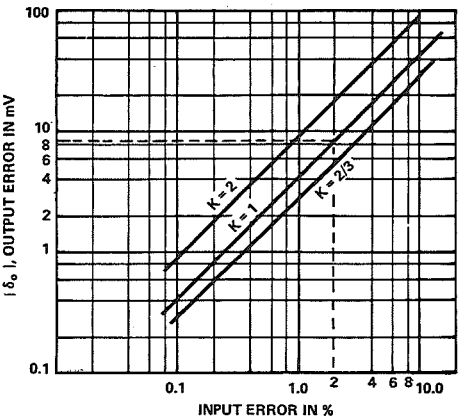


Table 4. Error conversion: $|\delta_O| = K \log_{10}(1 + \delta_i/100)$

For example, to determine the RTI error equivalent to 14mV out for K = 1, the nearest value to 14mV is 12.84mV, at 3.0%. To this should be added (4.0 – 3.0) (14 – 12.84)/(17.03 –12.84) = 0.28, for a total error of 3.3% RTI.

Offset Current (I_{os}): The offset current, I_{os}, of the log amplifier is the bias current of the internal amplifier. This parameter can be a significant source of error when processing signals in the nanoampere region. For this reason, it is important to select a log amplifier having bias current much less than the smallest signal to be processed. Error contribution of I_{os} is:

$$\% \text{ RTI} = (I_{os}/I_{IN})\ 100\% \qquad (10)$$

Reference Current (I_{REF}): I_{REF} is the internally-generated current source to which all input currents are compared. Tolerance errors in I_{REF} appear as a dc offset at the output. Other offsets appearing at the output cannot be differentiated from the effects of I_{REF} error. This is easily demonstrated by considering the transfer equation with an added offset

$$E_o = -K \log \frac{I_{IN}}{I_{REF}(1 \pm P/100)} \pm E_1 \qquad (11)$$

where P represents the percent tolerance in I_{REF} and E_1 is the output offset.

This equation can be rewritten

$$E_o = -K \log \frac{I_{IN}}{I_{REF}} + K \log (1 \pm P/100) \pm E_1 \qquad (12)$$

Since both the second and the third terms on the right-hand side of (12) are constants, they can be combined to form a constant E_2:

$$E_o = -K \log \frac{I_{IN}}{I_{REF}} \pm E_2 \qquad (13)$$

Table 4 can be used, as before, to determine the RTI equivalent of the combined offset, E_2, and this new tolerance (P′) can be part of the error in I_{REF}:

$$E_o = -K \log \frac{I_{IN}}{I_{REF}(1 \pm P'/100)} \qquad (14)$$

The specified tolerance for I_{REF} of log amplifiers includes dc output offset errors, since they are inseparable from the effects of I_{REF}.

The effect of I_{REF} tolerance errors can be compensated for by adding a constant at the output or in a stage following the output, or by trimming the input scale factor ahead of the log amplifier.

Reference Voltage (E_{REF}): E_{REF} is the effective internally-generated voltage to which all input voltages are compared. It is related to I_{REF} through the equation,

$$E_{REF} = I_{REF} R_{IN} \quad (15)$$

where R_{IN} is the total input-circuit resistance, including the input resistor, the signal source resistance, and any other appreciable series resistance. Virtually all the tolerance in E_{REF} is due to I_{REF}, provided R_{IN} is made up of stable precision resistors. Consequently, variations in I_{REF} cause a shift in E_{REF}.

The effects of E_{REF} tolerance errors are compensated for in the same manner as the similar effects of I_{REF}.

Scale Factor (K): Scale factor is the voltage change at the output for a decade (i.e., 10:1) change at the input. Scale-factor error is equivalent to a change in gain, or slope, and is specified in percent of the nominal value. An external adjustment may be performed to fine-trim the scale factor (usually preset) or it may be locally adjusted to a value that is several times the initial value by adding series resistance at the feedback terminal. It can also be manipulated by adjusting the gain of a stage following the log amplifier. (Its effect is the same as that of manipulation of the exponent of the log-amplifier input.)

ADJUSTING THE PARAMETERS OF LOG DEVICES

Adjusting E_{os}: The amplifier's offset voltage may be adjusted to near-zero by a very simple but unconventional procedure. Most users of op amps are accustomed to "zeroing" an op amp's offset voltage by adjusting for a zero-volt output. For log modules, this is not applicable, since a zero output corresponds to the log of 1 ($I_{IN} = I_{REF}$), and log (0) is not defined.

There is, however, a quite convenient method of adjusting E_{os} without disturbing the log circuit arrangement (except for grounding the input). The method is shown in Figure 9, and, while specifically applied to the 755, it is applicable to all log amplifiers. Under the conditions shown in Figure 9, the output is

$$E_o = -K \log \frac{V_{IN} - E_{os}}{E_{REF}} \quad (16)$$

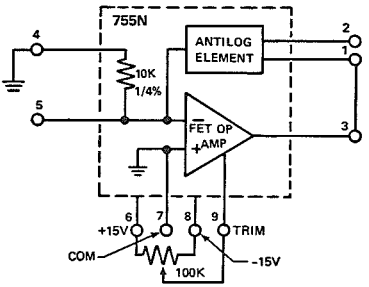


Figure 9. Trimming E_{OS}

Since the input terminal is grounded through the 10kΩ resistor, $V_{IN} = 0$. The equation for output voltage then becomes

$$E_o = -K \log \frac{-E_{os}}{E_{REF}} \qquad (17)$$

Remembering that the log is undefined for zero, assume a practical limitation on E_{os}, and then calculate E_o: Since the change in E_{os} with temperature for a good FET amplifier is in the range of 20μV/°C, it is reasonable to assume that adjustment of E_{os} to 10μV would be reasonable.

Using this value of E_{os} and the value of K and E_{REF} specified for the log amplifier, the output can be calculated. For Model 755N, as shown in Figure 9, the output is

$$E_o = -1V \log \left[\frac{-\pm 10\mu V}{100mV} \right] = 4V, \text{ for } E_{os} = -10\mu V \qquad (18)$$

The amplifier's offset voltage can therefore be adjusted to within 10μV by adjusting for a +4V output (for 755P, the output would be -4V). By adjusting for a higher output voltage, one can adjust the offset to a still smaller value. Care should be taken to ensure that the amplifier's output voltage specification is not exceeded, since this may lead to a false offset indication.

A volt-ohmmeter is all that is required to monitor the output, since the signal level of 4V is high, and impedances are low. If an oscilloscope is used to monitor the output, high noise levels will be

observed when performing this adjustment. This is to be expected, since the sensitivity is extremely high: for the next decade, (5V – 4V) out/(10μV – 1μV) in = 111,000, gain for input noise. The open-loop gain of the amplifier may, in some cases, limit the closeness with which zero input may be approached, beyond 4V out. For 755P, the output is adjusted to <–4V.

Reference-Current Adjustment: A shift of reference current results in a dc offset at the output. By adding a dc voltage to the output, one may change the reference current to the desired value. This can be accomplished in the amplifier stages following the log amplifier or by injecting a current into an unused scale-factor-feedback terminal. In the latter case, the impedance of the scale-factor terminal being used must be known. The current inserted into the unused terminal, multiplied by the resistance in series with the used terminal determines the amount of offset change. This point is illustrated in Figure 10.

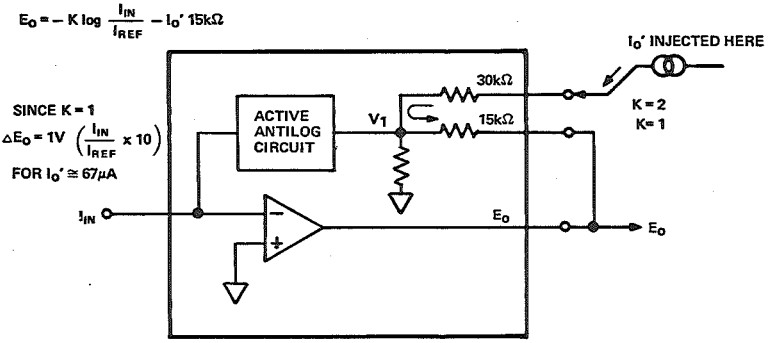


Figure 10. Adjusting I_{REF} by inserting current into unused scale-factor terminal. Since V_1 is determined by input only, I_O' must flow out through 15kΩ resistor, biasing E_O by (15kΩ) (I_O'). If $I_O' \cong 67\mu A$ at terminal 2, I_{REF} is, in effect, divided by 10.

It should be noted that shifting I_{REF} has no effect on the output other than changing the value of input at which zero output is obtained (Figure 11).

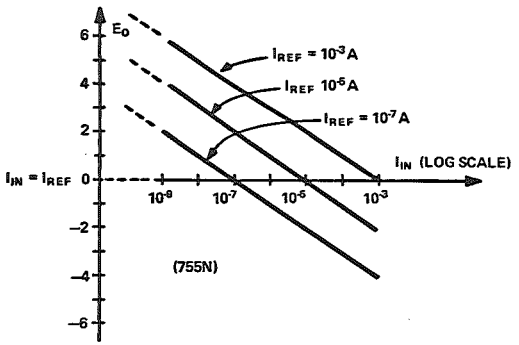


Figure 11. Output vs. input (log scale) as a function of I_{REF}

Reference-Voltage Adjustment: The reference voltage is defined in (15). Provided that R_{IN} is constant over the range of operation, the effects of changes of E_{REF} are the same as for those of I_{REF}, and the adjustment technique is exactly the same.

Scale-Factor Adjustment: Scale-factor may be adjusted by changing the total resistance between the output and the dummy summing junction shown in Figure 10. By adding resistance in series with one of the scale-factor terminals, the scale-factor may be increased from its nominal value. In general, the total resistance required to obtain any value of scale factor is

$$R_T = K R_1 \qquad (19)$$

where R_1 is the resistance of the resistor at the 1V/decade scale-factor terminal and K is the desired scale factor.

Example: To achieve a 5V/decade scale factor for a log amp having a 15kΩ input resistor at the 1V/decade terminal, calculate the external resistance required ($R_T - R_1$) or ($R_T - R_2$).

$$R_T = (5)(15k\Omega) = 75k\Omega \qquad (20)$$

The total resistance required is thus 75kΩ. If one uses the 1V/decade terminal, the external resistance required is (75 − 15)kΩ = 60kΩ. Alternatively, one might use the 2V/decade terminal, and connect an external resistance of (75 − 30)kΩ = 45kΩ.

APPLICATIONS

LOG OF VOLTAGE – DATA-COMPRESSION EXAMPLE

One of the more-interesting applications of a log module is in data compression. Suppose it is desirable to introduce a signal to a computer or data link, maintaining an accuracy within 1% of the signal throughout the range.

The conventional approach might be to select an A/D converter having sufficient resolution to meet the accuracy requirement. If the input range were 1V to 10V, the dynamic range would be from 1% of 1V to 10V, or 1000:1. To obtain this resolution, a 10-bit converter might be used,* and 1 LSB (least-significant bit) would represent 1% of the smallest signal. If the range were increased to 10mV to 10V, the converter would require a resolution of 1% of 10mV to 10V, or 1:100,000. To even approach this resolution, a 16-bit converter would be barely sufficient.* An economical alternative, maintaining the required 1%-of-signal accuracy error is to use a log module over a 3-decade range for data compression, and a *12-bit* A/D converter. The proposed scheme is shown in Figure 12.

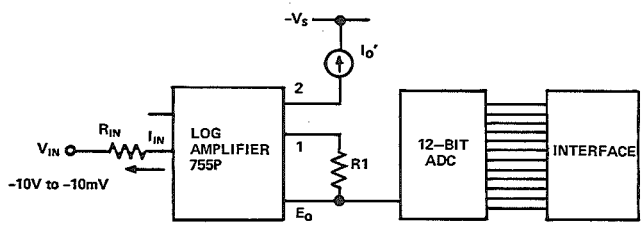


Figure 12. Data compression, using a log amplifier

In order to convert the log output to a unipolar signal, an external current source will be used to shift the reference current. To achieve the proper scale-factor, or gain, an external resistor, R1,

*2^{10} = 1024, 2^{16} = 65,536

has been added in series with the K = 1 output. The input resistance value, R_{IN}, will be chosen for the range of best log conformity, and connected at the current input, pin 5.

The first step in applying the log amplifier is to select the proper polarity. Since the input voltage is negative (-10mV to -10V), the P-type log amplifier is required. A Model 755P complete log amplifier is chosen, in order to minimize the design effort.

Choosing R_{IN}: After selecting the log amplifier, the region of best log conformity is noted, and an attempt is made to shift operation to those decades. For Model 755. the best log conformity is 0.5%, specified for the range from 10nA to 100μA. R_{IN} is selected, for use at the current input, to provide the highest input current desired (100μA) at the highest input voltage magnitude (10V).

$$R_{IN} = 10V/100\mu A = 100k\Omega \qquad (21)$$

The lowest value of input current expected is 10mV/100kΩ = 100nA. The input-current range is therefore well within the range of 0.5% log conformity.

Adjusting K: To determine the best value of K for the application, the input requirements of the following stage must be considered. If we assume the 12-bit converter to have an input range of 0 to +5V, K can be calculated. The total output voltage required is 5V, and the input range spans 3 decades. Therefore, K must be 5/3V.

From the data sheet for the log amplifier selected (755P), a value of 15kΩ is given as the input resistance of the 1V/decade terminal. The total resistance required for K = 5/3V is

$$R_T = (5/3)(15k\Omega) = 25k\Omega \qquad (22)$$

A nominal 10kΩ is required in series with the K = -1 terminal. To allow for tolerance of the internal resistor, a 10kΩ 10-turn pot in series with a 5kΩ resistor is adopted as R1.

Shifting I_{REF}: Since I_{REF} determines the point at which a zero output will be obtained, and since a zero output is desired for the smallest input current to be processed, it is this value of current, 100nA, that I_{REF} will be shifted to.

The transfer curves for the 755P (Figure 8) show that a -2V output would be obtained for 100nA input at K = -1V. Since this is the current level for which a *zero-volt* output is desired, the current I_o' injected into the unused scale-factor terminal must shift the output in the positive direction. Referring to Figure 10, one can see that a polarity inversion occurs between the unused scale-factor terminal and the output. To cause a shift in the positive direction, the current to be injected must be negative, i.e., derived from a negative voltage.

The amount of current to be injected can be calculated by Ohm's Law, using the total resistance of the scale-factor terminal connected to 1, the output, and the amount of voltage to be shifted.

$$I = \frac{2K}{R_T} = \frac{2 \times 5/3}{25k\Omega} = 133\mu A \qquad (23)$$

A resistor to the negative supply (of value 15V/133μA = 30kΩ) can be used to obtain this current, but shifts in the offset voltage

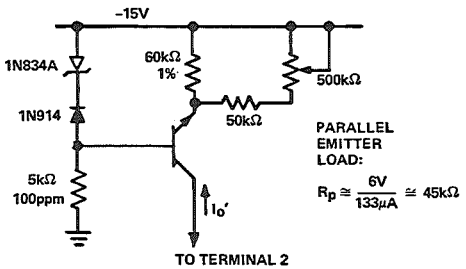


Figure 13. Constant-current source to shift reference current (I_o' = 133μA) in circuit of Figure 12.

at the dummy summing junction (Figure 10) of 60mV/decade can cause significant errors. For example, if I_{REF} were adjusted at 100nA I_{IN}, a shift of 180mV would occur as the input increased to 100μA (3 decades @ 60mV/decade), resulting in a shift of offset current of (180mV/15V) × 100 = 1.2%.

Therefore, a rudimentary current source, shown in Figure 13, is used.

Trim Procedure

1. E_{os}: The first step in the trim procedure is to adjust E_{os} of the log amp to nearly zero volts. As mentioned earlier, this can be accomplished by leaving pin 5 open (or V_{IN} disconnected), and grounding pin 4. The trim pots for I_{REF} and the scale factor should be set to midrange, in order to reduce interaction. R2 would then be adjusted for

$$\begin{aligned} E_o &= -K \log(10\mu V/E_{REF}) \\ &= (5/3) \log (10\mu V)/(100nA \times 10k\Omega) \\ &= -10/3\ V \end{aligned} \tag{24}$$

Adjusting for any voltage between -10/3V and -5V will insure that E_{os} has been adjusted to within 10μV.

2. I_{REF}: After E_{os} has been adjusted, I_{REF} can be adjusted by applying a value of input that will cause I_{REF} to flow into the log amplifier. To accomplish this, set V_{IN} to 10mV and adjust the reference-current source for zero volts out of the log amplifier.

3. K: To adjust K, the input signal should be increased to its maximum value of -10V. R1 is then adjusted for 5V output.

4. Because some interaction among the adjustments cannot be avoided, all adjustments should be repeated at least once, and in the same order as initially performed, E_{os}, I_{REF}, K.

Error Analysis

Parameter	Error	Comment
E_{REF}	$\cong 0$	Initial error is trimmed to zero
E_{REF} Drift	0.5% RTI	$\pm 0.1\%/^{\circ}C \times 5^{\circ}C = 0.5\%$
Log Conformity	0.5% RTI	Input was scaled to within range of ±0.5% log conformity
E_{os}	$\cong 0$	Initial error trimmed to zero
E_{os} Drift	0.75% RTI	$(\pm 15\mu V/^{\circ}C \times 5) / 10mV$ worst-case condition; occurs only for smallest input signal $(7.5\mu V/10mV)$ (100%) = 0.75%
I_{os}, I_{os} Drift	$\cong 0$	Negligible contribution (10 pA/100 nA) (100%) = 0.01%
K	$\cong 0$	Initial error trimmed to zero
K Drift	±10mV RTO	$\pm 5^{\circ}C \times 0.04\%/^{\circ}C \times K \log (V_{IN}/E_{REF}) = \pm(3 - 0.33)mv \log (V_{IN}/0.01V) = 10mV$ @ $V_{IN} = 10V$

Total error, referred to input, at constant temperature: ±0.5%.

Total error, RTI, over the temperature range, assuming a worst-case condition that all errors are additive:

$$(\pm 0.5 \pm 0.5 \pm 0.75)\% \text{ RTI} + 10mV \text{ RTO}$$

Converting 10mV RTO to an RTI term by Table 4 yields 1.4%.

Total error RTI over the 10°C temperature range is 3.15% (1.74% root-sum-squares).

A/D converter error: If the total converter error is kept to 1LSB = 1/4096F.S., the equivalent log-amplifier output error is 5/4096 = 1.22mV. From Table 4, this is equivalent to 0.28%, referred to the input, at any level.

LOG OF CURRENT – PHOTOMULTIPLIER EXAMPLE

In this example, the output current of a photomultiplier tube is to be applied to a log amplifier, as shown in Figure 14.

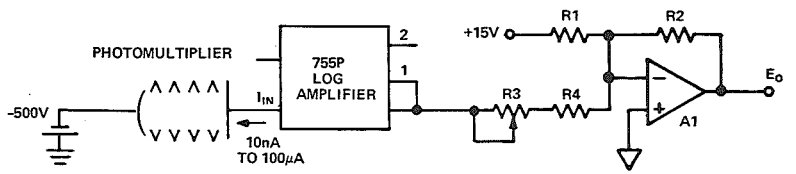


Figure 14. Log of current – photomultiplier input

Since the input is a current source, there is no need to perform the offset-voltage adjustment. This can be verified by determining the source resistance that will produce 0.5% error RTI at the lowest level: $R_S = 500\mu V/(0.005 \times 10nA) = 10M\Omega$, easily achievable with a photomultiplier.

The output of the 755P will be as predicted by the transfer curve (Figure 8). Level shifting, in this case, is accomplished by adding an offset to A1 *via* R1, and gain is trimmed by a small resistor R3 in series with R4.

For 0 to -10V output, the gain of A1 is 10/4, or 2.5, since 4V is the entire output range of the log module when spanning 4 decades at 1V/decade. The ratio of R_2 to $(R_3 + R_4)$ is then 2.5:1.

At the low end of the range (10nA), the corresponding output voltage is -3V. At the output of A1, it is amplified to (-3)(-2.5) = 7.5. In order to offset it to zero at the output of A1, R1 must have the value, determined by the gain equation

$$+15V(-R_2/R_1) = -7.5V$$

$$R_1 = 2R_2 \qquad (25)$$

If R2 is selected to be 25kΩ,

$$\begin{aligned} R_1 &= 50k\Omega \\ R_3 &= 10k\Omega \text{ pot} \\ R_4 &= 5k\Omega \end{aligned}$$

Error Analysis @ ±10° C Temperature Range

Parameter	Error	Comment
I_{REF}	≅0	Trimmed to zero by R1
I_{REF} Drift	±1%	±0.1%/°C x 10°C = ±1%
Log Conformity	±0.5%	Not trimmable
E_{os}, E_{os} Drift	≅0	Can neglect when equivalent (Thevenin) voltage is much greater than E_{os}
I_{os}	<0.1%	Worst case at lowest input current (10 nA/10 pA) (100%)
I_{os} Drift	<0.1%	Additional 10pA due to I_{os} doubling per 10°C increase
K	≅0	Initial error of 10mV trimmed to zero by R3
K Drift	12mV	±10°C x 0.04%/°C x K log (I_{IN}/10μA) = 4mV log (I_{IN}/10μA), worst-case at I_{IN} = 10nA

Total error, referred to input, at constant temperature: ±0.6%.

Total error, RTI over the temperature range:

1.7% + 12mV RTO = 4.5% RTI. Referred to the output by Table 4, 4.5% RTI is equivalent to 19.3mV, or less than 1/2% of F.S.

IV Log Ratio Applications

Chapter 2

The logarithm is a mathematical function. When it is employed to describe the behavior of a physical entity, its argument must be dimensionless. Accordingly, practical logarithmic devices always compute the log of a ratio of two voltages or currents; the numerator is termed the "signal," the denominator the "reference."

The distinction between "log" devices and "log-ratio" devices is practical, not semantic. It is determined by the requirements of the application on the "reference," and the consequent effects on the circuit design and external connections. If the reference is more-or-less fixed and considered a constant, the subject is a "log" device. If the reference is controlled by an external signal, or is simply considered to be freely variable, a different circuit design is usually employed, and it is called a "log-ratio" circuit. It is to the latter group of applications that this chapter is devoted.

A typical commercially-available log-ratio circuit (Model 756) has its performance defined over a range of 4 decades of signal current and 3 decades of reference current, or a total range of ratio of 10^7:1. While it is convenient to use and by no means expensive, the user can often find it a more practical matter to design a log ratio circuit to meet a set of *specific* needs with the aid of the basic log element (751). Log-ratio circuitry is somewhat simpler to deal with than log circuitry, because a separately-generated reference current is unnecessary.

Figure 1 shows the simplest temperature-compensated log-ratio circuit, driven by two current sources, I_{s1} and I_{s2}. Since the

operational amplifier maintains its inputs at essentially the same potential, V_A, the two log-diode-connected transistors are essentially in series-opposing, and the sum of their voltage drops, proportional to the log of their current ratio, appears at the tap of the voltage divider, V_B. If I_{s2} can be kept low enough so that it does not significantly load the voltage divider,

$$E_o \cong \left[1 + \frac{R_G}{R_{TC}}\right] \frac{kT}{q} \ln\left[\frac{I_{s1}}{I_{s2}}\right] \tag{1}$$

The divider incorporates a temperature-sensitive resistor, R_{TC}, which is designed to compensate for the temperature variation of kT/q. The resistance values of R_G and R_{TC} are chosen and trimmed to make

$$\left[1 + \frac{R_G}{R_{TC}}\right] \frac{kT}{q} \ln(10) \cong 1.00\text{V} \tag{2}$$

Therefore,

$$E_o \cong 1 \cdot \log\left[\frac{I_{s1}}{I_{s2}}\right] \qquad (1\text{V/decade}) \tag{3}$$

independently of temperature.

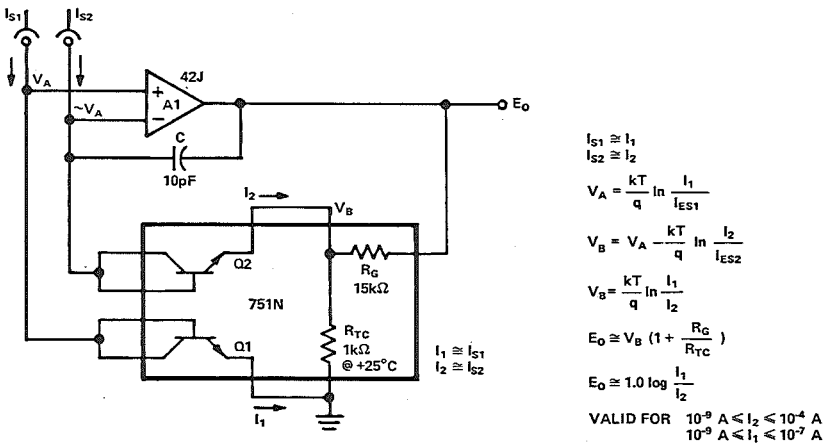


Figure 1. Simple temperature-compensated log-ratio circuit

VOLTAGE vs. CURRENT: INPUT-LOADING EFFECTS

Since the basic log elements convert linear current to log voltage, inputs in the form of current from ideal current sources having "infinite" source resistance can be used with any of the circuits to be discussed here. If the input signal is a voltage, it must first be converted to a current. This is, of course, an inherent feature of circuits that employ inverting operational amplifiers operating at zero common-mode potential.* A precise value of series resistance will determine the current scaling. However, in the simple circuit of Figure 1, employing a differential-input operational amplifier, a voltage source and its series resistor "look into" V_A. At the negative input terminal, V_A is a variable common-mode voltage; at the positive input terminal, it is a nonlinear load resistance. If the input voltages are V_{s1} and V_{s2}, in series with resistances R_{s1} and R_{s2}, then (Figure 2a)

$$\log\frac{I_1}{I_2} = \log\left[\frac{V_{s1} - V_A}{V_{s2} - V_A} \cdot \frac{R_{s2}}{R_{s1}}\right] \tag{4}$$

If the inputs are imperfect current sources, having non-infinite internal resistances, the effect is similar. The log ratio of the actual input currents is

$$\log\frac{I_1}{I_2} = \log\frac{I_{s1} - V_A/R_{s1}}{I_{s2} - V_A/R_{s2}} \tag{5}$$

V_A is an implicit function of I_{s1}, R_{s1}, V_A, and the reverse-saturation current of D1, I_{ES1}

$$V_A \cong \frac{kT}{q}\ln\frac{I_1}{I_{ES1}} = \frac{kT}{q}\ln\frac{I_{s1} - V_A/R_{s1}}{I_{ES1}} \tag{6}$$

While V_A cannot be determined explicitly, it can be plotted as a function of I_{s1} for various values of R_{s1} (Figure 2b). The plot is based on the assumption that I_{ES1} at 25°C is about 2×10^{-15} A, a realistic value for the best log transistors. For higher values of I_{ES1} or temperature, the plotted value of V_A is high, i.e., conservative, by about 60mV/decade of I_{ES} and 2mV/°C. Quite often, V_A is simply assumed to be about 0.6V; however, for

*See Fig. 8, this Chapter, and Fig. 9 in Chapter 3-1.

low-current operations, this figure could be conservative by a factor of 2 or more.

The output error attributable to V_A and finite source resistance is a term that adds to (3), approximately

$$1 \cdot \log \left[\frac{1 - V_A/R_{S1}I_{S1}}{1 - V_A/R_{S2}I_{S2}} \right] \tag{7}$$

The difference between the term inside the brackets and 1.00 is the ratio-error (%/100) contribution, referred to the input. The relationship between input and output errors can be seen in Table 4, Chapter 4-1 (K = 1).

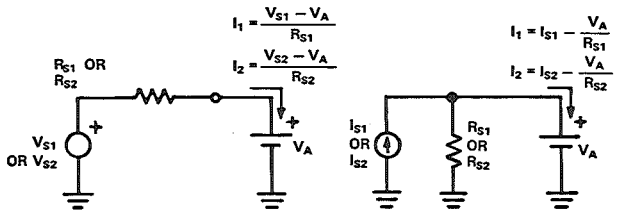


Figure 2a. Input current as a function of source voltage or current, source resistance, and V_A. Amplifier bias current and circuit leakage current are considered negligible here.

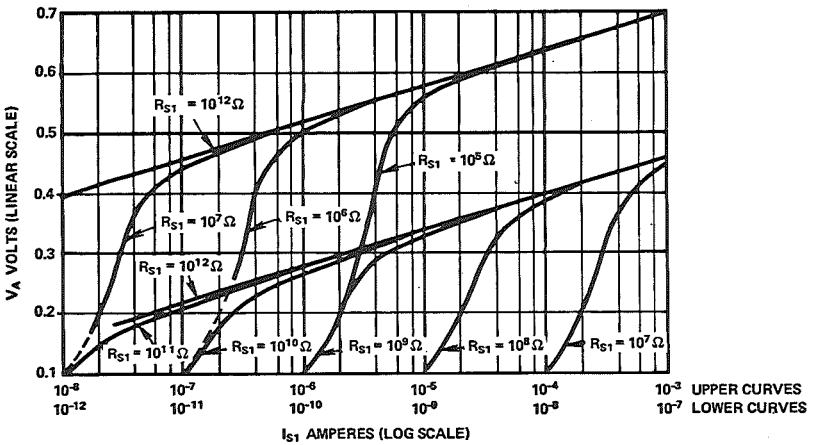


Figure 2b. V_A as a function of input current for various values of source resistance, assuming that $I_{ES} \cong 2 \times 10^{-15}$ A @ +25°C

It has been assumed that I_2 does not load the feedback voltage divider. To investigate the validity of this assumption, note that

$$E_o = V_B + R_G\left(\frac{V_B}{R_{TC}} - I_2\right) = V_B\left(1 + \frac{R_G}{R_{TC}}\right) - I_2 R_G \qquad (8)$$

The error, $I_2 R_G$, if $I_2 = 1\mu A$, is (for $R_G \cong 15k\Omega$) 15 mV, or about 4% referred to the input. For 1% error, RTI, the output error is 4.3mV, corresponding to a maximum I_2 of 290nA, for this circuit.

Because the properties of current sources may be affected by voltage, it is important, in such circuits as Figure 1, to ensure that the "compliance voltage" of the current inputs is greater than V_A, and that V_A does not seriously affect the parameters of the current source.

RESPONSE AND STABILITY

Since the transistors are connected as diodes, D2 is a passive feedback element, with a resistance = $r_E \cong (40I_2)^{-1}$. The 10pF feedback capacitance should be quite adequate to compensate for input strays (Figure 3).

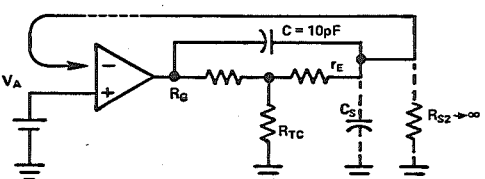


Figure 3. Dynamic model of log-ratio circuit

The effective net resistance of the feedback divider (output to summing point) is

$$R_{eff} = R_G + r_E\left(1 + \frac{R_G}{R_{TC}}\right) \cong R_G + \frac{16}{40I_2} \qquad (9)$$

For this circuit, because of the accuracy requirement implied by (8), I_2 is likely to be less than $1\mu A$, hence $R_{eff} \cong (2.5I_2)^{-1}$, and the small-signal time-constant, $R_{eff}C = C/(2.5I_2)$. For example, if C = 10pF and we are considering small-signal variations of I_2 in the neighborhood of 100nA, $\tau = 40\mu s$, $\omega = 25kr/s \rightarrow 4kHz$.

For small changes in I_1, which may be considered to be changes in V_A/r_E (I_{s2} fixed and having negligible admittance), the output will immediately change by V_A $(1 + C_s/C)$, then continue on to the final value with the same exponential time-constant as discussed above.

For transdiode applications, if feedback to the amplifier's positive input can be considered negligible, the stability considerations are quite similar to those discussed in Chapter 3-1 (Equations 10 to 16 and Figures 5, 6, and 7 are quite relevant). For stability explorations, the open-loop gain of the amplifier may be considered to be reduced by $(1 + R_G/R_{TC})$, thus lowering its Bodé plot by 20 log 16 = 24.1dB, and R_E is, in effect, the parallel combination of R_G and $R_{TC} \cong 940\Omega$.

APPLICATION CONSIDERATIONS

Thus far, there have been a number of tacit assumptions: that the diode-connected log elements are matched and are isothermal with each other and with the compensation resistors, that the diodes operate in the range for which h_{FE} is sufficiently large and the bulk resistance sufficiently small to cause negligible errors, and that the amplifier's offset voltage, bias current, and common-mode errors are negligible. We shall now look more closely at the amplifier requirements, at various elements of log-ratio-circuit performance specifications, and at a number of alternatives to the circuit of Figure 1.

CHOOSING THE OP AMP

In low-current operation, the time constants involved are significantly longer than amplifier time constants and preclude the possibility of operation at high frequency. The bandwidth restrictions on the choice of op amp are therefore minimal, unless log operation is confined to high current levels.

Bias current is the primary specification for all log applications involving current-input signals. The op amp's bias current is added to the input signal (±) and flows through the log element. Errors can be stated directly as percentage of input.

$$\%\ \text{error RTI due to } I_{BIAS} = 100\%\ (I_b/I_s) \qquad (10)$$

For log voltage ratio applications, the input signal is converted to a current by the input resistor. The resulting current should be the value of I_s that is compared with I_b in (10).

Offset voltage is of little importance in log current-ratio applications if the current signals are "true current sources." The effect of offset voltage (E_{os}) for either current or voltage applications is

$$\%\ \text{error RTI due to } E_{os} = 100\%\ (E_{os}/V_s) \qquad (11)$$

For voltage applications, V_s is the voltage signal to be logged. For current applications, V_s is the equivalent open-circuit voltage source corresponding to I_sR_s. If E_{os} is not very much smaller than the smallest value of V_s for which a stated accuracy level is desired, it can be a significant source of error and should be trimmed to zero. (Also, in such applications, the amplifier should be chosen for low thermal drift, as noted below.)

Offset-voltage drift is important for those applications in which the current input is not provided by an ideal current source. To determine the required amplifier-offset specification, the temperature range, the allowable % error over the temperature range, and the lowest voltage for which that % error must be maintained are decided upon. The maximum allowable amplifier offset temperature-coefficient is

$$E_{os}\text{T.C.} = \frac{V_{min}\ \delta_{max}}{\Delta T\quad 100} \qquad (12)$$

where V_{min} is the lowest input voltage

δ_{max} is the largest allowable % error at V_{min}

ΔT is the change of temperature from the temperature at which E_{os} was trimmed to zero.

For example, an input range of 10mV to 10V is to be applied to one terminal of a log-ratio device (assuming that the common-mode voltage is zero), and it is necessary the E_{os} contribute no more than 1% error over the range 20°C to 40°C. E_{os} might be

trimmed to zero at mid-range (30°C). Then the required offset temperature coefficient would be

$$E_{os}T.C. = \frac{0.01 \times 1}{\pm 10° \times 100} = 10\mu V/°C \qquad (13)$$

The same procedure would be followed to determine I_b and E_{os} requirements for the second input terminal.

Output-current rating, as with all op amp circuits, would be selected for the capability of supplying the maximum requirements of the load, in addition to the requirements of the feedback circuitry (usually negligible).

OTHER CONSIDERATIONS

Dynamic Range: The dynamic range of the circuitry used in a given application is determined by the logarithmic resolution of the device used as a log element, the dynamic range of the input signal, restrictions caused by characteristics of the specific circuit configuration and the devices used in it, and the desired accuracy level. A typical basic log element, such as Model 751N, can be used over a range of 100pA to 1mA with less than 2% error; over limited ranges, better accuracy can be obtained. For the circuit of Figure 1, dynamic range was limited primarily by the common-mode range for voltage sources and source resistance for current sources, at the low end, and by I_2R_G at the high end. More-sophisticated circuits are available, as will be shown in a later section, in which the characteristics of the log element are the primary limit to the dynamic range, assuming proper op-amp selection and care in circuiting.

Polarity of the Input Signal and of the Log Device: All log elements are restricted to inputs of a single polarity (but the outputs can be bipolar, with zero occurring at unity current ratio). By definition of the logarithm, the log of zero and the log of a negative number do not have real values. This means that for a given design, the input currents must both be of the same polarity, and of such polarity that the diodes are conducting in the forward direction, i.e., the most favorable direction for log behavior. Of course, input signals may be conditioned in preceding stages,

except in the case of extremely low currents, for which immediate conversion may be desirable.

If a transistor is diode-connected, either an N (NPN) or P (PNP) log element may be used, since the transistor is connected as a reversible two-terminal device. (In such cases, direct input currents of either polarity may be applied, and properly dealt-with in post-conversion conditioning.) In general, log-transistor connections (transdiode and follower) are not reversible, and polarity must be specified as "P" type for applications requiring PNP transistors (751P) and "N" type (751N) for applications requiring NPN transistors.

Temperature Range: Nearly all of today's commercially-available logarithmic modules, whether basic log elements, log transconductors, log amplifiers, or log-ratio modules, are temperature-compensated. Specially selected resistors (R_{TC} in the circuits discussed above), having resistance that increases predictably with temperature, are used to reduce the temperature-dependence of the log equation, (kT/q) ln (ratio), from 0.3%/°C to 0.04%/°C. Although this is an order-of-magnitude reduction of error, there can still be considerable contribution of scale-factor error if large temperature excursions are to be encountered. The offset voltage and bias current of op amps can also contribute significant error over wide temperature ranges. Of concern for measurements at very low currents, high temperatures may increase I_{ES} by several orders of magnitude; though the log transistors may still track, their log-conformity errors will be considerably increased.

For these reasons, the user of log devices who seeks high-accuracy wide-range operation is urged to limit ambient temperature variations to the vicinity of ±10°C. An analysis illustrating the effects of temperature in a typical application, involving the voltage/current log module Model 756, is given at the end of this chapter.

Output Polarity: The output voltage of the log-ratio circuit can be either positive, negative, or bipolar, depending on the ratio I_1/I_2, and whether or not offsets are added at the output. Figure 4 shows the output as a function of the ratio of input currents for

two different scale factors. For any given application, only a portion of the entire 14-decade (potential) range would be used. By determining the range of expected input signals and computing their ratios, one can use Figure 4 to predict the expected output-voltage range. I_1 and I_2 may be assigned arbitrarily, to match device performance to current range, but polarity should be observed.

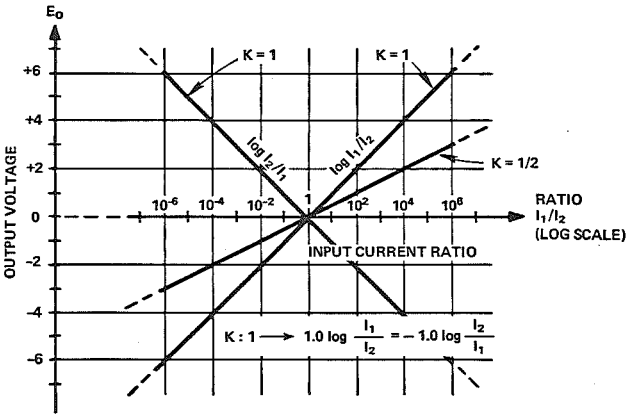


Figure 4. Output of ideal log-ratio circuit vs. input ratio, showing effect of exchanging numerator and denominator

If for any reason* it is necessary to change the effective input scaling, so that the zero-output point occurs at a ratio other than unity, but the input signals themselves are unavailable for scaling, the output can be offset by applying a current to the junction of R_G and R_{TC}, as shown in Figure 5. As noted earlier (Chapter 4-1), the voltage at this point (V_B) is determined by the *inputs*. Therefore, any current added must flow through R_G, offsetting the output by $-I_B R_G$.

Since V_B is a function of the input ratio (60mV per decade-change), the offsetting current source in Figure 5 should have high-enough source impedance to be unaffected by variations of V_B.

*Examples include: locating 0 at the middle or extremities of the range, and measuring deviations of equipment from a fixed gain or attenuation, e.g., determining by how many "dB", an actual gain differs from a nominal gain of 100X.

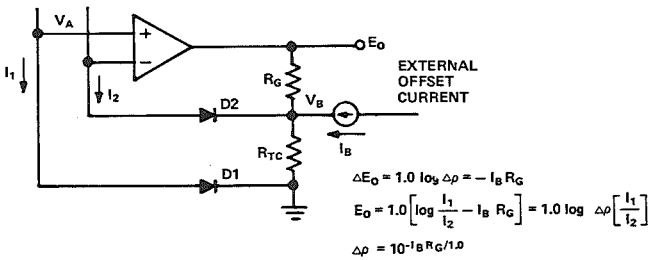


Figure 5. Offsetting the output to shift the zero output (unity ratio) coordinate. The output shift, ΔE_O, corresponds to the input ratio multiple $\Delta\rho$ (K = 1.0).

If the signal is to be processed beyond the log-ratio amplifier, it may be better and easier to simply add a constant voltage or current at an op-amp summing junction in a succeeding stage.

Log Conformity is the specification of logarithmic devices that is akin to *linearity* in linear devices. Log-conformity error is the difference between the theoretical value of the logarithm of a ratio and the actual value that appears at the output of a log-ratio circuit after initial zeroing at unity-ratio, and scale-factor adjustment (either by end-point or best-straight-line* method).

Log conformity is basically limited by degradation of transistor gain at low current levels and by base-spreading resistance at high current levels. The form of connection affects the gain at low current levels; for example, diode-connected log transistors have a useful log range that is limited to about 1nA at the low end. If the log devices are used as transistors ("transdiode") rather than as diodes (base and collector tied together), additional decades of performance are available at the low end.

Base-spreading resistance, for log transistors, is a small resistance of a few ohms that appears in series with the emitter. For an emitter current of 1mA and 1Ω of series resistance, an error of 1mV will be obtained. The feedback attenuator will cause it to be magnified by $(1 + R_G/R_{TC})$ at the output. For 1V/decade operation, a 16mV error will be obtained for every ohm of

*But "best straight line" implies the ability to measure log conformity *a priori*. Although "best straight line," usually specified, gives a 2X tighter specification, "end point" is easier to measure, since it is more easily located

base-spreading resistance. Referred to the input ratio, this is an error approaching 4%/Ω. This source of error can be reduced to a satisfactory level with most of the transistor types used for log operations by restricting input signals to about 100μA maximum.

Log Voltage-Ratio: Much that has been said about log current-ratio is also pertinent to log voltage-ratio as well. The only additional consideration for voltage applications is the means of converting voltage to the current needed by the log element. If the summing junctions of input amplifiers are available, the problem is trivial, for all that is required is to attach a resistor from the voltage source to the summing junction.

The input current I_{IN} is then

$$I_{IN} = \frac{V_{IN} - E_{os}}{R_{IN}} \tag{14}$$

The initial amplifier E_{os} should be trimmed to zero, and the amplifier chosen should have low E_{os} drift over the temperature range of concern.

As noted earlier, there are a number of circuit configurations that do not permit voltage to be easily and accurately converted to a current. These configurations are referred to as log current-ratio designs. Fortunately, many of the natural phenomena, for which log-ratio measurements are desired, are measured by transducers that provide current outputs. It is important that the designer assure himself that such transducers have sufficient "compliance voltage" to behave as ideal current sources in the presence of voltages of the order of 0.6-0.7V (V_A in Figure 1).

EXAMPLES OF LOG-RATIO CONFIGURATIONS

The circuit of Figure 6 is similar to that of Figure 1, but Q2 is connected as a "transdiode" rather than as a diode, extending its range at the low end. Currents from a few picoamperes to about 0.3μA may be converted with good accuracy.

Since I_{s1} must furnish the base current for Q2, while maintaining the base voltage at V_A, the range of I_{s1} is restricted at the low

end. For example, if h_{FE2} = 150 at I_{s2} = 0.3μA, then I_{s1} must furnish 2nA of base current to Q2. Even if this is the maximum base current that must be supplied, over the expected range of I_{s2}, it is evident that I_{s1} must always be greater than 400nA to ensure that the contribution of this source of error will be less than 0.5%.

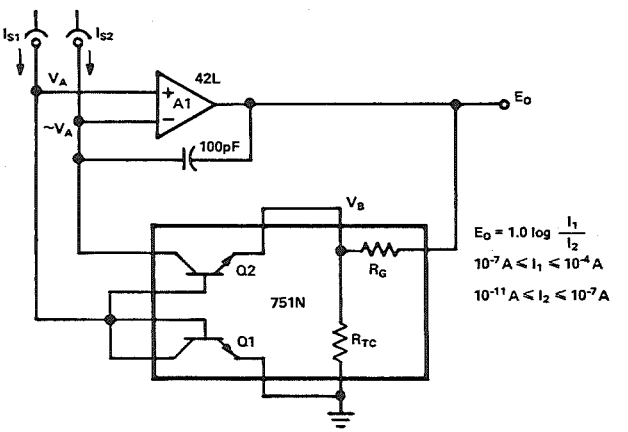


Figure 6. Modification of the circuit of Figure 1 to extend the range of I_{S2} at the low end

The amplifier is of the Model 42 family, with bias current considerably less than the smallest signal to be processed.

Even though the dynamic range of I_{s2} has been increased at the low end, the restriction on I_{s2} for currents higher than 0.3μA still persists, because of the error caused by the flow of I_2 through R_G.

If a follower-connected op amp is used to unload V_A and drive the base of Q2, the current swing of I_{s1} at the low end can be greatly extended.

In the circuit of Figure 7, which happens to have negative input currents but uses an N-type basic log element, the feedback element is a follower-connected log transistor. Since the current that flows through R_G is just the base current of Q1, the dynamic range is greatly improved at the high end. However, the low end for I_{s2} is still degraded, due to the diode connection of Q2. In addition, the log conformity error for the ratio will be increased because the base and collector of Q2 are at slightly-differing potentials.

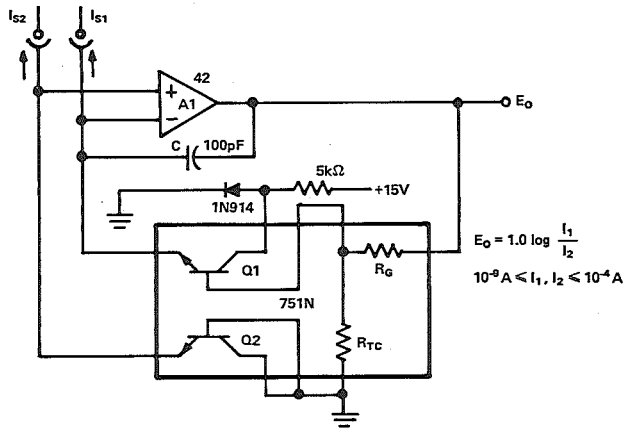


Figure 7. Follower-connected log transistor unloads the $R_G - R_{TC}$ divider, allows wider range of current swing

Figure 8 provides accurate wide-range log-ratio conversion for voltage and/or current inputs. Ideal for wide-range voltage signals, this circuit employs chopper-stabilized 234 amplifiers for low voltage offset and drift, enabling the accurate processing of signals ranging from 1mV to 10V. If higher input voltages are desired, the 100kΩ series input resistors would be scaled proportionally (e.g., 1MΩ for 100V). The dynamic range would be increased, because the low-end resolution would still be 1mV.

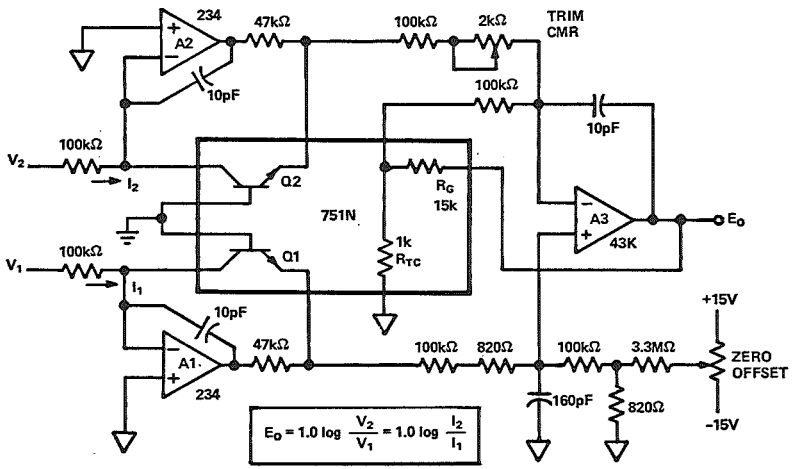


Figure 8. Wide-range log of voltage — or current — ratio

The individual log signals at the outputs of A1 and A2 are subtracted and amplified in A3's circuit, using precision resistors and the 751's temperature-compensating resistance network. As in the other circuits, temperature compensation and gain are provided by R_G and R_{TC}. The high-performance Model 43K was chosen to provide good common-mode rejection for low-level signals, low noise, and low offset drift.

LOG-RATIO MODULE

Figure 9 is a block diagram of a self-contained temperature-compensated log-ratio module, Model 756. Log current-ratio is computed by applying the input currents directly at the input terminals (amplifier summing junctions). Input voltages can be converted to current by applying them in series with external resistances, of appropriate magnitude and stability. The internal log amplifiers convert the input currents to log voltages, which are subtracted to obtain the log-ratio, and the difference is furnished at low impedance by the output amplifier.

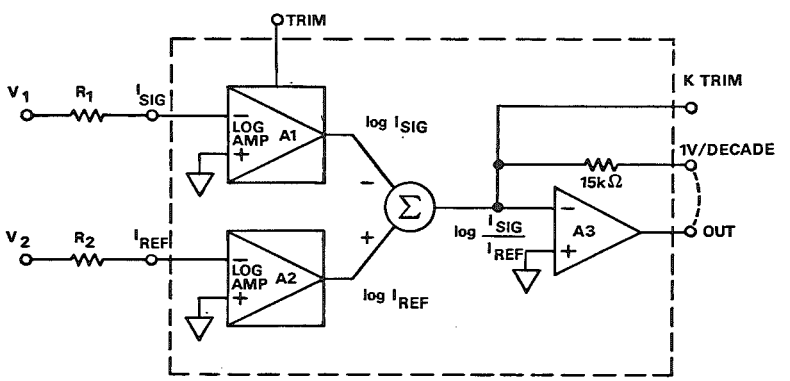


Figure 9. Functional block diagram of Model 756 log-ratio module

The 756 capitalizes on the asymmetry of typical applications that require log ratios, to obtain a near-optimum price/performance ratio: the "signal" input, channel 1, uses a high-performance FET-input amplifier with 10pA maximum bias current, which allows input signals from 1nA to 100μA to be processed accurately. The second input, the "reference," channel 2, can

process signals spanning 3 decades of current with good results For best results, if channel 2 is scaled to a geometric mean of 1μA, with variations of ±1 decade (from 100nA to 10μA), there will be no appreciable error as the input current at channel 1 is varied from 1nA to 100μA (7 decades of log ratio).

Figure 10 is a typical plot of log-conformity error as a function of I_1 for various intermediate values of I_2. (It must be emphasized that I_2, like I_1, is continuously variable.) The curve is typical for separate or simultaneous variation of I_1 and I_2.

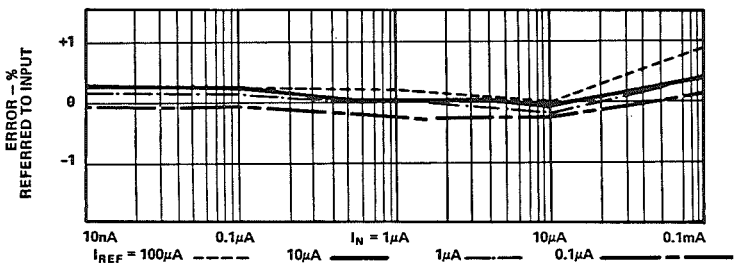


Figure 10. Typical log-conformity plot for Model 756 log-ratio module. (% Error (RTI) vs. I_{SIG})

The performance of the 756 is representative of performance that can be obtained using appropriate log-ratio schemes, involving the basic log element and op amps, provided that good design practice is adhered to.

Best overall operation (except for bandwidth) is almost always obtained when operating in the center of the range (geometric mean of the extremes), avoiding errors due to bias current and reduced transistor current-gain at the low end, and errors due to base-spreading resistance at the high end.

CHOOSING AN APPROACH

The alternatives facing a designer are essentially three:

1. To buy a self-contained log-ratio module

2. To assemble two log amplifiers and a difference amplifier in a configuration similar to that of Figure 9.

3. To design and build a circuit that is an optimum compromise between cost and performance, using basic log elements and operational amplifiers.

For the general run of applications for which its performance is suitable, in laboratory and instrumentation applications, systems, and equipment, option 1 is the best choice. It allows the designer complete freedom to deal with other system problems, once the choice is made. If the potential usage involves large numbers (e.g., more than 100 units), the designer may wish to investigate possible economies via option 3.

If the design problem involves current ranges at one (or both) inputs exceeding the available performance of the log-ratio module, the second option should be considered. It can make available from 12 to 14 decades of log-ratio (240 to 180 "dB"). Naturally, it is somewhat more expensive than the first option. If the potential usage involves large numbers, the designer may again wish to investigate possible economies via option 3.

The designer will consider option 3 where the quantity of devices required (especially if performance requirements are looser than those specified for packaged units) suggest the possibility of economy through a special-purpose design or a more-compact overall package. He should also consider the third option if, in addition, unusual combinations of dynamic range, input signal (voltage or current), polarity, scaling, or combined operations (log products and ratios) are involved.

If possible cost-savings over a standard module are the *sole* motive for considering option 3, the designer should take into account other costs in addition to parts and labor; these include, of course, design and development; they also include costs of parts procurement and inventory, availability of potting facilities (a *must* for reasonable performance of the basic log elements—see Chapter 4-1), test and temperature-performance trimming facilities, the unavoidable scrap, plus appropriate overhead rates. Often these hidden costs increase the attractiveness of complete-module prices in large quantity.

The form in which the input signal presents itself may play a large

part in narrowing the selection of designs. If the inputs are true current sources, any of the alternatives presented are suitable. But if V_A is an appreciable fraction of the input voltage, or if the signal is the short-circuit current of a very low voltage device, then amplifier summing junctions must be made available. Such applications suggest options 1 and 2.

A key step in the design is the consideration of polarity. For designs where positive current flow (opposite to electron flow) is from the source toward the input terminal, an N type module (NPN transistor) would be selected. If the current flow is negative (for instance, photomultipliers), positive current must flow toward the source, calling for a P-type module (PNP transistor)*. If the log transistors are both connected as two-terminal diodes, either polarity (N or P) may be used.

DESIGN EXAMPLE

Figure 11 shows a log-ratio module used in a photometer application. Two inputs represent the intensities of light transmitted through space and through a medium that absorbs light. The *absorbance* of the medium is given by the formula

$$-A = \log \frac{I_{signal}}{I_{reference}} \qquad (15)$$

where I_{signal} and $I_{reference}$ are the currents representing the received light intensities.

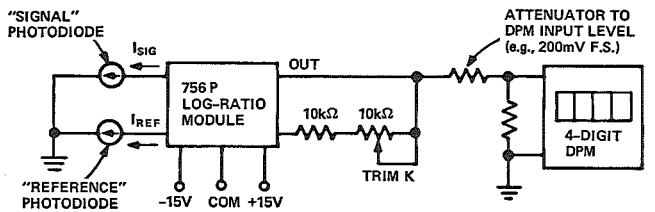


Figure 11. Log ratio applied to absorbance measurement

The transducers used in this application are photodiodes, devices that provide a short-circuit current that is proportional to the intensity of applied light.

*Figure 7 is an exception

The lowest value of absorbance is determined by the value of I_{ref}, since when $I_{sig} = I_{ref}$, A = 0. In this case, I_{ref} is assumed to be 10μA. The actual value for the specific application depends on the intensity of light and the characteristics of the photodiode employed.

The output of the log-ratio module is externally trimmed to be precisely 1V/decade and is applied to the input of a 4-digit DPM through the scaling network R1 and R2.

The 756 log-ratio module was chosen for the design, principally because it makes available both amplifier summing junctions. When the photodiodes are connected to the summing junctions, they are operated with zero volts, i.e., in the short-circuit mode.

Short-circuit loading is necessary, because accuracy of the photodiodes can be degraded several percent when operated with as little as 100mV of output voltage.

Error Analysis: Log Current-Ratio analysis for the absorbance measurements of Figure 11

Conditions: I_{sig} = 10nA to 10μA, I_{ref} = 10μA ±50%, temperature range = 25°C ± 10°C

Parameter	Error	Comment
Log Conformity	±0.5% RTI	Specified as ±0.5%max for Model 756
Scale Factor, K	≅0	Initial error of ±1% is trimmed to zero for this application
K Drift	12mV RTO	$\pm 10^{\circ}C \times 0.04\%/^{\circ}C \times K \times \log \frac{I_{sig}}{I_{ref}}$
I_{os}	≅0	I_{os} at I_{ref} input has negligible error due to the relatively high value of I_{ref}. I_{os} at I_{sig} input is 0.1% of smallest expected I_{sig}.
I_{os} Drift	−0.1%	Additional 10pA due to I_{os} doubling per 10°C
E_{os}, E_{os} Drift	≅0	This contribution is held to a negligible value due to the low initial offset and offset vs. temperature. The data sheet for the photodiode should be consulted to determine the error in I_{sc} due to E_{os} across the diode.

Total RTI error at 25°C = ±0.6%, or 2.6mV at the output, less than 0.1% of the 3V full-scale output range.

Total RTI error over the temperature range is

±0.7% RTI ±12mV RTO = 3.5% RTI, assuming all errors to be directly additive, a worst-case condition

Referring the 3.5% RTI error to the output results in 15mV of error, or 0.5% of the 3V maximum output.

SPECIFICATIONS OF MODEL 756N/P

Current Log Ratio
Transfer Equation $E_o = -K \log \frac{I_1}{I_2}$, I_1 = signal, I_2 = reference

Transfer Equation including Error Terms $E_o = -K\left[\log \frac{I_1 - I_{b1}}{I_2 - I_{b2}} + E_{os3}\right]$

Voltage Log Ratio
Transfer Equation $E_o = -K \log\left[\frac{V_1}{V_2} \times \frac{R_2}{R_1}\right]$

Transfer Equation including $E_o = -K\left[\log\left(\frac{\frac{V_1 - E_{os1}}{R_1} - I_{b1}}{\frac{V_2 - E_{os2}}{R_2} - I_{b2}}\right) + E_{os3}\right]$

Parameter	Value
Signal Current, I_1 [1]	10nA to 100μA (4 decades)
Reference Current, I_2 [1]	100nA to 100μA (3 decades)
Log Conformity [2]	±0.5% (2 decades, I_2 constant)
	±1.0% (4 decades, I_2 constant)
Scale Factor, K [1,3]	1V ±1% ±0.04%/°C
Bias Current, I_{b1}	10pA, doubles/10°C
Bias Current, I_{b2}	10nA, max, ±1%/°C
Offset Voltage, E_{os1} [3]	±1mV, max, 25μV/°C
Offset Voltage, E_{os2}	0.5mV, max, 30μV/°C max
Output Offset, E_{os3} [3]	±10mV, max, 85μV/°C

Small Signal Response

I_{IN}	f_t
1nA	1kHz
1μA	8kHz
100μA	25kHz

Rated Output

Log Mode	±10V at 5mA
Antilog Mode	±10V at 4mA

Response Time

I_{IN} (increasing)	time	I_{IN} (decreasing)	time
1nA to 10nA	70μs	10nA to 1nA	200μs
10nA to 100nA	25μs	100nA to 10nA	50μs
100nA to 1μA	25μs	1μA to 100nA	25μs
1μA to 100μA	20μs	100μA to 1μA	20μs

Noise in 10kHz B.W.

V_n, INPUT 1	3μV rms
V_n, INPUT 2	3μV rms
I_n, INPUT 1	0.1pA rms
I_n, INPUT 2	20pA rms

Power

Quiescent Current	3mA at ±15V
PSRR	54dB

[1] Positive for positive inputs (N type), negative for negative inputs (P type).

[2] The log conformity specification is referred to input (R.T.I.). Note: 1% error R.T.I. is equivalent to 4.3mV of error at output for K = 1V.

[3] Externally trimmable.

IV Antilog Applications

Chapter 3

The antilog(arithm) is the inverse of the logarithm. It is by definition the *exponential*, in which the logarithmic base is raised to a power. That is,

$$x = \log_B{}^{-1}(y) = B^y \tag{1}$$

If $y = \log_{10} x$, then $x = 10^y$. If $y = \ln x$, then $x = e^y$. The same argument can be expressed in terms of exponentials of any base. For example,

$$x = 10^y = (e^{\ln 10})^y = e^{y \cdot \ln(10)} = e^{y/(\log_{10} e)} \tag{2}$$

Logarithmic devices with the transfer function

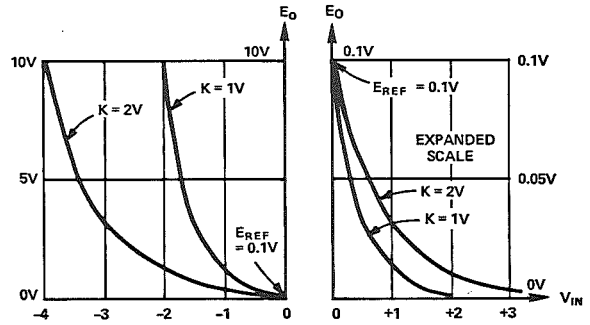
$$E_o = -K \log_{10} \frac{V_{IN}}{E_{REF}} \tag{3}$$

are usually available with a connection scheme that allows the input and feedback circuits to be interchanged to compute

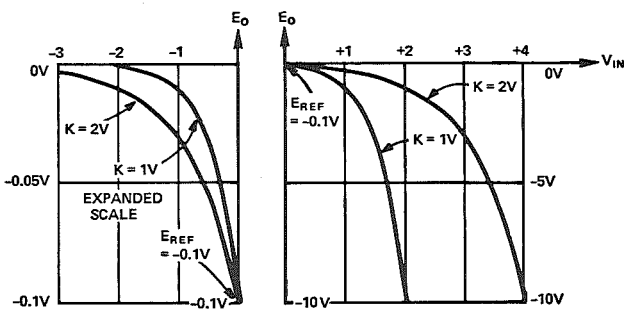
$$E_o = E_{REF} \cdot 10^{(V_{IN}/-K)} = I_{REF}\, R_f \cdot 10^{(V_{IN}/-K)} \tag{4}$$

Thus, if K = 1, (3) provides an output of 1 volt per-decade of the input ratio, while (4) provides an output that changes by 1 decade for each volt of input. E_{REF} in (3) is interpreted as the starting point (e.g., 0) for the log ratio, the input value at which the ratio is unity and the output is zero. In (4), E_{REF} is interpreted as the normalized value of the exponential, and each volt of input either multiplies or divides E_{REF} by an additional factor of 10.

Figure 1 is a plot of the exponential response of N-type and P-type modules with correct polarity on a linear scale. Because of the wide range of variation of the output, it would be difficult to show the output values accurately without changing scales for each decade. Alternatively, it is possible to compromise and plot output (on a log scale) against the input (Figure 2).



a) E_O vs. V_{IN} for N-type antilog operator. Vertical scale: 10V max, $V_{IN} \leq 0$; 0.1V max, $V_{IN} \geq 0$



b) E_O vs. V_{IN} for P-type antilog operator. Vertical Scale: -10V min, $V_{IN} \geq 0$; -0.1V min, $V_{IN} \leq 0$

Figure 1. Antilog-operator response curves (linear scale)

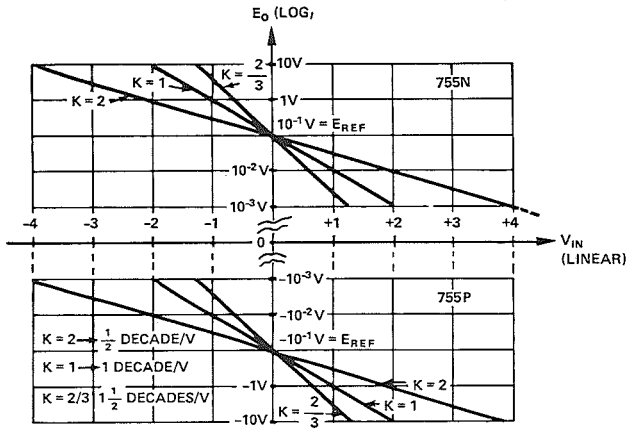


Figure 2. Antilog operator response curves, semilog scale.

$E_O = E_{REF}\ 10^{V_{IN}/-K}$

WHERE THEY ARE USED

Exponential devices are used in at least three classes of application

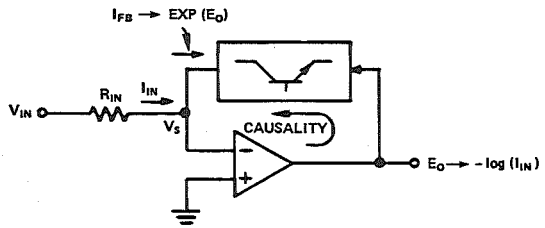
1. When compound multiplications, involving roots and powers, are performed (e.g., $x_1^{\alpha} \cdot x_2^{\beta} \cdot x_3^{\gamma} \cdot x_4^{\delta} \cdot \ldots$), each input is "logged", multiplied by a constant (or variable) exponent of appropriate magnitude and polarity, the terms are summed and/or differenced, then the antilog is taken to convert the result back to the "world of phenomena."

2. If measurements are performed by devices having logarithmic responses they may be linearized, if necessary, by the use of the antilog. An example is given in this chapter.

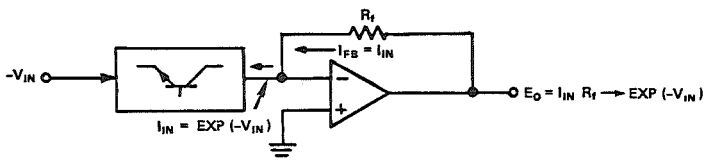
3. The exponential may be used in function fitting and function generation to obtain relationships or generate curves having voltage-programmable rates of growth or decay. For example, if V_{IN} is a ramp, E_o will be a widely-ranging exponential function of time, with time-constant determined by K, and scale-factor determined by E_{REF}. K can be manipulated by changing the input gain (variably with an IC multiplier, if desired).

AVAILABLE OPTIONS

The options available for antilog operation are essentially the same as those for log-voltage operation. Log-voltage circuits (Chapters 3-1, 4-1) become antilog circuits by interchanging the input and feedback circuit elements. In the case of logarithmic circuitry (Figure 3), the log is achieved by feeding back a current which is the antilog ($I = I_o e^{qV/kT}$) of the output; the operational amplifier forces this feedback current to be equal to the input current, therefore the output must be proportional to the log of the input. For antilog operation, the antilog element is placed in the forward path, and the feedback circuit is closed by a resistor that transduces the output voltage into a current to equal the exponential input current; the output voltage is thus forced to be proportional to the antilog of the input.



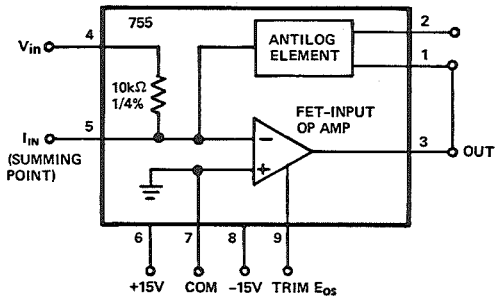
a) Antilog function in feedback path. Amplifier forces $I_{FB} = I_{IN}$ and $V_S = 0$ by making E_O proportional to log (I_{FB})



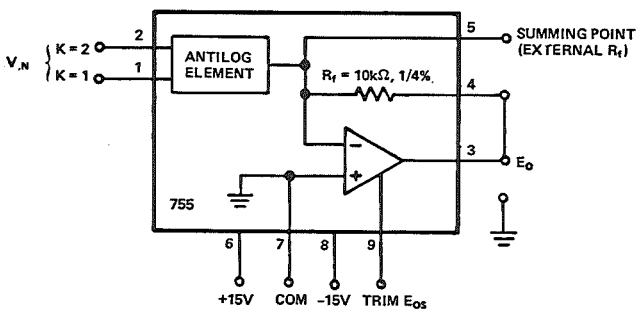
b) Antilog function in forward path converts input voltage to exponential current. Amplifier converts current to exponential voltage via R_f

Figure 3. Using feedback to enforce direct and inverse relationships

There are some log modules that are committed to log operation alone, but they are in the minority. Most commercially-available log amplifiers can also serve in antilog applications. Figure 4 shows how the Model 755 is connected in the log and antilog modes.



a) Log/antilog amplifier connected in the log mode (K = 1)



b) Log/antilog amplifier connected in the exponential mode

Figure 4. Log/antilog amplifer connections

The reader may observe that log modules are usually specified to have considerably greater dynamic range (of accurate operation) for current inputs than for voltage inputs (6 or 7 decades to 4). For normal, practical antilog circuitry, however, the output is from an operational amplifier, the input-offset of which imposes

the low-end output accuracy restriction (10μV offset, for example, is 1% of the lowest of 4 decades (1% of $10V/10^4 = 10\mu V$).*

OTHER BASES

For some applications, it may be desirable to interpret the exponential function (4) in terms of a base other than 10. This can be done easily by the use of the identity in (2). If $V_{IN}/-K$ in (4) is the same as y in (2), then to convert to a different base B, a new constant K′ may be defined such that

$$10^{V_{IN}/-K} = B^{V_{IN}/-K'} = B^{V_{IN}/(-K\log_{10}B)} \tag{5}$$

from which,

$$K' = K \log_{10} B \tag{6}$$

For example, if B = 1.10, which defines an exponential having a growth rate of 10% as V_{IN} becomes more negative, then K = 1 defines a negative-going input interval of

$$K' = 1 \cdot \log_{10} 1.10 = 0.0414V \tag{7}$$

for each 10% increase of the output. Put another way, it is analogous to a continuously compounded interest rate of 10% per-41.4mV "year." If B = 2, K′ = 0.3010; if B = e, K′ = 0.4343.

That the input intervals are negative-going is a consequence of the negative slopes that can be observed in Figure 1. This is accounted for by the fact that, like the log circuit, the antilog function is produced by essentially a single inverting operational amplifier,

*It should be noted, nevertheless, that the summing-point current from the input element is independent of small amplifier offsets and is imposed at high impedance (the antilog amplifier acts as a unity-gain follower for its offset voltage). In concept, then, if the feedback current could be tapped for a "downstream" element requiring a wide range of exponential current, antilog accuracy could be maintained over a wider dynamic range. In practice, this is difficult to achieve in a simple manner, unless the "load" is, in effect, a two-terminal device that can be connected in series in the feedback path of the amplifier.

which must have a transfer function with a negative slope. If the signal input were held constant and the reference input (if available) varied, the slope would be inverted. An easier way, with standard modules, is simply to use an inverting op amp to precede the antilog circuit; it can also be used to scale K′ to a convenient round-number value.

ERRORS

Although all the specifications for a log module apply to both log and antilog modes of operation, with "RTI" and "RTO" interchanged, the observed effect of each parameter is manifested at the output quite differently. By examining the transfer equation, one can predict these effects.

$$E_o = I_{REF}\ R_f \cdot 10^{V_{IN}/-K} + E_{os} \qquad (8)$$

Offset Voltage (E_{OS}): As noted earlier, it appears at the output as a constant dc voltage. Its percentage error contribution is 100% X (E_{os}/E_o). For small output signals, E_{os} is a major source of error. If output signals in the millivolt range are expected, E_{os} should be adjusted to zero. Since the device is operated in the voltage mode, the contribution of bias current to output offset is negligible (e.g., at 25°C, I_b for the 755 is 10^{-11}A; with a 10kΩ feedback resistance, the contribution is $10^{-11} \times 10^4 = 10^{-7}$V).

Adjusting E_{os} to Zero: To adjust E_{os} to zero, a value of input voltage is applied that will essentially cut off the flow of current to the summing point. Then the offset-adjust potentiometer is adjusted for zero output. For example, if the input terminal of an N-type module (K = 2) is connected to +15V (-15V for P types), the theoretical contribution of input to the output signal is 7.5 decades below 0.1V, well into the noise level. For reasonable sensitivity of output reading, a small resistance can be connected from the summing point to ground (100Ω to ground establishes a gain of 101, resulting in 1 mV out per 10μV of input offset), as shown in Figure 5.

After adjusting to zero, the jumper to 15V and the 100Ω resistor (if used) should be removed.

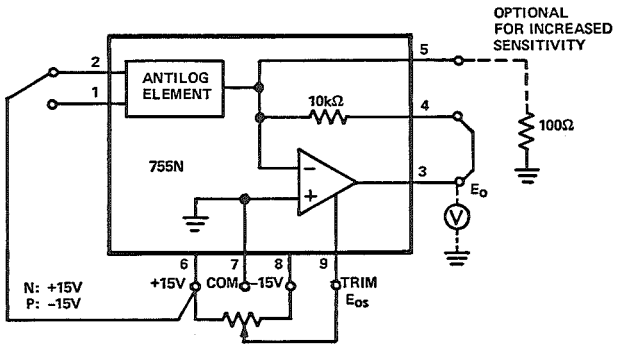


Figure 5. Circuit for trimming E_{OS} to zero in antilog mode

Reference Current (I_{REF}): Errors associated with $E_{REF} = I_{REF} R_f$ appear directly at the output, since I_{REF} acts as a gain factor. For example, if I_{REF} is 1% too high, it will cause the output voltage to be 1% too high. E_{REF} can be calibrated by applying 0 input (grounding the input), then trimming the feedback resistor (by series or parallel resistance) until the output is equal to E_{REF} (0.1V for the 755). It is more convenient to adjust R_f than I_{REF}, if an external means of adjusting I_{REF} has not been provided in the device. I_{REF} can also be adjusted by biasing the input.

Scale Factor (K): Errors associated with K are manifested as errors of the input scale factor; their effect on the output is a modification of the exponent. If the actual value of K is $K/(1 + \delta)$, then the error, defined as the difference between the actual and theoretical value of output, divided by the theoretical value, is

$$\frac{0.1 \times 10^{(1+\delta)V_{IN}/-K} - 0.1 \times 10^{V_{IN}/-K}}{0.1 \times 10^{V_{IN}/-K}} \tag{9}$$

$$= 10^{\delta V_{IN}/-K} - 1 \tag{10}$$

For $\delta = 0.01$ (1%), the fractional output error is $10^{0.01 V_{IN}/-K}$ For $V_{IN}/-K = 2$, the error is $1.047 - 1 = 0.047$, i.e., 4.7%.

The table provides a brief listing of output errors as a function of V_{IN}/K, for several values of δ. (The range of $V_{IN}/-K$ for the 755 is -2 to +2.) Linear interpolation may be used for intermediate values.

TABLE 1. OUTPUT ERRORS, AS A FUNCTION OF K ERRORS, IN % OF ACTUAL OUTPUT VALUE

$V_{IN}/-K$	K Error (100% X δ)						
	+1%	+0.3%	+0.1%	0	−0.1%	−0.3%	−1%
4	9.6	2.8	0.93	0	−0.92	−2.7	−8.8
3	7.2	2.1	0.69	0	−0.69	−2.1	−6.7
2	4.7	1.4	0.46	0	−0.46	−1.4	−4.5
1	2.3	0.7	0.23	0	−0.23	−0.7	−2.3
0	0	0	0	0	0	0	0
−1	−2.3	−0.7	−0.23	0	0.23	0.7	2.3
−2	−4.5	−1.4	−0.46	0	0.46	1.4	4.7
−3	−6.7	−2.1	−0.69	0	0.69	2.1	7.2
−4	−8.8	−2.7	−0.92	0	0.93	2.8	9.6

Output Errors (%)

Log Conformity is specified in %, referred to the input, in the log mode, all other errors adjusted to zero. The relationship between log-conformity errors referred to the input and to the output is discussed in Chapter 4-1, and Table 4 in that chapter, to be found on page 434, provides ready conversion between input and output error. Since input and output are exchanged in antilog applications, the same table may be used here, with the headings exchanged. For example, if a log conformity error is 1%, referred to the input, corresponding to 4.32mV at the output, then in the antilog mode, a 4.32mV error referred to the input is a constant 1% error at any output level. For a given input log-conformity error, γ,

$$E_o = E_{REF} \cdot 10^{(V_{IN}/-K)+\gamma} = E_{REF} \cdot 10^{(V_{IN}/-K)} \cdot 10^{\gamma} \quad (11)$$

Since γ is specified independently of V_{IN}, 10^{γ} is a constant multiplier; if γ = 4.3mV, $10^{\gamma} = 1.01$.

APPLICATION EXAMPLE–LINEARIZING LOGARITHMIC OUTPUTS

In pollution monitoring, oxygen detectors that have output voltages that measure pO_2, the log concentration of oxygen, are frequently used. If it is desired to determine the actual concentration of oxygen, some form of exponential processing is necessary. This example will consider the design of an analog linearizing circuit employing logarithmic devices.

The objective is to design a circuit that will obtain a linear concentration reading from the logarithmic output of an oxygen detector, the response of which is characterized as follows:

O_2 Concentration	Output Voltage
10%	0mV
1%	−60mV
0.1%	−120mV
0.01%	−180mV

The first step is to reduce the measured data to the form of an equation, if possible. In this example, the output of the transducer varies at -60mV per decade change of concentration. It can be expressed by the equation

$$E_{OD} = 60 \times 10^{-3} \log_{10} \frac{100C_{O_2}}{10} = 0.06 \log_{10} 10C_{O_2} \qquad (12)$$

$$10^{-4} \leqq C_{O_2} \leqq 10^{-1}$$

The second step is to characterize a circuit that will have a response determined by the inverse of (12). The inverse of (12) is

$$10C_{O_2} = 10^{E_{OD}/0.06} \qquad (13)$$

It is evident that a function of the desired form can be performed by circuits employing either a basic log circuit (751), log

transconductor (752), or log amplifier (755). For example, the 755N's transfer relationship is

$$E_o = E_{REF}\ 10^{V_{IN}/-K}\ (E_{REF}\ \text{positive}) \tag{14}$$

The next step is to determine scale factors, and any external circuitry necessary to accommodate the range of the 755 to the range of the oxygen detector.

To scale the exponential device, it is necessary first to determine the range of E_o that will correspond to the range of O_2 concentration and the range of V_{IN} that will correspond to the range of E_{OD}.

Since C_{O_2} ranges from 10% down to 0.01%, a useful maximum value for E_o is 10V, which allows the output to be read directly in percentage concentration (1V/1%). Since at $V_{IN} = 0$, $10^\circ = 1$, and $E_o = 10V$, corresponding to $E_{OD} = 0$, at $10C_{O_2} = 100$

$$\frac{E_o}{E_{REF}} = 1 \tag{15}$$

$$E_{REF} = E_o = 10V \tag{16}$$

which happens to be 100 × the nominal E_{REF} for the 755N, equivalent to a -2V input bias (K = 1).

For a factor-of-10 change in concentration, $E_{OD}/0.06 = 1$, and similarly, for a factor of 10 change in E_o,

$$\frac{V_{IN}}{-K} = \frac{GE_{OD}}{-K} = 1, \text{ hence } \frac{G}{K} = \frac{-1}{0.06V} \tag{17}$$

where G is an external coefficient between the output of the oxygen detector and the input of the exponential circuit.

In determining the value of G, it is useful to note that the internal gain developed by the 755 is independent of the choice of K; the K connection simply determines the input attenuation, without affecting any other aspect of performance. Thus, one might make

the arbitrary choice of K = 1, to simplify the mathematics. If K = 1, G = -16.7, which could be developed by an inverting preamplifier.

Figure 6 shows a linearizing scheme based on the above discussion; Figure 7 shows a similar scheme employing the 752N log transconductor with an external operational amplifier. If the scheme of Figure 6 is used, the G trim allows the overall coefficient (G/K) of the exponent to be trimmed, taking into account errors in the value of K. E_{REF} is perhaps most easily achieved by biasing the input by -2V, and trimming for 10 volts out with 0 volts in. E_{os} is trimmed by the method mentioned earlier, with V_{IN} at +15V, or by applying a value of V_{IN} that maintains the output of A1 at $\geq$ +10V.

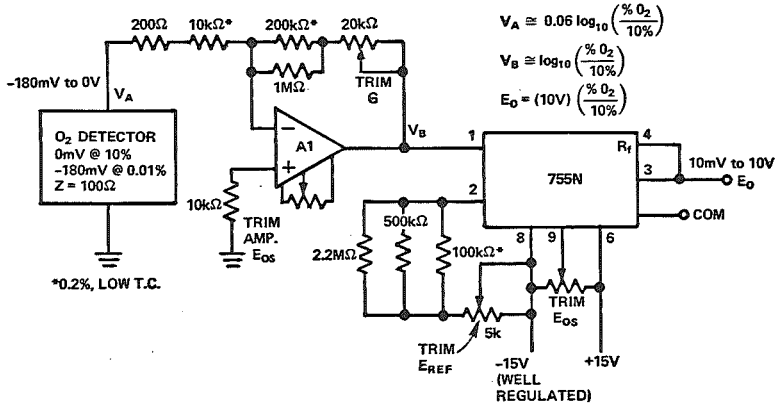


Figure 6. Linearizer for oxygen detector, using log amplifier.
Trim procedure:

A. Trim A1 output to zero with zero input
B. Trim E_O to zero with $V_B \geq 10V$
C. Trim E_O to +10V (trim E_{REF}) with zero input
D. Trim E_O to +10mV (trim G) with -180mV input

The transconductor approach (Figure 7) lends somewhat more flexibility to the computation, since I_{REF} is adjustable. For example, in this case, where V_{REF} = 10V, I_{REF} can be set at 100μA, and the feedback resistor at 100kΩ, without a need for biasing the input or using a greater value of feedback resistance.

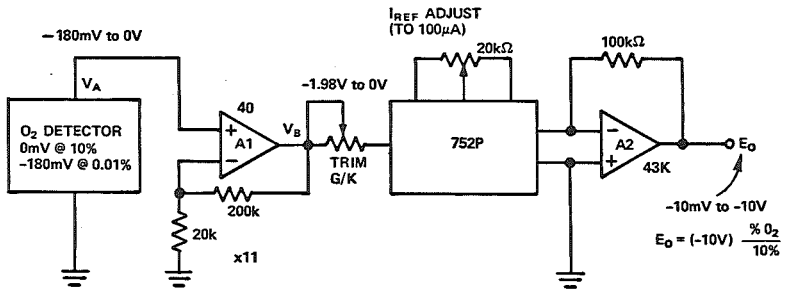


Figure 7. Linearizer for oxygen detector using high-impedance follower-connected op amp and log transconductor. Trim procedure:

A. Trim A1 output to zero with zero input
B. Trim E_O to zero (A2 output) with $V_B \geq 10V$
C. Trim E_O to −10V (I_{REF} adjust) with zero input
D. Trim E_O to −10mV (trim G/K) with −180mV input

As shown here (Figure 6), the input amplifier is connected in the inverting configuration, and consequently loads the input signal source. If high input impedance is necessary, the "P" version of the log transconductor or log amplifier could be used with a non-inverting input-amplifier, but the output polarity (Figure 7) would be negative instead of positive (usually a minor consideration because it can be easily dealt with).

The exponential circuit could also be built "from scratch", using the 751 basic log element, and the principles discussed in Chapters 3-1 and 4-1.

Selecting the Operational Amplifiers

Amplifier A1 is a general-purpose op amp selected for low offset temperature-coefficients. If it is a non-inverting amplifier (with "P" versions), it should also have good common-mode rejection at low levels.

The worst-case error occurs at $(V_{IN}/K) = 3$, which gives the greatest error (% of output); for example, if V_{IN}/K is associated with a 0.1% error, the output error would be 0.7% (from Table 1). If, on the other hand, the maximum output error allowable due to

errors in the input circuitry were 0.1%, the input errors would have to be kept at about 1/7 of 0.1%, or 0.014%.

As an aid to considering the effect of millivolt errors at the input on the output, Table 2 may be found useful (K = 1).

TABLE 2. MILLIVOLT RTI VS. % RTO ERROR. Equal Numbers of Millivolts of Error in the Exponent Correspond to Constant Percentage Error at the Output at any Level. (Figures are for K = 1)

RTI Error millivolts	RTO Error percent
0.1	0.02
0.5	0.1
1.0	0.2
2.0	0.5
3.0	0.7
4.0	0.9
5.0	1.2
10.0	2.3
30.0	4.2
100.0	25.9

From the table, it can be seen that noise or drift, resulting in a 167μV error at the output of A1 (10μV error at the input) would create a 0.04% output error.

In choosing A2 for this application, a low-noise, low-drift operational amplifier is required. The output impedance of the current presented to the summing point by the log transconductor varies with current level and may be approximated as

$$Z_O = 1k\Omega + \frac{40}{I_C},$$

where I_C is the current in mA.

At worst, its minimum value of 1kΩ should be considered as the summing-point load. With R_f = 100kΩ, the "noise gain" is about 100, and consequently the noise and drift of A2 will be magnified by 100. For this reason, the Model 43K was chosen, based on its guaranteed maximum noise of 2μV rms in a 1kHz bandwidth and its maximum specified drift of 5μV/°C.

Bias current is also an important concern in selecting A2, since for the smallest output (feedback) current level (0.15μA), a 1% error would result if the bias current were to exceed 1% of 0.15μA, i.e., 1.5nA. The FET-input Model 43K, with bias current of 20pA maximum at 25°C, easily meets this requirement over a wide range of temperature.

IV Multiplying And Squaring

Chapter 4

MULTIPLYING AND SQUARING

In Part 1, the properties and applications of multipliers were described briefly; in Part 2, applications of nonlinear devices were suggested, including a great many that involved multiplication. Chapter 3-2 discussed at length the design, nature, specifications, and foibles of multipliers, and means of measuring their properties. In this chapter, we consider some of the factors involved in choosing and applying a multiplier to perform multiplication and squaring applications.

SELECTION GUIDELINES

It has been determined that multiplication or squaring is required for a given application. Now it is necessary to choose a multiplier that will do the required job at the lowest cost, and to interface it to the rest of the circuit in an optimal manner. Since the choice of the multiplier and the manner of using it are interdependent, they should be considered together. There are a number of questions, the answers to which affect both choice and use. They are grouped here for discussion.

1. *What is the required transfer function? Does it involve simple multiplication, division, or multiplication combined with division? Is the scale factor fixed, adjustable, or variable? What are the polarities of the inputs? What is the polarity of the output? What is the polarity relationship? How many quadrants of operation are involved?*

The usual multiplier transfer function is $E_o = K(V_x \cdot V_y)$, where K represents the constant of proportionality, commonly called the scale factor. For most electronic analog multipliers, K = 1/(10V), in order to obtain 10-volt full-scale output response for 10V full-scale input signals. There are several designs, however (e.g., AD531 and Models 433 and 434), that allow the user considerable freedom in the selection of the scale factor: it may be fixed at some arbitrary value, switched among several arbitrary values, or even varied continuously by an external voltage or current (in effect, combining multiplication and division).*

A multiplication ideally results in a product that has the proper algebraic polarity (1 X 1 = 1, -1 X 1 = -1, -1 X -1 = 1, 1 X -1 = -1). However, not all multipliers accept both input signal polarities or provide both positive and negative output voltage. The number of quadrants of operation (on a plot of one input against the other) is defined in Chapter 3-2.†

In order to make the multiplication operation, as envisioned on a block diagram, correspond to the performance ranges of the hardware to be used, it is often necessary to provide gain scaling, either ahead of one or both inputs, or following the output. All such gains should be taken into account in the overall mathematical transfer equation to ensure that the measured output of the circuit is indeed related to the inputs in the expected manner (Figure 1).

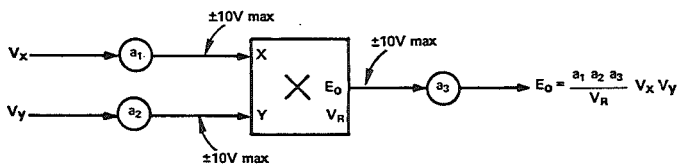


Figure 1. Effects of external scaling (amplification or attenuation) on the overall multiplier scale factor

*For division alone, best accuracy and dynamic range are achieved with specialized dividers, such as 434 or 436.

†It is strongly urged that the reader prepare himself for this chapter by ensuring that he is familiar with the general characteristics of multipliers and the definitions of the specifications in Chapter 3-2.

General-purpose 4-quadrant multipliers may be readily used for one- or two-quadrant operations (where one or both input variables is of restricted polarity), often with the advantage that tighter adjustment is possible in a restricted range. However, one-quadrant multipliers are not quite as easily used for multiple-quadrant operations. Chapter 3-2 (Figure 21) shows one way of accomplishing this, by offsetting the input signals. For squaring of 2-quadrant signals, a 1-quadrant multiplier may be preceded by an absolute-value circuit.

Finally, if either input signal, the output, and/or the gain relationship is of an undesired polarity, it can be easily corrected by the use of external unity-gain inverting op amps at the appropriate locations, or by appropriate connections to differential inputs, if available (as in the AD532).

2. What is the range of input magnitudes? What is the range of output magnitudes? What is the input resolution? What is the output resolution?

It is usually desirable to scale inputs and output to full-scale rated input. However, for some applications (e.g., gain control), linearity can be improved by restricting the range of one or both variables. Naturally, offset errors increase in importance, since a given offset represents a larger fraction of a reduced signal.

If one variable has a relatively small range of variation, the output resolution (dynamic range) is the same as that of the other input. However, if both variables have wide swings (e.g., in squaring), the required output resolution is the product of the input dynamic ranges. For example, if both inputs have 100:1 ranges (10V to 0.1V), the output resolution must be 1 in 10,000 (1mV out of 10V). Whether all of it is needed depends on what is to be done with the output signal.

In a frequency-doubler application, all that is needed is a reasonably undistorted sine wave; hence 1mV uncertainty at the low end is irrelevant; in many cases 50mV would be adequate. However if the output of a squarer is to be averaged, then square-rooted (as in a straightforward open-loop rms application),

the high sensitivity of the square-rooter at small signals requires that the squarer output actually have the full implied resolution. Fortunately, most commercially-available multipliers have excellent "resolution" near zero – but noise and drifts may mask small ac signal components.

3. Is the application "ac" or "dc?" What properties of the product are important (i.e., instant-by-instant value, or some measure, such as average, peak, peak-to-peak, phase, etc.)? Is the application dc-dc, ac-ac, or ac-dc?

For some "ac" applications, such as modulators, frequency-doublers, and gain-control circuits, output offset may be unimportant. For others, good linearity may be necessary only for one of the inputs (in a modulator, the modulation input; in a gain control, the signal input). In a modulator, dc feedthrough may be important on the modulation signal channel, ac feedthrough on a high-frequency signal channel.

Bandwidth requirements are a function of the job the multiplier performs: for mean-square measurements, average-power measurements, correlation, and phase measurements, where the average value of the output is of interest, output bandwidth can be quite narrow, but the inputs must have negligible phase difference.* For such functions as amplitude modulation, peak-demodulation, frequency-doubling, and AGC, the output amplitude-envelope must be maintained to the desired accuracy (1%, -3dB, etc.). The most-exacting applications are those in which phase must be preserved, that is, the output must follow the input "instantaneously," as predicted by the settling-time specifications or (for sine waves) the "vector" error.

4. What measures of accuracy are important? (overall error? nonlinearity? feedthrough? offsets? noise? gain error?) Over what dynamic range of inputs (output) must accuracy be maintained?

If no adjustments are permissible, overall error may be the key accuracy criterion. On the other hand, offsets, feedthrough, gain

*Also, it is desirable to avoid signal amplitudes (rise times) that cause (asymmetrical) limiting or slewing; this will also affect the average value at the output.

error, and – in some cases – nonlinearity may be reduced by external adjustments, allowing a nominally lower-performance device to be used at lower cost, if its drift specifications indicate that the error components will not change excessively over a reasonable range of temperature.

For some applications, the error must be a given fraction of the actual output voltage (say 0.5%) over a range of output values; in other cases, it is sufficient to specify the error as a fraction of full-scale output (say 0.5% of 10V, or 50mV). Nonlinearity and linear feedthrough errors are referred to the inputs; other errors are usually referred to the output (see Chapter 3-2). As noted earlier, external adjustments can be used to further reduce errors over limited ranges of voltage magnitude, and in a restricted number of quadrants.

5. What scope can be allowed for adjustability? Must the device be installed without initial tweaking? Without calibration? Must the installation be factory-adjustable? Field adjustable? To what degree can adjustability be traded for basic device cost?.

Without question, performance of the lowest-cost general-purpose devices can be greatly improved by adjustment. However, adjustment has costs of its own, in terms of additional parts, "real estate," procedures, fixtures, and instructions. Higher-cost pre-trimmed devices include these extra costs in their performance guarantees.

Pre-trimmed modular devices are generally close to optimum. Pre-trimmed IC.s, such as the AD532, can often benefit by further trimming, since the automatic laser-trimming process must take into account variations due to warmup, handling, packaging, and aging; this results in a wider specified range of individual variation, but still considerably lower error than untrimmed IC's, and lower cost than most pre-trimmed modular devices. Besides the usual offset, linear-feedthrough, and gain trims, IC multipliers generally can obtain greatly improved performance with cross-feed linearity trimming to reduce the quadratic nonlinearity component (Chapter 3-2, Figures 14, 15, 16, 17, 18).

Multiplier adjustments can often be replaced by overall calibration adjustments to the equipment incorporating the multiplier, since the adjusted variables are input and output bias voltages and overall gain. Gains and additive voltages elsewhere in the system can be manipulated (in the right order, by an appropriate procedure) to compensate for multiplier offset, linear-feedthrough, and gain errors.

Some applications, by their nature, call for fewer adjustments. For example, in squaring, one of the feedthrough adjustments can be eliminated, and quadratic nonlinearity can be eliminated by appropriate gain adjustment. Another example: an amplitude modulator with ac coupling can eliminate *all* local adjustments (dc feedthrough at the modulating input is incorporated in the modulating-signal bias; gain can be controlled in the modulating signal, the carrier, or beyond the output; and dc feedthrough at the carrier input and dc output offset are irrelevant with ac coupling).

For applications where *ac* feedthrough must be reduced (at all costs) at high frequencies, the input signals can in some cases be fed capacitively, with appropriate polarity, into a summing amplifier and summed with the multiplier output out-of-phase, to cancel internal capacitive feedthrough.

6. What are the needs of dynamic response: input frequency range, output frequency range, allowable attenuation and phase shift, slewing rate, settling time, distortion? (See 3.)

7. What are the environmental constraints (temperature variation, humidity, shock, vibration, warmup, power supply, physical size, external circuitry)?

8. What other requirements on the inputs and outputs are not expressed in the transfer function? Differential vs. single-ended? Loading of the signal sources by the multiplier inputs? Output current requirements: boosting, isolation, capacitive load?

9. Finally (and perhaps the most perplexing question) what weight should be assigned to the various costs (what is their relative tolerability?):

A. The cost of the device itself?

B. The cost of adjustments and their procedures, to the degree they are needed?

C. The cost of any other external circuitry peculiar to a given device? Size?

D. Reduced performance or system reliability as a consequence of compromises to A or B?

The investigation of alternatives should start with a translation of the requirements outlined above into a preferred circuit configuration and a set of tentative specifications. The specifications, including size and cost, should be listed in order of priority, taking into account the tradeoffs between cost of an untrimmed device with external trim circuitry and that of a pre-trimmed device.

If, for example, size is of the essence, it will be near the top of the list and will probably result in a restriction of the field to integrated circuits, with no external adjustments. If linearity is the most important criterion, the field will be narrowed to those devices having the desired linearity, or something approaching it.

By listing the specifications in order of priority, one can generally narrow the field of choice very quickly, so that the relative merits of just a few devices may be compared in depth. If the process eliminates *all* available devices, it quickly establishes the need for compromise (or for consultation with a manufacturer).

Most manufacturers (including Analog Devices) group their multipliers into several classes, that make the narrowing easy to accomplish in a general way. For example, integrated-circuit devices are listed in a separate table. Because IC's have minimum size and (often) minimum cost, the rule of the thumb is often used: "choose the cheapest IC that will do the job satisfactorily;" the separate listing allows one to study the whole panoply of IC's at a glance.

If, on the other hand, the priority is given to other considerations, one can find devices under such headings as: High Accuracy, Accurate Low-Drift, Accurate Wideband, Wideband, General-

Purpose, Economy, etc. Table 1 is a thumbnail sketch of the key features and typical applications of each of the Analog Devices multiplier families. Each family has two or more members, graded in terms of one or more key specifications, e.g., nonlinearity, feedthrough, drift (429 vs. 429B; 427J vs. 427K; AD532J, AD532K, AD532L, AD532S, etc.)

TABLE 1. APPLICATION GUIDE BY KEY FEATURE

Key Feature	Multiplier Application	Multiplier Family
Highest precision, lowest noise & drift	Analog computation, dividers, servo multipliers, correlators	424, 427, 436
Low drift, good accuracy, lower cost	Wide temperature range, general purpose multiply/divide	428
Bandwidth, accuracy	Graphic displays, dividers	429, 422
Wide dynamic range, accuracy	Root and power generation, $Y\ Z/X$, $Y(Z/X)^m$	427, 433, 434
External trim for high accuracy	R & D, medical, laboratory, analog computation	424, 425
Economy, size	OEM designs, general purpose multiply/divide	530, 532, 533, 426, 432, 531
MIL spec. available	Military grade design	530, 531, 532, 533, 432, 428

Obviously, if one starts without any prior knowledge of the available devices, the job of choosing a suitable device may involve considerable searching. To make the job somewhat easier, a table (Table 2) has been prepared that selects several salient criteria and divides the specification ranges into convenient increments ("levels"). Then, each and every standard device is listed, in terms of descending desirability for each of the parameters.

For example, considering feedthrough, the best possible choice would be the 424K, with 1mV at the X input, 2mV at the Y input. The worst possible choice would be the AD532J (without external trim) with a possible maximum of 200mV at both inputs. Considering bandwidth, the 429 family would be the best choice, with 10MHz typical -3dB bandwidth, while the 424 or 427 might be the worst choice, with 100kHz bandwidth.

Thus, it is possible to apply the list of priority specifications to Table 2, and, from it to determine whether any of the devices

listed there fits the required profile; if none do, the necessary compromises are instantly evident.

Naturally, the utility of the table is limited to "First Resort," for several reasons

1. It represents a tabulation of general-purpose 4-quadrant devices (not including the excellent 433 and 434 YZ/X 1-quadrant-device families).

2. It represents the state of the Analog Devices product line in late 1973. At the time you read this, newer products, lower prices, better specs may be available on the market, from Analog Devices and/or other manufacturers.

3. All specifications are not listed. Not even all salient specifications (for your application). However, the number of data sheets (or catalog tabulations) that must be consulted can be greatly decreased, since the number of devices to be considered is narrowed.

4. "All prices and specifications are subject to change."

5. Some of the figures given are "typical," rather than min/max. The decision to make a specification "typical" is usually an economic decision: certainty of achieving a given performance level is traded for a lower price. In effect, any "typical" specification should be moved down one or more levels, or its price rating should be moved down one level (representing the higher price that might have to be paid to have the spec guaranteed, if feasible).

6. Prices shown are for 1 unit. Since discounts in quantity may be substantial, devices should not be ignored if they are one level too low in their price rating.

NOTES FOR THE USER

1. Improved linearity at low levels. By taking advantage of the nonlinearity specifications, the user can often use a less-costly multiplier to obtain adequate small-signal accuracy. This is done

TABLE 2. 4-QUADRANT MULTIPLIER SELECTION GUIDE

	ERROR (Int. Trim) max. %	ERROR (Ext. Trim) max. %	NONLINEARITY (x, y) max. %	FEEDTHROUGH (Ext. Trim) (x, y) max mV p-p	DRIFT (Total Error) max. %/°C
LEVEL ONE	≤0.3%	≤0.1%	≤0.1%	≤5mV	≤0.01%
	427K .2 427J .25	424K .1 427K .1	424K .04 427K .04 428K .08 424J .08 427J .08	424K 1-2 424J 2-4 427J 4-5 427K 4-5	AD533L* AD530L* AD533S* AD531L*
LEVEL TWO	≤0.5%	≤0.3%	≤0.3%	≤20mV	≤0.02%
	426L 428J 428K 429B	427J* .15 424J .2 428J* .25 428K* .25 429B* .3	429B .2 426L .25 428J .25 AD530L*, AD531L* .3-.2	428J, 428K 10-10 429B 10-20 426L 20-20	AD532S* AD530S AD531S 428J/K 424J/K 427J/K
LEVEL THREE	≤1%	≤0.5%	≤0.5%	≤50mV	≤0.03%
	AD532K/S* 426A/K 432K 429A 422A/K	426L* .35 AD533L AD530L* AD531L*	AD530K/S*, AD532K/S* .5-.2 AD533K/L/S* AD531K/S*, 429A .5-.3	422A/K 8-35 AD530L 40-30 AD531L 40-30 429A 16-50 AD533L 50-50	AD533K* AD530K* AD532K* AD531K*
LEVEL FOUR	≤2%	≤0.7%	≤0.7%	≤100mV	≤0.04%
	AD532J* 432J	432K* .6 426A/K* .6 429A* .7 422A/K* .7	432K 426A/K 422A/K (.6-.3)	426A/K 20-60 AD530K/S, AD531K/S 80-60 432K† 50-100 AD533K/S AD532K/S†	AD533J* 432K* 426K/L 429B 422K
LEVEL FIVE		≤1%	≤1%	≤150mV	≤0.05%
		AD533K/S 432J* AD530K/S* AD532K/S* AD531K/S*	AD533J*, AD530J*, AD532J*, AD531J* .8-.3 432J* .8-.4	432J† 80-120 AD530J, AD531J 150-100	426A* 429A* 422A*
LEVEL SIX		≤2%		≤200mV	≤0.06%
		AD533J AD530J* AD532J* AD531J*		AD533J 150-200 AD532J† 200-200	AD530J* AD532J* 432J* AD531J*

*Typical
†Int. Trim

OFFSET DRIFT max. mV/°C	TEMP. RANGE Rated Drift Performance	BANDWIDTH small-signal -3dB min. (by family)	COST (1's) $U.S.	SIZE Pkg. or vol. (by family)
≤0.2	-55°C to +125°C	≥10MHz	<$20	IC (TO-100 or TO-116) (or chips)
AD530J/K/L/S* AD531J/K/L/S* 428K 424J*/K 427J*/K	AD533S AD532S AD530S AD531S	429*	AD533J AD533K	AD533 AD530 AD532
≤0.5	-25°C to +85°C	≥5MHz	<$30	IC (TO-116) (or chips)
428J*	426A 429A/B 422A	422	AD530J AD532J AD531J 432J	AD531
≤0.7	0 to +70°C	≥1MHz	<$50	8cm³
AD533J/K/L/S* AD532J/K	AD533J/K/L AD530J/K/L AD532J/K/L AD531J/K/L 432J/K 426K/L 428J/K 422K 424J/K 427J/K	AD533* AD530* AD532* AD531* 432*	AD530K/L AD532K/L AD533L/S AD531K 426A 432K	432
≤1		≥300kHz	<$100	22cm³
432K* 426K/L 429B 422K		426* (400) 428* (300)	AD530S AD531L/S 426K/L 428J	426 428 429 422
≤2		≥100kHz	>$100	47cm³
432J* 426A* AD532S 429A* 422A*		424 427	428K 429A/B 422A/K 424J/K 427J/K	424 427

See Descriptive Notes on next page.

BRIEF DESCRIPTIONS OF 4-QUADRANT DEVICE FAMILIES – NOTES TO TABLE 2

Prefix AD: Integrated Circuits

AD533: lowest cost, general-purpose variable-transconductance, 4-quadrant. Thin-film-on-silicon monolithic construction.

AD530: low-cost, general-purpose variable-transconductance, 4-quadrant. Better specs than AD533. Thin-film-on-silicon monolithic construction.

AD532: internally-trimmed low-cost, general-purpose, variable transconductance, 4-quadrant. Thin-film (laser-trimmed) on-silicon monolithic construction. Both inputs differential.

AD531: similar to AD530, but scale factor is adjustable by an input current (XY/I). Can be used as a three-variable multiplier-divider, to perform vector, square-root, rms, absolute-value operations. Available in TO-116 dual in-line package only. X-input differential.

No Prefix: Modular Packages

427: highest accuracy, lowest noise and drift, pulse-height, pulse-width modulated, internally trimmed.

424: highest accuracy, lowest noise and drift, pulse-height, pulse-width modulated, externally trimmable. Requires external amplifier for division.

428: low-drift, good accuracy, reasonable cost, variable-transconductance type.

429: combines 10MHz bandwidth and good low-frequency performance, variable-transconductance.

422: wideband variable-transconductance type.

426: low-cost general-purpose variable-transconductance type.

432: lowest-cost internally-trimmed general-purpose variable-transconductance in small modular package.

Not Listed in Table 2

434: high-accuracy multiplier-divider (YZ/X), especially useful for dividing and square-rooting. Wide dynamic range, log-antilog type, 1 quadrant.

433: multifunction module $Y(Z/X)^m$, performs 434 operations and also obtains powers and roots from 1 to 5. Wide dynamic range, log-antilog type, 1 quadrant.

425: The 424, mounted on a card, with adjustments.

436: high-accuracy variable-transconductance divider-only – 2-quadrant numerator, positive denominator.

by using the nearly-always-conservative approximation that the nonlinearity error $f(X,Y)$

$$f(X,Y) \cong |V_x| \epsilon_x + |V_y| \epsilon_y$$

where ϵ_x and ϵ_y are the fractional nonlinearities, i.e., % nonlinearity/100, specified for the X and Y inputs respectively.

Example: For Model AD530K, $\epsilon_x = 0.5\%$ and $\epsilon_y = 0.2\%$. What is the maximum error for $V_x = 5V$ and $V_y = 1V$? What happens if the inputs are reversed?

A. Nominal output is $V_x V_y/10 = 5 \times 1/10 = 500mV$.

B. Expected linearity error is $5(0.005) + 1(0.002) = 27mV$, or 5.4% of the output (0.27% of full-scale).

C. Interchanging the inputs, 1(0.005) + 5(0.002) = 15mV, or 3% of the output (0.15% of full-scale).

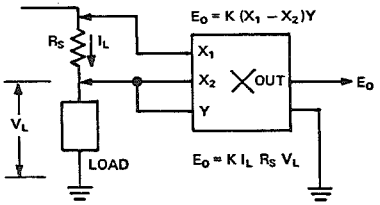
It is evident that for this application, the inputs should indeed be interchanged, if the voltages in the problem statement are the respective maxima. In any event, the errors computed here should be contrasted with the overall 1%-of-full-scale predicted specification: 100mV, or *20%* of the 500mV output, surely belt-and-suspenders conservatism!

This discussion relates only to the nonlinearity specification. All dc errors should have been zeroed, and the range of temperature variation should be small to avoid introducing excessive errors when computing at such low levels.

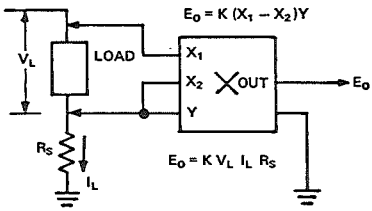
2. Common-Mode Rejection: Some multipliers have one or more differential inputs, which can prove useful in instrumentation (e.g., power measurement, Figure 2) or applications involving passive sums and differences, such as vector subtraction, without additional op amps. Examples of such devices include the AD531 and AD532.

Common-mode error generally manifests itself as an apparent differential input signal δ_{CM}, which is a function of common-mode signal level $V_{CM} = (V_1 + V_2)/2$. It is measured by setting up the multiplier for unity gain (e.g., for an $(X_1 - X_2)Y/10$ multiplier, set Y = 10V) and connecting a low-frequency sine-wave generator (20Vp-p @50Hz) in common to both differential inputs (Figure 3). The resulting peak-to-peak output error measurement is the common-mode error. The fractional common-mode error is the ratio of this measured voltage to the common-mode input swing. Common-mode rejection ratio (CMRR) is the reciprocal of the fractional common-mode error, and log common-mode rejection (CMR) = 20 log(CMRR), in "dB."

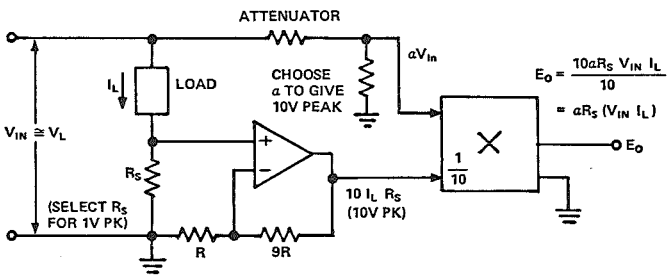
As a practical matter, it should be noted that the absolute magnitude of the signal level at each of the differential inputs is a composite of the differential signal and the common-mode signal (if they are applied separately). The user should be careful that the combined voltage swing does not result in saturated inputs.



a) High shunt (differential-input multiplier)



b) High load (differential-input multiplier)



c) High voltage (e.g., ac line)

Figure 2. Multiplier applied to power measurement

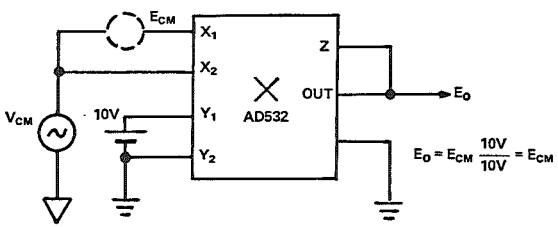


Figure 3. Common-mode-error measurement

3. Balanced Modulator Application (Figure 4)

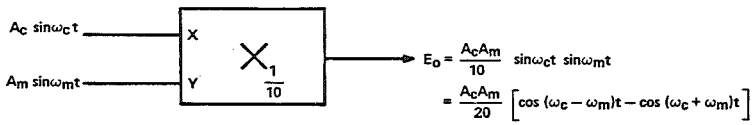


Figure 4. Balanced modulator circuit

The balanced modulator is discussed in Chapter 2-4 (Figure 4a). If the multiplier errors are included, the equation

$$10E_o = A_c \sin\omega_c t \cdot A_m \sin\omega_m t$$

becomes

$$10E_o = (A_c \sin\omega_c t + X_{os})(A_m \sin\omega_m t + Y_{os}) + Z_{os} + f(x,y)$$

$$= \underbrace{A_c \sin\omega_c t \cdot A_m \sin\omega_m t}_{\text{desired performance}} + \underbrace{Y_{os} A_c \sin\omega_c t}_{\text{carrier feedthrough}}$$

$$+ \underbrace{X_{os} \sin\omega_m t + X_{os} Y_{os} + Z_{os}}_{\text{low freq. and dc terms}} + \underbrace{f(x,y)}_{\text{harmonics and cross-products}}$$

The low-frequency and dc terms are usually inconsequential, because they can be filtered out by a high-pass filter. The carrier feedthrough (linear) term can be adjusted to zero by tweaking Y_{os}; but it will creep back in with changes in temperature. Thus the error will consist of a nonlinear term plus a temperature-sensitive carrier feedthrough.

If an AD530K is considered for this application, its nonlinearity error is 0.5% (50mV) for x and 0.2% (20mV) for y, and its Y_{os} temperature sensitivity is 2mVp-p/°C. For a 20Vp-p signal swing,

the nonlinearity error is 0.5% (-46db at room temperature), and the additional carrier feedthrough for a 45°C temperature change is 90mVp-p. If they add linearly (more likely, they will add root-sum-of-squares fashion), the error will be 190mV/20V = 0.95%, or in terms of "dB" (20 log 0.0095), about 40dB of carrier, harmonic, and cross-product suppression.

To make the modulator insensitive to variations in carrier amplitude, some means must be provided either to hard-limit the carrier input or provide some means for controlling its amplitude with an AGC circuit. The AGC approach can be achieved concurrently with the modulation process, if an XY/Z multiplier is used (such as the AD531), as shown in Figure 5. This circuit multiplies the modulating signal (Y input) by the carrier (X input); the gain $(1/V_r)$ is determined by a measure of the carrier amplitude, hence the output amplitude is a function of the modulating-signal amplitude only.

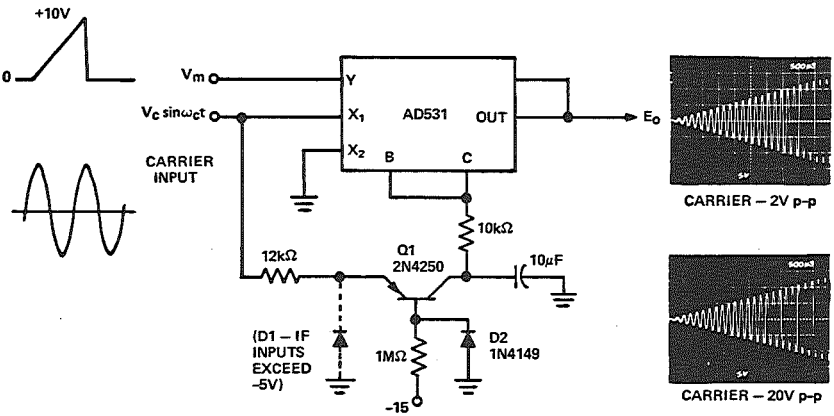


Figure 5. Balanced modulator with carrier level-compensation

The emitter circuit of the transistor acts as a rectifier, to measure the carrier amplitude. Filtering occurs in the collector circuit, and the resulting current, approximately proportional to the carrier input, provides a denominator input current that adjusts the multiplier gain to maintain the output amplitude independent of variations in the carrier amplitude, over a range of 1–10V, and at

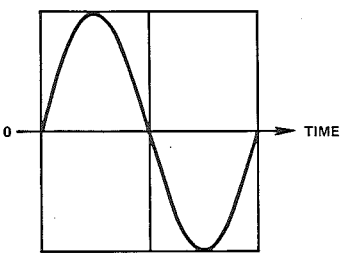
frequencies down to 20 Hz. The diode D2 maintains a current in the collector circuit to keep the denominator from going to zero for very low values of carrier amplitude (including zero).

4. Squarer Application Notes

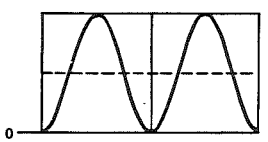
When a sine-wave is applied to a multiplier, connected as a squarer, one would expect the time plot of the output to be a double-frequency sine-wave of amplitude $\frac{1}{2}A^2/10$, with a bias of $\frac{1}{2}A^2/10$, from the trigonometric identity.

$$\sin^2 \theta = \tfrac{1}{2}(1 - \cos 2\theta)$$

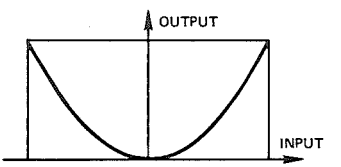
On an oscilloscope, the time plot and X-Y plot should appear as in Figures 6b and c, at low frequencies.



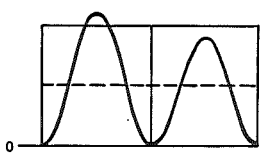
a) Input



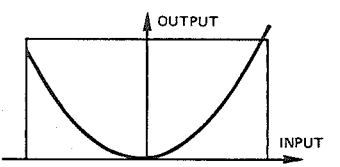
b) Ideal output vs. time



c) Ideal output vs. input



d) Output vs. time – linear feedthrough



e) Output vs. input – linear feedthrough

Figure 6. Waveforms of ideal squarer and squarer with feedthrough error

An asymmetry, such as that observed in Figures 6d and e, is due to an input offset, caused either by multiplier feedthrough or a dc component on the sine wave (or both). It adds a linear term to the squared output (plus a negligible offset):

$$(X\sin\omega t + X_{os})\,(X\sin\omega t + Y_{os})$$

$$= X^2\sin^2\omega t + (X_{os} + Y_{os})X\sin\omega t + X_{os}Y_{os}$$

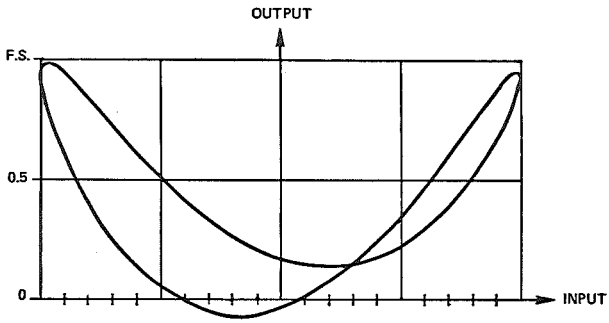
The offsets of the input (if small) and of the multiplier can be compensated for at room temperature by adjusting either X_{os} or Y_{os} to equalize the alternating peaks.

At high frequencies, the phase shift will be worse for the squarer than for the sine-wave-times-a-constant, because of frequency doubling. Also, as frequency increases, an asymmetry will appear, due to the increase of feedthrough at higher frequencies (Figure 7).

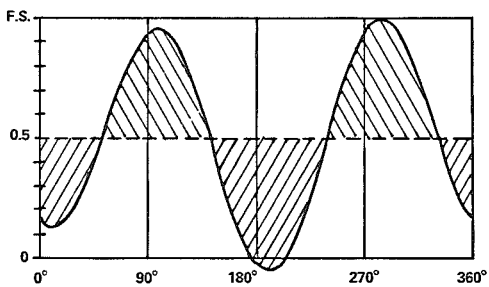
Such response need not be alarming for many applications. It is interesting to note that the average response, as measured by a dc meter, is essentially independent of frequency up to quite high frequencies. What this means to the user is:

A. If you're interested in the average value of the output, as in rms measurements, power measurements, or phase-angle measurements (between the inputs), then the phase shift (and even attenuation) of the double-frequency is of no concern, and ac feedthrough of the fundamental is similarly of little moment. The output is going to be filtered, or integrated; the high-frequency attenuation of the output stage can be viewed as a modicum of pre-filtering. (In fact, if the output-stage summing point is available, a feedback capacitor can be used to provide internal first-order-lag filtering.) What is important is the constancy of the average value, which is quite good over the entire range of frequency for which the unit is rated.

B. If one is interested in the *amplitude* of the ac component of the output, as in frequency doubling or amplitude modulation, then the phase shift is again unimportant, until it is accompanied by attenuation, starting at about 1/10 the rated frequency range.



a) Typical plot of output vs. input for squarer at high frequency, showing phase shift and high-frequency feedthrough



b) Time plot of the above, showing equal areas about 0.5, despite phase distortion

Figure 7. High-frequency response of squarer to sinusoidal input

C. The phase-shift is important if one is interested in the *instantaneous* value of the output, a small but important class of multiplier applications. An example is use of the squarer in linearity correction of high-frequency oscilloscope displays.

In frequency-doubling applications, the output amplitude is proportional to the square of the input amplitude. For most cases, the amplitude of a frequency-doubler output is not of importance. For applications where the amplitude *must* respond linearly (for example, to an input with slowly-varying amplitude modulation),

the circuit of Figure 8 may be found useful. The "dc" component of the output of a squarer-connected multiplier (AD531) is filtered and fed back as a denominator signal to control the gain. Thus,

$$E_o = \frac{(1 - \sin 2\omega t)\, E_1^{\,2}/2}{\overline{E_o}}$$

$$= \frac{E_1^{\,2}}{2\overline{E_o}} - \frac{E_1^{\,2}}{2\overline{E_o}} \sin 2\omega t$$

Since

$$\overline{E_o} = \frac{E_1^{\,2}}{2\overline{E_o}},$$

$$\overline{E_o} = \sqrt{E_1^{\,2}/2} = E_1/\sqrt{2}$$

and

$$E_o = \frac{E_1}{\sqrt{2}} - \frac{E_1}{\sqrt{2}} \sin 2\omega t$$

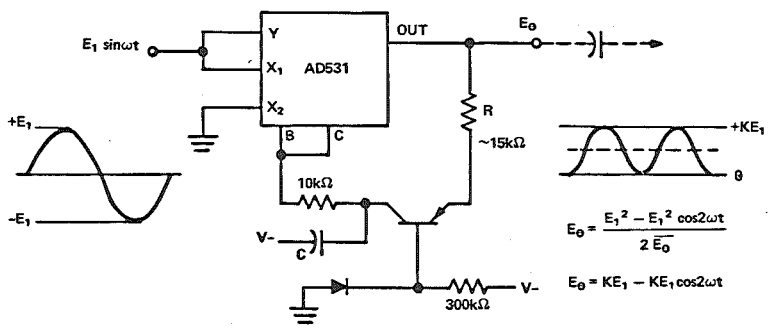


Figure 8. Frequency doubler with linear amplitude response

Therefore, the amplitude of the double-frequency signal is proportional to the input amplitude. The dc component of the output may, of course, be removed by capacitive coupling.