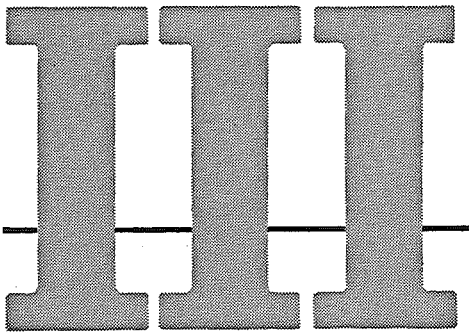


Logarithmic Circuits

Chapter 1

Today's logarithmic circuits almost invariably use the inherent logarithmic properties of silicon junction devices. Readily available in monolithically-matched pairs, they are easily compensated for temperature variation, low in cost, and characterized by wide dynamic range, typically 10^{-2}A to 10^{-11}A.

In this chapter, we discuss their basic properties, techniques for obtaining both thermal and dynamic stability, some commonly-used circuits, specifications and definitions, and means of adjustment and test.

BASIC CONSIDERATIONS

An "ideal logarithmic diode" would be characterized by the current-voltage relationship

$$I = I_o\ (\epsilon^{qV/kT} - 1) \tag{1}$$

Connected in the feedback path of an operational amplifier (Figure 1), it would constrain the output voltage to be

$$E_o = \frac{kT}{q} \ln(I/I_o) = \frac{kT}{q} \ln(10) \cdot \log(I/I_o) \tag{2}$$

as long as $I/I_o >> 1$.

q is a constant equal to the unit charge 1.60219×10^{-19}C
k is Boltzmann's constant, 1.38062×10^{-23}J/°K
T is absolute temperature, °K = °C + 273.15
I_o is the extrapolated current for E_o (= V) = 0

Typical round-number values in the vicinity of room temperature are:

°C	T(°K)	$\frac{kT}{q}$	$\frac{kT}{q}\ln(10)$
24.21	297.36	25.62mV	→59. mV
→25.	298.15	25.69mV	59.16mV
26.85	→300.	25.85mV	59.52mV
28.58	301.73	→26. mV	59.87mV
29.25	302.4	26.06mV	→60. mV

Thus, at 25°C, a 10:1 change of I would produce a 59.16mV change of E_o; an ϵ:1 change (2.7183) of I would result in a 25.69mV change of E_o.

Such a diode would be very useful. Since it is a 2-terminal device, it can be used for currents of either polarity; a number of them could be "stacked up" in series to obtain greater voltage; it can operate away from ground. Unfortunately, most diodes that are available as two-terminal devices have a limited range of logarithmic behavior. At the high end, ohmic bulk resistance produces an additional voltage drop:

$$V = \frac{kT}{q} \ln(I/I_o) + IR_B \tag{3}$$

At the low end, the slope undergoes one or more changes of a multiple m* ($1 \leqslant m \leqslant 4$) to

$$V = m\frac{kT}{q} \ln (I/I_o) \tag{4}$$

Since both the magnitude of m and the value of voltage at which the slope changes are functions of the individual device (within a family), general-purpose diodes are impractical for accurate

*This factor has been attributed to diffusion current flow in extended regions such as surface inversion layers or channels and to generation-recombination mechanisms in space-charge regions.

logarithmic operations over more than 1 or 2 decades, even though it is possible to devise a circuit to balance out the ohmic resistance. And special-purpose diodes are hardly price-competitive with diode-connected monolithic dual transistors.

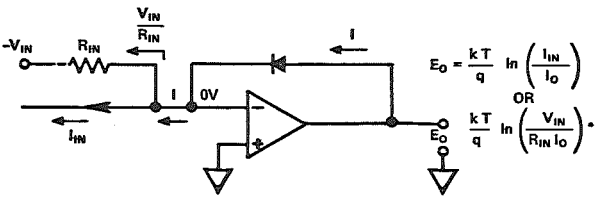


Figure 1. Ideal-log-diode circuit

THE TRANSDIODE CONFIGURATION

Figure 2a shows a transistor connected in the feedback path of an operational amplifier. The collector current is determined by the input current or voltage. The operational amplifier ideally maintains the collector current equal to the input current and holds the collector voltage at zero. Since the base is grounded, the collector and base are at the same potential, though the base current flows independently. The amplifier output voltage, which is also the emitter-to-base voltage, must be whatever value is necessary to meet the collector constraints, while furnishing any necessary amount of emitter current.

Let us now investigate the relationships governing this circuit. The modified Ebers and Moll equations[1] for emitter and collector currents of a grounded-base bipolar transistor are

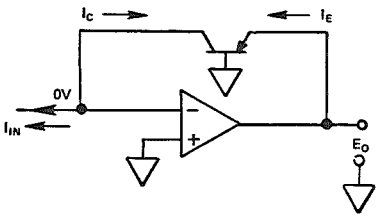
$$I_E = I_{ES}(\epsilon^{qV_E/kT} - 1) - \alpha_I I_{CS}(\epsilon^{qV_C/kT} - 1) + \Sigma I_{ES_i}(\epsilon^{qV_E/m_i kT} - 1) \quad (5)$$

$$I_C = -\alpha_N I_{ES}(\epsilon^{qV_E/kT} - 1) + I_{CS}(\epsilon^{qV_C/kT} - 1) + \Sigma I_{CS_j}(\epsilon^{qV_C/m_j kT} - 1) \quad (6)$$

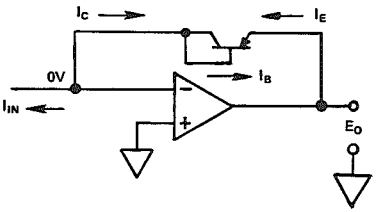
[1] "Multiplication and Logarithmic Conversion by Operational-Amplifier-Transistor Circuits," by W. L. Paterson, *The Review of Scientific Instruments*, 34-12, December 1963.

where

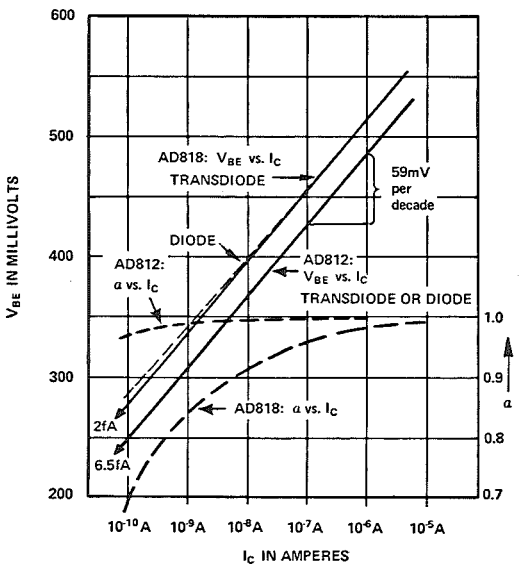
V_E and V_C are the emitter-base and collector-base voltages
I_{ES} and I_{CS} are the emitter and collector saturation currents
α_N and α_I are the current-transfer ratios in the normal and reverse directions
$m_i > 1$, $m_j > 1$ are "uncollected" current components that flow through the base circuit.



a. Transdiode (PNP)



b. Diode-connected transistor. As a two-terminal device, only one kind (NPN or PNP) will serve for either polarity of input current.



c. Transdiode and diode V_{BE} and α vs. I_C for two dual transistor types

Figure 2. Transdiodes and diode-connected transistors

For the circuit of Figure 2a, since V_C is held at zero, the relationship between collector current and emitter voltage (6) becomes

$$I_C = -\alpha_N I_{ES}(\epsilon^{qV_E/kT} - 1) \tag{6a}$$

Since the operational amplifier holds the collector current equal and opposite to the input current, the output voltage, V_E must be

$$V_E = \frac{kT}{q} \ln(I_{IN}/I_{ES}) - \frac{kT}{q} \ln \alpha_N \tag{6b}$$

for $I_{IN}/I_{ES} >> 1$. Typically, I_{ES} is of the order of 10^{-13} A or less for most of the silicon planar transistor types used for log operations; therefore the relationship of (6b) should be valid over a very wide range of current. α_N is very nearly unity and essentially constant over the range of current for which (6b) is valid; therefore the $(\ln \alpha_N)$ term is negligible (if $\alpha_N = 0.99$, its contribution is about ¼mV of constant offset). α_N in this equation should not be confused with the commonly-used grounded-base current gain $\alpha = I_C/I_E$: Since the emitter current includes both the collector current and the $m_i > 1$ terms, $\alpha = I_C/I_E$, always less than α_N, is a function of emitter voltage that decreases substantially at low values of current. Figure 2c shows plots of V_{BE} and α for two dual-transistor types widely used in logarithmic circuitry. Note that fidelity to logarithmic response is excellent, even at currents for which α is much less than 1.

If the collector and base of a transistor are connected together, a two-terminal diode is created (Figure 2b). Since the current that flows through it is the emitter current, its behavior, according to this model, is governed by (5). The first term is very nearly equal to the collector current, the second term is zero, and the sum of

*For PNP transistors, the input current I_{IN} is positive in the direction shown. If the input current is positive in the opposite direction, an NPN transistor is used. The polarities of the currents and voltages in equations (5) and (6) are reversed.

the $m_i > 1$ terms is therefore equal to the base current. Because

$$I_{IN} = -I_C - I_B = -I_C \left[1 + \frac{1}{h_{FE}}\right]$$

$$= \alpha_N I_{ES}(e^{qV_E/kT} - 1)\left[1 + \frac{1}{h_{FE}}\right] \tag{7}$$

it is reasonable to consider that $1/h_{FE}$ is a measure of the $m_i > 1$ terms. From (7),

$$V_E = \frac{kT}{q} \ln(I_{IN}/I_{ES}) - \frac{kT}{q} \ln\left[\alpha_N\left(1 + \frac{1}{h_{FE}}\right)\right] \tag{7a}$$

$1/h_{FE}$ is equal to $(1-\alpha)/\alpha$, therefore the error term is equal to $+kT/q \ln(\alpha/\alpha_N)$. Typical values of error, according to this model, are

h_{FE} ($\alpha_N \cong 1$)	α/α_N	$-\frac{kT}{q} \ln(\alpha/\alpha_N)$ mV @ 25°C
∞	1	0
1000	0.999	0.03
200	0.995	0.13
100	0.99	0.26
50	0.98	0.51
19	0.95	1.32
11.5	0.92	2.14
9	0.9	2.7
4	0.8	5.7
3	0.75	7.4
1	0.5	17.8

It is clear that a transistor to be used as a log diode should have high h_{FE} and maintain it over a wide range of emitter current. Figure 2c shows a comparison of AD812 (a high-h_{FE} dual monolithic transistor) and AD818 (a large-geometry dual-

monolithic transistor having low bulk resistance), connected as transdiodes and as 2-terminal diodes. Though the AD818 would appear to have poor performance as a log diode at low current, its low series-resistance makes it suitable for log operation at currents exceeding 1mA, more than an order-of-magnitude better than the AD812 at high current.

OTHER SOURCES OF ERROR

If $V_{CB} \neq 0$, the other terms of equation (6) will contribute error currents that may significantly affect V_E, especially for low values of input current. From (6), in the forward conducting region,

$$V_E = \frac{kT}{q} \ln \left[\frac{I_{IN}}{\alpha_N I_{ES}} + \frac{I_{CS}}{\alpha_N I_{ES}} (e^{qV_C/kT} - 1) + \Sigma \text{ (etc.)} \right] \quad (8)$$

For grounded-base applications, the amplifier offset voltage V_{os} will bias the collector voltage, as will any common-mode input voltage. For applications with the base driven, the designer should ensure that the expected swing of V_{CB} and the desired low-current range are compatible for the device employed in the application. The magnitude of the effective collector-current errors may be determined experimentally by connecting emitter and base together, and applying a voltage V_C.* The collector current will consist only of the $V_C \neq 0$ terms, since $V_E = 0$. This measurement with the collector-base diode forward-biased is worst-case, since error current is extremely low with reverse bias. Care should be taken to avoid applying excessive currents or voltages.

Amplifier bias current, I_b, will cause linearity errors, referred to the input, and log-conformance errors at the output (Figure 3).

*V_{CB} positive for PNP transistors, negative for NPN's.

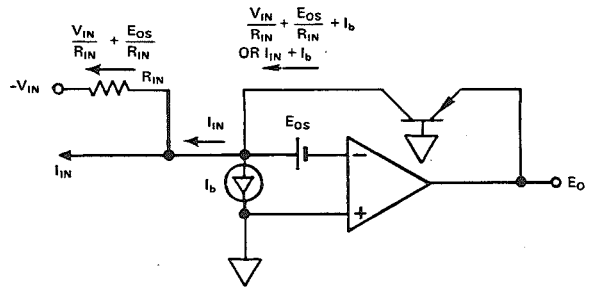


Figure 3. Offset voltage and bias-current errors

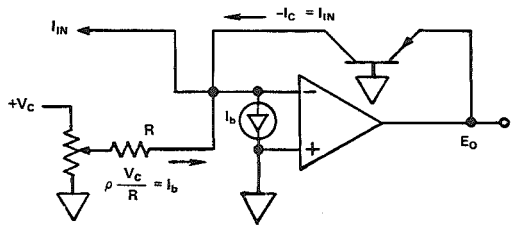
INPUT $\frac{I_{IN} + I_b}{I_{IN}}$	ERROR $\frac{kT}{q}\left(\ln\left[\frac{I_{IN} + I_b}{\alpha I_{ES}}\right] - \ln\frac{I_{IN}}{I_{ES}}\right)$
0.9	− 2.7 mV
0.99	− 0.26mV
0.999	−26. μV
1.000	0
1.001	26. μV
1.01	0.26mV
1.1	2.45mV

Amplifier offset voltage E_{OS} will develop an error current in the feedback path, as a function of the input resistance: E_{OS}/R_{IN}. This current will have the same effect as bias-current error. For measurements of current sources, where $1/R_{IN} \rightarrow 0$, the major contribution of E_{OS} will be through its effect on V_{CB}.

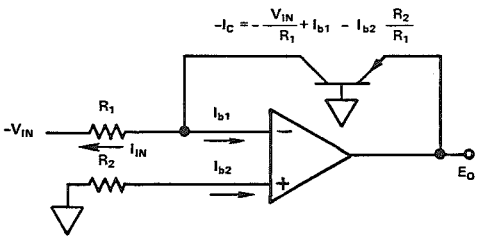
Bias current errors may be reduced in several ways. The most effective and obvious is the choice of an amplifier having appropriate specifications. However, an amplifier with more modest performance (and price) may be used. In the configuration of Figure 4a, a compensating current is summed, nulling the bias current error at one temperature. In the configuration of 4b, a compensating resistance in series with the positive input provides tracking bias-current compensation (if the amplifier inputs track)

$$-I_C = I_{IN} + I_{b_1} - I_{b_2}\frac{R_2}{R_1} \tag{9}$$

If, for example, $I_{b_1} = I_{b_2}$ and $R_1 = R_2$, $-I_C = I_{IN}$. $I_{b_2}R_2$ should not be large enough to cause V_C effects to be significant. This is seldom a problem for current levels that permit the use of bipolar-transistor-input op amps.



a. Nulling the effects of I_b with a compensating current



b. Nulling the effects of I_b through symmetry

Figure 4. Bias-current nulling

Offset-voltage-caused current errors are reduced at one temperature (and—to some degree—over the temperature range) by zeroing the amplifier. Otherwise, either the ambient temperature should be controlled or an amplifier having appropriate performance should be specified. Because I_{ES} may be at 10^{-14}A or less, it is important that careful consideration be given to the selection of an operational amplifier, and to sources of summing-point leakage current, since the lower limit of the log-performance range is usually determined by the amplifier input characteristics and the designer's skill in circuiting.

There are two additional sources of error, inherent in the use of

single transistors and diodes, that can be minimized by the circuit techniques to be discussed later in this chapter. They are the temperature variation of I_{ES} (doubling per ~10°C increase) and the proportionality of kT/q to temperature (0.33%/°C at 25°C), amounting to about 2mV/°C, an intolerable 8%/°C (per ϵ) change.

CLOSED-LOOP STABILITY

In operational amplifier circuits, a necessary condition for stability is that phase shift around the loop be less than 180° at the frequency at which the loop gain $A\beta$ drops through unity. On a Bodé plot for a circuit using minimum-phase (RC) networks, this implies that A and β have slopes differing by less than 40dB/decade when they cross at unity loop gain (Figure 5). In operational amplifier circuits with passive feedback components, $1/\beta$ is never less than unity. Therefore, if the amplifier gain rolls off at 20dB per decade to unity, the circuit must be stable with resistive feedback.

However, in the transdiode connection, the feedback path, both active and nonlinear, may have voltage gain at the higher input-current levels, and even purely-resistive feedback (if possible) would not insure stability, since the unity-gain crossover may occur at a frequency at which the *amplifier* gain is considerably less than unity, accompanied by large phase shift. Moreover, the fact that gain is a function of signal level may force a choice between stability at high levels and bandwidth at low levels.

The effective feedback admittance, for small changes of the emitter voltage, is

$$\frac{dI_C}{dV_E} = \frac{q}{kT} I_C \cong \frac{I_C}{0.026} = \frac{1}{r_E} \tag{10}$$

Since the emitter and collector currents are nearly equal at the high end, the resistance looking into the emitter circuit is also $0.026/I_C$.

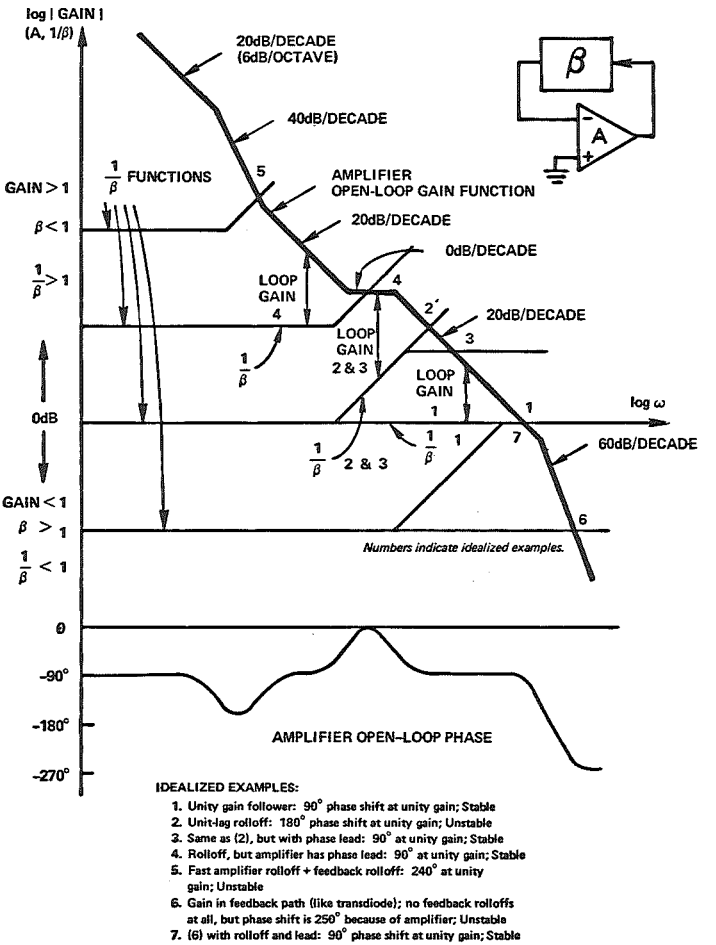


Figure 5. Bodé-plot stability analysis showing stable and unstable loop-gain (Aβ) situations. Aβ = A/(1/β). On log scale, loop-gain can be estimated graphically (log Aβ = log A − log (1/β)), 0 dB at crossing. Numbers indicate idealized examples.

The range of r_E is quite large: for example, it is 26 ohms at 1mA, and 26 megohms at 1nA. Therefore, it is impractical to seek to stabilize the circuit by the conventional tactic of connecting capacitance directly across this feedback element. For example, to obtain a break frequency of 1.6MHz at the high end, 0.039μF

would have to be paralleled with the log transistor. This means that at the low end, the break frequency is 1.6Hz! Furthermore, the amplifier might have difficulty driving a 26-ohm load, even if to only about 0.6V maximum. (Most op amps are rated for loads of 1kΩ or more.)

A simple solution to this dilemma is to connect a resistor R_E in series with the amplifier output and the emitter (Figure 6). It unloads the amplifier and serves as an attenuator between the amplifier output and the emitter. The feedback capacitor C_c, connected from the amplifier output to the summing junction, can now be considerably reduced in magnitude; however, since the output is still taken from the emitter (and still servo'd by the loop), the circuit will be considerably faster in response. R_E should be as large as possible, consistent with the output specification of the amplifier. Since the current through it is equal to the emitter current plus the load current, and the maximum diode voltage is about 0.7V, then, for a 10V amplifier,

$$R_E \cong \frac{9.3V}{I_C + I_L} \tag{11}$$

R_E also protects the junction against excessive values of forward voltage.

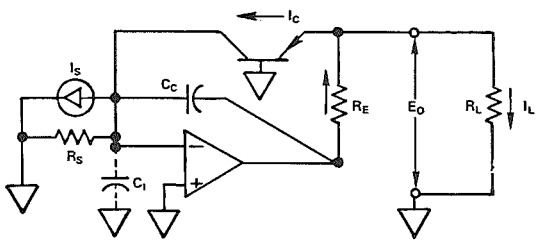


Figure 6. Transdiode circuit with stabilizing elements R_E and C_C

The choice of feedback capacitance depends on the summing-point capacitance and the maximum and minimum current levels. Its value can be determined from the Bodé plot (Figure 7), obtained as follows:

The small-signal response of the feedback portion of the loop, $\beta = \Delta V_f/\Delta E_A$ can be obtained from

$$\frac{\Delta V_f}{R_s}(1 + R_s C_I p) = (\Delta E_A - \Delta V_f)C_c p + \Delta I_c \tag{12}$$

where

$$\Delta I_c = \frac{\Delta E_o}{r_E} = \frac{\Delta E_A}{R_E + r_E} \quad *$$

Solving for β,

$$\beta = \frac{\Delta V_f}{\Delta E_A} = \frac{R_s}{R_E + r_E}\frac{1 + (R_E + r_E)C_c p}{1 + R_s(C_I + C_c)p} \tag{13}$$

If the input is a current source ($R_s \to \infty$)

$$\beta = \frac{1 + (R_E + r_E)C_c p}{(R_E + r_E)(C_I + C_c)p} \tag{14}$$

At high frequencies ($p \to j\omega >> 2\pi f_T$)

$$\beta = \frac{C_c}{C_I + C_c} \tag{15}$$

At low frequencies, for the voltage case (R_s finite)

$$\beta = \frac{R_s}{R_E + r_E} \tag{16}$$

Noting that r_E is inversely proportional to I_C (from 10), the time constants containing r_E will be proportional to r_E for low values of I_C and constant ($\cong R_E$) for high values of I_C.

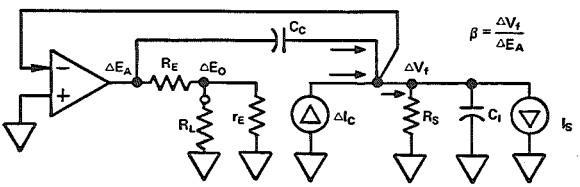
*The effect of load resistance can be included by adding $r_E R_E/R_L$ to $(R_E + r_E)$ wherever it appears.

In order to achieve small-signal stability, the numerator break frequency $\omega_c = 1/(R_E + r_E)C_c$ should be at least 1 octave less than (i.e., ½) the frequency at which $1/\beta = 1 + C_I/C_c$ crosses the amplifier's open-loop gain plot, at the highest value of I_C.

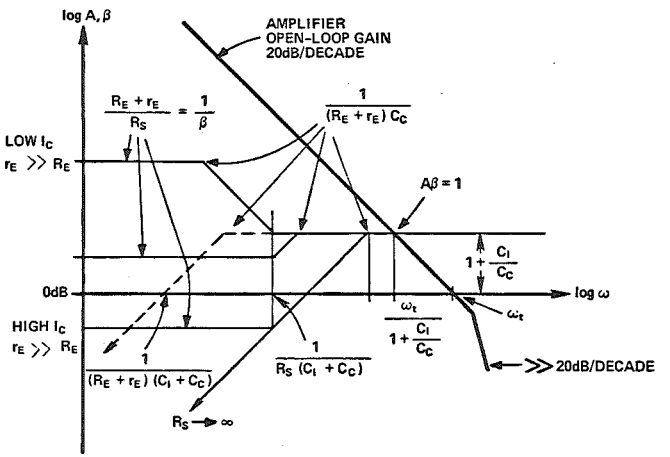
For example, if $R_E = 2.2k\Omega$, $\omega_t = 10^7$ rad/s, $C_I = 10pF$, r_E (@1mA) $= 26\Omega$,

$$\frac{1}{2200C_c} = \frac{1}{2}\frac{\omega_t}{1 + C_I/C_c} \tag{17}$$

Solving for C_c gives: 88pF; hence, 100pF would be a reasonable value.



a) Model for stability analysis



b) Bodė magnitude plot

Figure 7. Bodė plot stability analysis of transdiode circuit

PRACTICAL CIRCUITS

The basic circuits that we have considered so far are of little practical value because of their temperature sensitivity. Also, the output level depends on the value of the reference current, αI_{ES}, which differs from device to device, and is in any event quite sensitive to temperature, approximately doubling for each 10°C increment. The scale factor, kT/q, changes in proportion to absolute temperature, 0.33%/°C in the vicinity of room temperature (27°C).

For two matched transistors (V_{BE} match for constant collector current and temperature) the ratio of the αI_{ES} terms tends to be constant with temperature. For this reason, log transistors are nearly always used in pairs, in order to compensate for variations of αI_{ES} with temperature. Compensation is achieved by performing the subtraction:

$$\frac{kT}{q}\ln\frac{I_1}{\alpha I_{ES_1}} - \frac{kT}{q}\ln\frac{I_2}{\alpha I_{ES_2}} = \frac{kT}{q}\left[\ln\frac{I_1}{I_2} + \ln\frac{\alpha I_{ES_2}}{\alpha I_{ES_1}}\right] \qquad (18)$$

The error term is a constant very nearly equal to $\ln(1) = 0$; if it cannot be ignored, it can be biased out by a fixed value of voltage or current in a subsequent stage.

The subtraction may be performed with a subtractor, as in Figures 8 and 9, or by connecting the log elements in series opposing, as shown in Figures 10, 11, and 12.

In Figure 8, the outputs of A1 and A2, shown with NPN transistors,

$$E_{o_1} = -\frac{kT}{q}\ln\frac{I_1}{\alpha I_{ES_1}}, \quad E_{o_2} = -\frac{kT}{q}\ln\frac{I_2}{\alpha I_{ES_2}} \qquad (19)$$

are subtracted in the circuit of A3 to obtain the output

$$E_o = \frac{R_2}{R_1}\frac{kT}{q}\left(\ln\left[\frac{I_1}{I_2}\right] + \text{const.}\right) \quad \text{const.} \to 0 \qquad (20)$$

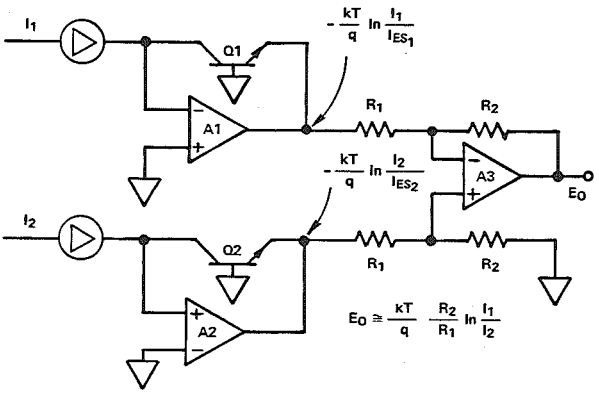


Figure 8. Log ratio circuit with temperature-compensated I_{ES}

Performance of this log ratio circuit is now independent of I_{ES}, if the transistors are adequately matched. For a single input, I_1, the ratio reference I_2 may be fixed at whatever value is desired to normalize I_1. That is, if $I_2 = I_1$, $\ln(I_1/I_2) = 0$. I_2 may be set, for example, at the upper or lower end of I_1's range, or at the geometric mean, for symmetry.

Since kT/q is not usually considered a convenient value of voltage, R_2/R_1 can be scaled to provide an appropriate value of gain. If, for example, it is desired that the output of the circuit have a scale factor of 1V/decade

$$E_o = K \log_{10}(I_1/I_2) = 1.0 \log_{10}(I_1/I_2) \qquad (21)$$

then $R_2/R_1 = q/(kT\ 1n10) = 16.903$ at 25°C.

If the temperature sensitivity of this circuit (0.33%/°C) is too great for the desired stability and range of temperature variation, it may be followed by a gain stage having an equal-and-opposite temperature coefficient. In Figure 9, the unity-gain subtractor is followed by a follower-with-gain circuit. The resistor R_{TC} is chosen so that the gain equation

$$G = 1 + \frac{R_3}{R_{TC}} \qquad (22)$$

has a sensitivity of –0.33%/°C. For example, if G = 16.9, and R_{TC} = 1kΩ at 25°C, R_3 = 15.9kΩ, and the temperature coefficient of $R_{TC} \cong +0.35\%/°C$.

For the convenience of the circuit-designer, the Model 751 logarithmic circuit element contains a pair of matched transistors (751P: PNP's, 751N: NPN's) and a resistive divider designed to provide a temperature-compensated gain in log transistor circuits (See Chapter 4-1).

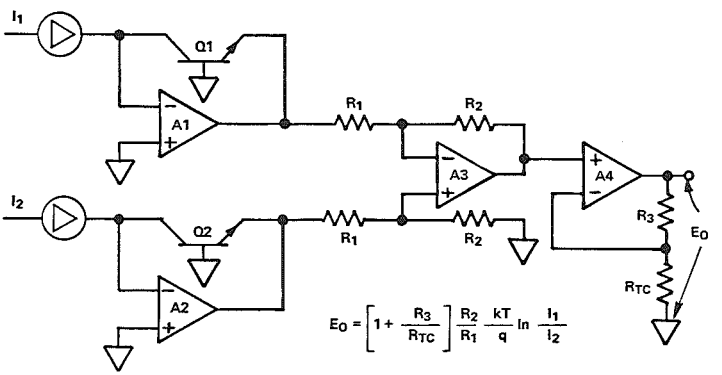


Figure 9. Log ratio circuit with compensation for both I_{ES} and k T/q

The circuits of Figure 8 and Figure 9 were shown without the dynamic stabilization elements R_E and C_c, for clarity in presentation. However, they would be used in the manner of Figure 6 in the circuits of both A1 and A2.

While the circuits of Figures 8 and 9 are workable, they tend to be expensive to implement and are rarely used by designers of constant-reference logarithmic converters. The circuits of Figures 10 and 11 are somewhat more representative. With minor modification, they can be used for antilog operations. They differ from the circuits of Figures 8 and 9 in that they perform the subtraction by a series-opposing connection of the log diodes.

Figure 10 demonstrates the principle. I_1 is the input current; it may be furnished by a current source, or it may be developed through an input resistor R_{IN} by an input voltage V_{IN}. I_2 is either a reference or a second input current furnished by a current

source. The emitter-to-base voltage of Q1 is $-kT/q \ln (I_1/\alpha I_{ES1})$. Assuming that Q2 has high h_{FE} (and that the base current is therefore negligible), the emitter-base voltage of Q2 is $-kT/q \ln (I_2/\alpha I_{ES2})$.

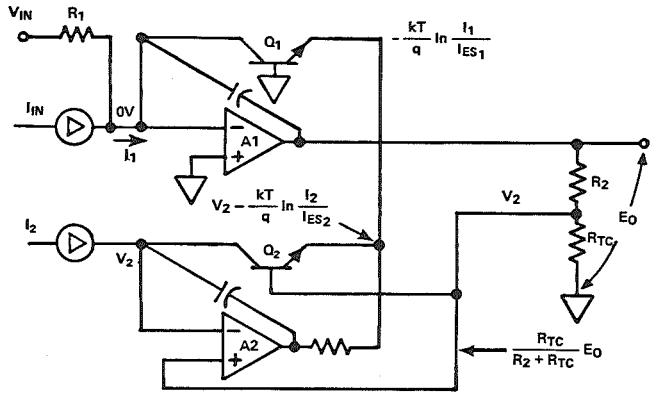


Figure 10. Temperature-compensated log circuit

Inasmuch as the base voltage of Q2 is $E_o R_{TC}/(R_2 + R_{TC})$, the base voltage of Q1 is 0, and both emitters are at the same voltage,

$$V_2 - \frac{kT}{q} \ln \frac{I_2}{\alpha I_{ES_2}} = -\frac{kT}{q} \ln \frac{I_1}{\alpha I_{ES_1}} \tag{23}$$

$$E_o = \left[1 + \frac{R_2}{R_{TC}}\right] V_2 = -\left[1 + \frac{R}{R_{TC}}\right] \frac{kT}{q} \ln \left[\frac{I_1}{I_2} \frac{\alpha I_{ES_2}}{\alpha I_{ES_1}}\right] \tag{24}$$

The "bootstrap" connection of V_2 to the reference input of A2 ensures that the collector-base voltage of Q2 is held at zero, since the negative input of A2 follows V_2. However, it also requires that I_2 be furnished from either a current source, a voltage source referenced to V_2, or a high voltage source in series with a large value of resistance.

The resistive divider compensates for the temperature variation of kT/q and provides a magnified scale factor. If $(1 + R_2/R_{TC}) = 16.9$, at 25°C,

$$E_o = -\,1V \cdot \log_{10} \frac{I_1}{I_2} \tag{25}$$

Figure 11 shows a similar circuit, with a fixed current reference, for accurate log conversion of a single current or voltage input signal (or sum). The reference current is equal to V_{Z_1}/R_3.

$$E_o = K \log_{10} \frac{I_{IN}}{I_{REF}} = K \log_{10} \frac{V_{IN}}{E_{REF}} \tag{26}$$

where

$$E_{REF} = V_{Z1} \left[\frac{R_{IN}}{R_3} \right]$$

and

$$K = \left[1 + \frac{R_2}{R_{TC}} \right] \frac{kT}{q} \ln 10$$

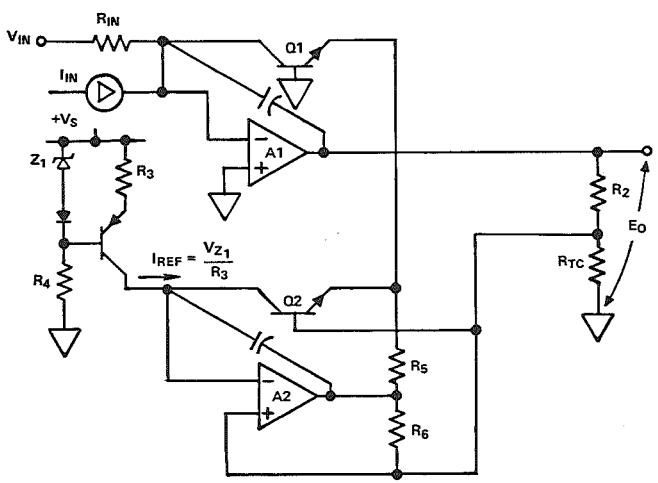


Figure 11. Temperature-compensated log circuit with internal current reference

Resistor R6 allows the high end of the dynamic range to be extended beyond 1mA; its negative-resistance effect tends to cancel the voltage drop of the bulk resistance of Q1. It is calculated by the formula of (27)

$$R_6 = \frac{R_5}{R_B} \frac{R_{TC}R_2}{R_{TC}+R_2} \tag{27}$$

where R_B = Bulk Resistance.

INVERSE OPERATION

If the positions of the input resistor and the log element are interchanged, the same basic circuit configuration may be used to obtain the antilog

$$E_o = -E_{REF}\, e^{-V_{IN}/K} = -E_{REF}\,(10)^{-V_{IN}/K_{10}} \tag{28}*$$

In Figure 12, assuming that Q2 operates with a value of reference current sufficient to ensure logarithmic operation unaffected by base-voltage variations of ±600mV,

$$-\frac{kT}{q}\,1n\left[\frac{E_o}{R_1\alpha I_{ES_1}}\right] = \left[\frac{R_{TC}}{R_2+R_{TC}}\right]V_{IN} - \frac{kT}{q}\,1n\left[\frac{I_{REF}}{\alpha I_{ES_2}}\right] \tag{29}$$

$$\frac{q}{kT}\left[\frac{R_{TC}}{R_2+R_{TC}}\right]V_{IN} = -1n\left[\frac{E_o}{R_1 I_{REF}}\,\frac{\alpha I_{ES_2}}{\alpha I_{ES_1}}\right] \tag{30}$$

or, to base 10,

$$= -(1n\ 10)\log_{10}\left[\frac{E_o}{R_1 I_{REF}}\,\frac{\alpha I_{ES_2}}{\alpha I_{ES_1}}\right] \tag{31}$$

*$E_{REF} = I_{REF}\,R_1$

If $\alpha I_{ES_2} = \alpha I_{ES_1}$, and

$$\frac{kT}{q}\left[1 + \frac{R_2}{R_{TC}}\right] 1n\ 10 = K_{10}$$

then

$$E_o = R_1 I_{REF} (10)^{-V_{IN}/K_{10}} \qquad (31)$$

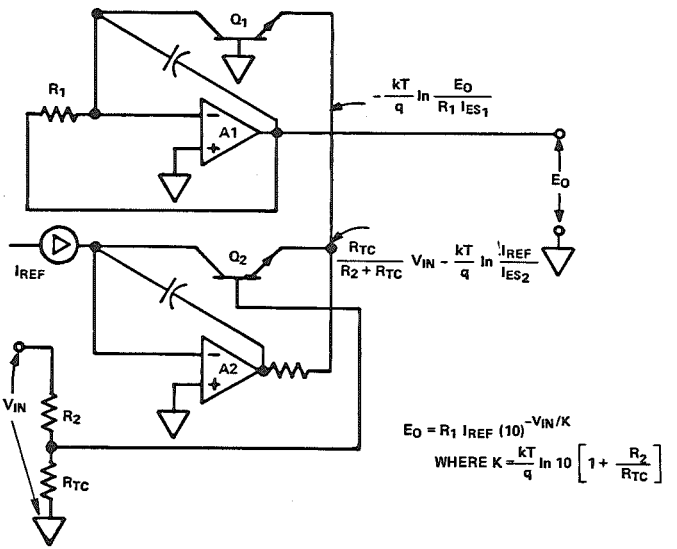


Figure 12. Antilog (exponential) circuit

LOG MODULES

The circuit of Figure 11 is similar to the circuit used for Models 755 (N and P) and 752 (N and P). The principal difference between the two families is that the 755 is a complete, self-contained log circuit, including output amplifier A1, with fixed choices of K (2/3, 1, and 2) and fixed (but modifiable) I_{REF}, specified for operation over 4 decades of voltage and 6 decades of current, while the 752 has a 7-decade range of input current, requires an external amplifier, and has an approximately 10:1 range of adjustment for both K and I_{REF} (Figure 13). Since the major source of error in the 755 at the low end is the amplifier,

the 752 can be used with a choice of operational amplifiers to obtain a wider current or voltage range. It also permits greater flexibility of parameter choice and can be used in complementary pairs to assemble sinh or $\sinh^{-1}$ ("bipolar log") functions.

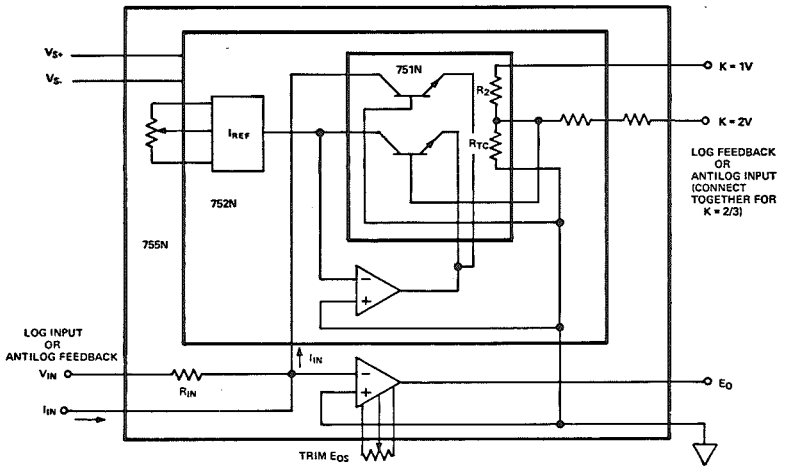


Figure 13. Comparative block diagrams of log/antilog modules (simplified)

NOMENCLATURE AND CHARACTERISTICS (N vs. P)

For all logarithmic devices that offer a choice between an "N" and a "P" version, *N* signifies that an NPN transistor is used as the basic log element; *P* signifies a PNP transistor.

For *N* versions (Figure 14),

- Input voltage or current for the log connection is always positive.
- Output voltage for the antilog (exponential) connection is always positive.
- Output voltage for the log connection is negative for $V_{IN} > E_{REF}$ or $I_{IN} > I_{REF}$, positive for $V_{IN} < E_{REF}$ or $I_{IN} < I_{REF}$.
- Output voltage for the antilog connection is more positive

than E_{REF} with negative inputs, less positive than E_{REF} with positive inputs, equal to E_{REF} for zero input.

- In the log connection, output approaches positive limits as V_{IN} or I_{IN} approach zero.
- In the antilog connection, output approaches zero when the input has large positive values.

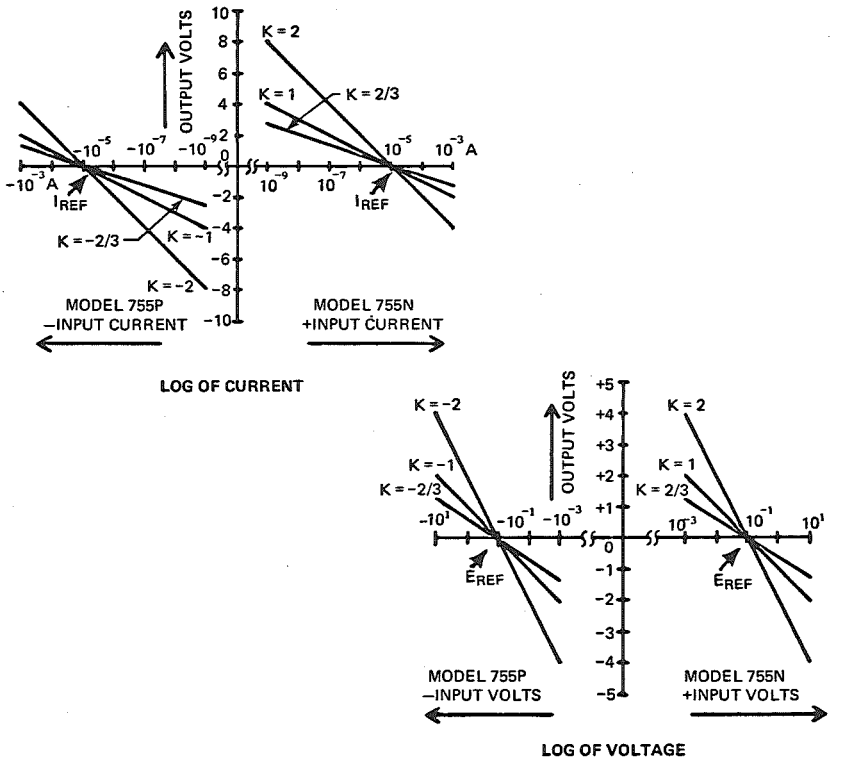


Figure 14. Output vs. input of Model 755N & 755P in log connection (log input scales), showing voltage, and polarity relationships

For *P* versions,

- Input voltage or current for the log connection is always *negative.*
- Output voltage for the antilog (exponential) connection is always negative.

- Output voltage for the log connection is negative for $V_{IN} > E_{REF}$* or $I_{IN} > I_{REF}$, positive for $V_{IN} < E_{REF}$ or $I_{IN} < I_{REF}$.
- Output voltage for the antilog connection is more positive (less negative) than E_{REF} with negative inputs, less positive than E_{REF} with positive inputs, equal to E_{REF} for zero input.
- In the log connection, output approaches negative limits as V_{IN} or I_{IN} approach zero.
- In the antilog connection, output approaches zero when the input has large negative values.

SPECIFYING LOGARITHMIC DEVICES

Errors of logarithmic devices may be referred to either the input or the output. Since it is a useful property of the logarithm that equal ratios of input produce equal output increments (for a given scale factor) we may translate percentage errors at any level of the input to millivolt-level changes at the output, or vice versa. For the purpose of specifying log devices, it is conservative to assume that, if the direction of an error is unknown, it be considered to reduce the magnitude of the argument (i.e., log 0.8, 20% low, is −0.097, while log 1.2, 20% high, is only 0.079). The following table† relates percentage input errors (low) to millivolt output increments for 3 commonly-used values of K. K is in volts/decade (volts per change-by-a-factor-of-ten).

TABLE OF EQUIVALENT ERRORS

Error R.T.I. % low	Output error (mV) Error RTO = $-K \log_{10} (1 - RTI/100)$ K = 1V	K = 2V	K = 2/3V
0.1	0.43	0.87	0.29
0.5	2.18	4.35	1.45
1.0	4.36	8.73	2.91
3.0	13.2	26.5	8.82
4.0	17.7	35.5	11.8
5.0	22.3	44.6	14.9
10.0	45.8	91.5	30.5

*i.e., V_{IN} more positive or less negative than E_{REF}

†See also Table 4, Chapter 4-1

For intermediate values, linear interpolation is quite adequate.

It is not considered good practice to state (log) output error in percent unless it is clearly stated that the error is in percent of nominal K or of full-scale (= nK) or of some other such measure.

When applying devices such as the Model 755 (used as our example here), a firm understanding of the error sources associated with log amplifiers is beneficial for achieving best results. The principal error sources are of two kinds:

1. Parametric errors, due to tolerances and changes in the constants of the ideal log equations, including offsets.
2. Log conformity error, the error that remains when all parametric effects have been removed by nulling and calibration.

Parametric errors are stated separately for voltage and for current operations, as defined in the equations

$$E_o = -K \log_{10} \frac{V_{IN} - E_{os}}{E_{REF}}$$

and

$$E_o = -K \log_{10} \frac{I_{IN} - I_{os}}{I_{REF}} \qquad (32)$$

Scale Factor (K) is the voltage change at the output for a decade (i.e., a 10:1) change at the input, when connected in the log mode. Error in scale factor is equivalent to a change in gain, or slope, and is specified in percent of the nominal value. K is positive for "N" types and negative for "P" types. Its specification for Model 755 is 1% maximum tolerance and 0.04%/°C maximum change with temperature (0°-70°C).

Offset Voltage (E_{os}) depends on the operational amplifier used for the log operation. Its effect is that of a small voltage in series with the input resistor. For current logging operations with high-

impedance sources, its error contribution is negligible. However, for voltage logging, it modifies the value of V_{IN}. Though it can be adjusted to zero at room temperature, its drift over the temperature range should be considered. In the 755, E_{os} is zero ±400μV, with a maximum drift of ±15μV/°C.

Reference Voltage (E_{REF}) is the effective internally-generated voltage to which all input voltages are compared. It is related to the internally-generated reference current I_{REF} by the equation: $E_{REF} = I_{REF} R_{IN}$, where R_{IN} is the value of input resistance. Typically, I_{REF} is considerably less stable than R_{IN}; therefore, practically all the tolerance is due to I_{REF}. In the 755N, E_{REF} is nominally +0.1V ± 3% (3mV *max*), with a maximum temperature coefficient of 0.1%/°C. In the 755P, $E_{REF} \cong -0.1$V, same tolerances.

Offset Current (I_{os}) is the bias current of the amplifier, plus any stray leakage currents. This parameter can be a significant source of error when processing signals in the nanoampere region. For this reason, it is held to within 10pA (doubling per 10°C increase) in such devices as the 755.

Reference Current (I_{REF}) is the internally-generated current source output to which all values of input current are compared. I_{REF} tolerance errors appear as a DC offset at the output. For the 755N, I_{REF} is +10μA ± 3% ± 0.1%/°C *max* (polarity of I_{REF} is negative in 755P). From the table, ±3% tolerance of this input parameter corresponds to ±13.2mV at the output, an offset that is independent of input signal and removable by adjusting the reference current (where possible), adding a voltage to the output by injecting a current into the scale-factor attenuator, or simply by adding a constant bias at the output's destination.

In addition to the parametric errors, *log-conformity error* must be considered. When the parameters have been adjusted to compensate for offset, scale-factor, and reference errors, the output will be found to still deviate from ideal logarithmic behavior (principally at the extremes of the range). Since the behavior of an ideal log device is linear on a semi-log plot, *log conformity error* is the deviation from a straight line on a semi-log plot over the range of

interest. For Model 755, the best linearity of the log relationship is found in the middle 4 decades of the current range (10nA to 100μA). For this range, the log-conformity error is ±0.5% RTI or 2.18mV RTO (K = 1).

It should be obvious that the large number of degrees of freedom, both parametrically, and in terms of the user's variables, would make it difficult to summarize a log devices's specifications in one overall number. As an alternative, sufficient information is provided to calculate performance to fit the desired range. While the Model 755 specifications were cited for the sake of example, the reader should naturally seek to acquaint himself with the properties of devices available at the time he initiates a design effort, via data sheets, the *A D Product Guide*, and other media. Complete specifications of the 755 are listed at the end of this chapter, to aid the reader's understanding of device behavior. Applications information about specific devices is available in great detail on their data sheets.

LOG AND ANTILOG DEVICES

In logarithmic circuits of the type we have been discussing, we can view the causal explanation of what basically happens as follows:

1. Current is applied at the input of the circuit, developing an amplifier input voltage.

2. The amplifier output voltage changes in the opposite direction.

3. The amplifier output voltage, applied to the input (V_{BE}) of the log diode, causes a collector current to flow that balances the amplifier's input current, and holds the input voltage at zero.

4. The amplifier's output is proportional to the log of the input current; but the log diode's output current is proportional to the antilog of *its* input voltage.

Thus, we can consider any log device as consisting of an operational amplifier and an antilog (exponential) circuit. As noted earlier, if we interchange the input resistor and the feedback element, we will therefore have a circuit that develops an antilog input current at the summing point, and a corresponding antilog voltage at the output.*

In the antilog connection, the same sources of error are present and can be considered in the characteristic equation

$$E_o = E_{REF}(10)^{-V_{IN}/K} \pm E_{os} \qquad (33)$$

Errors appearing as constant increments of input will give rise to constant percentage errors at the output.

The 755 can be connected for either log or antilog operation. The 752 can be connected for either log or antilog operation when used with an external operational amplifier. The chart (Figure 15) compares the operating ranges of the 752, with a variety of op amp types, and the 755, subject to the constraint of ±2% error over a ±10°C range. A chopper-stabilized amplifier (233J) maximizes the voltage range; a low-bias-current FET (42J) maximizes the current range; a general-purpose FET (40J) minimizes cost.

LOG MODULE	755	752 OPERATING WITH OP AMP		
Op Amp Type →	Internal-High Performance FET	233J Chopper Stabilized	42J Electrometer FET	40J Economy FET
Input Range for ±2% Error, Over ±10°C				
V_{in}[1]	3.5mV to 10V	500μV to 10V	37.5mV to 10V	25mV to 10V
E_{OS} Drift	150μV	10μV	750μV	500μV
I_{in}	1nA to 1mA	3.5nA to 1mA	50pA[2] to 1mA	5nA to 1mA
$I_{OS} + I_{OS}$ Drift	20pA	70pA	1pA	100pA
Selection Criteria	Complete log amplifier, high performance, trimmed internally	Extends lower limit of voltage range. Minimum drift and offset errors, long term stability	Extends lower limit of current range	Lowest cost for a complete log amplifier
Relative Costs (1–9)	100%	140%	104%	80%

[1] Values selected are consistent with a 10kΩ input register.
[2] Log conformity error restricts the lowest input signal to 100pA.

Figure 15. Comparison of capabilities of 755 complete log/antilog module and 752 log/antilog transconductor

*It is also possible to consider the log diode as a *current* follower, isolated from the amplifier's output voltage by R_E, that develops the log voltage as an *output* (by-product) across r_E.

For applications calling for a variable reference, or the log of a ratio, the 756 has been designed. It has log ratio conformity of 1%, typically over 7 decades (4 decades of numerator change, 3 decades of denominator). Figure 16 shows typical % error, referred to the ratio, as a function of I_N, for 4 values of I_D.

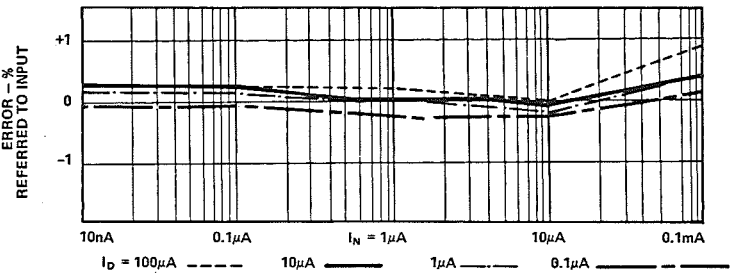


Figure 16. Log-conformity errors of Model 756 log-ratio module

DYNAMIC ERRORS

Speed and frequency response of logarithmic devices depend on scaling, the signal level and the direction of change. Typically, above 1μA, the response is dominated by the integrator time constant, changing little with signal level. Below 1μA, $r_E C_c$ dominates the response, reducing speed in proportion to the input current. A tabulation of typical 755 response time follows. It is interesting to note that response time is shorter for increasing signal magnitude than for the same decreasing increment, because the new current value determines the speed.

I_{IN} (Increasing)	Time	I_{IN} (Decreasing)	Time
1nA to 10nA	1ms	10nA to 1nA	4.5ms
10nA to 100nA	100μs	100nA to 10nA	400μs
100nA to 1μA	7μs	1μA to 100nA	30μs
1μA to 1mA	4μs	1mA to 1μA	7μs

The logarithmic response will of course distort wide-ranging sinusoids, as will the asymmetric and nonlinear delay times. Frequency response is therefore given in terms of *small-signal*

response at differing current levels. Typical frequency response (−3dB) of the 755 is

I_{IN}	−3dB frequency
1nA	80Hz
1μA	10kHz
10μA	40kHz
1mA	100kHz

TESTING LOG DEVICES

The following equipment (or its equivalent) will be found useful in performing the basic tests to be discussed.

Picoampere Current Source	Keithley 261
Precision dc Voltage Standard	Electronic Development Corp. 100N
Function Generator	Hewlett-Packard 3310A
Digital Voltmeter	Hewlett-Packard 8300A
Oscilloscope	Tektronix 543B with Type 1A5 preamplifier

In this section, circuits and techniques will be discussed for the evaluation of some of the basic log-device parameters, such as Scale Factor, Log-Conformity Error, Reference-Current accuracy, Response Time, Bandwidth, and Input Offset (to the degree that they apply to a given log device). For the 755, which is a complete, self-contained "black box," all of these parameters apply; they will be discussed in the context of measurements of a 755.

For brevity, pin-number connections will be referred to. The relationship between pin connections and circuit functions can be seen in Figure 17, a simplified functional diagram of the 755N. The principles, however, are applicable to all similar devices. The results will depend on the care with which measurements are performed.

Scale Factor (K) has been defined as the change in output voltage

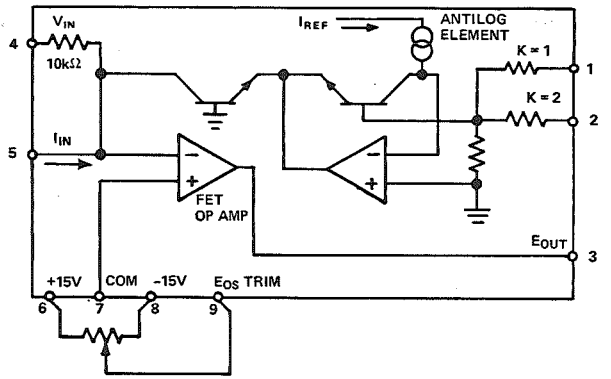


Figure 17. Connection diagram of model 755

for a decade (10:1) change at the input, when connected in the log configuration. It is the slope of a semi-log plot of the output.

Scale factor is most-easily measured using a current source (Figure 18). Apply a value of current I_1 to pin 5 (input summing point) and measure the output. Increase the current by a factor of exactly 10 to $10I_1$ and again measure the output. The scale factor K is simply the difference between the two measurements.

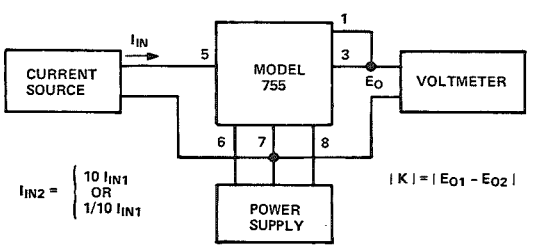


Figure 18. Scale-factor measurement with current input (shown for k = 1)

If it is desired to measure scale factor in the voltage mode, it is first necessary to carefully adjust the input voltage offset to a value near zero. A sensitive adjustment can be performed using the circuit of Figure 19, with the voltage input (pin 4) grounded. Using an external 100kΩ 10-turn trim pot, the output is adjusted (K = 1) to a value between +4V and +5V, for N-type devices. (For 755P, the value would be between −4V and −5V.) Since E_{REF} is 10^{-1}V, an output voltage between 4V and 5V, with the input

grounded, indicates that E_{os} is between 4 and 5 decades lower, or 1–10μV.

After adjusting the offset voltage, the scale factor can be measured in the same way as for a current input (Figure 18), by taking the difference between the outputs for successive values of input V_{IN_1} and $10V_{IN_1}$, applied to pin 4.

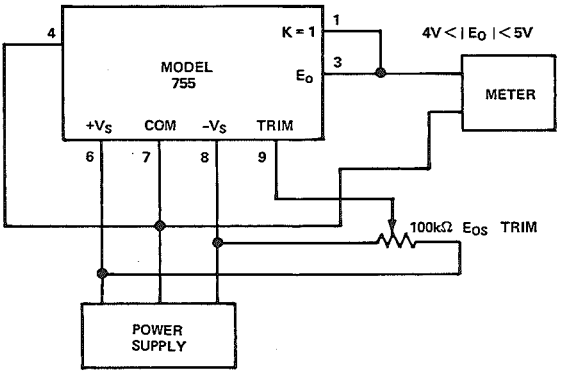


Figure 19. Trimming E_{OS} in the log mode

Reference Voltage is the input voltage at which the ratio of input-to-reference becomes unity; the log output at that value should be zero. The value of reference voltage for a given unit is thus measured by empirically applying precisely-determined voltage to the input (4) in the neighborhood of E_{REF} (0.1V for 755N), and adjusting for zero output. The reference voltage can be modified either by connecting an external resistance of appropriate value to the current input (5) and using it as the input resistor, by modifying the current reference, or by adding a constant in an external summing amplifier at the output. In any of these instances, the new value of reference voltage can be calibrated by applying precisely the value desired at the input, and adjusting for zero output.

Reference Current is the value of input current at which the ratio of input-to-reference becomes unity; the log output at that value should be zero. It is measured similarly to reference voltage, by applying a precisely-measured adjustable input current and adjusting for zero output. I_{REF} for 755N is about 10μA. I_{REF} can be

modified by adding a constant in an external summing amplifier at the output or by modifying the reference source. It is an input variable in the 756 log ratio unit, adjustable in the 752 log/antilog transconductor, and fixed in the 755. However, it can be modified in the 755 by applying a current from a current-source to an unused K pin (1 or 2). The value of current required is 66μA per decade of shift. If it is required for correction only, 0.29μA per 1% change is the approximate sensitivity; for small shifts, the current may be developed by voltage in series with a high value of resistance ($\geqslant$ 2.2MΩ).

Log Conformity error is the difference between the actual output voltage and the output voltage predicted by the log transfer equation, with the effects of offsets, reference shifts, and scale factor either nullified or taken into account. A plot of output vs. input on semi-log paper should be a straight line. Any deviation from a straight line is log conformity error. (Output is measured on the linear scale, input on the log scale.) Apply enough input voltage or current values over the range of interest to allow a smooth curve to be drawn connecting the plotted values of output. The input should be accurately determined, the output accurately measured, and the paper sufficiently large to permit tolerances of the magnitude of interest to be observed. A "best straight" line may then be drawn; the deviations from it represent log-conformity error.

A more sensitive way of plotting is to subtract the expected value of output from the actual value and plot that result (the total error) on the linear scale vs. input on the log scale. A "best straight line" will then show the average slope and offset error, and the deviations from it the log-conformity error. Output error may be referred to the input via the Table of Equivalent Errors (p. 188).

Dynamic Measurements are performed by observing small changes from or about an appropriate bias level. The current input may be used to sum a dc bias and a voltage input (in series with a large external resistance) for incremental changes (Figure 20).

For example, to measure the response time for I_{IN} increasing from 10nA to 100nA or decreasing from 100nA to 10nA, apply 10nA to pin 5 (of the 755N). Through a 10MΩ resistor, apply a 0.9V square pulse, starting from 0V. This will produce an incremental current step of 90nA, and an overall input swing of 10-100nA. Assuming that the pulse is of adequate width, response to both increasing and decreasing steps can be seen at the same time. At the output (K = 1), the increasing-input step response will swing from +4V to +3V; the decreasing-input response will swing from +3V to +4V.

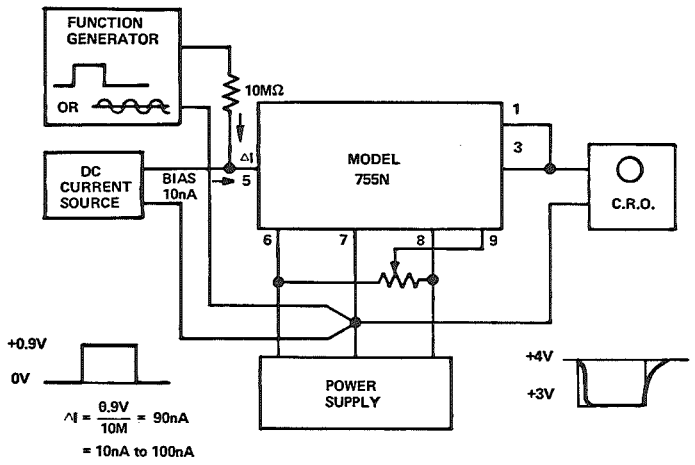


Figure 20. Performing incremental response measurements

Frequency response is measured typically by using a ±5% sinusoidal deviation about a fixed input value. For example, at the 1μA level, the deviation will be ±50nA. Apply 1μA dc to the current input (5), and sum it with 100mVp-p through a 1MΩ resistor. The output swing at low frequencies should be 43.5mVp-p. Increase the frequency, maintaining the input amplitude constant, until the output amplitude is 30.5mVp-p. This is the frequency at which the output amplitude is down 3dB from its low-frequency value.

CONCLUSION

Logarithmic devices have been summarized in Part 1, and applications have appeared throughout Part 2. This chapter has discussed the basic properties of logarithmic devices, techniques for obtaining thermal and dynamic stability, some commonly-used circuits, specifications and definitions, and means of adjustment and test. Chapters 4-1, 4-2, 4-3, "Aids for the Designer," will provide further information, as well as guidelines for selection and use of devices for log, log ratio, and antilog applications.

APPENDIX TO CHAPTER 3-1 · COMPLETE SPECIFICATIONS OF A TYPICAL LOG/ANTILOG MODULE (MODELS 755N & 755P)

(typical @ +25°C and ±15VDC unless otherwise noted)

TRANSFER FUNCTIONS — DYNAMIC RANGE OF INPUT

Log of Current — 120dB

$$E_o = -K \log_{10} \frac{I_{in} - I_{OS}}{I_{REF}}$$

1nA to 1mA (755N)
−1nA to −1mA (755P)

Log of Voltage — 80dB

$$E_o = -K \log_{10} \frac{E_{in} - E_{OS}}{E_{REF}}$$

1mV to 10V (755N)
−1mV to −10V (755P)

Antilog of Voltage

$$E_o = E_{REF}\, 10^{-E_{in}/K} \pm E_{OS} \qquad -2 \leqslant E_{in}/K \leqslant 2$$

TRANSFER FUNCTION PARAMETERS

Symbol	Value	Tolerance	Drift	Note
K	2/3, 1, 2V	1% max	±0.04%/°C max	1, 2
E_{REF}	0.1V	3% max	±0.1%/°C max	2
I_{REF}	10μA	3% max	±0.1%/°C max	2
E_{OS}	0 ± tol.	±400μV	±15μV/°C max	3
I_{OS}	0 ± tol.	+0, −10pA max	2x/10°C	

LOG CONFORMITY ERROR REFERRED TO INPUT

Input Current Range	Conformity Error	Input Voltage Range	Conformity Error
1nA to 10nA	±1% max		
10nA to 100μA	±0.5% max	1mV to 1V	±0.5% max
100μA to 1mA	±1% max	1V to 10V	±1% max
1nA to 1mA (Total Range)	±1% max		

RESPONSE TIME

I_{in} (increasing)	Time	I_{in} (decreasing)	Time
1nA to 10nA	1ms	10nA to 1nA	4.5ms
10nA to 100nA	100μs	100nA to 10nA	400μs
100nA to 1μA	7μs	1μA to 100nA	30μs
1μA to 1mA	4μs	1mA to 1μA	7μs

SMALL SIGNAL FREQUENCY RESPONSE

I_{IN}(Level)	3dB Down At
1nA	80Hz
1μA	10kHz
10μA	40kHz
1mA	100kHz

NOISE REFERRED TO INPUT, 10kHz BANDWIDTH

Noise Voltage	2μV rms
Noise Current	2pA rms

RATED OUTPUT (Note 4)

±10V, ±5mA

POWER REQUIREMENTS (QUIESCENT)

±15V, regulated ±1%, 7mA

TEMPERATURE

Operating	0°C to +70°C
Derated	–25°C to +85°C
Storage	–55°C to +125°C

MECHANICAL

Case Size	1.5" X 1.5" X 0.4"
Weight	38.1 X 38.1 X 10.2 mm
	1 oz. (28.3g)

PRICES

(1–9)	$55.00
(10–24)	$49.00

NOTES:

1. Use terminal 1 for K = 1V, terminal 2 for K = 2V, terminals 1 and 2 (shorted together) for K = 2/3V.
2. Parameter is + for 755N, – for 755P.
3. Externally adjustable to zero.
4. No device damage due to any pin being shorted to ground.
5. Specifications subject to change without notice.

III Multipliers

Chapter 2

An analog multiplier is a device that produces an output voltage or current that is proportional to the product of two or more independent input voltages or currents

$$E_o = V_x V_y / V_r = K V_x V_y \qquad (1)$$

The proportionality constant, $1/V_r$, has the dimension V^{-1}. V_r may be identifiable with a specific voltage or current in the circuit, or it may be independently determined. It is usually fixed at 10V.

The operating range of a multiplier may be defined in terms of its inputs. For two inputs, and a possibility of two polarities for each input, there are four combinations of polarity. They can be visualized as the four quadrants of the X-Y plane (Figure 1).

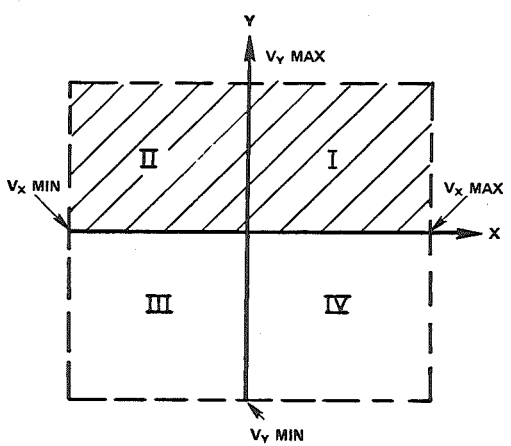


Figure 1. Multiplier operating coordinates

A pair of inputs within the operating region uniquely determines the multiplier's output voltage. A multiplier that can accept all four combinations of inputs and provide outputs of appropriate polarity is referred to as a "4-quadrant multiplier." "Two-quadrant" multipliers respond to a ± signal at one input and a unipolar signal at the other. For instance, if a multiplier responds to $\pm V_x$, but only $+V_y$, will it operate in the half-plane of quadrants I and II, indicated by shading.

One-quadrant multipliers respond to unipolar inputs in a single quadrant only. If both V_x and V_y are limited to positive values, the multiplier operates in the first quadrant. Occasionally, one will find a multiplier that responds to the appropriate number of quadrants, but with inverted output polarity. Its equation is $E_o = -KV_xV_y$. A multiplier that responds to one or more of its inputs in a single quadrant can be used for multiple-quadrant operation by being preceded by an absolute-value circuit, and followed by a sign-magnitude output circuit, with output polarity determined by input polarity (a procedure almost as cumbersome as it sounds but typical of such devices as some multiplying D/A converters). Multi-quadrant operation can also be achieved by offsetting the inputs and output (see Figure 21).

TECHNIQUES OF MULTIPLICATION

At present, the two most-common means of performing electronic analog multiplication are *variable-transconductance* and *pulse-width, pulse-height* modulation. A third method, *log-antilog*, is gaining in popularity, particularly for low-speed high-accuracy calculations.

The circuit design, and the factors affecting overall performance of these three types of multipliers will be discussed in detail in this chapter.

Many other types of multipliers and modulators have been, and still are, used in analog-computing, communications, and instrumentation circuits. Examples of these are quarter-square, diode-ring, FET, and magnetic (e.g., Hall effect). The design of these

types will not be covered here; however, much of the discussion of specifications and testing could be applied to them.

CHARACTERISTICS OF MULTIPLICATION

Since the algebraic properties of multiplication are the determining factors in the design and specification of analog multipliers, a review of a few of these properties and their correspondence to physical multiplier performance will aid understanding.

One of the most salient properties of multiplication, with direct implications for design and characterization, is the fact that the product is zero for three kinds of input pairings.

Input State	Theoretical Output	Error Parameter
1	$0 \cdot 0 = 0$	Offset
2	$0 \cdot Y = 0$	Y-Null, or Y Feedthrough
3	$X \cdot 0 = 0$	X-Null, or X Feedthrough

Another important property is the relationship of the magnitude of the product to the inputs. If we assume that both products are always less than V_r (i.e., V_r is full scale), as is the case for most popular multipliers, then the product is always less than or equal to V_r

4	$0 \leqq \lvert V_x, V_y \rvert \leqq V_r$	Input Constraint	(2)
5	$\lvert V_x \cdot V_y / V_r \rvert \leqq V_r$	Output Constraint	(3)

If the two inputs are not equal, the product will be less than the smaller input, if the conditions of (2) are met, i.e., if

$$\lvert V_x \rvert < \lvert V_y \rvert \tag{4}$$

and

$$|V_x V_y / V_r| < V_r \tag{5}$$

then

$$|V_x V_y / V_r| < V_x \tag{6}$$

Equations 2-6 illustrate that the output of an ideal multiplier is well-behaved for small inputs: the output goes to zero as either or both inputs are reduced to zero. The analog multiplier circuits discussed in this chapter come surprisingly close to following this ideal behavior, assuming that the first-order (or linear) errors are adjusted to zero. The reason for this is that the nonlinear component of error ($f(V_x,V_y)$) is a continuous function of V_x and V_y that goes to zero as V_x and V_y are decreased to zero. The following sections, describing the sources of multiplier errors, and the relationship to circuit design, will show why this is so.

The multiplication function can be represented by a surface in three dimensions embodying the equation

$$Z = X\,Y \tag{7}$$

The shape of the surface can be outlined in terms of the following characteristics

1. Output (Z) is zero along the X and Y axes (zero feedthrough).

2. If one input is constant, then the output is linearly proportional to the other input, with a slope ("Gain") determined by the constant input.

3. If the two inputs are equal (X = Y, or X = –Y), then the output is proportional to the input squared. This produces two tangent parabolas of opposite polarity at right angles corresponding to the diagonals in I-III and II-IV.

The surface that fits these requirements is the hyperbolic paraboloid, or "saddle-surface," as sketched in Figure 2. The parabolic branches correspond to the intersections of the surface with verti-

cal planes through the diagonals and parallel to the diagonals (condition 3). The straight-line elements correspond to the intersections of the surface with vertical planes parallel to the X and Y axes (condition 2), and the surface passes through the X-Y plane along the X and Y axes and their intersection of 0 (condition 1).

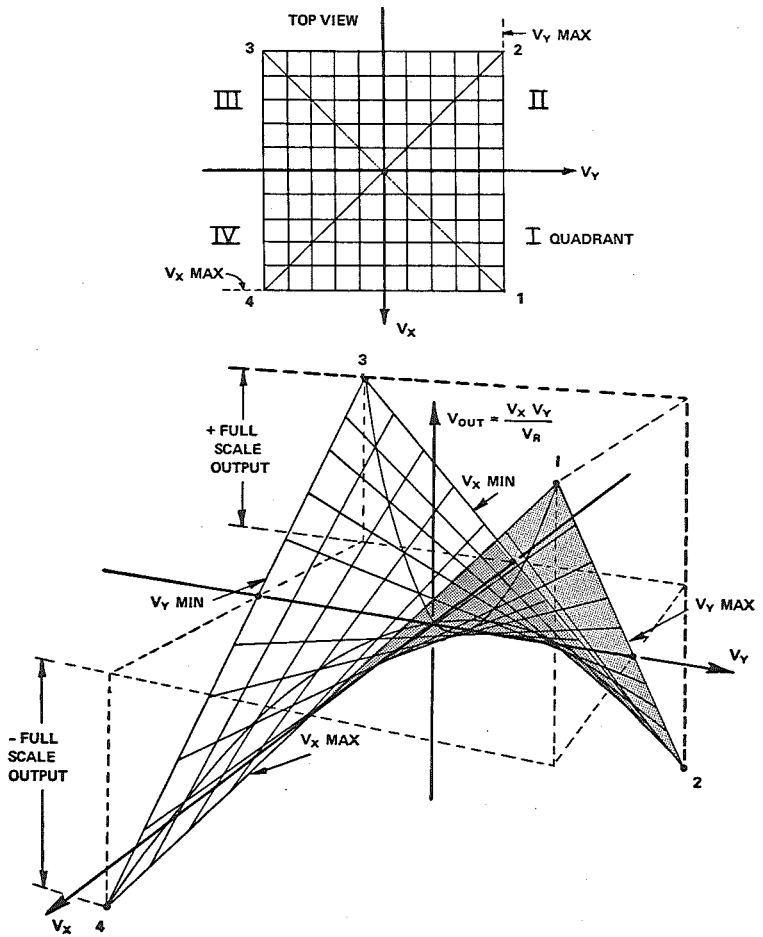


Figure 2. Four quadrant multiplier – input/output surface

Horizontal planes intersect the function in hyperbolas. That is, a contour map would show a family of right hyperbolas climbing hills along diagonal I-III and sinking into valleys along diagonal II-IV (Figure 5).

The corners of the surface labeled 1, 2, 3, 4 in the figure represent the maximum outputs of the multiplier in the respective quadrants. These maxima occur at the four combinations of ±X and ±Y.

To some, the thought of a multiplier as a nonlinear device may seem paradoxical, despite the fact that it is clearly nonlinear. After all, any practical measurement of a multiplier's gain characteristics, performed at constant values of X or Y, will yield a linear output-input relationship, that is, the multiplier acts as a linear amplifier with gain KX. In fact, one thinks of a "linear" multiplier as one that obeys the ideal relationships of (1).

Clearly, with one input fixed, the multiplier is indeed a linear device and could, in concept, be replaced by a fixed-gain amplifier. The signal input can not cause the gain to vary, so it will be linearly reproduced at the output.

If both inputs are varied, the response is indeed nonlinear. For example, if the same input is applied to both X and Y, the output will be proportional to the square of the input. This is clearly nonlinear behavior, fitting neither the proportionality nor the superposition criteria for linearity (see p. 1).

$$\text{If } V_{IN} = V_1 \qquad E_{out} = KV_1^2 \tag{8}$$

$$\text{If } V_{IN} = V_2 \qquad E_{out} = KV_2^2 \tag{9}$$

$$\text{If } V_{IN} = V_1 + V_2 \qquad E_{out} \neq K(V_1^2 + V_2^2) \tag{10}$$

The geometrical interpretation is that the hyperbolic paraboloid is a developed surface, a curved surface that can be constructed from straight-line elements – like the cylinder or the cone.

That the ideal analog multiplier is a linear device, if one input is maintained at a constant value, is a useful fact, one that makes it easy to characterize, adjust, calibrate, and measure the behavior of real multipliers in linear terms despite their inherently nonlinear nature.

ERRORS IN PRACTICAL ANALOG MULTIPLIERS

The output of a practical multiplier will differ from the theoretical product of its inputs by a generally unpredictable amount, ϵ, as defined in the equation

$$E_o = K V_x V_y \pm \epsilon(V_x, V_y) \qquad (11)$$

It will be quite helpful in discussing multiplier circuit properties to expand the error indicated symbolically in (11) into terms directly related to error sources in the circuit. There are four primary sources of static (or dc) error in an analog multiplier (dynamic errors are discussed later, in the section on multiplier specifications)

	Error	Symbol
1.	Input Offsets	X_{os}, Y_{os}
2.	Output Offset	Z_{os}
3.	Scale Factor	ΔK
4.	Nonlinearity	$f(X,Y)$

The influences of these errors can be applied as follows

$$E_o = (K + \Delta K)\left\{(V_x + X_{os})(V_y + Y_{os}) + Z_{os} + f(X,Y)\right\} \qquad (12)$$

Multiplying out and combining terms

$$E_o = KV_xV_y + \underbrace{\Delta KV_xV_y + (K+\Delta K)\left\{V_xY_{os} + V_yX_{os} + Y_{os}X_{os} + Z_{os} + f(X,Y)\right\}}_{\epsilon(X,Y)} \qquad (13)$$

This lengthy array of error terms can be untangled by considering each separately:

Term	Description	Dependence on Input
KV_xV_y	True Product	Goes to zero as either or both inputs go to zero
ΔKV_xV_y	Scale-Factor Error	Goes to zero at V_x, $V_y = 0$

Strictly speaking, the following terms are multiplied by $K + \Delta K$, but the effect of ΔK can be ignored, since the product of ΔK and another error is a second-order error, and hence negligible.

$V_X Y_{os}$	Linear "X" Feedthrough Due to Y-input dc Offset	Proportional to V_x
$V_y X_{os}$	Linear "Y" Feedthrough Due to X-input dc offset	Proportional to V_y
$X_{os} Y_{os}$	Output Offset due to X,Y Input Offsets	Independent of V_x,V_y
Z_{os}	Output Offset	Independent of V_x,V_y
$f(X,Y)$	Nonlinearity	Depends on both V_x, V_y. Contains terms dependent on V_x,V_y, their powers and cross-products.

The error of a practical analog multiplier, $\epsilon(X,Y)$, can be visualized as a surface representing the difference between the actual multiplier output and the theoretical value. The error surface will be, in general, warped, twisted, and not level, much like a section of hilly countryside. Figure 3 shows a hypothetical error surface for a four-quadrant multiplier. The elevation, or Z coordinate of the graph, represents the error, $\epsilon(X,Y)$ defined by

$$\epsilon(X,Y) = E_o(\text{actual}) - KV_x V_y = E_o - V_x V_y / V_r \qquad (14)$$

where

E_o = measured value of multiplier output voltage

V_x = X input voltage

V_y = Y input voltage

$KV_x V_y$ = Ideal output voltage

$\epsilon(X,Y)$ is the measured voltage corresponding to the sum of the error terms in (13).

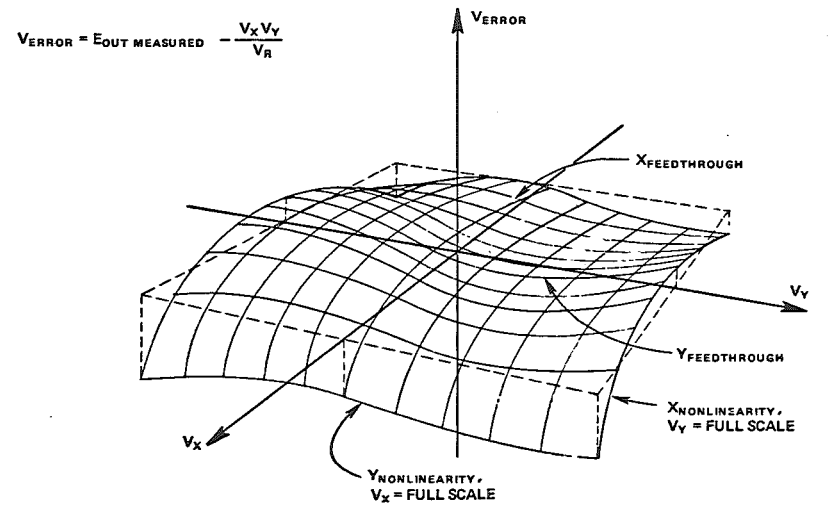


Figure 3. Multiplier error plane

Using an error surface to describe the static error of an analog multiplier may seem awkward, but it is the easiest way to visualize the *whole* three-dimensional effects of the individual error components in (13).*

For example, consider the effect of "linear" X feedthrough $V_X Y_{OS}$. Assuming that Y_{OS} is a small positive quantity, then as V_X increases, the output of the multiplier will increase in proportion. As V_X goes negative, the output will go negative. This effect is clearly independent of the Y input, since equation 10 shows $V_X Y_{OS}$ as an additive error. The result of the linear X feedthrough is to tilt the plane about the Y axis, as shown in an end-on view of the XY plane, Figure 4.

Similarly, the effect of X offset ("linear" Y feedthrough) is to tilt the whole error plane about the X axis. The effect of dc offset, $X_{OS}Y_{OS} + Z_{OS}$, is to move the whole plane up or down on the Z (output) axis.

*The error surface is primarily an aid to visualization. It, and the 2-dimensional contour representation ("iso-vers": *iso*-equal, *ver(ity)*-accuracy), have been used for this purpose. However, because of wide differences in form of the error function from unit to unit, and for a given unit under various stages of adjustment and thermal environment, error surfaces are of little use as compact presentations of data for individual devices.

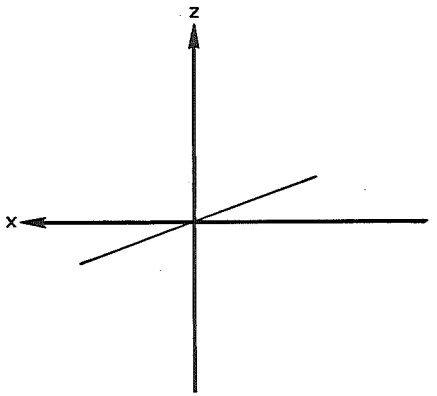


Figure 4. Linear X feedthrough, can be viewed as section of the error surface at Y = 0

The effect of the scale factor, ΔK, considered alone, is to create an error surface defined by

$$\epsilon(XY)_K = \Delta K V_x V_y \tag{15}$$

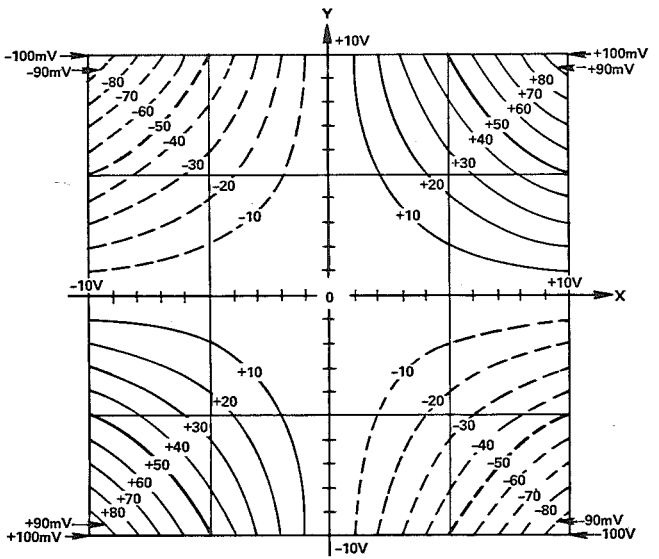


Figure 5. ISO-VER representation of 1% positive-scale-factor-error surface (all other errors zero), contour interval: 10mV

This is just a scaled-down version of the multiplier output $V_z = KV_xV_y$. Therefore, the scale-factor error surface must be a hyperbolic paraboloid, as sketched in Figure 2, but much smaller. Figure 5 is a 2-dimensional contour ("Iso-ver") representation. The effect of nonlinearity, $f(X,Y)$, is to introduce curvature on the nominally-straight-line elements parallel to the X or Y axis. That is, a section through the multiplier output surface parallel to the XZ or YZ plane is no longer a straight line (Figure 6).

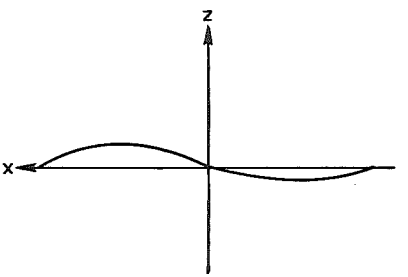


Figure 6. X nonlinearity can be viewed as section of the error surface at any value of Y

To summarize, a two-input analog multiplier has 4 sources of "trimmable" static error. Referring to (13), these are

1. X-input offset (Linear Y feedthrough)
2. Y-input offset (Linear X feedthrough)
3. Output offset
4. Scale-factor error

The effects of these four errors can be reduced to zero by introducing equal and opposite offsets for errors 1, 2, 3, and by precise adjustment of the scale factor, or gain, for 4. After the four errors are adjusted to zero, the remaining error will be due to the inherent nonlinearity of the multiplier, $f(X,Y)$. The nonlinearity is generally irreducible; however, in certain cases, a large percentage of it can be cancelled, as will be described in the *transconductance multiplier* section.

TRANSCONDUCTANCE MULTIPLIERS

The variable-transconductance multiplier is the simplest type of analog multiplier, at least in concept. One input variable controls the gain (transconductance) of an active device, which amplifies the other input in proportion to the control input.

A wide variety of active devices, such as transistors, FET's, vacuum tubes have been used, with varying degrees of success, to make "transconductance" (or "transresistance") multipliers and modulators for analog computing or communications signal-processing. However, almost all of the "transconductance" multipliers available today use silicon junction transistors as the active elements, because of the transistor's linear and consistent relationship between collector current and transconductance, given by equation (16)

$$\frac{dI_c}{dV_{be}} = \frac{q}{kT} I_c \tag{16}$$

where

I_c = collector current in amperes

V_{be} = base-emitter voltage, in volts

q = unit of electronic charge = 1.60219×10^{-19} coulombs

k = Boltzmann's constant = 1.38062×10^{-23} joules/°K

T = absolute temperature, degrees Kelvin = °C + 273.15°

q/kT = 1/(25.69mV) at 25°C

The multiplicative property can be seen for sufficiently small increments ΔI_c, ΔV_{be} (Figure 7)

$$\Delta I_c = \frac{q}{kT} I_c \cdot \Delta V_{be} \tag{17}$$

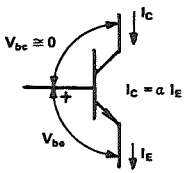


Figure 7. NPN transistor nomenclature

Equation (16) is derived by differentiating the simplified junction equation*

$$I_c = \alpha_N I_{ES}(\epsilon^{qV_{be}/kT} - 1) \tag{18}$$

α_N = charge transport factor $\cong$ 0.99

I_{ES} = emitter saturation current, 10^{-12} to 10^{-14} A @25°C

with the assumption that the collector-base voltage of the transistor is zero,

$$\frac{I_c}{I_{ES}} >> 1,$$

yet the current levels are low enough so that ohmic resistances (e.g., base spreading resistance, emitter contact resistance, and bulk resistance) are negligible. For a typical monolithic dual transistor, this means collector currents of 100μA or less. At 100μA, the transconductance is about 1/260mho at 26°C; parasitic resistances of about 3Ω, typical of monolithic transistors, reduce the transconductance by about 1%.

A simple, 2-quadrant variable-transconductance multiplier can be constructed from a pair of transistors and a few resistors, as shown in Figure 8. If the output of this multiplier is considered to be the difference between the collector currents of Q1, Q2, then equations 19 and 20 define the output-input relationship for this circuit

$$I_{c_1} - I_{c_2} = \Delta I_c = \frac{q}{kT} \frac{V_y + 0.6}{4.7 \times 10^3} 10^{-3} V_x \tag{19}$$

$$\Delta I_c = 8.3 \times 10^{-6} (V_y + 0.6) V_x \quad \text{at } 25°C \tag{20}$$

*See equation (6), Chapter 3-1.

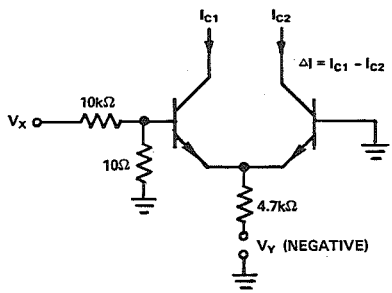


Figure 8. Simple 2-quadrant variable-transconductance multiplier

As (20) shows, the output collector-current difference is proportional to the product of the input voltages, V_x, V_y, with the following limitations:

1. The Y input has a 0.6V offset due to the assumed (constant) V_{BE}'s of Q1 and Q2. Thus, the most-positive value of V_y that can be accepted is –0.6V. Also, V_{be} is not constant. The V_{be} of Q1, Q2 increases as $|V_y|$ increases, introducing nonlinearity on the Y input. Both problems can be fixed by using a more-elaborate voltage-to-current converter to replace the Y-input resistor.

2. The scale factor is a function of temperature, decreasing at –0.33%/°C near 25°C. This might be fixed by using temperature-compensating resistors on the X input, but it is hard to get precise compensation.

3. The X input is nonlinear, due to the exponential relationship between collector current and base-emitter voltage (18). The 1000:1 attenuator on the X input reduces the ±10V range to ±10mV between the bases, so that the actual X signal is less than the junction constant kT/q (25.69mV @ 25°C). However, even this small signal can result in 7% nonlinearity for X-input signals. The nonlinearity can be decreased by increasing the X-input attenuation, but at the cost of decreased signal-to-noise.

For the above reasons, the differential pair is not particularly useful or attractive as a high-level analog multiplier. However, it is quite effective as a mixer in RF applications, where the incoming signal is already quite small (millivolts or less).

There is a good, inherently simple solution to the nonlinearity, limited-dynamic-range, and temperature-coefficient problems of the simple differential pair[1]. Gilbert's circuit has rapidly gained universal acceptance, because of its low errors (~1%), wide bandwidth (>100MHz possible), and relative simplicity. In fact, it has become synonymous with "transconductance" multiplication. The basic circuit, shown in Figure 9, uses the logarithmic properties of diodes (or diode-connected transistors) to compensate for the exponential nonlinearity on the base inputs (hereafter labeled "X" input, for convenience) of the differential pair.

The balanced X input currents, I_{D_1}, I_{D_2}, flow through diodes D1, D2, establishing voltages V_1, V_2, which are proportional to the log-of-current ($\alpha_N \cong 1$)

$$V_1 = \frac{kT}{q} \ln \frac{I_{D_1}}{I_{ES_1}} \tag{21}$$

$$V_2 = \frac{kT}{q} \ln \frac{I_{D_2}}{I_{ES_2}} \tag{22}$$

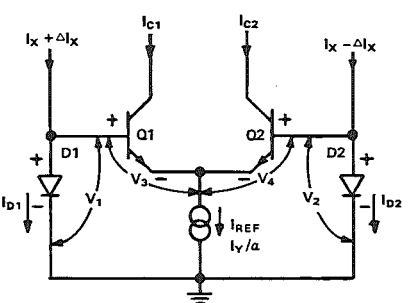


Figure 9. Linearized 2-quadrant multiplier (principle)

[1]"A New Wide-Band Amplifier Technique," by Barrie Gilbert, *IEEE Journal of Solid-State Circuits*, December, 1968, Volume SC-3, No. 4, pp. 353-365.

Since the collector currents of Q1 and Q2 are exponential functions of their base-emitter voltages (18) or the differential input voltage ($V_{BE_1} - V_{BE_2}$), it is reasonable to assume that the logarithmic input voltages provided by D1, D2 will cancel some, if not all, of the exponential nonlinearity of Q1 and Q2, resulting in a linear relationship between I_{D_1}, I_{D_2}, and I_{C_1}, I_{C_2}. In fact, the linearization is perfect in theory, and almost perfect in practice, a surprising and useful result that can be demonstrated as follows:

Assumptions:

1. Pairs Q1, Q2 and D1, D2 have zero differential offset voltage if $I_{C_1} = I_{C_2}$ and $I_{D_1} = I_{D_2}$.

2. Q1, Q2, D1, D2 obey the ideal junction equation (18)

The sum of the voltages V_1 to V_4 around the loop from the cathode of D1 to Q1, Q2, and the cathode of D2, must be zero

$$V_1 - V_3 + V_4 - V_2 = 0 \tag{23}$$

$$V_1 - V_2 = V_3 - V_4 \tag{24}$$

The base-to-emitter voltages of Q1, Q2 are proportional to the logarithms of their collector currents

$$V_{BE_1} = V_3 = \frac{kT}{q} \ln \frac{I_{C_1}}{I_{ESQ_1}} \tag{25}$$

$$V_{BE_2} = V_4 = \frac{kT}{q} \ln \frac{I_{C_2}}{I_{ESQ_2}} \tag{26}$$

Substituting for V1 through V4 in (24)

$$\frac{kT}{q} \ln \frac{I_{D_1}}{I_{ES_1}} - \frac{kT}{q} \ln \frac{I_{D_2}}{I_{ES_2}} = \frac{kT}{q} \ln \frac{I_{C_1}}{I_{ESQ_1}} - \frac{kT}{q} \ln \frac{I_{C_2}}{I_{ESQ_2}} \tag{27}$$

Cancelling the kT/q terms and rewriting the differences of logs as logs of ratios

$$\ln \frac{I_{D_1} I_{ES_2}}{I_{D_2} I_{ES_1}} = \ln \frac{I_{C_1} I_{ESQ_2}}{I_{C_2} I_{ESQ_1}} \tag{28}$$

The constants will all be equal if the transistors and diodes are matched, as has been assumed

$$\ln \frac{I_{D_1}}{I_{D_2}} = \ln \frac{I_{C_1}}{I_{C_2}} \tag{29}$$

If the logs of the ratios are equal, then the ratios must be equal

$$\frac{I_{D_1}}{I_{D_2}} = \frac{I_{C_1}}{I_{C_2}} \tag{30}$$

This important result states that the ratio of the "output" currents I_{C_1}, I_{C_2} is linearly proportional to the ratio of the input currents, I_{D_1}, I_{D_2}, irrespective of temperature or the magnitudes of the currents! In other words, the linearization is ideally perfect, and the input-output transfer of X is constant with temperature.

The multiplier relationship can be derived directly from (30). The X input is assumed to be a difference $2\Delta I_x$ between the two diode currents I_{D_1} and I_{D_2}. The Y input controls the emitter currents I_{REF}. The multiplier output is the difference $2\Delta I_C$ in the collector currents of Q1 and Q2.

$$I_{D_1} = I_x + \Delta I_x \tag{31}$$

$$I_{D_2} = I_x - \Delta I_x \tag{32}$$

$$-I_x < \Delta I_x < I_x \tag{33}$$

$$I_{C_1} + I_{C_2} = \alpha I_{REF} \cong I_y \quad (\alpha \cong 1) \tag{34}$$

Q1, Q2 and D1, D2 are assumed matched, and Q1, Q2 have high β ($> 100, \alpha \cong 1$).

$$I_{C_1} = I_y/2 + \Delta I_C/2 \tag{35}$$

$$I_{C_2} = I_y/2 - \Delta I_C/2 \tag{36}$$

$$-I_y/2 < \Delta I_C < I_y/2, \quad I_y > 0 \tag{37}$$

Substituting for I_C and I_D in (29)

$$\frac{I_X + \Delta I_X}{I_X - \Delta I_X} = \frac{I_y/2 + \Delta I_C/2}{I_y/2 - \Delta I_C/2} \tag{38}$$

with a little bit of algebra,

$$\Delta I_C = \frac{\Delta I_x \cdot I_y}{I_x} \tag{39}$$

The output current is proportional to the product of the X input difference current ΔI_x and the Y input current, and inversely proportional to the X static current I_x, which can be seen to determine the scale factor as a linear 2-quadrant multiplier (bipolar ΔX input and unipolar Y input). The circuit can also function as a two-quadrant divider, with I_y constant, a unipolar denominator (I_x), and a bipolar numerator (ΔI_x). This linearized multiplier (Figure 9) has outstanding performance, and it represents a great improvement over the simple differential multiplier in the following ways.

1. Wide bandwidth: the circuit is basically "current-mode." At current levels of several mA, bandwidths over 100MHz can be obtained. At the lower current levels (< 1mA) normally used in multipliers, bandwidths of 1 to 10 MHz are readily achieved.

2. Excellent linearity: (39) indicates that the input-output relationship is exact for multiplication. In practice, there are

some small errors, < 1%, that will be discussed later. Nevertheless, it is greatly improved over the unlinearized multiplier.

3. Excellent temperature stability: (39) indicates that the input-output relationship is independent of temperature. In a practical circuit, there will be some slight temperature dependence due, in part, to the change in β of transistors with temperature (we have assumed β effects negligible in arriving at (39)). Changes in gain with temperature can be held to 0.02%/°C or less – more than an order-of-magnitude improvement over the simple differential multiplier (0.3%/°C).

4. Wide dynamic range: Since the X (base) input is linearized, the ratio of X input currents can be varied over a range almost equal to $-I_x < \Delta I_x < I_x$, allowing much greater input signals than the differential pair.

As a consequence of these advantages, the linearized "gain cell" has become almost universally accepted as a general-purpose multiplier building-block. With slight modification, it can be used directly as a 2-quadrant multiplier circuit.

Two-Quadrant Multiplier

The circuit of Figure 10 is an example of a workable 2-quadrant multiplier. The differential X input current is obtained from a differential pair Q6, Q7 with emitters coupled by resistor R1. Constant-current sources Q8, Q9 provide the I_x bias to the emitters of Q6, Q7. The 100kΩ emitter resistor R1 determines the differential X current, ΔI_x, per volt of input, V_x.

The X input current drives the emitters of the diode-connected transistors Q2A-B, rather than the collectors (or anodes) as in the circuit of Figure 9. This "inverted" connection is much easier to drive, since the emitters present low impedance and readily accept the current from the X input stage, Q6, Q7. The only practical difference between the "inverted" circuit and the basic current cell is that the output will also be inverted (i.e., "180° out of

phase with the input"). This is easily corrected by proper phasing of the output amplifier.

The Y input current is derived from the closed-loop controlled current source A1-Q5. If Q5 has very high β (> 400), then the collector current of Q5 will be V_y/R_2, with negligible error. Diode D1 protects the base-emitter junction of Q5 from breakdown, in the event of positive Y input voltage. The differential output current (between the collectors of Q1A-Q1B) is converted to a single-ended voltage by the dynamic bridge R3, R4, R5, R6, and A2. The resistances must be very closely matched (0.1%) to minimize output voltage errors due to changing common-mode input voltage with the Y input signal.

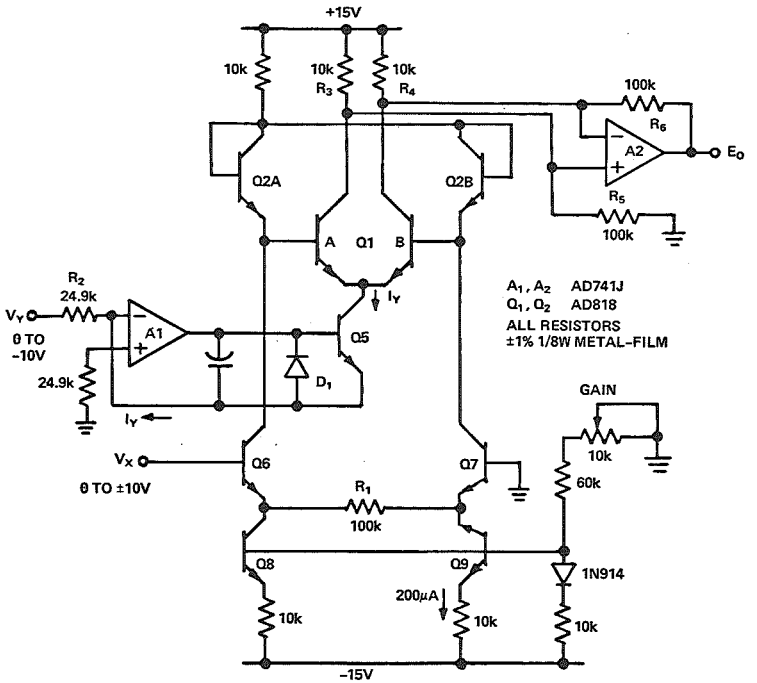


Figure 10. Practical 2-quadrant variable-transconductance multiplier

The two-quadrant multiplier is especially useful where very low feedthrough on one input is required. With the Y input at zero, the output is effectively disconnected from the input, providing at

least 80 dB attenuation of any X input signal. Along with this advantage goes a disadvantage: as the Y input is reduced in magnitude, the current in Q1A and Q1B decreases, and the bandwidth of the circuit is reduced.

Four-Quadrant Multiplier

The basic two-quadrant linearized multiplier circuit can be extended to operate in 4 quadrants, accepting bipolar signals on either the X or Y inputs. This is accomplished by adding a second differential pair, Q3A-B, with bases connected in parallel with the bases of Q1, as shown in Figure 11. The collectors of the added pair are cross-connected to the collectors of Q1A-B. The single-ended Y current source of the 2-quadrant multiplier is replaced by a differential current source, Q10, R2, Q11, identical to the X current source.

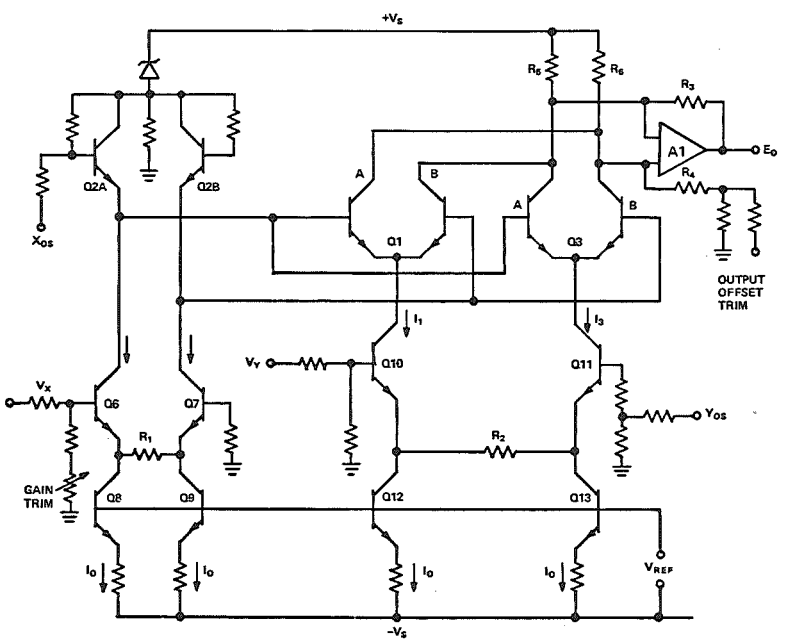


Figure 11. 4-quadrant variable-transconductance multiplier

One output of the paired Y current source is connected to the emitters of Q1A-B, the other to the emitters of Q3A-B. V_y now varies the ratio of the currents through the differential pairs, Q1A-B, and Q3A-B, and therefore controls their relative gains. For example, if Y = 0, then $I_1 = I_3$, and the gains of the two pairs are equal. Since their collectors are cross-coupled (bases in parallel), the outputs subtract, so there will be zero net gain for a signal on the X input. In this "balanced" condition, the X input experiences null suppression

$$E_o = V_x \cdot 0 = 0 \tag{40}$$

if $V_y = 0$.

If a non-zero voltage is applied to the Y input, then the currents I_1 and I_3 will be unbalanced

$$I_1 = I_{10} + V_y/R_2 \tag{41}$$

$$I_3 = I_{30} - V_y/R_2 \tag{42}$$

This unbalance allows an X input signal to appear at the multiplier output, since the gains of pairs Q1A-B and Q3A-B no longer cancel. For a positive Y input, I_1 will be greater than I_3, and the gain of Q1A-B will predominate; this will produce a positive output voltage (for positive X). On the other hand, the gain of Q3A-B predominates for negative Y inputs, causing a negative output voltage for a positive X input, or a positive output voltage for a negative X input.

The signal transfer operation from Y input to output is analogous to that in the 2-quadrant multiplier. If the X input is zero, and transistor pairs Q1, Q2, Q3 are matched, there will be zero output for any value of Y, since the change in currents I_1 and I_3 will divide equally between the sides of Q1A-B and Q3A-B.

$$E_o = 0 \cdot V_y = 0 \tag{43}$$

The overall output-input relationship of the multiplier can be developed from (39) as follows ($I_o = I_x$). The output of Q1A-B is

$$\Delta I_{C_1} = \frac{\Delta I_x I_1}{I_o} \tag{44}$$

Similarly, for Q3A-B,

$$\Delta I_{C_3} = \frac{\Delta I_x I_3}{I_o} \tag{45}$$

Since the collectors of Q1A-B and Q3A-B are cross-coupled, the output currents will subtract. The difference is ΔI_c:

$$\Delta I_c = \Delta I_{C_1} - \Delta I_{C_3} \tag{46}$$

$$\Delta I_c = \frac{\Delta I_x}{I_o} (I_1 - I_3) \tag{47}$$

Substituting for I_1 and I_3 from (41) and (42)

$$\Delta I_C = \frac{\Delta I_x}{I_o} (I_{10} + V_y/R_2 - I_{30} + V_y/R_2) \tag{48}$$

Since $I_{10} = I_{30}$

$$\Delta I_C = 2 \frac{\Delta I_x}{I_o} \cdot \frac{V_y}{R_2} \tag{49}$$

The net differential output current will be converted to a single-ended output voltage by A1 and R3, R4, R5, R6, just as for the two-quadrant multiplier

$$E_o = \Delta I_c R_3 \tag{50}$$

(50) can be reduced to

$$E_O = \frac{2R_3}{R_1 R_2 I_O} V_X \cdot V_y \tag{51}$$

$$-I_o R_2 < V_y < I_o R_2 \tag{52}$$

$$-I_o R_1 < V_x < I_o R_1 \tag{53}$$

The scale factor of the multiplier is set by $R_3/R_1 R_2 I_o$, which has the required dimension of V^{-1}.

Performance of the 4-Quadrant Transconductance Multiplier

The overall performance of the variable-transconductance multiplier is excellent, making it the most popular type of electronic analog multiplier. The reasons for the success of the Gilbert linearized multiplier are threefold:

1. Good accuracy: Overall error of less than ±1% of full scale (100mV in 10V) is easily achieved. Errors are proportional to input levels and tend towards zero as the inputs go to zero (except for dc offsets, which can be adjusted to zero). In fact, the "nonlinear" errors can be bounded by a simple linear equation

$$\epsilon(X,Y) = \frac{\epsilon_x}{100} V_x + \frac{\epsilon_y}{100} V_y \tag{54}$$

where

ϵ_x = specified % nonlinearity on X input

ϵ_y = specified % nonlinearity on Y input

2. Wide bandwidth: up to 10MHz for voltage-output multipliers, over 100MHz with current output. Bandwidth is independent of signal level or input path (X or Y), for bandwidths < 10MHz.

3. Relative simplicity and low cost: The variable-transconductance multiplier can be constructed using "discrete" components, or it can be made in "monolithic" form. In either case, the inherent simplicity and consistency of performance of the circuit make it less expensive than any other four-quadrant multiplier. We will discuss each of these factors in more detail, to relate them to the practical circuit and limitations of the components.

Factors Affecting Accuracy of the Transconductance Multiplier

So far, in our discussion of the variable-transconductance multiplier, we have assumed that the transistors obey the ideal junction equation, are perfectly matched, and have infinite current gain. We also assumed that all currents in symmetrical paths are equal, except for differences caused by injection of signals. In a practical circuit, the transistors and resistors are not "ideal" and are never (well, hardly ever) perfectly matched. These mismatches and departures from "ideal" behavior give rise to linear errors (input and output offsets, scale-factor errors) and nonlinear errors (2nd and 3rd harmonic distortions).

The linear errors can be theoretically adjusted to zero, and practically adjusted to negligible levels, as discussed in the introduction to this chapter. Four trim points are indicated in Figure 11:

1. X Offset: used to adjust linear Y feedthrough to zero

2. Y Offset: Adjusts linear X feedthrough to zero

3. Output Offset

4. Scale Factor, or "gain"

Nonlinear Errors

The primary source of nonlinearity in the variable-transconductance multiplier is current unbalance or offset-voltage mismatch between the two differential pairs, Q1A-B and Q3A-B. A 500μV mismatch between the offsets of these pairs will cause 1% (of full-scale) nonlinearity and feedthrough on the X input. This nonlinearity will be proportional to V_x^2, as illustrated in Figure 12. Fortunately, since it is possible to "match-up" pairs in a discrete circuit, or lay out "identical" transistors in an integrated circuit, for an average offset mismatch less than 500μV, the X nonlinearity is usually less than 1%.

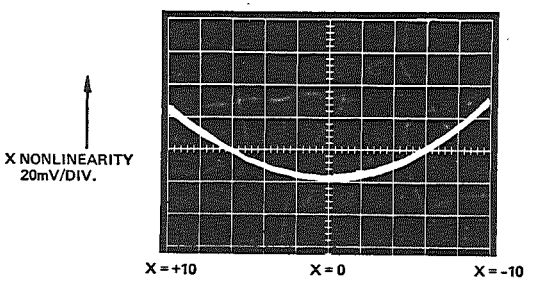


Figure 12. Parabolic X nonlinearity

Because the second-order X nonlinearity is relatively independent of the Y input signal amplitude, the X^2 nonlinearity can be significantly reduced by cross-coupling a fraction of the X input signal into the Y input, as will shortly be described.

Another source of potential X^2 nonlinearity is unbalance of the currents through the diode-connected transistors, Q2A, Q2B, when $V_x = 0$. The currents can be equalized by using closely-matched resistors in the X current sources.

The X input can exhibit considerable third-order (S-shape) nonlinearity under some conditions, as Figure 13 illustrates. The cubic distortion is caused by an ohmic component of emitter resistance in the differential pairs Q1A-B, Q3A-B. The ohmic (or constant) resistance decreases the transconductance from the

theoretical value of qI_c/kT and thus causes nonlinearity. Since high-speed multipliers are operated at high current, these ohmic nonlinearities will be seen to force a speed-vs.-accuracy tradeoff.

The Y input of the transconductance multiplier has relatively low nonlinearity, typically ±0.1% to ±0.2%. The offset-voltage mismatch in the differential pairs, Q1A-B and Q3A-B, and the initial Y input currently unbalance have negligible effect on the Y nonlinearity and feedthrough, so it is consistently low.

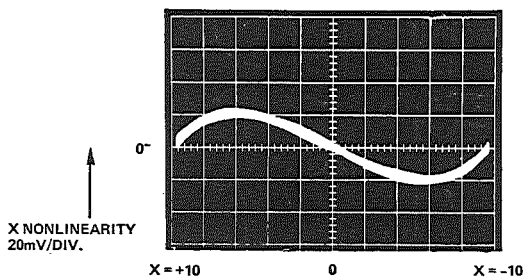


Figure 13. Cubic X nonlinearity

The X and Y input-voltages to differential-current converters can introduce nonlinearity if the emitter resistors are not large compared to kT/qI_c (26Ω at I_c = 1mA, T = 300°K).

Dynamics of the Transconductance Multiplier

The transconductance multiplier has wide bandwidth and fast transient response, since it is basically a current-mode circuit. Current-output bandwidths of 100MHz and greater can be obtained by operating the multiplier transistors at emitter currents of 10mA or more. However, circuits designed for the best dc accuracy operate at much lower currents: 10μA to 1mA, with bandwidths of 1 to 10MHz. The bandwidth limitation is primarily due to the output amplifier, which converts the difference of the collector currents to an output voltage.

The bandwidth of the 4-quadrant variable-transconductance multiplier is the same for the X or Y input, and is independent of signal level, except for the slew-rate limit of the output amplifier.

Linearizing the Transconductance Multiplier

The 4-quadrant variable-transconductance multiplier circuit, Figure 11, has predominantly second-order nonlinearity and feedthrough on the X input, for the reasons discussed above. The nonlinearity on the Y input is usually negligible compared to the "X" distortion. If all of the first-order errors – linear feedthrough, output offset, scale-factor error – are adjusted to zero, then the multiplier input-output relationship can be closely approximated by

$$E_o = KV_x V_y \pm \delta V_x^2 f(V_y) \qquad (55)$$

If the nonlinear term, $\delta V_x^2 f(V_y)$ is independent of (or not strongly influenced by) V_y, then the δV_x^2 nonlinearity could be cancelled by adding or subtracting a portion of the X input signal to the Y input, as shown in Figure 14.

Fortunately, the δX^2 nonlinearity is not a strong function of the Y input (i.e., $f(Y)$ is nearly constant), so the cancellation scheme works reasonably well in practice. Usually, the X^2 component of feedthrough (Y = 0) can be reduced to less than 0.1% of full scale (60dB null suppression), and the X nonlinearity (V_y = 10V) can be reduced by a factor of 2, with a corresponding reduction of overall error.

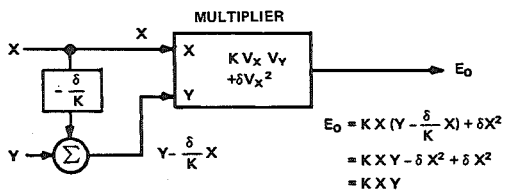


Figure 14. Improving linearity by cancelling second-harmonic distortion

A method of applying the X linearization to a multiplier is shown in Figure 15. This approach relies on fairly low source resistances, 100Ω or less, and the availability of both + and – (differential) Y inputs. On many multipliers (e.g., all Analog Devices multipliers of this type), the Y_o trim terminal can be used as the –Y input, for the linearization circuit (but not always with the same sensitivity).

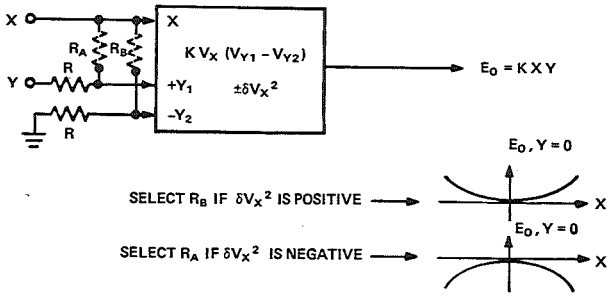
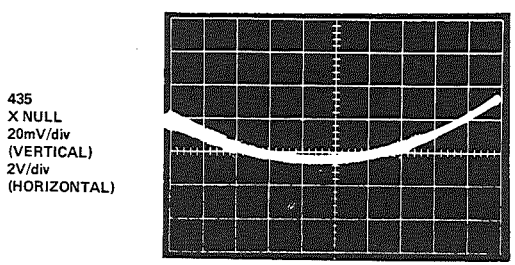


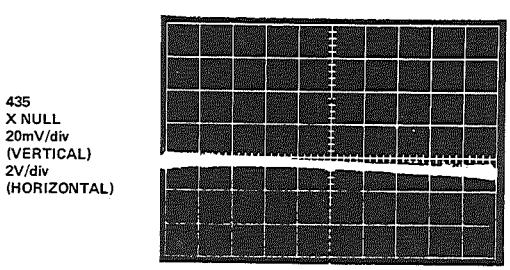
Figure 15. Applying linearization to a multiplier

Figures 16 to 18 show the results of applying the linearization to a multiplier. Note especially the reduction in both low-frequency and high-frequency feedthrough.

The cross-coupling linearization technique could be applied to the Y input, but the Y nonlinearity is generally already so low that "diminishing returns" sets in.

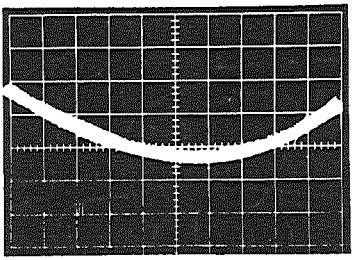


a. Before

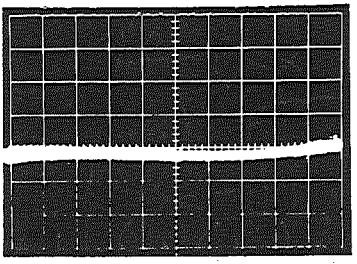


b. After

Figure 16. Effect of X-linearization of a transconductance multiplier X = ±10V, Y = 0, 20mV/div. vertical scale

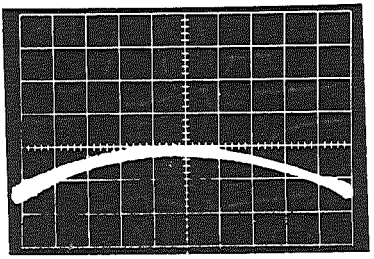


a. Before

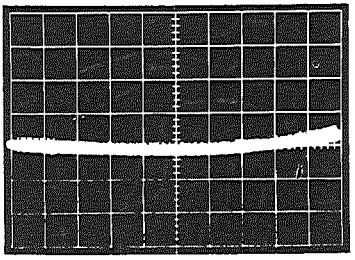


b. After

Figure 17. Effect of X-linearization of the same multiplier as Figure 16. X = ±10V, Y = +10V, 20mV/div. vertical scale



a. Before



b. After

Figure 18. Effect of X-linearization of the same multiplier as Figure 16. X = ±10V, Y = −10V, 20mV/div. vertical scale

The cross-coupling linearization technique can be applied to any multiplier that has second-order nonlinearity on one or both inputs. The amount of reduction of overall error will depend on the degree to which the nonlinearity on one input is independent of the signal level at the other input.

In general, complete cancellation of the second-order nonlinearity on one input will occur for only one value of the other input. For example, the second-order component of X *feedthrough* (X = ±F.S., Y = 0) may be completely cancelled, but the second-order X *nonlinearity* will be partially cancelled, or may even increase under some circumstances.

LOG-ANTILOG MULTIPLIERS

The log-antilog multiplier is an electrical analog of the C and D scales on a slide rule, since it forms the product of two or more variables by addition of their logarithms

$$X \cdot Y = \epsilon^{(\ln X + \ln Y)} \tag{56}$$

The accuracy and temperature-stability of log-antilog multipliers is excellent, approaching the performance of the more-complex pulse-modulation multipliers. Errors of less than 0.25% of full-scale, with drifts of 0.01%/°C are readily achieved. Although operation of the basic log-antilog multiplier is restricted to one quadrant (typically the first quadrant), it can be offset to operate in four quadrants, as will be explained later. (The offsetting technique, or absolute-value-sign-magnitude technique mentioned earlier, can be applied to any 1-quadrant multiplier.)

Circuit Description

The log-antilog multiplier circuit is closely-related to the transconductance multiplier circuit, in that it relies on the logarithmic properties of silicon-junction transistors.

The basic building block of the log-antilog multiplier is the Paterson diode, or "transdiode" log amplifier, described in detail in Chapter 3-1. This circuit makes the best use of the log properties of the transistor (especially at low currents) and is also the easiest to combine into more-complex circuits, such as an analog multiplier.

The operation of the basic transdiode log amplifier, Figure 19, will be reviewed here for convenience.

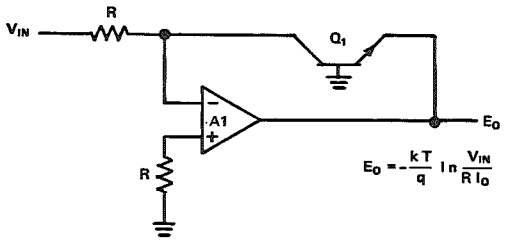


Figure 19. Basic transdiode log amplifier

If we assume that operational amplifier A1 has zero offset current and voltage, then the collector current of Q1 will be V_{in}/R. The output of A1 drives the emitter of Q1, so that the emitter-base voltage of Q1 is

$$E_o = V_{EB} = -\frac{kT}{q} \ln \frac{V_{IN}/R}{\alpha_N I_{ES}} \tag{57}$$

$\alpha_N \cong 1$

I_{ES} = emitter saturation current, $\sim 10^{-14}$ A

Let $\alpha_N I_{ES} = I_o$

The output of A1 is therefore proportional to the logarithm of the input voltage, and also variable with temperature, both through kT/q and through I_o. The temperature-dependence will be cancelled when the log amplifier is used in a multiplier circuit.

A schematic of a two-input log-antilog multiplier can be seen in Figure 20. The two inputs, V_x, V_y, drive two independent trans-

diode log amps, A1-Q1A and A2-Q2A. The base of Q2A is at ground potential, while the base of Q1A is tied to the emitter of Q2A. Therefore, the voltage at the emitter of Q1A will be proportional to the sum of the logs of V_x and V_y, as follows

$$V_{EB_{2A}} = -\frac{kT}{q} \ln \frac{V_x}{R_x I_{o_{2A}}} \tag{58}$$

$$V_{EB_{1A}} = -\frac{kT}{q} \ln \frac{V_y}{R_y I_{o_{1A}}} \tag{59}$$

$$V_3 = V_{1_A} + V_{2_A} \tag{60}$$

$$-V_3 = \frac{kT}{q} \left(\ln \frac{V_x}{R_x I_{o_{2A}}} + \ln \frac{V_y}{R_y I_{o_{1A}}} \right) \tag{61}$$

$$V_3 = -\frac{kT}{q} \ln \frac{V_x \cdot V_y}{R_x R_y I_{o_{2A}} I_{o_{1A}}} \tag{62}$$

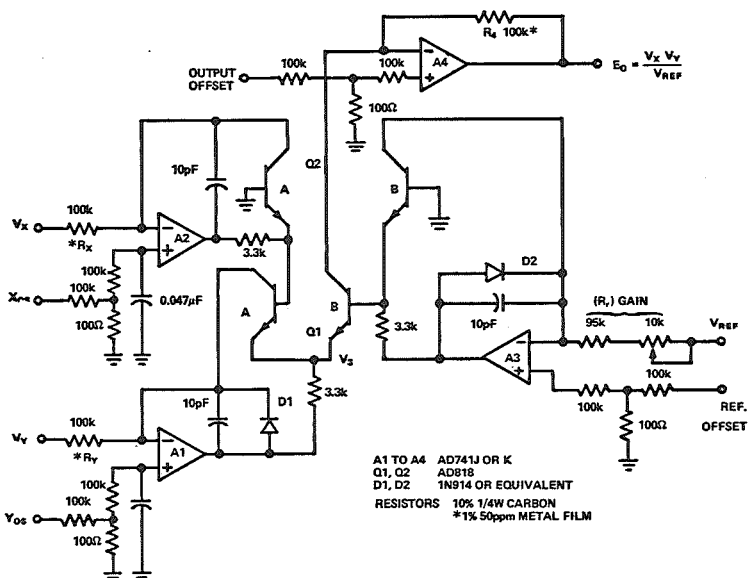


Figure 20. Log-antilog multiplier

The next step is to take the antilog of V_3, in a way that will cancel the temperature-dependence. Note that V_3 appears across the base-emitter circuits of the "B" sides of Q1 and Q2 in series.

$$V_3 = V_{EB1A} + V_{EB2A} = V_{EB1B} + V_{EB2B} \tag{63}$$

Assuming a constant reference input, V_{REF}

$$V_{EB2B} = -\frac{kT}{q} \ln \frac{V_{REF}}{R_r I_{o_{2B}}} \tag{64}$$

Solving (63) for V_{EB1B}

$$V_{EB1B} = V_{EB1A} + V_{EB2A} - V_{EB2B} \tag{65}$$

$$V_{EB1B} = \frac{kT}{q} \ln \frac{V_x V_y R_r I_{o_{2B}}}{V_{REF} R_x R_y I_{o_{2A}} I_{o_{1A}}} \tag{66}$$

For $V_{EB1B} > 100\text{mV}$, the collector current is exponentially related to the base-emitter voltage,

$$I_{C1B} = I_{o_{1B}} \epsilon^{qV_{EB1B}/kT} \tag{67}$$

Combining (66) and (67),

$$I_{C1B} = I_{o_{1B}} \exp\left\{\frac{q}{kT} \frac{kT}{q} \ln \frac{V_x V_y R_r I_{o_{2B}}}{V_{REF} R_x R_y I_{o_{2A}} I_{o_{1A}}}\right\} \tag{68}$$

$$I_{C1B} = \frac{I_{o_{1B}} I_{o_{2B}} V_x V_y R_r}{I_{o_{1A}} I_{o_{2A}} V_{REF} R_x R_y} \tag{69}$$

If transistors Q1 and Q2 are monolithic duals, the I_o terms cancel

$$\frac{I_{o_{1B}}}{I_{o_{1A}}} = \frac{I_{o_{2B}}}{I_{o_{2A}}} = 1 \tag{70}$$

The output amplifier A4 and feedback resistor R4 will convert I_{C1B} to a voltage

$$E_o = R_4 \cdot I_{C1B} \tag{71}$$

$$E_o = \left\{\frac{R_4 R_r}{R_x R_y}\right\} \frac{V_x V_y}{V_{REF}} \tag{72}$$

$$V_x, V_y \geqq 0, V_{REF} > 0$$

Thus, the circuit of Figure 20 will multiply and divide with a scale factor that is independent of temperature (to the degree that the resistances track, which can be excellent). The output-input transfer function is also independent of the transistor current gains (β).

Performance of the Log-Antilog Multiplier

The actual performance of a practical log-antilog multiplier closely approaches the ideal as given. The static accuracy error and temperature drift are very low. The primary sources of static errors in the log-antilog multiplier are:

1. Transistor log conformity errors: For X or Y inputs near full-scale, the current in the log transistors, Q1A, Q2A, is about 100μA. At this current level, the effects of ohmic emitter resistance become noticeable and will result in about 0.1% nonlinearity. Limiting the full-scale current to 100μA prevents greater nonlinearity.

2. Input current and offset voltage of the operational amplifiers, A1-A4 introduce "offset" errors at the X, Y, and reference inputs and signal outputs. Of the order of about 5mV, these offsets can be easily trimmed to less than 0.1mV by offsetting the reference (i.e. "+") inputs of amplifiers A1-A4.

3. Resistance tolerance: this causes an error in the scale factor, which can be adjusted by the "gain" pot.

4. Offset voltages in transistor pairs Q1A-B, Q2A-B cause scale-factor error of 4% per millivolt of offset. Gain-trim removes this error.

The temperature stability of the log-antilog multiplier is excellent. The scale-factor drift will be about 0.01%/°C with 50ppm resistors for R_x, R_y, R_r, and R_4. The input and output offset drift is determined by the op amps, and so will be about 20μV/°C for V_{REF} = 10V. For lower values of V_{REF}, the input offset drift will be multiplied by $10/V_{REF}$ at the output.

As is true for other log circuits, the bandwidth of the log-antilog multiplier is proportional to the magnitudes of the inputs. This effect is due to decreased loop gain, with a corresponding increase in loop time constant, at reduced currents. Typically, the multiplier will have 100kHz bandwidth for 10V inputs, decreasing to 1kHz at 0.1V.

The total error of the log-antilog multiplier will be less than ±10mV (out of 10V) when the input and output offsets and scale factor have been adjusted. The error will decrease with decreasing inputs and will typically be less than 0.1% of output, plus a fixed output offset, over the 0 to +10V output range.

Offsetting a 1-Quadrant Multiplier for Operation in 4 Quadrants

Any 1-quadrant multiplier may be made to operate in 4 quadrants, by properly offsetting the inputs and output. The multiplier itself remains a 1-quadrant device, operating about a bias point

centred within its usual unipolar range. The offsetting scheme can be developed by considering the effect of an offset on the X and Y inputs.

$$E_o = K_1(V_x + X_{os})(V_y + Y_{os}) \tag{73}$$

$$E_o = K_1(V_xV_y + X_{os}V_y + V_xY_{os} + X_{os}Y_{os}) \tag{74}$$

The effect of the input offsets is to introduce an output offset $X_{os}Y_{os}$ and two linear feedthrough terms, $X_{os}V_y$ and V_xY_{os}. If $X_{os} > |V_x|_{max}$ and $Y_{os} > |V_y|_{max}$, then V_x and V_y can be either positive or negative, and E_o in (74) will still be positive. If the undesired terms – those other than $K_1V_xV_y$ – are subtracted from (74), then E_o can be positive or negative: the desired result.

$$E_o = K_1V_xV_y + K_1(X_{os}V_y + V_xY_{os} + X_{os}Y_{os}) - K_0 - K_2V_x - K_3V_y \tag{75}$$

If $K_0 = K_1X_{os}Y_{os}$, $K_2 = K_1Y_{os}$, and $K_3 = K_1X_{os}$, then

$$E_o = K_1V_xV_y \tag{76}$$

for V_x and V_y of any polarity.

The offsetting and input coupling are shown in the block diagram, Figure 21. This offsetting scheme can be used with the log-antilog multiplier shown in Figure 20. It adds considerable complexity to the initial adjustment of the multiplier, and the reference voltage (V_{REF}) must be constant, or the "feedthrough" and offset will not stay cancelled. In addition, the 4-quadrant log-antilog multiplier will be slower for negative X and Y inputs (less current in the log transistors) than for positive inputs, making the scheme less effective for waveforms symmetrical about zero.

In spite of these shortcomings, the offset multiplier can be adjusted for errors of 0.1% of full scale, with nonlinearities of the order of 0.05%.

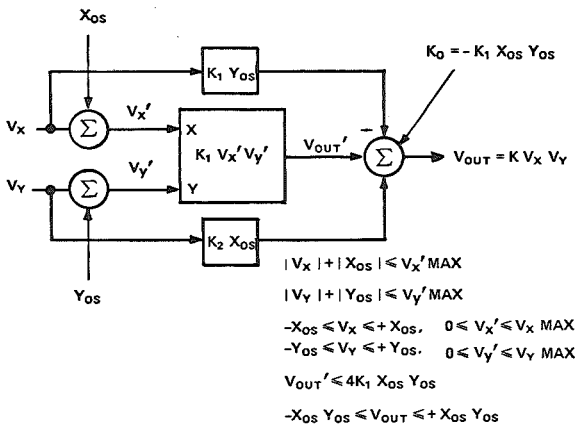


Figure 21. Offsetting 1-quadrant multiplier for 4-quadrant operation. Scale factor change in multiplier produces output offset and feedthrough shift at summed output.

PULSE-MODULATION MULTIPLIERS

The pulse-modulation multiplier operates on the principle that the area under a rectangular pulse is proportional to the product of the pulse amplitude and pulse duration (Figure 22).

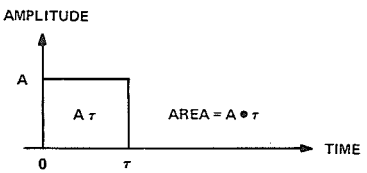


Figure 22. Basic principle of pulse modulation

It then follows that the average magnitude of a train of rectangular pulses is proportional to the product of the pulse amplitude and ratio of *on* time to period (duty cycle). (Figure 23).

A multiplier may be constructed using this technique. One input is used to control the amplitude of the pulse, the other the duty cycle. The resulting pulse train is low-pass filtered, yielding the average value, which is proportional to the product of the two inputs. A block diagram of a simple, two-quadrant pulse-modulation multiplier is shown in Figure 24.

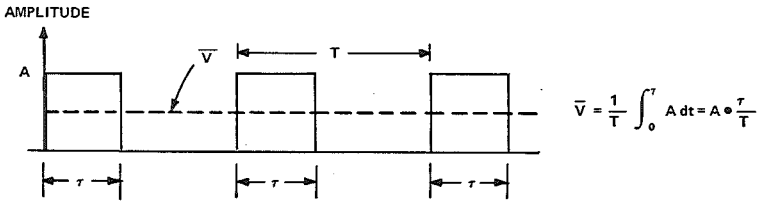


Figure 23. Average value of train of square pulses is proportional to product of amplitude and duty cycle

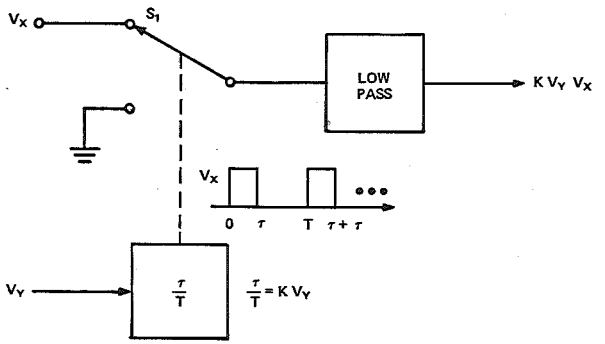


Figure 24. Two-quadrant pulse-modulated multiplier block diagram

The Y input controls the duty cycle of a pulse train, which in turn drives a switch S1. The switch alternates between the input and ground, dwelling at the input for a time proportional to the duty cycle. The output of the averaging filter will be proportional to the product $V_x V_y$. The X input can be either positive or negative, but the Y input is limited to positive values, since the duty cycle, τ/T, cannot be "negative."

The pulse-modulation technique can be extended to four-quadrant operation by using a "balanced" switching and duty-cycle generator, so that a zero Y input results in a 50% duty cycle, as the block diagram in Figure 25 illustrates.

Performance of the Pulse Modulation Multiplier

Pulse-width-pulse-height modulation is inherently the most accurate method of performing analog multiplication. Errors of less than 0.1% of full scale and nonlinearities of 0.02% can be readily

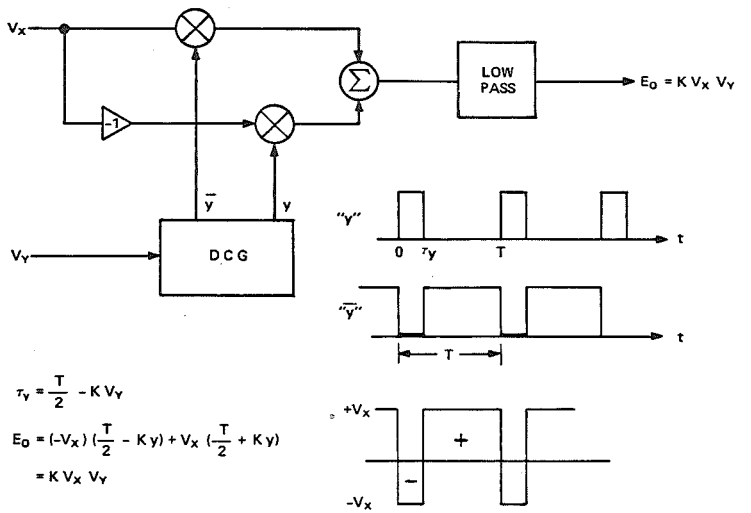


Figure 25. Four-quadrant pulse-modulation multiplier

achieved. The high accuracy is the result of using the nonlinear elements (FET's or transistors) as switches, rather than relying on the exact relationship between their "gain" and input voltage.

Though the pulse-modulation multiplier is ideally 100% accurate, there are several sources of error that limit the accuracy of practical multipliers. Most of the limitations arise from the non-ideal behavior of real switches and duty-cycle generators. However, there is one limitation inherent in the modulation technique itself: the signal frequency must be much less than the averaging frequency to allow sufficient averaging time. Analog averaging will always leave a finite (but usually negligible) ripple component on the output. Generally, the carrier/frequency should be at least 10 to 100 times the signal frequency.

The carrier frequency is in turn limited by component-determined errors:

1. Capacitance between the switch-control terminal and the signal path, e.g., gate-to-channel capacitance of a FET. This capacitance couples a charge into the signal path each time the switch is turned on or off, resulting in an offset voltage. The offset may change with signal level, resulting in a non-

linearity. The "dumped charge" effect can be minimized by using low-capacitance switches or lower carrier frequency to reduce the average charge (current) coupled into the signal path.

2. On-off resistance of switches: FET or CMOS switches (even reed relays) have measurable *on* and finite *off* resistance. As long as the ratio of *off* to *on* is high (> 10,000), errors from this source will be small. If the ratio is low, then some of the input signal will leak into the output when the switch is *off*, increasing the feedthrough.

3. Linearity of the duty-cycle generator: The variable duty-cycle pulse generator is potentially the most significant source of nonlinearity. The controlling input, i.e., V_y, must determine the ratio of *on* to *off* time precisely, over a fairly wide range, especially in a 4-quadrant multiplier. As the duty cycle is reduced, any fixed timing errors, e.g., delays, become a more-significant portion of the *on* time, as shown in Figure 26, introducing nonlinearity.

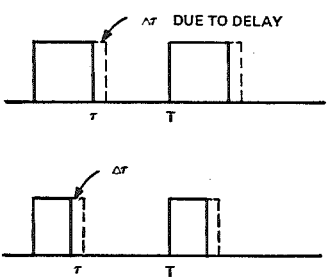


Figure 26. Nonlinear error produced by fixed delay asymmetry in duty-cycle-generator-plus-switch. $\Delta\tau$ is the same whether τ is large or small, a deviation from proportionality.

The nonlinearity of the duty-cycle generator can be reduced to an arbitrarily-low level by using a closed-loop circuit, illustrated in the block diagram of Figure 27.

The input voltage, V_y, is compared to the average value of a chopped reference voltage. The output of the comparator controls

the *on* to *off* time of the chopper, so that the average value of the voltage out of the chopper will equal V_y in the steady-state.

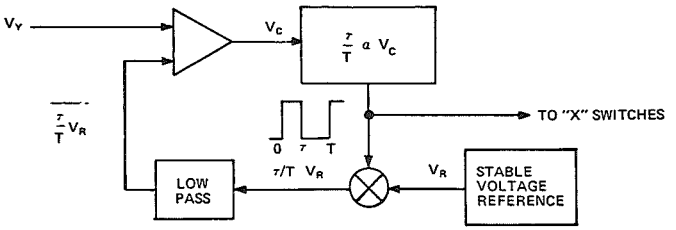


Figure 27. Closed-loop duty-cycle generator

The relationship between duty cycle, τ/T, and comparator output voltage is not important, as long as it is single-valued. The linearity of the overall system is determined by the threshold accuracy of the comparator and the averaging time. Nonlinearities of less than 0.01% can be achieved by this approach.

MULTIPLIER SPECIFICATIONS

Perhaps the best way of gaining an understanding of multiplier specifications and their dependence on multiplier circuit design is to review the specifications as set forth in a multiplier data sheet. The accompanying comparative table lists specifications for modular multipliers using the three techniques discussed in this chapter: transconductance (432, 429), pulse-modulation (427), and log-antilog (434).

The 432 is a low-cost 4-quadrant transconductance multiplier, with 1%-2% error, good bandwidth, and small size. It is comparable to the integrated-circuit AD533 with external trims, drawing a little more power than the internally-trimmed AD532.

The 429 is a fast (10MHz), 4-quadrant transconductance multiplier with low error (0.5%) and low nonlinearity. It is a no-compromise discrete design that uses monolithic dual transistors in the multiplier section and a fast discrete-component output amplifier.

The 427 is a high-accuracy (0.25% error) pulse-modulation 4-quadrant multiplier. The use of a high-frequency carrier (3MHz)

allows a signal bandwidth of 100kHz, 100 to 1000 times greater than the usual bandwidth for pulse-modulation multipliers.

The 434 is a 1-quadrant log-antilog multiplier that combines high accuracy (0.25% error) and versatility, since both multiplication and division can be performed simultaneously.

SPECIFICATIONS (pp. 246–247)

The first four lines of the comparative-specification table* summarize the salient features of the multiplier, to guide the reader immediately to the ones most likely to fill the needs of his application. The "Aids for the Designer," Chapter 4–4, provides considerable detail on multiplier selection, so it will not be covered here.

MULTIPLICATION CHARACTERISTICS

This block of specifications deals with overall static errors from all sources that are covered in detail in the succeeding Specification blocks (Offset, Scale Factor, Nonlinearity, Feed-through).

Output Function: Defines the ideal functional relationship between the two input voltages, V_x, V_y, the output voltage E_o, and the scale constant, V_r. All errors are defined as deviations from this transfer function and are specified as percentages of full scale, 10V. A typical transfer function is

$$E_o = \frac{V_x V_y}{10V} \tag{77}$$

For $V_x = V_y = 10V$,

$$E_o = \frac{10 \times 10}{10} = 10V \tag{78}$$

*This table is an abbreviated example involving a few contrasting modular multiplier types, with information valid as of Summer 1973. For further information on these or the many more types available within each class, as well as the many IC types, it is suggested that the reader consult the most recent edition of the Analog Devices *Product Guide* or supplements.

MULTIPLIERS/DIVIDERS (Discrete)

SPECIFICATION SUMMARY (Typical @ 25°C and ±15VDC unless otherwise specified)

MULTIPLICATION TECHNIQUE	TRANSCONDUCTANCE	
Model[1]	Economy 432J (432K)	Accurate Wideband 429A (429B)
Price *1-9	$29 ($45)	$109 ($139)
Price 10-24	$27 ($43)	$104 ($129)
Full Scale Accuracy[2]	2% (1%)	1% (0.5%)
Divides and Square Roots	YES	YES
Multiplication Characteristics		
Output Function	XY/10	XY/10
Error, Internal Trim (±)	2%(1%) max	1%(0.5%) max
Error, External Trim (±)	1.0% (0.6%)	0.7% (0.3%)
Accuracy vs. Temperature (±)	0.06%/°C (0.04%/°C)	0.05%/°C (0.04%/°C max)
Accuracy vs. Supply (±)	0.1%/%	0.03%/%
Warm up Time to Specifications	1 min	1 sec
Output Offset (±)		
Initial	20mV (25mV max)	20mV (10mV) max
Average vs. Temperature 0°C to +70°C	2mV/°C (1mV/°C)	2mV/°C (1mV/°C max)
Average vs. Supply	10mV/%	1mV/%
Scale Factor (±)		
Initial Error	1%(0.5%)	0.5% (0.25%)
Non Linearity (±)		
X Input (X = 20V p-p, Y = ±10VDC)	0.8% (0.6% max)	0.5% (0.2%) max
Y Input (Y = 20V p-p, X = ±10VDC)	0.4% (0.3% max)	0.3% (0.2%) max
Feedthrough		
X = 0, Y = 20V p-p 50Hz	80mV (50mV) p-p max	25mV (10mV) p-p max
with external trim	30mV p-p	8mV (5mV) p-p
Y = 0, X = 20V p-p 50Hz	120mV (100mV) p-p max	50mV (15mV) p-p max
with external trim	N/A	35mV (10mV) p-p
Feedthrough vs. Temperature, each input	1mV p-p/°C	2mV p-p/°C
Bandwidth		
-3dB Small Signal	1MHz	10MHz
Full Power Response	700kHz	2MHz min
Slew Rate	45V/μsec	120V/μsec min.
Small Signal Amplitude Error (±)	1% @ 40kHz	1% at 300kHz min
Small Signal Vector Error (±)	1% @ 10kHz	1% at 50kHz min
Settling Time for ±10V Step	1μsec to 2%	0.5μsec to 1%
Overload Recovery	3μsec	0.15μsec
Output Noise		
5Hz to 10kHz	600μV rms	500μV rms
5Hz to 5MHz	3mV rms	2.5mV rms
Output Characteristics		
Voltage at Rated Load (min)	±10V	±11V
Current (min)	±5mA	±11mA
Load Capacitance Limit	0.001μF	0.01μF
Input Resistance		
X/Y/Z Input	10MΩ/10kΩ/36kΩ	10kΩ/11kΩ/27kΩ
Input Bias Current		
X/Y/Z Input	2μA each	+100nA/+100nA/±20nA
Maximum Input Voltage		
For Rated Accuracy	±10.1V	±10.5V
Safe Level	±Vs	±16V
Power Supply (V_s)		
Rated Performance	±15V	±14.7 to ±15.3V
Operating	±12 to ±18V	±14 to ±16V
Quiescent Current	±4.5mA	±12mA
Temperature Range		
Rated Performance	0°C to +70°C	-25°C to +85°C
Operating	-25°C to +85°C	-25°C to +85°C
Storage	-55°C to +125°C	-55°C to +125°C
Package Outline	QC-2	FA-4
Case Dimensions	1.1" X 1.1" X 0.4" 28 X 28 X 10.2mm	1.5" X 1.5" X 0.6" 38.1 X 38.1 X 15.2mm

*Summer, 1973. Price is listed here as a measure of relative cost, not primarily as a commercial inducement. Those interested further should consult recent Product Guides or

PULSE TYPES	LOG-ANTILOG
High Accuracy	
427J (427K)	**434A (434B)**
$159 ($210)	75(87)
$143 ($189)	69(77)
0.25% (0.2%)	0.5% (0.25%)
YES	YES
XY/10	YZ/X
0.25% (0.2%) max	0.5% (0.25%) max
0.15% (0.1% max)	0.3% (0.1%)
0.02%/°C max	0.02% (0.02%/°C max)
0.02%/%	0.02%/%
1 min	1 min
5 mV	2mV (2mV max)
0.2mV/°C (0.2mV/°C max)	1mV/°C (1mV/°C max)
1mV/%	1mV/%
0.1% (0.05%)	0.2% (0.1%)
0.08% (0.04%) max	0.2% (0.1%)[2]
0.08% (0.04%) max	0.2% (0.1%)[2]
20mV p-p max	+2 mV Peak Max
4mV p-p	—
20mV p-p max	+2mV Peak Max
5mV p-p	—
0.2mV p-p/°C	—
100kHz	100kHz[3]
30kHz	30kHz
2V/μsec	2V/μsec
0.1% at 4kHz	
1% at 700Hz	
20μsec to 0.1%	40μsec to 0.1%
10μsec	20μsec
50μV rms	300μV rms
1mV rms	1mV rms
±10.2V	+11V
±7mA	+5mA
0.01μF	0.01μF
10kΩ/10kΩ/33kΩ	100kΩ/90kΩ/100kΩ
±3μA/±3μA/±10μA	10nA/100nA/10nA
±10.5V	+10.5V
±16V	±16V
±14.8 to ±15.3V	±14.4 to ±15.6
±14.8 to ±16V	±10V to ± 18V
±16mA	±10mA
0°C to +70°C	-25°C to +85°C
-25°C to +85°C	-55°C to +125°C
-55°C to +125°C	-55°C to +125°C
D-2	
1.6" X 3.0" X 0.6"	1.5 X 1.5 X 0.6
40.6 X 76.2 X 15.2mm	38.1 X 38.1 X 15.2mm

NOTES:

[1]Parentheses indicate specification for the high performance (K version) model of each multiplier when it differs from the J or A version. For example, order Model 427J for 0.25% accuracy, Model 427K for 0.2% accuracy.

[2]434 is a one quadrant device: specs are for inputs between 0 and +10V only

[3]Bandwidth depends on level of input. Specs given for 10V

price lists, or the nearest Sales office, since prices are subject to change. See also Table 2 in Chapter 3-3.

A scale factor ($1/V_r$) of 1/10/V is almost universal at present, but others, such as 1/V, 1/5/V, or 1/100/V have been used. The scale factor can also be adjustable (or even variable over a wide range, as shown for the 434 log-antilog multiplier). Where the scale factor is adjustable or variable, the multiplier specifications are usually given for a 1/10/V scale factor, and deviations from these limits are elaborated as a function of scale factor.

Actual error (V) and percentage error (of 10V F.S.) are related as follows:

$$\epsilon = V_{measured} - \frac{V_x V_y}{10V} \tag{79}$$

$$\% \text{ Error} = 100 \frac{\epsilon}{10V} = 10 \cdot \epsilon \tag{80}$$

Error, Internal Trim: the maximum difference between the multiplier's actual and ideal output values for any pair of dc input voltages within the multiplier input range at 25°C without the intervention of any external adjustments. The error is expressed as a percentage of full scale (80); thus, 1% error is 0.01·10V=100mV.

The maximum error almost always occurs for full-scale inputs (±10V), as discussed in detail under nonlinearity. The error includes offset, feedthrough, nonlinearity, and scale-factor errors. This specification characterizes the "accuracy" of the multiplier.

As a practical matter, the measurement is made at the "end-points" of the four quadrants, (V_x, V_y) = (+10V, +10V), (−10V, + 10V), (−10V, −10V), (+10V, −10V).

The maximum error for the 432J is ±2%, which implies that full-scale output may be between ±9.8V and 10.2V; the 427K has one-tenth the maximum error of the 432, i.e., ±0.2% or ±20mV (untrimmed).

Error, External Trim: the error remaining after the X and Y feedthroughs and output offset have been nulled out using external potentiometers or voltage dividers. This is a measure of the irreduc-

ible component of error, approximately equal to the nonlinearity (see also *scale factor* and *nonlinearity*).

Accuracy vs. Temperature (Error vs. Temperature): The rate at which the error, as defined above, changes with temperature. It is expressed as a percentage of full scale (10V) per degree centigrade. This coefficient includes the effects of output offset drift, feedthrough drift, and scale-factor drift, and so can be used to predict the maximum error expected over a temperature range as follows (e.g., $T_H > 25°C$)

$$\text{Error(V)} = \frac{1}{10}\left\{\left|\%\ \text{error}\right|_{25°C} + \left|\frac{\Delta(\%\ \text{error})}{\Delta T}\right| (T_H - 25°C)\right\} \quad (81)$$

For example, the 429B has an error of 0.5% maximum at 25°C, and an error drift of ±0.04%/°C(max). To calculate the maximum error at 70°C:

$$\epsilon_{70°C} = \frac{1}{10}\left\{0.5 + 0.04\,(70 - 25)\right\} \quad (82)$$

$$\epsilon_{70°C} = 0.1(0.5 + 1.8) = 0.23\text{V} = \pm 230\text{mV} \quad (83)$$

The error calculated in this fashion represents error at or near full-scale output, where error due to scale-factor drift predominates. If both inputs are less than 1/3 of full scale (1/10 full-scale *output*) the drift is considerably less, since output offset drift predominates.

Accuracy vs. Supply (Error vs. Supply): the sensitivity of the multiplier output voltage to changes in power-supply voltage, expressed as %(full-scale)/%(supply-voltage change). It includes the effects of scale factor, feedthrough, and offset vs. supply at dc.

Example: for the 432, this error is specified at $\pm 0.1\%/\%\Delta V_s$.

$$0.1\% \text{ (full scale)} = 10\text{mV}$$

$$1\%\Delta V_s = 150\text{mV}$$

Therefore, the output of the 432J will change

$$\frac{10\text{mV}}{150\text{mV}} = \pm 0.067\text{V/V} = 67\text{mV/V} \tag{84}$$

Another way of looking at power-supply rejection is to recognize that the multiplier's internal reference circuit attenuates changes in the power-supply voltage. This ranges from a power-supply rejection ratio (PSRR) of 15:1 (PSR ≅ 23dB) for the 432 to 75:1 (≅ 38dB) for the 427K. In general, the more accurate the multiplier, the less sensitive it is to supply changes.

Warmup Time to Specifications: The time elapsed after the dc power is applied to the multiplier, before the errors are expected to be within the specified limits. While this does not include the time required for the multiplier to stabilize *completely*, it does indicate how long it will be before changes in output due to warmup will be small compared to the specified error.

In general, most modular multipliers are operating at their rated specifications within a few milliseconds after turn-on, since their internal temperature rise is only a few °C. Also great care is taken in the design and packaging to minimize the temperature coefficients and internal thermal gradients.

OUTPUT OFFSET

Initial Output Offset: the output voltage for $V_x = V_y = 0\text{V}$. This specification gives the maximum offset at 25°C with no external adjustment. In all cases, this offset can be adjusted to zero with an external potentiometer or voltage divider. Offset is the principal error when the output is less than 1V.

Initial offset has a non-zero value due to shifts in encapsulation and tolerances of internal trims. The higher the accuracy rating of the multiplier, the less the initial offset.

Average Offset vs. Temperature: the dependence of the output offset on temperature. Unlike operational amplifiers, the average offset vs. temperature in multipliers is independent of the initial offset.

Example – 429B: Offset = ±10mV *max* untrimmed
Offset vs. temperature = ±1mV/°C *max*

To calculate maximum offset at 70°C,

$$E_{os70°C} = |E_{os25°C}| + \frac{\Delta E_{os}}{\Delta T} \quad (70°C - 25°C) \tag{85}$$

$$E_{os70°C} = 10mV + 1(45) = \pm 55mV \text{ } max \tag{86}$$

Average Offset vs. Supply: the sensitivity of output offset to changes of supply voltage, expressed as millivolts per % change of supply voltage at dc. Like the total error vs. supply, this quantity can be expressed in volts/volt, inversely as power-supply rejection ratio (PSRR) for offset, and in log (dB) form: PSR = $20\log_{10}$PSRR. For example, the 429 and the 427 have offset sensitivity of 1mV/1%ΔV_s, or 1mV/150mV. The offset PSRR is thus 150, and the PSR is about 43dB.

SCALE FACTOR

Scale Factor – Static, or low-frequency – The difference between the average scale factor and the ideal scale factor of 1/10/V. Errors due to this factor are expressed in % of output signal; that is, a 0.5% scale-factor error will cause a 50mV error at E_o = 10V, and a 5mV error at E_o = 1V. The scale-factor error includes only the average linear gain error (i.e., the error in the slope of a "best straight line" through the range of output for one input constant,

the other swinging through its range). The nonlinear component is discussed under *nonlinearity.*

The scale-factor error can be adjusted to zero at any one point. However, the nonlinearity makes it impossible to adjust the scale-factor error to zero over the entire X-Y operating range. The *average* scale-factor error can be adjusted for minimum error over limited regions (e.g., one or two quadrants), or for the best compromise over all values of input.

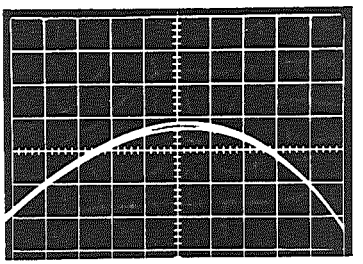
NONLINEARITY

Nonlinearity: the irreducible component of error. The specification represents the peak difference between the multiplier output and the theoretical output with the average scale-factor error adjusted to zero under the specified test conditions. Schemes for testing nonlinearity will be found in Figures 40, 46, and 47 at the end of this chapter. Since the output and input waveforms should have the same shape (one input constant), the test circuit displays the difference between the multiplier output voltage and an input that swings over the entire range, while the other input is held constant. The average scale-factor error (slope) is adjusted out.

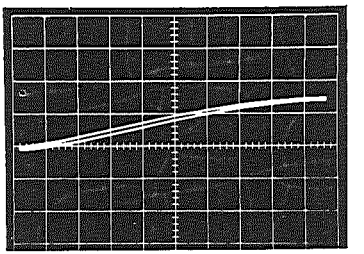
Typical nonlinearity curves for the 432 and the 427, measured in this way, can be seen in Figures 28 a-d, for one polarity of constant voltage. For each of these curves, corresponding curves exist (not necessarily of the same shape) for the opposite polarity. Note that the curves are smooth and without discontinuities at the origin. The parabolic shape of the 432's X nonlinearity indicates that the X input has primarily second-harmonic distortion (proportional to X^2). The S-shaped 427 nonlinearity curves indicate predominantly cubic distortion.

FEEDTHROUGH

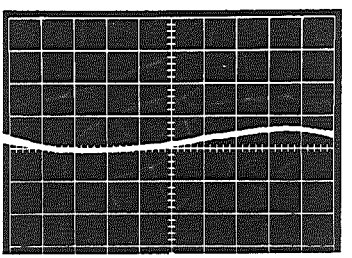
Feedthrough. Ideally, the output of the multiplier should be zero if either input is zero, independently of the signal applied to the other input. Actually, a certain fraction of the non-zero input will



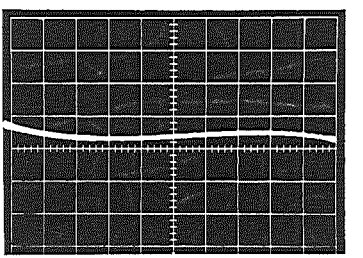
a. Model 432 X-input nonlinearity for ±10V input signal, Y = 10V, vertical scale: 20mV/div.



b. Model 432 Y-input nonlinearity for ±10V input signal, X = 10V, vertical scale: 20mV/div.



c. Model 427 X-input nonlinearity for ±10V input signal, Y = 10V, vertical scale: 10mV/div.



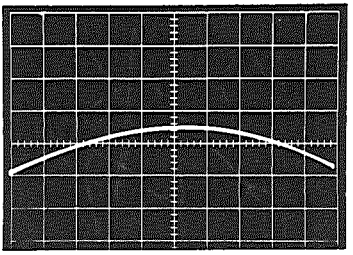
d. Model 427 Y-input nonlinearity for ±10V input signal, X = 10V, vertical scale: 10mV/div.

Figure 28. Typical nonlinearity curves

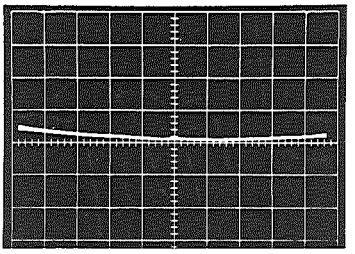
"feed through" and appear at the output. The feedthrough signal is composed of two components, one linear, the other nonlinear. The linear component is the product of the voltage on the varying input and the effective offset voltage of the "zero" input. This can be trimmed to zero by introducing an equal and opposite offset at the trim input (X_o, Y_o).

The nonlinear component, which cannot be reduced by zero by an offset adjustment, is due to the nonlinearity of the multiplier circuit. Graphically, it is the intersection of the nonlinearity sur-

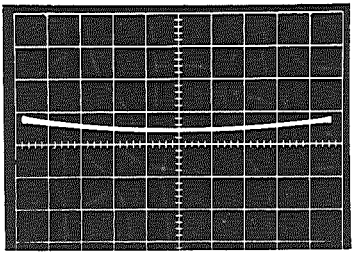
face with the XZ and YZ planes (Figures 3 and 4, this chapter). Figures 29 (a-d) show typical X and Y feedthrough waveforms for



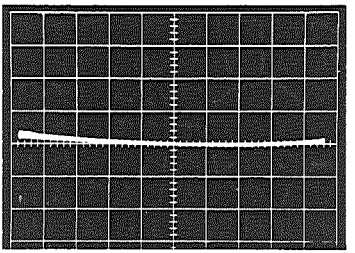
a. Model 432 X Feedthrough, X = ±10V, Y = 0, vertical scale: 50mV/div.



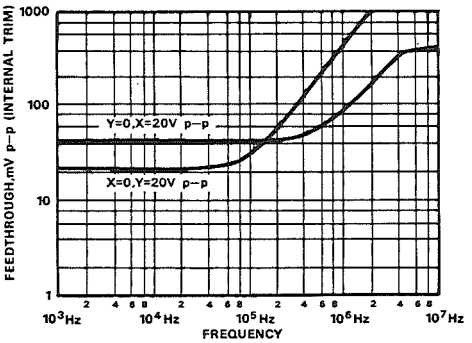
b. Model 432 Y Feedthrough, Y = ±10V, X = 0, vertical scale: 50mV/div.



c. Model 427 X Feedthrough, X = ±10V, Y = 0, vertical scale: 10mV/div.



d. Model 427 Y Feedthrough, Y = ±10V, X = 0, vertical scale: 10mV/div.



e. Model 429 Feedthrough vs. frequency

Figure 29. Typical feedthrough curves

the 432 and the 427. Note that the 432 has pronounced parabolic X feedthrough, which greatly resembles the nonlinearity at the extremes.

Feedthrough vs. Frequency. Feedthrough increases with frequency, due to capacitive coupling between the inputs and the output stage. Figure 29e is a plot of both X and Y feedthrough vs. frequency for the 429.

BANDWIDTH (High-Frequency Dynamic Parameters)

Bandwidth, -3dB Small-Signal: The output frequency at which the scale-factor of the multiplier has decreased to 0.7 times its dc value. "Small" signal usually means an output of less than 5% of full scale, e.g., 1Vp-p for a ±10V(FS) multiplier. Bandwidth is usually measured with a full-scale dc voltage on one input, a 1Vp-p sine wave on the other. It can be seen on the chart that the two transconductance multiplier types have wider bandwidths that either the pulse-modulated or log-antilog types.

The term "output frequency" is significant. For example, the low-frequency output of a multiplier connected as a squarer (X = Y), for sine-wave input, is a double-frequency sine wave with an amplitude of one-half the square of the input amplitude, biased by a like amount. The output amplitude will be down 3dB for an input of lower frequency than for the dc × sine case, because of the frequency doubling. On the other hand, the "dc" component of the output can remain unaffected up to considerably higher frequencies.

Full-Power Response: the maximum frequency at which the multiplier output can product full-scale voltage at rated current, without noticeable distortion. This is measured by applying 10Vdc to one input and a 20Vp-p sine wave to the other (and vice versa). Again, the transconductance multipliers are much faster than the pulse-modulation or logarithmic types.

Slew(ing) Rate: the maximum rate of change of output voltage for large signals. It is measured with one input at 10V, the other a step swing of 10 or 20V. A typical 429 step response, showing the slewing rate, is shown in Figure 30. The approximate relationship between slewing rate and full-power bandwidth is

$$S \simeq A\, 2\pi\, f_P$$

where

S = Slewing rate, in volts/microsecond

A = Peak sine-wave amplitude, in volts

f_P = Measured frequency for full output, in MHz

For example, the 429 has f_P = 2MHz(*min*). For A = 10V,

$$S \simeq 10 \times 2\pi \times 2 = 126\text{V}/\mu\text{s} \qquad (88)$$

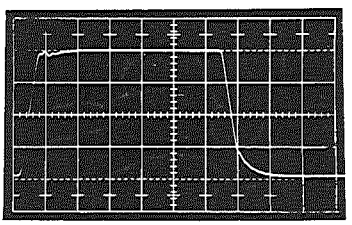


Figure 30. Step response, showing slew rate of Model 429. Voltage scale: 5V/div; time scale: 200ns/div. V_X = 20V p-p 400kHz square wave V_Y = +10.0V

Small-Signal Amplitude Error. This is the frequency at which the amplitude response, or scale factor, is down by 1% (0.1%, for high-accuracy types), measured with a "small" signal, e.g., 10% of full-scale. If, for a given type, this frequency turns out to be 1/3 or less of the full-power frequency, then signals as large as full scale fit the definition of "small signals." For example, $f_{-1\%}$ for both the 429 and the 432 is less than 1/6 of f_P; therefore $f_{-1\%}$ applies to any signal in the whole ±10V range.

The 1% error bandwidth is related to small-signal bandwidth and the rolloff rate (depending on the number of poles in the transfer function). For responses governed by a single pole, the -1% error bandwidth occurs at about 1/7 of the -3dB bandwidth

$$|A| = 0.99 = \left| \frac{1}{1 + j\omega/\omega_0} \right| = \frac{1}{\sqrt{1 + (\omega/\omega_0)^2}} \qquad (89)$$

whence $(\omega/\omega_0) \cong 1/7$

It is interesting to note that the output bandwidth or speed of transconductance and pulse-modulation multipliers is essentially independent of signal level (except for slewing rates), or of choice of input (X or Y). And, of particular interest, the measured bandwidth is independent of any dc bias level added to the measuring "small" signal.

Vector Error: the frequency f_V at which the instantaneous, or vector difference between an input signal and the output, of the same frequency, becomes equal to 1%. For a single-pole rolloff (first-order lag), it is the frequency at which the phase shift becomes 0.01% of a radian, or 0.57° — 1/100 of the -3dB frequency. Vector error is due primarily to phase shift, since the attenuation of magnitude at f_V is only 0.05% (Figure 31).

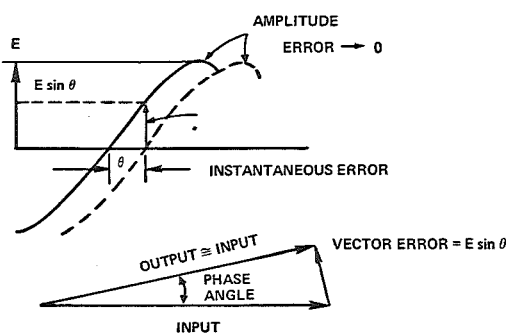


Figure 31. Vector error (at unity gain), a measure of instantaneous error

Settling Time for ±10V Step: the time required for the output voltage to approach within a specified percentage of its *final* value, in response to a 10V (full scale) input step. The time is measured from the instant the step is applied, until the output has entered the specified error band (for the last time), and therefore includes transport delay, slewing time, and linear-settling time.

Overload Recovery: the time required for the output of the multiplier to return to within its linear region, after a 50% over-voltage (where permissible, 15V for 10V-scaled devices) has been removed from the input.

OUTPUT NOISE

Output Noise: The rms value of the noise at the output of the multiplier, in a 5Hz to 10kHz bandwidth, measured with both inputs at zero. Noise is not appreciably affected by input voltage, so the specified value can be applied to any input level in the operating region. Peak-to-peak noise is usually taken to be about 6.6 times the rms level for Gaussian noise (see Figure 14, Chapter 2-3); multiplier noise can usually be safely assumed to be Gaussian.

Wideband Noise: For low-bandwidth multipliers, this includes any out-of-band effects, such as carrier leakage to the output of pulse-height-pulsewidth types (like the 427). The variable-transconductance types have fairly constant noise spectral density over their bandwidth, with no out-of-band components.

OUTPUT CHARACTERISTICS

Output Voltage at Rated Load: the minimum output voltage range at dc with the multiplier supplying the specified load current.

Output Current: The minimum current available from the multiplier output at full-scale output voltage.

Load Capacitance: The maximum value of capacitance that can be connected to the output, with no oscillations resulting, in the *multiply* mode.

INPUT RESISTANCE

The resistance between the input terminal and power common. This may be an actual resistor, or the effective input resistance of an input-amplifier circuit. Typically, input resistance is in the 10kΩ to 100kΩ range, a reasonable level, since multipliers are usually driven from low-impedance sources, such as closed-loop op-amp outputs.

INPUT BIAS CURRENT

The current flowing into or out of the input terminal with zero volts at the input. This is due to the bias current of the internal circuit, e.g., base current of input transistors.

MAXIMUM INPUT VOLTAGE

For Rated Accuracy: the maximum voltage that, when applied to either or both inputs, will produce an output voltage within the specified error limits. Usually, it provides a slight overrange capability. The multiplier will work with higher inputs, as long as the product of the inputs is within the output voltage range.

Safe Level: The Maximum Voltage that Will Not Damage the Input Circuit. The notation $\pm V_s$ means that the input can be no greater than the supply; if the supply is zero (or disconnected), the input must be zero (applicable especially to IC multipliers and the 432). For the other types, it is stated as an absolute-maximum voltage; i.e., the 429 will be safe with ±16V in and zero or rated supply voltage.

POWER SUPPLY

V_s *for Rated Performance*: the power-supply voltage at which all *min/max* error specifications are guaranteed; normally ±15V, ±2%.

Operating: the range of power-supply voltages over which the multiplier will operate normally, but with increased error, as calculated from the power-supply-rejection coefficients. Over this range, the multiplier will accept ±10V inputs and provide ±10V output. For some multipliers, graphs of input and output voltage swing vs. V_s are provided.

Quiescent Current: the current drawn from the $\pm V_s$ supplies, with the inputs and outputs at zero volts. Under full-output conditions, this current will increase by an amount approximately equal to the load current, since most multipliers have Class AB output stages.

TEMPERATURE RANGE

Rated Performance: the range over which the temperature coefficients apply, and other parameters remain within min/max limits.

Operating: the temperature range over which the multiplier will operate, with generally slight degradation of specified temperature coefficients.

Storage: the maximum temperature extremes that the multiplier can withstand, without power applied.

PACKAGE OUTLINE

This refers to a standard Analog Devices drawing, showing the pin configuration and mechanical dimensions; since multipliers vary widely in size and pinout, it is a good idea to check this out.

Case Dimensions (self-explanatory). The higher-accuracy, pulse-modulation types (427) are at present larger than the transconductance or log types (429, 434). The smallest modular case is the transconductance IC type, such as the 432. IC's are available in TO-116 hermetic 14-pin dual in-line and TO-100 10-pin metal-can packages.

CHECKLIST OF MULTIPLIER PARAMETERS

A. Static or Low-Frequency Errors (Accuracy)

1. Output Offset Voltage
2. X and Y Feedthrough
3. X and Y Nonlinearity
4. Total Error
5. Changes of Above Parameters with Temperature or Power-Supply Voltage

B. Dynamic Performance

1. -3dB Small-Signal Bandwidth
2. Phase Shift vs. Frequency
3. Full-Output Bandwidth
4. Slewing Rate
5. Rise Time
6. Settling Time
7. Frequency for 1% Vector Error
8. Frequency for 1% Amplitude Error
9. Nonlinearity vs. Frequency
10. Feedthrough vs. Frequency
11. Differential Phase Shift
12. Overload Recovery Time

C. Input and Output Characteristics

1. Input Resistance
2. Input Current
3. Output Voltage
4. Output Current
5. Output Resistance
6. Input and Output Voltage Limits vs. Power-Supply Voltage
7. Quiescent Current

TESTING

TEST EQUIPMENT

Depending on the parameters to be measured, and the number of multipliers to be tested, the equipment used to test multiplier characteristics can range from a self-contained multiplier test set to a simple arrangement of ordinary laboratory instruments. Some of the most-useful test equipment is listed below:

1. Digital Voltmeter – essential for measuring dc offsets, and input and output voltages for determining "accuracy" of multipliers. 4½-digit resolution, with $<\pm 0.02\%$ error is adequate for most measurements. 1Vdc and 10Vdc ranges will be the most used.

2. Precision dc Voltage Reference – to supply input voltage for "accuracy" measurements, stable reference for non-linearity tests. Should be capable of supplying both plus and minus 10.000V at 1mA *simultaneously*, adjustable in 100mV steps down to zero volts.

3. Function Generator – provides low-frequency sinusoidal input signal for crossplot tests; and square waves or pulses for dynamic tests. Generator output voltage should be adjustable from zero to 20Vp-p into 1kΩ over frequency range of 1Hz to 1MHz (5 or 10MHz is desirable for testing the faster multipliers).

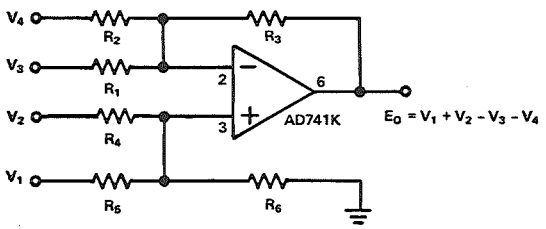
4. Variable dual 15-volt Power Supply, 50mA output current, with adjustable current limit. A variable supply is useful for measuring multiplier input and output voltage limits as a function of supply voltage.

5. Oscilloscope – for crossplots and dynamic tests. Calibrated, dc-coupled vertical and horizontal inputs are required for crossplots. Vertical deflection factors of 5mV/cm (for testing "high-accuracy" multipliers) to 5V/cm are most useful.

Horizontal deflection factors of 0.5V/cm to 5V/cm are adequate. Bandwidth of 100kHz on both axes is sufficient for "static" error measurements.

A wideband oscilloscope – at least 10MHz bandwidth – is essential for dynamic tests

6. Precision adder/subtractor – for measuring nonlinearity. This can be constructed according to the schematic Figure 32.



R_1 TO R_6: 10kΩ PRECISION RESISTORS, TOLERANCE ±0.1%, TEMPCO ≤ 50ppm; ratio-match R_1 AND R_2 TO R_3 AS CLOSELY AS POSSIBLE, DO THE SAME FOR R_4 AND R_5 TO R_6.

Figure 32. High-precision adder subtractor

TEST CIRCUITS

The crossplot is one of the most powerful and useful techniques for performing sensitive adjustments and measuring multiplier errors, for example feedthrough and nonlinearity, by plotting such quantities as a function of the input variable. This is most easily done by displaying the error on the vertical axis of the oscilloscope and using the multiplier input signal to drive the horizontal input.

A crossplot test setup for measuring X feedthrough is shown in Figure 33. In this case, the X input of the multiplier (an X-Y plotter could be used in place of the oscilloscope, to obtain a large-scale permanent record) is driven by a 20Vp-p 10Hz sine wave, and the Y input is grounded. The output of the multiplier is connected to the vertical channel of an oscilloscope with sensitivity of 20mV/cm, direct-coupled. The sinusoidal X drive signal is connected to the horizontal input of the oscilloscope,

sensitivity 2V/cm direct-coupled (±10V F.S.). The oscilloscope trace is centered on the screen (zero input and zero feedthrough is at the Origin).

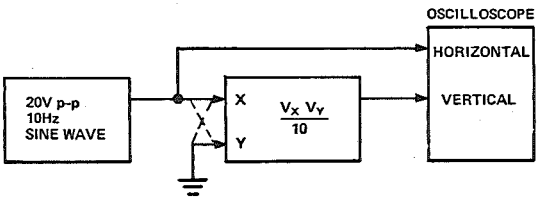


Figure 33. Cross plot test setup connected to measure X feedthrough. For Y feedthrough exchange X and Y inputs.

A photograph of the X feedthrough of a transconductance multiplier produced with the aid of this test setup is shown in Figure 34. The symmetrical parabolic shape indicates that the nonlinear component of X feedthrough is proportional to X^2. The peak value of X feedthrough is 50mV, occurring at X = +10V and -10V. Figure 35 illustrates the effect of an additive linear component to the X feedthrough, produced by Y_{os}. The parabola is no longer symmetrical; the +10V end is higher than the -10V

TABLE: MULTIPLIER TEST MATRIX

Test	V_x	V_y	E_o	Read Error On
Offset	0	0	$0 \pm E_{os}$	DVM
X Feedthrough	20V p-p	0		Scope
Y Feedthrough	0	20V p-p		Scope
X Nonlinearity	20V p-p	+10V		Scope
X Nonlinearity	20V p-p	-10V		Scope
Y Nonlinearity	+10V	20V p-p		Scope
Y Nonlinearity	-10V	20V p-p		Scope
Full-Scale Errors				
I	+10V	+10	$+10V \pm \epsilon$	DVM
II	-10V	+10V	$-10V \pm \epsilon$	DVM
III	-10V	-10V	$+10V \pm \epsilon$	DVM
IV	+10V	-10V	$-10V \pm \epsilon$	DVM

end, with a difference of 40mV. This indicates that there is 20mVp-p of "linear" X feedthrough (that can be cancelled out by a Y_{os} adjustment).

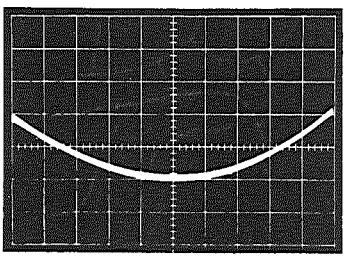


Figure 34. Measurement of X feedthrough showing nonlinear (parabolic) component only, X = ±10V. Vertical scale: 20mV/div.

The Y feedthrough can be cross-plotted by interchanging the X and Y inputs on the test setup.

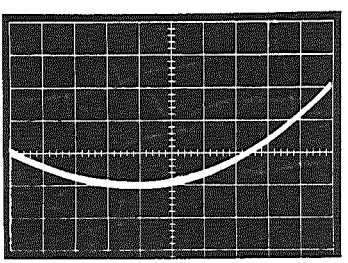


Figure 35. Measurement of X feedthrough with Y_{os} not optimized, X = ±10V. Vertical scale: 20mV/div. Additive linear term = 40mV p-p; Y_{os} = 20mV.

The crossplot technique can be extended to the measurement of nonlinearity, as illustrated in Figure 36.

Figure 37. DC Accuracy (Error), V_{OUT}, I_{OUT}, Z_{OUT}

Figure 38. Offset

Figure 39. Low-Frequency Feedthrough, Crossplot

Figure 40. Nonlinearity, Crossplot

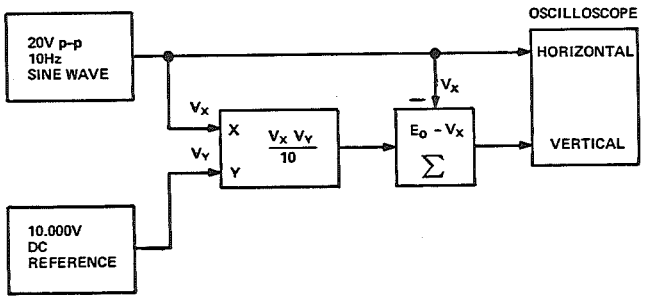


Figure 36. Cross plot setup for measuring X nonlinearity at Y = 10V. For Y = -10V, summing block should compute $E_o + V_x$. Interchange X and Y to measure Y nonlinearity.

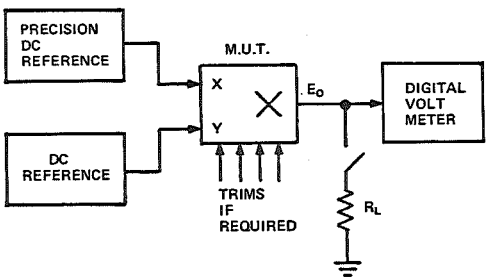


Figure 37. Test setup for measuring DC accuracy, output voltage and current range at rated load, output resistance.

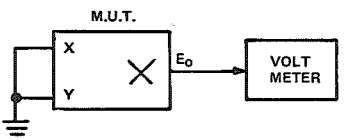


Figure 38. Output offset measurement

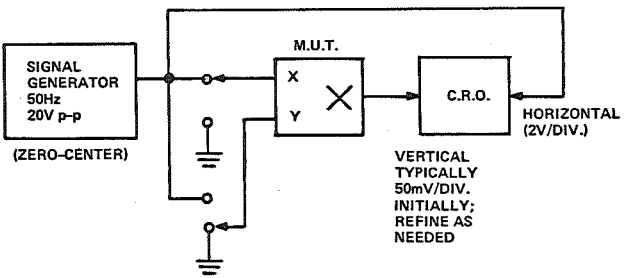


Figure 39. Low-frequency feedthrough crossplot

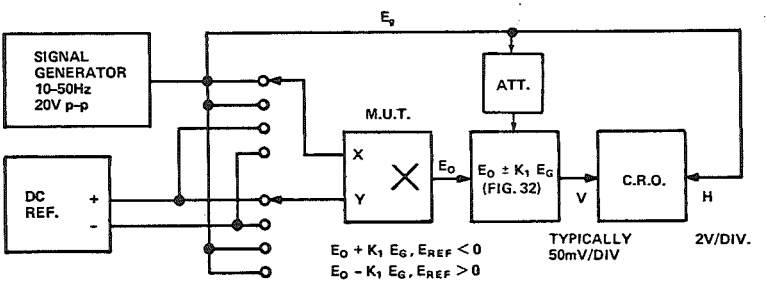


Figure 40. Nonlinearity crossplot

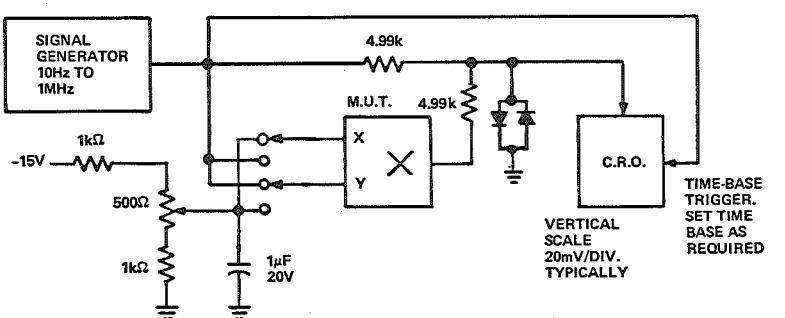


Figure 41. Vector (instantaneous) error, settling time

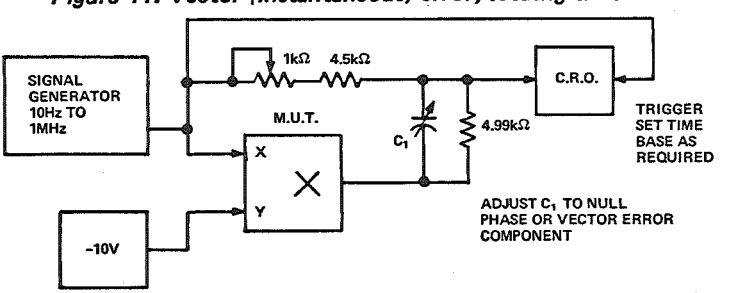


Figure 42. 1% error bandwidth, X nonlinearity vs. frequency (3rd & 4th quadrants)

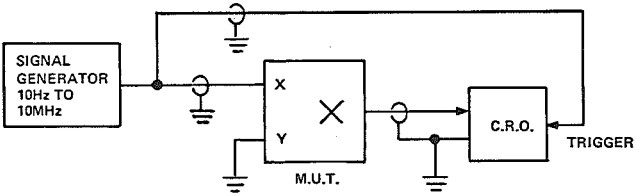


Figure 43. X feedthrough vs. frequency

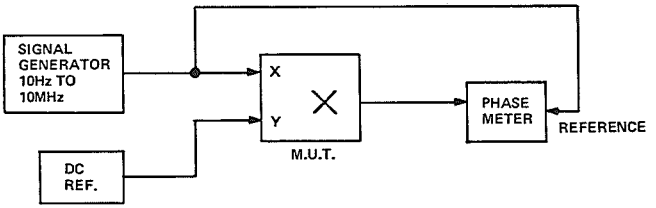


Figure 44. Phase shift, differential phase shift

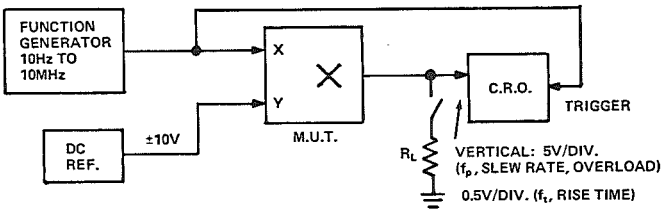


Figure 45. Full-power frequency, slewing rate, overload recovery; small-signal amplitude response and rise time; output current and voltage

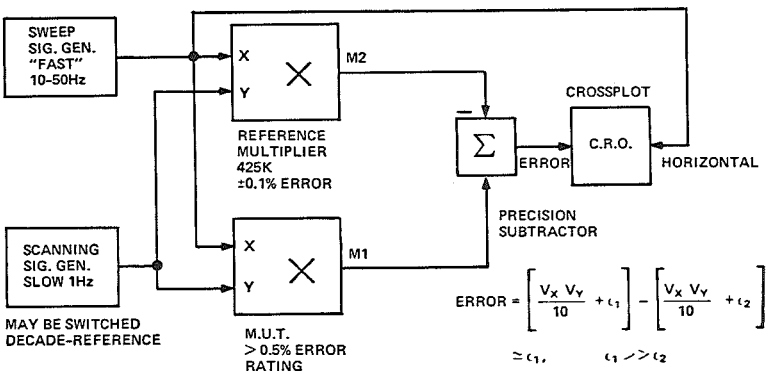


Figure 46. Sophisticated X nonlinearity test, using accurate multiplier as reference. The X input is swept at a "reasonable" frequency, and the Y input signal swings slowly over its range. The inputs are reversed to check Y nonlinearity. If Y is swept continuously, the signal envelope is the worst-case error magnitude.

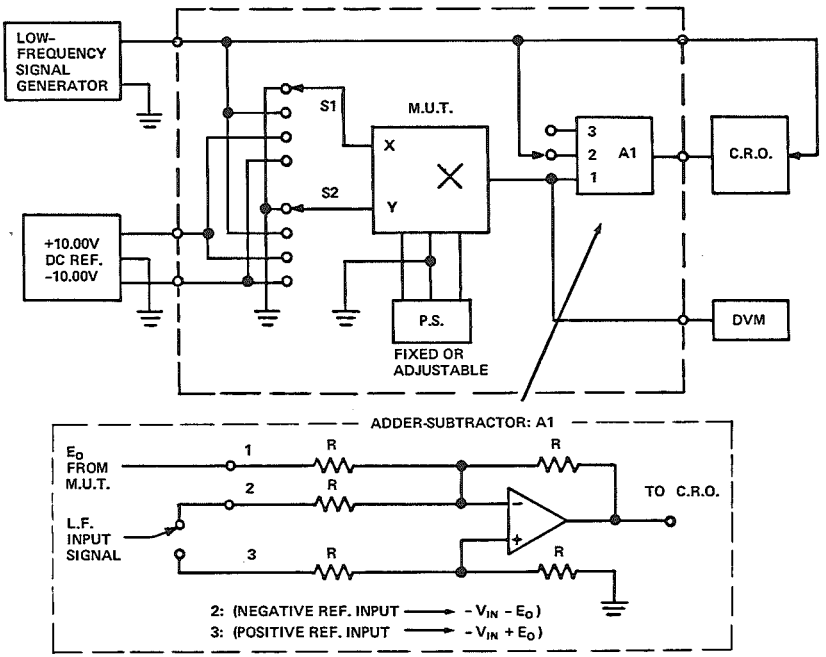


Figure 47. Multipurpose test box

Note: These test circuits are principally designed for testing 4-quadrant devices. Testing of single-quadrant devices is in some respects similar: however, here are a few differences:

1. Tests using a negative voltage at one input and passive summation of input and output, taking advantage of the negative gain of the device in the 2nd and 3rd and the 3rd and 4th quadrants, cannot be used. Either precise subtraction or CRO differential inputs (if sufficiently accurate) should be used.

2. Single-quadrant devices generally require half-scale biasing of the input signal generator output; peak-to-peak swing is 10V (for 0 to 10V devices).

3. For a complete response picture, logarithmic devices may require several sets of small-signal tests, employing small signals biased at intervals, e.g., 9V ±1V, 0.9V ±0.1V, etc.

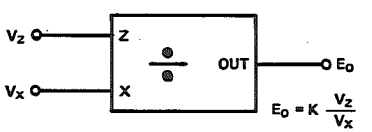
III Dividers (Ratio Circuits)

Chapter 3

An analog "divider" circuit produces an output voltage or current proportional to the ratio of two input voltages or currents. For convenience and clarity, in this chapter, it is to be assumed that the inputs and outputs are voltages (unless noted otherwise).

$$E_o = K\frac{V_z}{V_x} = V_r\frac{V_z}{V_x} \qquad (1)$$

The denominator is denoted V_x, the numerator V_z, and the output E_o. The dimensional scale factor K (or V_r), is usually 10 volts. If the ratio of the inputs is unity, the output is equal to K. The input/output relationship for an ideal analog divider is summarized in Figures 1, 2, and 3.



K = SCALE FACTOR (VOLTS) = 10V (MOST COMMON)

K = 1V IS USEFUL FOR $V_z > V_x$

Figure 1. Block diagram of divider

The operating region of the variables (quadrants of operation) is defined by the polarity and magnitude ranges of the numerator and denominator inputs, and of the output. Figure 2 depicts the operating region of the inputs of a 2-quadrant divider with normal polarity relationships (bipolar numerator, positive denominator).

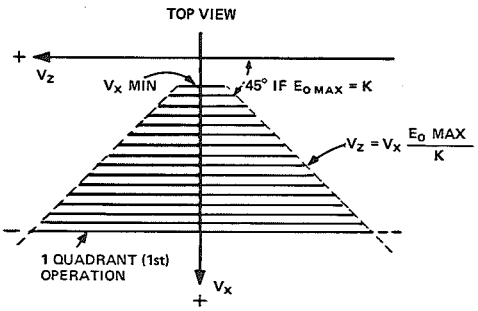


Figure 2. Top view of 2-quadrant divider-function surface, showing constant-denominator elements.

If the numerator and denominator are both restricted to a single polarity (usually positive), the divider is said to operate in a single quadrant, indicated by shading. Generally, the denominator is restricted to a single polarity, since the transition from one polarity to another would require the denominator to pass through zero, which would call for infinite output (unless the numerator were simultaneously zero).*

Besides excluding the vicinity of $V_X = 0$, the operating region of a practical analog divider does not cover an entire quadrant or half-plane, because the maximum allowable numerator magnitude depends on the denominator magnitude and either the output range or the scale factor.

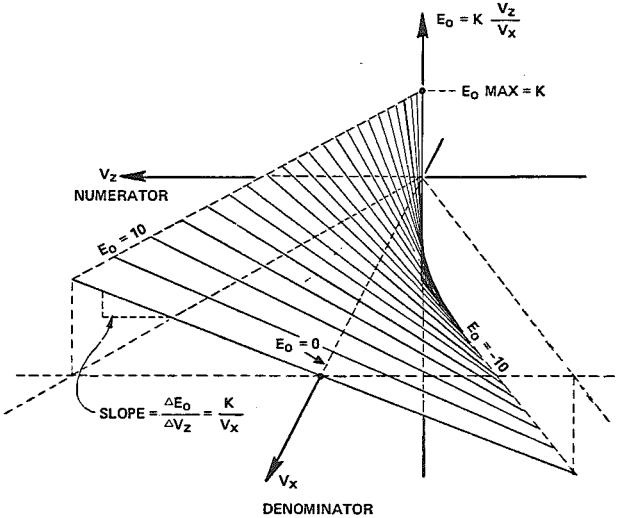
$$V_{z_{max}} = \frac{E_{o_{max}}}{V_r} \cdot V_x \qquad (2)$$

In the case, where $E_{o_{max}} = K$ (= 10V), the input region is bounded by the 45° line, $V_z \leqslant V_x$. For small values of V_x, the operating region is further limited by the minimum value of denominator $V_{x_{min}}$ that will allow reasonable performance.

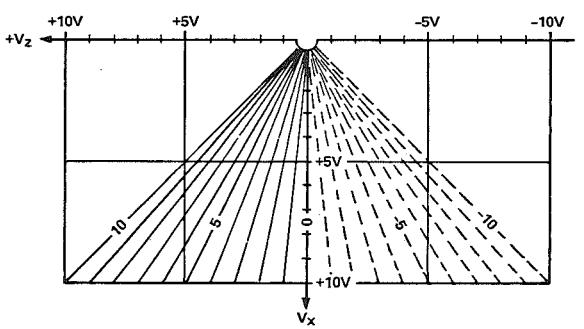
The input-output relationship of an ideal divider can be visualized by imagining the three-dimensional surface relating the three

*It is possible to construct a 4-quadrant divider that accepts bipolar numerator and denominator (except for a "forbidden zone" in the vicinity of zero denominator) and provides an output with proper polarity relationships, but it has few useful applications.

variables. Figure 2 is a top view of the surface, showing the constant-x elements; for each value of V_x, the output is linear in V_z. Figure 3a is a view of the surface in perspective. It is a developed surface generated by two sets of straight-line elements, (1) constant V_x and (2) constant E_o. Figure 3b is a top view showing the contours of constant E_o. E_o is seen to be equal to zero along the V_x axis, equal to K at the intersection of the $V_x = V_y$ plane and the E_o = K plane, and linearly proportional to V_z



a. Two-quadrant divider input-output surface, showing constant-denominator elements



b. Contours of equal E_o, 1V contour interval, for $E_o = 10V_z/V_x$, $V_x > 0$

Figure 3. Two quadrant divider — input/output surface

where it intersects any plane perpendicular to the V_x axis. E_o is inversely proportional to V_x where the surface intersects any plane perpendicular to the V_z axis. The surface approaches verticality as V_x approaches zero, tending towards $+\infty$ for positive V_z and towards $-\infty$ for negative V_z; however, it is truncated considerably earlier by the intersection of the $E_o = K$ plane and the $V_x = V_z$ plane.

Theoretically, the output will approach the value $\pm K$ as $\pm V_z$ and V_x approach zero together

$$\lim_{|V_z| = V_x \to 0} K \frac{V_z}{V_x} = K \tag{3}$$

In contrast with the theory, the output of real dividers is generally undefined for denominators smaller than some minimum value, typically in the range from 10mV to 1V, depending on the properties of the device.

ERRORS OF ANALOG DIVIDERS

Division has long been the most difficult of the four arithmetic functions to implement with analog computing devices. This difficulty stems primarily from the nature of division: the magnitude of a ratio becomes quite large, approaching infinity, for a denominator that approaches zero (and a non-zero numerator). Thus, an ideal divider must have potentially "infinite" gain and infinite dynamic range. For a real divider, both of these factors are limited by the magnification of drift and noise at low values of V_x.

In other words, the "gain" of a divider for the numerator is inversely dependent on the value of the denominator (Figure 4). On the other hand, if the ratio of numerator to denominator remains constant as their magnitudes vary, the quotient is constant (Figure 5).

The output of a practical analog divider will differ from the theoretical ratio of its inputs by an amount that is, in general,

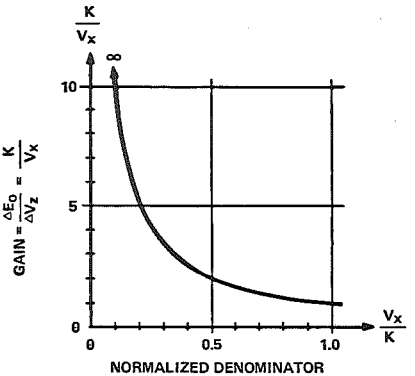


Figure 4. Divider gain as a function of denominator voltage

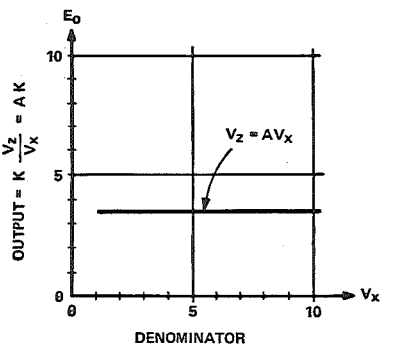


Figure 5. Divider output for constant ratio (A) of numerator to denominator

dependent on the magnitudes of the inputs. The overall error is the net effect of several factors, of which the most important are:

Type of Error	Approximate Range of Magnitude
1. Numerator offset, Z_{os}	1% to 0.001% of $V_{z_{max}}$
2. Denominator offset, X_{os}	1% to 0.001% of $V_{x_{max}}$
3. Output offset, E_{os}	1% to 0.01% of $E_{o_{max}}$
4. Scale-factor error, ΔK	1% to 0.05% of K
5. Nonlinearity, $f(V_z, V_x)$	5% to 0.05% of V_z, V_x

The effects of these errors can be seen more plainly when they are introduced into the "ideal" divider equation

$$E_o = (K + \Delta K)\frac{V_z + Z_{os}}{V_x + X_{os}} + E_{os} + f(V_z, V_x) \qquad (4)$$

The equation can be rewritten to sort out the effects of the combined errors on the output

$$E_o = (K + \Delta K)\frac{V_z}{V_x + X_{os}} + \underbrace{\frac{(K + \Delta K)Z_{os}}{V_x + X_{os}}}_{\text{input offset referred to output}} + \underbrace{E_{os}}_{\text{output stage offset}} + \underbrace{f(V_z, V_x)}_{\text{non-linearity}} \qquad (5)$$

scale-factor error; ratio error; total output offset

Considering these terms separately,

1. The scale-factor error, ΔK, is independent of the level of V_z or V_x. However, as will be shown, there is an additional error due to X_{os}, which may be viewed either as an additional X-linearity error or as a variable scale factor on V_z, depending on the interpretation of V_x and the portion of the range that is used. If $X_{os} = 0$, the term simply represents the ideal division, with a ΔK error. As X_{os} becomes more significant in relation to V_x, if affects the slope of the E_o/V_z relationship. If X_{os} is negative, (and V_z non-zero), as V_x approaches the positive value, $-X_{os}$, the ratio tends to "blow up" (Figure 6). If V_z is precisely zero, the output

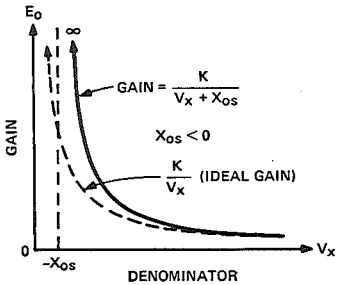


Figure 6. Divider gain error at output as a function of denominator X ($X_{os} < 0$)

will be limited to K + ΔK, small comfort, since K is usually full scale, and an infinitesimal deviation of V_z from zero will drive the output into limits. If X_{os} is positive, the gain will not become infinite within the range of V_x, but large linearity errors will result for small values of V_x (Figure 7). In particular, at $V_x = X_{os}$, the gain will have halved.

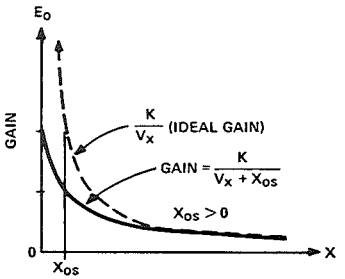


Figure 7. Divider gain error at output as a function of denominator X ($X_{os} > 0$)

2. The "input offset" error, referred to the output,

$$(K + \Delta K)\frac{Z_{os}}{V_x + X_{os}} \cong K\frac{Z_{os}}{V_x + X_{os}}$$

The numerator offset, Z_{os}, is subjected to a gain $K/(V_x + X_{os})$. If X_{os} is zero and Z_{os} is non-zero, this term tends to "blow up" as V_x approaches zero; in any event Z_{os} will be magnified for all $V_x < K$. The value of X_{os} serves to modify the "blowup point" (asymptote): if X_{os} is negative, the offset error will become "infinite" when V_x has the positive value $-X_{os}$. If X_{os} is positive, the offset error will become high, but not infinite (small comfort again!). If $Z_{os} = 0$, then the input offset error, referred to the output, will be zero (except at $V_x + X_{ox} = 0$, when it becomes equal to K).

3. The output-stage offset is independent of V_z and V_x, and, since it undergoes no magnification, it is generally a negligible source of error, compared to the output errors produced by the input offsets. Its contribution is most salient in such applications

as linearizing, where the dynamic range of the denominator is not usually large; for such applications, E_{os} should be trimmed to zero, and the effect of its temperature coefficient should be considered.

4. The output nonlinearity $f(V_z, V_x)$ is identifiable in terms of the nonlinearity of the straight-line elements (Figure 3), with all other errors tweaked to zero. V_z (numerator) nonlinearity is the departure of E_o from proportionality to V_z at constant V_x. Figure 8 is a typical plot of numerator nonlinearity, measured by subtracting KV_z/V_x from the output. Nonlinearity as a function of denominator (actually as a function of *ratio*) is defined in terms of deviation of the measured ratio from the theoretical ratio as V_x and $\pm V_y$ are varied together in a constant ratio (the radial "spiral-staircase" straight-line elements in Figure 3b).

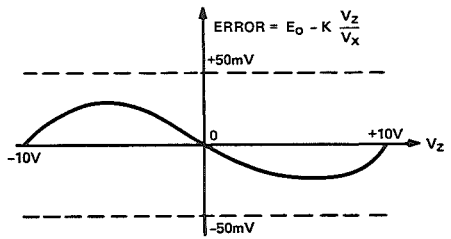


Figure 8. Nonlinearity as a function of numerator voltage (V_Z). Denominator = constant

Besides these easily-determined deviations, stated in terms of the familiar concept of *linearity*, it is also possible (but less practical) to consider the *fidelity to hyperbolic form*, comparing the output, as a function of V_x (V_z held constant), with the ideal output. Errors due to denominator offset, numerator offset, and scale-factor error are excluded. Generally, the nonlinearity takes the form of limited gain at small values of denominator voltage, as shown in Figure 9. Gain, K/V_x, is plotted vertically against V_x horizontally, for constant V_z. As V_x is reduced, the gain increases hyperbolically, until, at small values of V_x, a peak is reached, then the gain decreases to zero at $V_x = 0$. This kind of gross "denominator nonlinearity" is fairly common in analog dividers, since a zero X-input may correspond to shutting off a current or voltage in the circuit, reducing the gain to zero.

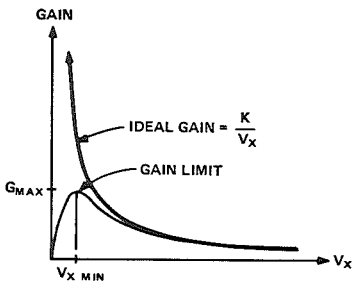


Figure 9. Gain limit at low values of denominator voltage

Divider Errors – Summary

Based on all of the above considerations, a good analog divider is identified by the following properties:

1. Fidelity to the Ratio Function: "Gain" (K/V_x) must vary inversely with the denominator over a wide range of denominator values.

2. Numerator and denominator input errors, such as offsets, noise, and drift, must be much less than the smallest input signals.

3. If requirements (1) and (2) are met, the output of the divider should be constant for constant ratios of numerator and denominator, independent of their magnitudes. For example, 10/10 = 0.01/0.01 = 1, and 1/10 = 0.001/0.01 = 0.1.

DIVIDER CIRCUITS

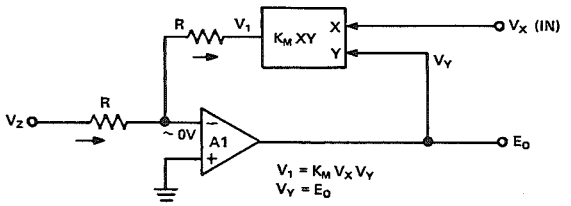
This section deals with three of the most common divider circuits.

1. Inverted multiplier
2. Direct variable-transconductance divider
3. Log-antilog divider

The design of these circuits is largely based on the multiplier circuits discussed in Chapter 3-2; they are similar in principle, in circuitry, and in physical appearance; in fact, some are identical. While other techniques for division exist, the three listed above are the most popular, and a detailed discussion of their design and performance should provide adequate insight into analog-dividers-in-general to suit any practical purpose.

INVERTED MULTIPLIERS

The "inverted multiplier" is by far the most commonly-used analog divider circuit. Nearly all general-purpose 2-input multipliers can (and most do) use this technique to achieve division. The circuit consists of a multiplier connected as the feedback element of an operational amplifier configuration, as shown in Figure 10. The forward transfer function of this circuit will be the inverse of the feedback function; thus, the multiplication function is inverted to form a divider.



IN THE STEADY STATE, THE SUMMING JUNCTION OF A1 MUST BE NULLED. THEREFORE

$$-\frac{V_1}{R} = \frac{V_Z}{R}$$

$$V_1 = -V_Z$$

$$K_M V_X E_O = -V_Z$$

$$E_O = -\frac{1}{K_M}\frac{V_Z}{V_X} = -K\frac{V_Z}{V_X}, V_X > 0$$

Figure 10. "Inverted-multiplier" divider circuit

In more specific terms, the multiplier, like a voltage-controlled potentiometer, controls the loop gain of the negative feedback circuit around the op amp. As the X input voltage to the multiplier is decreased, the gain from the Y input to the multiplier output is reduced proportionally, reducing the negative feedback (and the loop gain). Since the multiplier output must balance the Z input, the multiplier Y input must be increased proportionally. Since the multiplier Y input is supplied by the output of the circuit, the Z input is magnified in the same ratio that X is decreased.

If the X (or denominator) input is reduced to zero, then the feedback is zero, and the gain between the Z input and the amplifier output will be the open-loop gain of the op amp. If the op amp and the multiplier are "ideal," then the forward gain will

be infinite for zero denominator. Of course, real op amps do not have infinite gain, and real multipliers always have finite feedthrough, so real dividers have finite gain for zero denominator (however, noise and offset errors tend to render the finite-gain question academic, at least for low frequencies, where op amps generally have plenty of open-loop gain).

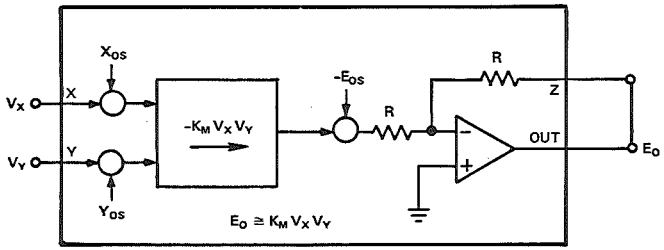
Any multiplier circuit, whatever its operating principle, can (in concept) be made to divide in this manner. But practical problems, such as stabilizing the closed loop, incompatible forms of inputs, slow response, high cost, etc., tend to narrow the field. Since it is the case (as we have shown in Chapter 3-2) that the variable-transconductance multiplier offers an excellent overall combination of cost, speed, accuracy, and (in I.C. form) size, it is reasonable to assume that inverting such multipliers to form dividers would be popular as a means of division.

Performance of Practical Inverted-Multiplier Dividers

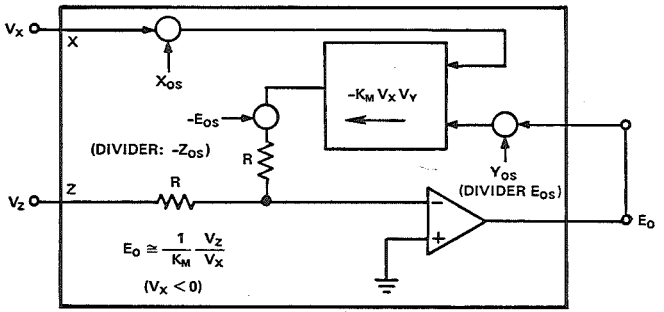
Any multiplier can, in concept, be converted into a divider by adding an operational amplifier and two resistors, as shown in Figure 10. However, most general-purpose, 4-quadrant multipliers include an output amplifier and associated resistors, and call for *external* closure of the output-amplifier loop. They can readily be inverted to 2-quadrant dividers by reconnecting the multiplier inputs and the feedback resistor, as shown in Figure 11.

The performance of the inverted-multiplier divider circuit depends primarily on the performance of the multiplier, since (except for wideband devices) the op amp usually has insignificant errors compared to the multiplier. Depending on the desired divider performance, variable-transconductance multipliers, with errors ranging upwards from 1%, or the more-accurate pulse-modulation types, with errors in the vicinity of 0.1%, might be used. Characteristics and circuitry of these multipliers are discussed in Chapter 3-2.

A 1% multiplier usually has appreciable offsets and nonlinearity; as a divider, the dynamic range of its denominator is limited to about 10:1, i.e., a 10X magnification of error and drift. The lower



a. Multiplier connection, showing effective location of offset errors



b. Divider connection, showing equivalent divider offset errors

Figure 11. Relationship of multiplier and divider errors in "inverted-multiplier" divider

errors and drift of the 0.1% multiplier will increase the useful denominator dynamic range to 100:1, but the errors and drift are still significant beyond a 10:1 range (Figure 12).

Specified multiplier performance can be used to predict divider errors. Their relationship is outlined in Table 1. Equation (5) can be rewritten in terms of the multiplier parameters to describe divider performance based on multiplier specs:

$$E_o = \frac{1}{K_m - \Delta K} \cdot \frac{V_z}{V_x + X_{os}} + \frac{1}{K_m} \cdot \frac{E_{os}}{V_x + X_{os}} + Y_{os} + f(E_o, V_x) \qquad (6)$$

where K_m is the multiplier scale constant = $1/V_r$

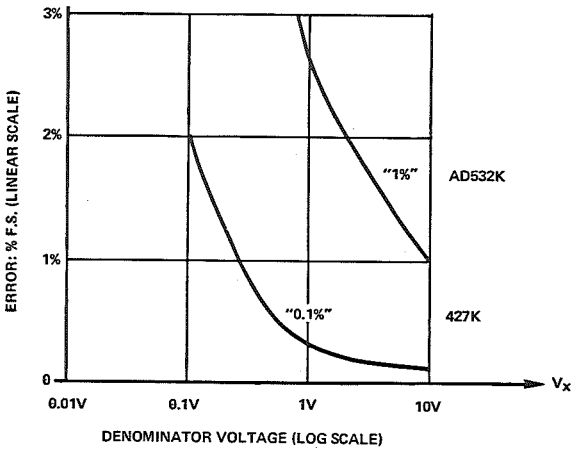


Figure 12. Total error vs. denominator for 1% and 0.1% "inverted multiplier" dividers

TABLE 1. RELATIONSHIP OF DIVIDER PARAMETERS TO MULTIPLIER PARAMETERS

Multiplier Parameter	Corresponding Divider Parameter	Principal Output Component of Divider
A. "Linear" Effects		
1. Output offset, E_{os}	Numerator offset, Z_{os}	KE_{os}/V_x
2. X-Input offset, X_{os}	Denominator offset, X_{os}	$KV_z/(V_x + X_{os})$
3. Y-Input offset, Y_{os}	Output offset, E_{os}	Y_{os}
4. Scale factor, $K_m = 1/V_r$	Scale factor, $K = V_r$	KV_z/V_x
B. Nonlinear Effects (other errors minimized)		
5. X Nonlinearity	Nonlinearity of constant ratio, $V_y = E_o$	$(K_mV_xV_y - E_o)/K_mV_x$ (V_y const) X_{NL}/K_mV_x
6. Y Nonlinearity	Numerator nonlinearity	$(K_mV_xV_y - E_o)/K_mV_x$ (V_x const) Y_{NL}/K_mV_x
C. Dynamic Error (incremental)		
7. Bandwidth (-3dB frequency)	Bandwidth (—3dB frequency)	$f_{-3dB}V_x/K$

Figure 13 is a graph of incremental frequency response for two representative dividers at unity gain ($K/V_X = 1$) and higher gains within their respective practical ranges of division.

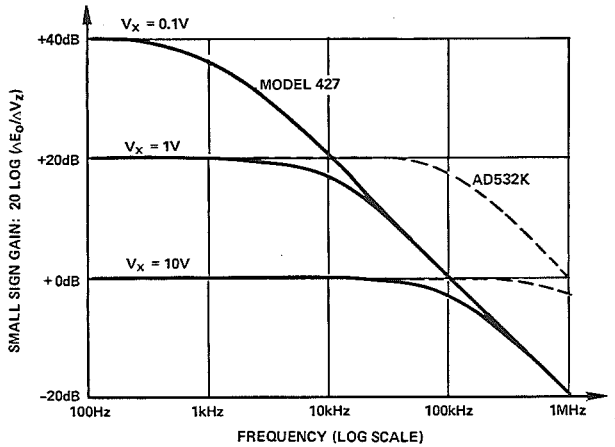


Figure 13. Small-signal response as a function of denominator voltage for two multiplier-dividers connected in the "divide" mode

Since "inverted-multiplier" dividers have such limited performance, and present many pitfalls to the unwary designer, their use (involving low-cost general-purpose IC multipliers, at any rate) should be limited to such applications as linearizing, that involve a small dynamic range of denominator variation, and where lowest device cost is essential. The following guidelines are offered to make the best of a "bad thing."

1. Avoid using an "inverted-multiplier" unless low cost is essential and adequate pains can be taken to be sure of best results. Be prepared to consider as an alternative a specialized internally-trimmed 1- or 2-quadrant divider that has guaranteed-maximum error specifications over the expected denominator and ambient-temperature ranges.

2. If a general-purpose multiplier/divider is used as a divider, some thought should be given to performance, primarily in the areas of bandwidth, accuracy, and drift errors vs. denominator. For many applications, a faster or more-accurate multiplier will be

found necessary than may have been expected at first. If possible, external trims should be provided for input and output offsets, and the trim procedure outlined in *Testing and Adjusting Dividers* (later in this chapter) should be followed. The following specific points should be considered in applying Guideline 2.

A. Allow for increased error, at room temperature, as the denominator magnitude decreases. Always use preamplification for small signals to scale the denominator to 10V full scale; use the smallest dynamic range of denominator that the application will tolerate. Use a multiplier/divider having higher accuracy than is required at full-scale denominator: As a rule-of-thumb, a multiplier used for division will have about 3X larger total error (than multiplication) at V_X = 1V, if external trimming is used. Without external trimming, it will have 10X greater total error. For a graphical comparison of divider errors, among a number of devices, see Figure 24.

Example: A system requires a 2-quadrant divider with less than 1% (of 10V full-scale) error and a 1V to 10V denominator range. Choose a multiplier with approximately (1/3)% error (e.g., one might consider 427J–0.25% or 426L–0.5%) if trimming is permissible (one objection to trimming might be that it would complicate field replacement, since each replacement unit would have to be "tweaked-in"). If trimming is excluded, a multiplier divider with (1/10)% error would be required; stated another way, a 0.1% multiplier/divider will have a ±1% = 0.1V error in the *divide* mode with a 1V denominator.

B. Allow for increased offset and scale-factor drift, and increased noise, at decreased denominator magnitudes. As discussed earlier, the noise and offset drift errors are inversely proportional to denominator magnitude. Furthermore, the scale factor will also drift, because of the effect of denominator drift on the magnitude of the apparent scale factor.

Example: System requirements dictate a maximum offset of ±20mV for a 10:1 denominator range and ±5°C temperature range. Allowable multiplier offset drift is:

$$\frac{20\text{mV}}{5^\circ\text{C}} \times \frac{1\text{V}}{10\text{V}} = 0.4\text{mV}/^\circ\text{C}$$

Figures 26 and 29 provide information about the drift of specific devices with temperature, as a function of denominator voltage.

C. Allow for decreased bandwidth as denominator decreases. The small-signal bandwidth of all "inverted-multiplier" dividers is directly dependent on denominator magnitude. Since most of these dividers have -6dB/octave gain rolloff, the bandwidth is linearly related to the denominator level:

$$f_c = f_{c_{max}} \frac{V_x}{K}$$

where f_c is the -3dB bandwidth, and K is the divider scale factor, usually 10V.

Bandwidth vs. denominator data for several dividers are plotted in Figures 27 and 28.

D. Provide adjustments for numerator, denominator, and output offsets, if possible. A scale-factor trim may be used, but it is often unnecessary, because scale factor can be adjusted elsewhere in the system, as a gain adjustment on either input variable or at the destination of the output. For best accuracy, trim the divider according to the procedure outlined in *Testing and Adjusting Dividers*. If all three offset trims cannot be used, choose at least one of the following:

1. Numerator offset trim (Z_{os} or E_{os}) controls the shift in output offset with varying denominator. This trim is essential when the denominator range is greater than 3:1.

2. Output offset (Y_{os} if the feedback is via the Y-input of the multiplier) controls the fixed portion of the total output offset. The Y_{os} adjustment can be used to minimize the total output offset for a denominator range of 3:1 or less.

3. Denominator offset (X_{os} if the X input is the denominator) controls the change in apparent scale factor as the denominator is varied. The X_{os} trim can be eliminated if the range of V_x is expected to be limited to about 3:1 (from full-scale input).

2-QUADRANT VARIABLE-TRANSCONDUCTANCE DIVIDER

The direct variable-transconductance divider is based on the linearized variable-transconductance multiplier circuit explained in Chapter 3.2. The basic input/output transfer equation for the multiplier circuit is

$$E_o = \frac{V_x V_y}{K_m I_{REF}} \tag{7}$$

If I_{REF} is used as an input, then the circuit becomes a 3-input simultaneous multiplier-divider. The schematic of the 2-quadrant variable-transconductance divider appears in Figure 14, which is

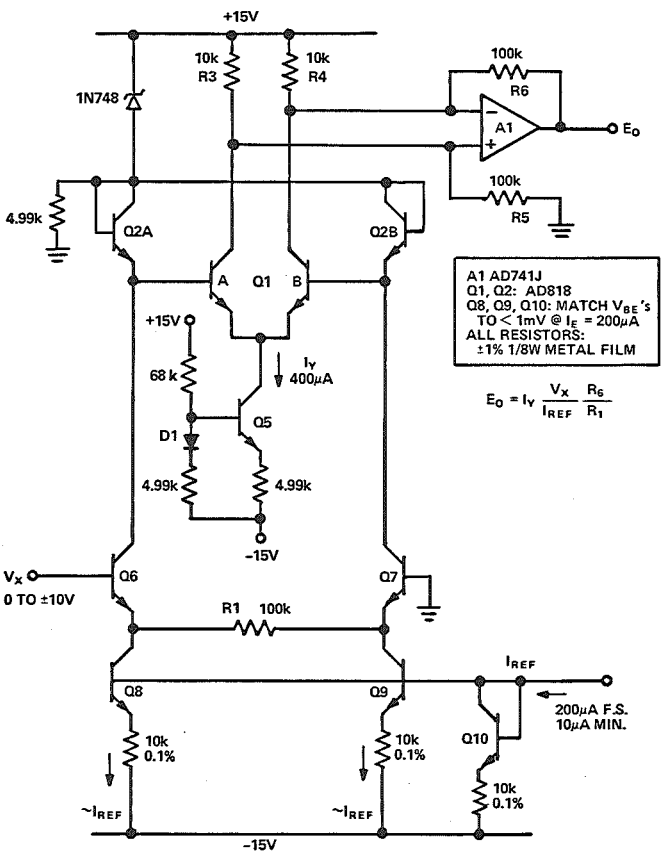


Figure 14. Practical two-quadrant variable-transconductance divider

quite similar to Figure 10, Chapter 3-2. The current I_{REF} determines the standby current through the diode-connected transistors (Q2). As I_{REF} increases, the dynamic resistance of the diodes decreases

$$r_E = \frac{kT}{qI_{REF}} \tag{8}$$

The X input voltage produces a division of the total current between the two diodes (and hence a greater voltage drop across one than across the other). The difference current is

$$\Delta I = \frac{V_x}{R_1} \tag{9}$$

Clearly, if an increase in I_{REF} produces lower resistance in the diodes, the incremental voltage drops across each caused by ΔI will decrease. Conversely, as I_{REF} decreases, the change of voltage across the diodes, as a function of V_x, increases.

The difference in diode voltage is amplified at fixed gain (assuming constant Y input) by the differential pair Q1 A-B. Thus, the overall gain is inversely dependent on I_{REF} (as Eq. 7 indicates), and the ideal division equation will be followed over a fairly wide range of I_{REF}, typically 20:1. The dynamic range of response to I_{REF} is limited primarily by the β's of the diodes and differential transistors, and by the increase in emitter resistance of the X-input amplifier as I_{REF} is reduced.

This version of the variable-transconductance divider has very wide bandwidth; up to 5MHz can be achieved, and the bandwidth is not strongly dependent on the denominator magnitude. For instance, the AD531 integrated-circuit multiplier-divider uses just this scheme for division – it has a nearly constant bandwidth of 750kHz for a 20:1 range of denominator. Discrete versions of this divider can have 5MHz bandwidth over a 10:1 range of denominator. The accuracy of this circuit can be reasonably good, with errors of about 0.5% at $I_{REF} = 200\mu A$ and 2% at $I_{REF} = 10\mu A$.

IMPROVED 2-QUADRANT VARIABLE-TRANSCONDUCTANCE DIVIDER

The accuracy and dynamic range of the 2-quadrant transconductance divider described above can be greatly improved by a few refinements. The modified circuit can divide accurately over a 1000:1 (10mV to 10V) denominator range and can easily achieve less than ±0.5% error over a 100:1 range without requiring external trimming. In addition, the numerator nonlinearity is extremely low, ±0.05%, and independent of denominator magnitude.

The variable-transconductance circuit can also be considered as a log circuit and analyzed in terms of the logarithmic behavior of its elements, since the slope of the natural logarithm of a number is inversely dependent on the magnitude of the number (r_E in Eq. 8 is such a slope).

$$\frac{d(\ln x)}{dx} = \frac{1}{x} \tag{10}$$

$$\int \frac{1}{x} dx = \ln x + C \tag{11}$$

In the variable-transconductance divider, the denominator controls the magnitude of x (I_{REF}) and therefore the "gain" for the numerator, or V_x (in Fig. 14) signal.

The improved 2-quadrant divider uses a differential log-antilog function to directly synthesize the division function. A simplified schematic of the divider circuit, similar to that of the Model 436 Divider, is shown in Figure 15.

The denominator voltage, V_x is applied to two symmetrically-arranged transdiode log circuits (see Chapter 3-1), Q1A-A1 & Q1B-A2, through R1 and R2. The numerator voltage, V_z, is applied to Q1A-A1 directly through R3, and inverted ($-V_z$) through R4 to Q1B-A2.

The numerator, V_z, and denominator, V_x, voltages are converted to currents that are summed at the inputs of A1 and A2. Since R3

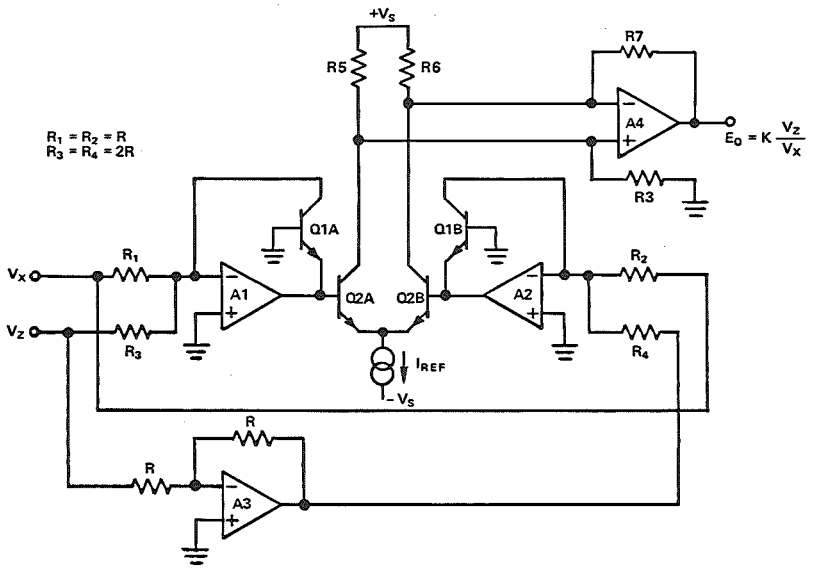


Figure 15. Two-quadrant variable-transconductance divider

and R4 are 2X R1 and R2, the currents in Q1A and Q1B are proportional to $V_x + \frac{1}{2}V_z$ and $V_x - \frac{1}{2}V_z$. The output voltages of A1 and A2 are therefore proportional to the logarithms of the sums and differences, since

$$V_{EB} = -\frac{kT}{q} \ln \frac{I_c}{a_N I_{ES}} \qquad (V_{cb} = 0) \qquad (12)$$

The voltages at the emitters of Q1A and Q1B are applied to a differential antilog circuit, Q2A-Q2B, which operates at a constant sum (reference current I_{REF}). The form of the currents to be differenced in A4 is

$$I_c = a_N I_{ES} (e^{qV_{BE}/kT} - 1) \qquad (13)$$

assuming that $V_{CB} = 0$.

The difference of the collector currents of Q2A-Q2B is converted to an output voltage $2\ \Delta I_c\ R_7$, by the collector-loading and

summing resistors R5 to R8, and amplifier A4. By an analysis similar to that for the Gilbert transconductance multiplier in Chapter 3-2, it is fairly easy to show that

$$\Delta I_c = \frac{I_{REF}}{2} \cdot \frac{I_z}{I_x} \tag{14}$$

where

$$I_z = \frac{V_z}{2R}, \quad I_x = \frac{V_x}{R} \tag{15}$$

$$E_o = \frac{R_7 I_{REF}}{2} \cdot \frac{V_z}{V_x}, \quad |I_z| < |I_x| \tag{16}$$

The ratio relationship between V_z and V_x is precise to the extent that the transistors obey the ideal junction equations, and the effects of the op-amp input offset currents (A1, A2) can be ignored. Practically speaking, the limitations of the amplifiers are more significant than those of the transistors, since (it has been shown that) the transistors follow the ideal current-voltage relationship from at least 10pA to 100μA (7 decades, or a dynamic range of 10^7), while low-cost bipolar-input amplifiers have input offset currents of 0.5nA (AD308) to 5nA (AD201A). The dynamic range for 1% error, due to op-amp input current, is then 0.01 X 100μA/0.5nA, or 2000:1.

The symmetrical arrangement of the circuit is essential to its operation in two quadrants with low distortion. In fact, all currents in symmetrical paths must be perfectly balanced, or second-harmonic distortion will be introduced into the numerator and denominator. Interestingly, the oscilloscope photographs showing numerator nonlinearity, Figures 16 & 17, show only third-order (S-shaped) distortion, due to emitter resistance in Q2A&B. Matching of the X and Z input resistors, and the balanced circuit configuration combine to eliminate second-order distortion in the input log amplifiers.

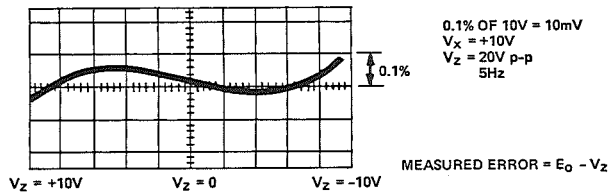


Figure 16. Nonlinearity of two-quadrant divider as a function of numerator input. Denominator is constant at +10V

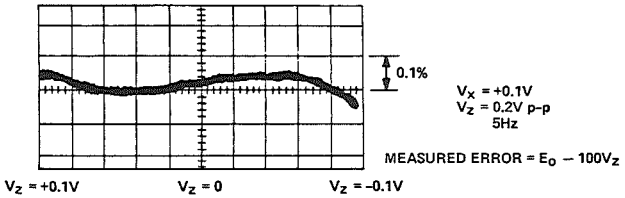


Figure 17. Same as Figure 16, but denominator is 0.1V; numerator swing is ±0.1V for full-scale ±10V output swing

The bandwidth of this variable-transconductance divider is not strongly dependent on the denominator magnitude, as Figure 18 shows. The reason for this is that the output section, Q2A&B and A4, operate at an essentially constant high (200μA) current level, while the log amps, A1 & A2, operate in a quasi-current mode, with very low (~0.3V) output swings and high loop gain.

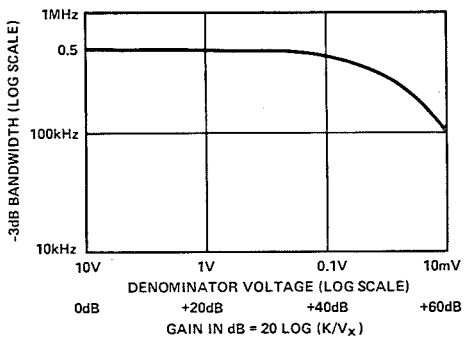


Figure 18. Small-signal bandwidth (-3dB) of the two-quadrant variable-transconductance divider, as a function of denominator voltage.

To summarize, the wide dynamic range, low errors, and wide bandwidth of the variable-transconductance divider are the result of four features of the circuit:

1. Numerator and denominator inputs to summing junctions of operational amplifiers ensure lowest-possible input offset, noise, and drift. The input errors are still magnified by K/denominator at the output, but the input drifts are less than $10\mu V/^{\circ}C$, resulting in an output offset drift of $1mV/^{\circ}C$ for $V_x = K/100$.

2. Fidelity to the Division function: The log-antilog synthesis of the linear ratio is theoretically exact for all finite denominators, $0 < x < \infty$. The only limitation in dynamic range lies in deviations from ideal performance of the hardware; the transistors operate over 7 decades, the op amps over 3 decades (limited by offsets and drift). Errors less than 0.5% of full scale can be achieved over a 100:1 denominator range. Figure 19 shows the effect of denominator voltage on total error.

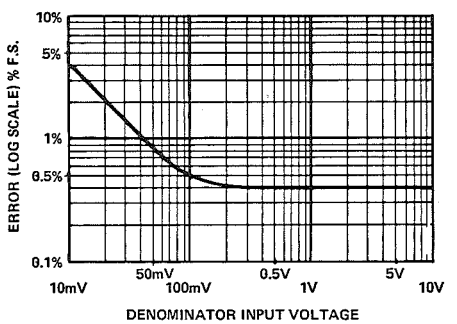


Figure 19. Total error of the two-quadrant variable-transconductance divider, as a function of denominator voltage

3. Low numerator distortion (0.05%): The symmetry of the circuit (and available components) permit low distortion, independent of the denominator (Figs. 16 and 17).

4. Wide bandwidth (500kHz), low output-stage drift: Operation of the output section at a constant high current level ($200\mu A$) produces wide bandwidth and low output-stage offset drift. The small internal voltage swings and high loop gain of the input log amplifiers reduce the dependence of bandwidth on the denominator, as Figure 18 demonstrates.

Besides all its performance advantages, the concept and circuitry of the variable-transconductance divider are relatively simple, compared to almost any other 2-quadrant-divider approach.

LOG-ANTILOG DIVIDER

The log-antilog multiplier circuit discussed earlier (Chapter 3-2, Figure 20) also makes an excellent divider. In fact, it is probably the most accurate one-quadrant divider circuit available.

If the V_{REF} input of the log-antilog multiplier circuit is used as a denominator and relabeled V_x, and the X input is relabeled V_z, the circuit becomes Figure 20 (this chapter), with the transfer function

$$E_o = \frac{V_y V_z}{V_x} \tag{17}$$

An additional advantage of the log-antilog circuit is that it is a three-input circuit that performs multiplication and division simultaneously and with equal accuracy, greatly increasing its usefulness for a wide variety of applications, such as implicit solutions of all types, including square roots, rms, and vector equations (see Chapters 2-3, 2-5, and 3-6). For square-rooting, with wide dynamic range, one simply connects the output to the denominator input; then $E_o = 10V_z/E_o = \sqrt{10V_z}$.

In effect, the circuit will do the work of two independent one-quadrant multiplier/dividers, thus simplifying the implementation of equations requiring multiplication and division.

Circuit Description

The operation of the log-antilog multiplier-divider circuit, Figure 20, has been described in detail in Chapter 3-2; only a brief summary will be given here.

The three input variables, X, Y, and Z (V_x or I_x, V_y or I_y, V_z or I_z), are applied to three independent transdiode log amplifiers, A1-Q1A, A2-Q2A, and A3-Q2B. The outputs of the log amplifiers,

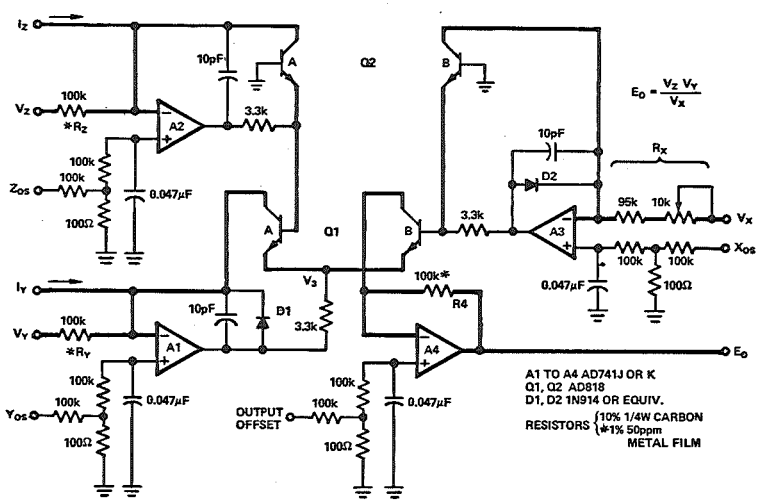


Figure 20. Log-antilog divider-multiplier. Heavy lines trace signal paths.

equal to the emitter-base voltages of the transistors, are proportional to the logarithms of the input variables. For example, for V_Z

$$-V_A = \frac{kT}{q} \ln \frac{V_z}{R_z I_{ES}} \tag{18}$$

The sum of the base-emitter voltages around the loop from the base of Q2A to the base of Q2B is

$$0 = V_{BE2A} + V_{BE1A} - V_{BE1B} - V_{BE2B} \tag{19}$$

Substituting the log relationships between input currents and base-emitter voltages, and cancelling matching constants, as discussed in Chapter 3-2,

$$\ln \frac{V_z}{R_z I_o} + \ln \frac{V_y}{R_y I_o} - \ln \frac{I_{c1B}}{I_o} - \ln \frac{V_x}{R_x I_o} = 0 \tag{20}$$

Since the sum of the logarithms is equal to the log of the product of the summed arguments, and the difference of logs is equal to the log of the ratio of the arguments,

$$\ln \frac{I_{c1B}}{I_o} = \ln \left[\frac{V_z V_y}{I_o V_x} \cdot \frac{R_x}{R_z R_y} \right] \tag{21}$$

and

$$I_{c1B} = \frac{V_z V_y}{V_x} \cdot \frac{R_x}{R_z R_y} \tag{22}$$

R4 in the feedback circuit of A4 converts the collector current of Q1B to the output voltage

$$E_o = \frac{R_4 R_x}{R_z R_y} \cdot \frac{V_z V_y}{V_x} = K \frac{V_z V_y}{V_x} \tag{23}$$

Note that the output is independent of temperature, and that the scale factor is determined by only four resistors, which can easily be matched, both for initial value and for temperature coefficient.

Performance of the Log-Antilog Divider

The log-antilog circuit is capable of high accuracy, wide-dynamic-range division and multiplication for three reasons:

1. Very low errors at the signal inputs: The input amplifiers A1, A2, A3 can have offsets less than 100μV and input currents of 5nA or less, with offset voltage drifts of 10μV/°C or less. This results in an input error of 0.1% or less for inputs as low as 100mV.

2. Use of summation of the logarithms of currents allows a wide dynamic range; the V_{BE} of a log transistor changes only about 60mV per decade at room temperature, thus many decades may be accommodated without danger of saturation or other problems inherent in dealing with wide-dynamic-range signals directly. In fact, the dynamic range is limited primarily by the offset current of the input amplifiers A1 to A3 (0.1nA typically),

that sets a lower limit on the input voltage or current in low-cost general-purpose devices using bipolar transistors. The high end of the dynamic range is limited to 1mA or less (usually 100μA) by emitter and base resistances in the log transistors.

3. Low nonlinearity due to excellent log-conformity of monolithic dual transistors for currents between 1nA and 100μA: Overall nonlinearity of 0.05% can be achieved in a properly designed circuit.

As an indication of the accuracy and dynamic range that can be achieved in practice, Figure 21 shows the error (as a function of denominator) for the Analog Devices 434 log-antilog divider. The 434B typically has less than 0.2% error over 2 decades of denominator, and 1% or less error over 3 decades – without any external adjustment. If the numerator and denominator input offsets are adjusted externally, the error can be held to 0.2% over three decades: 1000-to-1.

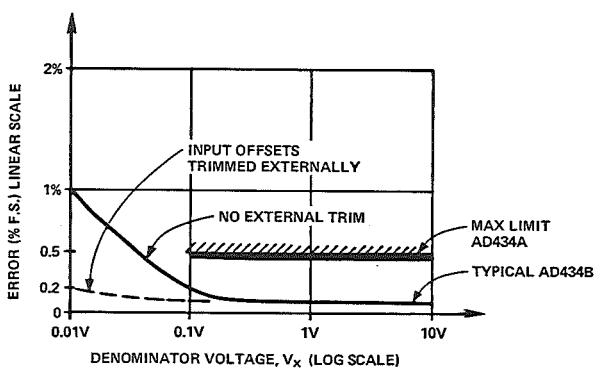


Figure 21. Log-antilog divider: total error as a function of denominator voltage

In common with other logarithmic circuits, the bandwidth of the log-antilog divider is dependent on input signal magnitude. For instance, if the bandwidth is 100kHz for a 10V numerator input, it will be about 10kHz for a 1V numerator input. This is a direct result of the change in loop gain with signal level in transdiode log amplifiers.

Using a 1-Quadrant Analog Divider in 2 Quadrants

A one-quadrant divider, such as the log-antilog circuit discussed here, will accept only single-polarity numerator and denominator inputs. In many cases, it is essential to have a two-quadrant divider that will accept a bipolar numerator (e.g., a sine-wave centered around zero volts) and a unipolar denominator.

Any one-quadrant divider will work as a two-quadrant divider if a fraction of the denominator input is used to bias or offset the numerator input, as outlined in Figure 22. The divider circuit itself remains unipolar, with an output offset of ½ of full scale. The offset can be removed by subtraction (Figure 22) or by ac coupling (Figure 23) to yield an output centered about zero.

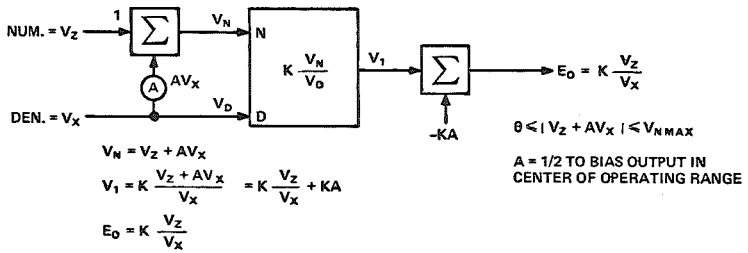


Figure 22. Offsetting a 1-quadrant divider for operation in two quadrants

In general, the performance of the "offset" two-quadrant divider will not be as good as the performance of the single-quadrant divider, but it will be much better in terms of accuracy and dynamic range than the two-quadrant "inverted-multiplier" dividers.

If the log-antilog divider is offset for 2-quadrant operation, the performance will be reduced in two areas:

1. Bandwidth: The bandwidth will depend on both numerator and denominator levels. As the numerator swings towards its negative extremity, the magnitude of the input to the circuit tends towards zero. This reduces the bandwidth and can cause distortion on negative half cycles.

2. Output offset variation with denominator level: Since the zero-output point of the offset divider is really the half-scale point of the basic circuit, the nonlinearity of the circuit will cause the offset to shift with denominator (a common problem with one-quadrant circuits that are offset to provide a semblance of 2-quadrant performance).

Measurement of the performance of the 434A log-antilog divider in the circuit of Figure 23 typically yields the following results:

Denominator Voltage (V_X)	Output Error Variation from value @ V_X = 10V	-3dB Bandwidth (Numerator or Denominator)
+10	0	55kHz
+1	+20mV	5.5kHz
+0.1	+25mV	550Hz

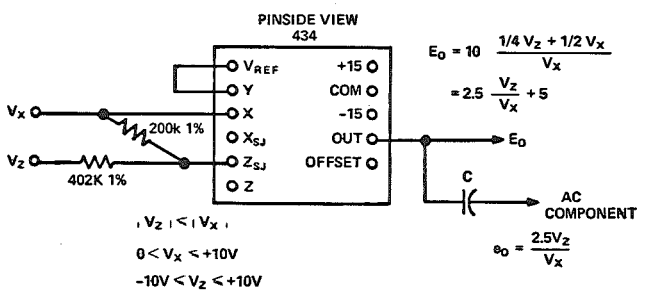


Figure 23. Offsetting AD434 for two-quadrant operation

A one-quadrant divider may be used in two quadrants if it is preceded by an absolute-value circuit having polarity sensing, and if the output is applied to a sign-magnitude circuit (e.g., Chapter 3-5, Figure 15) to restore the polarity. While eliminating the offset problem, this circuit (using a log-antilog divider) will still have bandwidth difficulties, because the signal will slow down each time the numerator crosses through zero.

DIVIDER SPECIFICATIONS

Analog dividers have not, in the past, been as thoroughly specified as analog multipliers. There are at least two reasons for this state of affairs:

1. Until recently, division existed principally as a form of application of a multiplier that could be connected as a divider. Most suppliers of modular and IC multiplier-dividers have placed primary emphasis on the underlying device, the multiplier.

2. Until recently, most analog dividers have had poor to fair performance, for the reasons discussed earlier in this chapter. Since their usefulness was somewhat limited, many manufacturers concluded that there was little point to attempting complete characterization so early in the game.

In this section, we shall seek to provide a format that embraces a large number of the key accuracy and dynamic specifications, and shows their relationship to the denominator voltage. The comparative specifications of a representative variety of commercially-available divider circuits in use as of late 1973 are listed in Table 2. They include the errors at maximum and minimum useful denominator values, and are accompanied by graphs (Figures 24-30) which show the errors as functions of the denominator. The dividers listed in the table employ all three of the techniques discussed in this chapter:

1. *"Inverted-Multiplier" Divider* The AD532K IC multiplier (connected as shown in Figure 31) is a low-cost transconductance multiplier/divider, internally trimmed for multiplication with less than 1% error; external trims are essential for best performance as a divider. Model 427J (connected as shown in Figure 32) is a high-performance pulse-modulation multiplier/divider. Though one of the best "inverted-multiplier" dividers available, it still requires external trim adjustments to make best use of its excellent multiplying characteristics in division.

2. *Direct Variable-Transconductance Divider (2-Quadrant)* The AD531K (connected as shown in Figure 33) uses the basic transconductance cell (Figure 14). Its error is less than 1%, and it has a bandwidth somewhat less than 1MHz. It is the best IC divider available at this writing. Model 436 (connected as shown in Figure 34) uses the improved transconductance circuit of Figure 15 to achieve errors less than 0.5% *over a 100:1 dynamic range*, and 500kHz bandwidth. It requires no external trimming, but outperforms all other 2-quadrant dividers.

3. *Log-Antilog Divider* Model 434B (connected as shown in Figure 35) has the highest accuracy of any 1-quadrant divider available at this writing. It operates over a 100:1 range of denominator with a maximum error of 0.25%, without external trimming.

INTERPRETING THE SPECIFICATIONS

Transfer Function is the ideal relationship between the divider inputs and output, including the scale factor, which is either fixed or set at a nominal 10V. The AD532K can accept a differential denominator input (and the AD531K can accept a differential "X" numerator input), but it will be assumed that $X_1 = V_x$ and $X_2 = 0$ when considering the performance characteristics listed here. The 434B and AD531K can multiply and divide simultaneously, because of the three input variables. The specifications listed here will be considered for constant Y input equivalent to a 10V scale factor. The AD531K is assumed to be connected in the circuit of Figure 33, with a voltage input, V_D.

Quadrants of Operation defines whether the divider will accept a bipolar numerator (*two-quadrant*) or a unipolar numerator (*one-quadrant*). The denominator is limited to one polarity for virtually all analog dividers – including these. The denominator polarity differs from type to type; its polarity and range are given in the "Denominator, X" specification.

Total Error (accuracy) @ Maximum Denominator specifies the error, or difference between the actual and the theoretical output of the divider at full-scale denominator and (usually) full-scale output. As the denominator is decreased in magnitude from its full-scale value, the error increases (AD532K, 427J) or stays about the same (AD531K, 434, 436), as Figure 24 shows. As noted by the groupings of devices, the AD531K, AD532K, and 427J require 3 external adjustments to meet the typical figure for total error in Table 2 (the adjustment procedure is described in the *testing* section). This requirement is typical for all general-purpose multiplier/dividers. In contrast, the two specialized types are internally trimmed, and need no external trimming to meet the *maximum* error specifications listed in Table 2.

TABLE 2. SPECIFICATIONS OF DIVIDER CIRCUITS[1,2]

Parameter	WITH EXTERNAL TRIM		
	AD531K	AD532K	427J
Transfer Function	$\frac{10(X_1 - X_2)}{V_D}$	$\frac{10Z}{X_1 - X_2}$	$10\frac{Z}{X}$
Configuration (Figure)	33	31	32
Quadrants of Operation	2	2	2
Total Error (%), Max. Denominator (V) (Figure 24)	1, +10	1, −10	0.2, −10
Total Error (%), Min. Denominator (V)	3, 0.5	3, −1.0	2, −1.0
Small-signal Bandwidth (−3dB, kHz), Max. Denominator (V) (Figure 27)	1000, +10	1000, −10	100, −10
Bandwidth (−3dB, kHz), Min. Denominator (V)	1000, +0.5	100, −1.0	1, −0.1
Output Offset Drift (mV/°C), Max. Denominator (V) (Figure 28)	1, +10	1, −10	0.25, −10
Output Offset Drift (mV/°C), Min. Denominator (V)	2, +0.5	10, −0.5	25, −0.1
INPUT CHARACTERISTICS			
Numerator, Z			
Voltage Range (V)	±10	±10	±10
Maximum safe voltage	$\pm V_s$	$\pm V_s$	$\pm V_s$
Input Resistance (kΩ)	10MΩ("X")	36	33
Input Current (μA)	8*	10	3
Input Offset Voltage (μV)	N.S.†	N.S.†	N.S.†
Offset Voltage Drift (μV/°C)	N.S.†	N.S.†	N.S.†
Denominator, X			
Voltage Range to Meet Spec[3] (V)	N.S.†	N.S.†	N.S.†
Voltage Range to Meet Spec, External Trim (V)	+0.5 to +10	−1 to −10	−0.1 to −10
Maximum Safe Voltage	$\pm V_s$	$\pm V_s$	$\pm V_s$
Input Resistance (kΩ)	30	10MΩ	10
Input Current (μA)	0.5	3	3
Offset Voltage (μV)	N.S.	N.S.	N.S.
Offset Voltage Drift (μV/°C)	N.S.	N.S.	N.S.
OUTPUT CHARACTERISTICS			
Voltage Range (V, minimum)	±10	±10	±10
Current Range (mA, minimum)	±5	±5	±5
Resistance (Ω)	1.0	1.0	0.1
Capacitive Load (pF)	1000	1000	1000
POWER SUPPLY			
Specified Performance (V)	±15	±15	±15 ±1%
Operating (±V)	12–18	12–18	12–18
Quiescent Current (±mA)	4(AD531 only)	4	15
PHYSICAL SIZE (mm)	I.C.§	I.C. §	41 X 76 X 15
PRICE ($ U.S., 1-9)	45	36	159

NOTES

[1] All specifications typical at 25°C, ±15V supply, unless noted otherwise, circuit connected in divider configuration of Figures 31–35

[2] All errors specified in % are % of 10V Full Scale (1% = 0.1V)

[3] External trim not required to meet specs, except as noted

WITHOUT EXTERNAL TRIM[3]		
	436	434B
	$10\frac{Z}{X}$	$Y\frac{Z}{X}, 10\frac{Z}{X}$
	34	35
	2	1
	0.5, +10*	0.25, +10*
	0.5, +0.1*	0.25, +0.1*
	500, +10	100, +10
	300, +0.1	1, +0.1
	0.3, +10	0.1, +10
	1, +0.1	1, +0.1
	±10	0 to +10
	$\pm V_s$	$\pm V_s$
	10	100
	±0.1	±0.01
	±100*	±100*
	15	15
	+0.1 to +10	+0.1 to +10
	5mV to +10	5mV to +10
	$\pm V_s$	$\pm V_s$
	25	100
	0.1	0.01
	±100*	±100*
	15	15
	±10	±10
	±5	±5
	0.1	0.1
	1000	1000
	±15 ±3%	±15 ±3%
	12–18	12–18
	10	10
	38 X 38 X 15	38 X 38 X 15
	80 (Approx.)	87

*Maximum specification

†Not specified

§IC's may be available in choice of packages and chip form; consult product data sheets

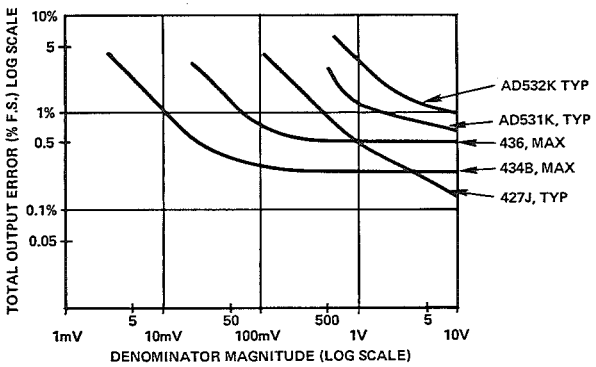


Figure 24. Total error vs. denominator at constant ratio = 10V full-scale output, 1% = 100mV

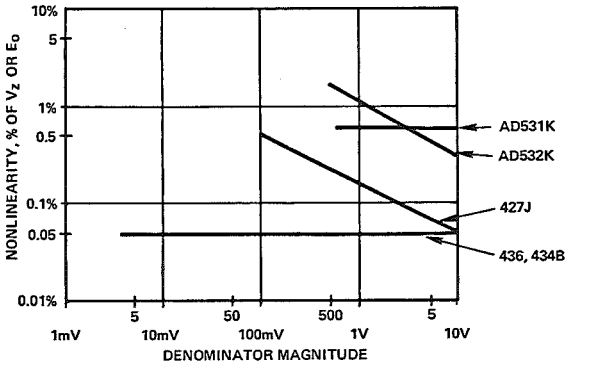


Figure 25. Nonlinearity (at constant denominator) vs. denominator, % of numerator (log scales)

The total error includes the errors from all sources, and so represents a worst-case condition. There are six major sources of error included:

1. Numerator nonlinearity (Figure 25)
2. Denominator nonlinearity
3. Scale-factor error
4. Numerator offset, referred to the output
5. Denominator offset, referred to the output
6. Output amplifier offset

Errors (3) through (6) can be theoretically adjusted to zero at a fixed temperature and denominator level, while the input nonlinearities are inherent and cannot be removed (except perhaps for some reduction of second-order error by the "cross-feed" technique discussed in 3-2, applied to divider-connected transconductance multipliers). Rather than specify each of these six errors individually, it is usually easier to measure the overall effect of the errors, which is by definition the total error.

Total Error at Minimum Denominator specifies the error, as just defined, at the minimum useful denominator magnitude. This represents the worst-case operating conditions for a divider, since the errors are at a maximum. The "inverted-multiplier" dividers, 427J and 532K, show the greatest increase of error at small denominator voltages, as might have been expected. The log-antilog and variable-transconductance dividers show no increase in the specified error, even with the denominator voltage at 1/100 of full scale, as one might have predicted from the analysis of these circuits.

The increase of error of the 532K and 427J is caused principally by the magnification of the numerator and denominator offsets by $10/V_X$, and by the denominator nonlinearity, which causes an apparent scale-factor error. The AD531K maintains error at the 1% level over a 10:1 range, then the error increases sharply due to decreasing current in the X input circuit, causing the gain to go to zero (Figure 9). The 436 and the 434B have very small (100μV) input offsets and very low nonlinearity; they have relatively-little difficulty with small denominator voltage.

Total-Error Drift (with Temperature) vs. Denominator. The change in total error per °C change in ambient temperature increases as the denominator decreases, as shown in Figure 26. This effect is more noticeable with the inverted-multiplier types, 427J and AD532K. The 434B and 436 show a slight increase in drift at the low end (100mV denominator).

"Total-error drift" is the sum of the total output-offset drift and scale-factor drift. The numerator and denominator nonlinearities are relatively insensitive to temperature.

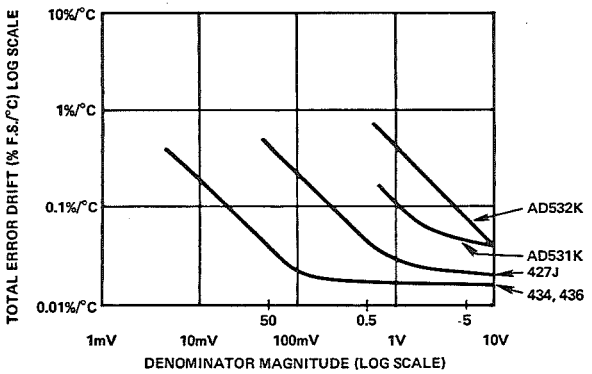


Figure 26. Total error drift vs. denominator voltage (% full-scale/°C)

Bandwidth (Small-Signal, -3dB) at Maximum Denominator: the frequency at which the numerator or denominator input-to-output "gain" is reduced to 70% (-3dB) of its dc value. The input must be "small," that is, less than 10% of either full-scale or denominator magnitude, to avoid excessive distortion (which would invalidate sine-wave analysis). The small-signal bandwidth of the 427, AD532K, and 434, are directly dependent on denominator magnitude, as the graph (Figure 27) shows.

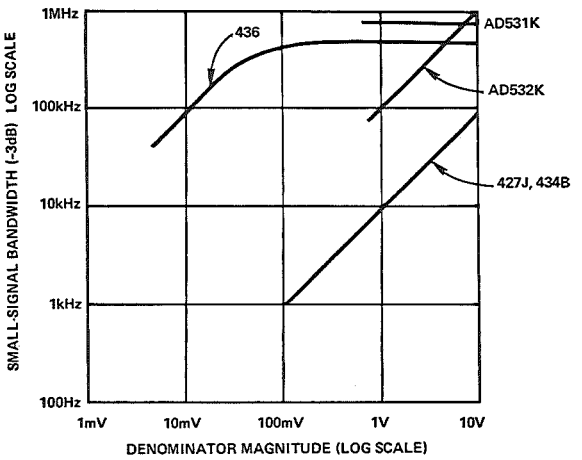


Figure 27. Bandwidth (-3dB) vs. denominator (K = 10V)

Interpreting denominator voltage as "1/gain," (Figure 28), the 436 is seen to be unique, because its bandwidth is essentially independent of denominator; it achieves a 30MHz gain-bandwidth product at 100mV denominator! Similarly, the AD531K has about 750kHz numerator bandwidth over a 20:1 denominator range; it is thus the fastest in terms of absolute bandwidth (over a limited range of denominator). (Gain = $10V/V_x = 10/0.1 = 100$; if bandwidth = 300kHz, Gain-bandwidth = $100 \times 0.3 \times 10^6$ = 30MHz.)

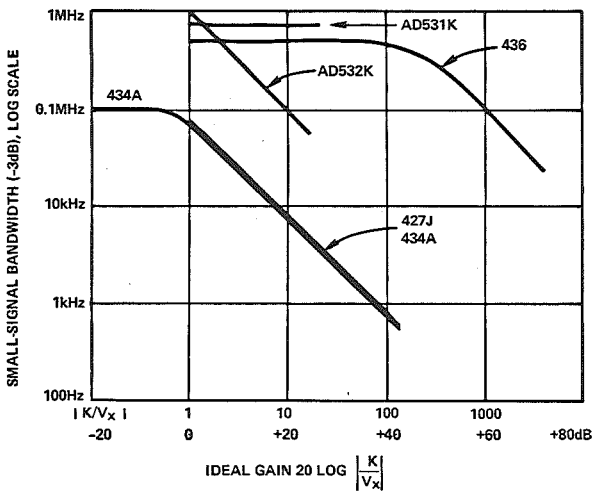


Figure 28. Bandwidth (-3dB) vs. gain (K/V_X)

Output Offset Drift vs. Denominator: The rate at which the total output offset changes with temperature, as a function of the denominator. The two components of this drift are numerator-input offset drift, multiplied by gain (K/V_x), and output-stage offset drift. As Figure 29 shows, the 427, 434, and 436 have drifts of about 0.2mV/°C at V_x = 10V, while the AD532K drifts at about 1mV/°C. The drift of the 427 and AD532K increase as the denominator is reduced, because the numerator offset drift is greater than the output-stage drift; hence the sum is dominated by the 1/X relationship. Since the numerator offset drift of the 434 and 436 is small (about 10μV/°C, compared to the output-stage drift of 300μV/°C – the total offset drift at G = 1 or V_x = 10V), the total output drift increases by only a factor of 2 for a 30:1

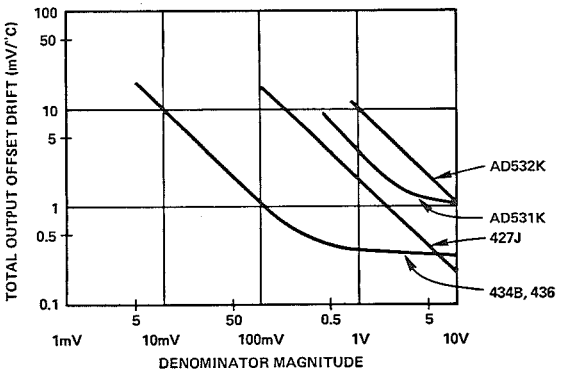


Figure 29. Total output offset drift vs. denominator voltage (log scales)

change in denominator. The AD531K offset drift is almost independent of temperature, but it is not as low as for the 434 and 436; however, it is much lower than for any other IC.

The total output offset drift is

$$\frac{\Delta V_{os}}{\Delta T} = \frac{K}{V_x}\frac{\Delta Z_{os}}{\Delta T} + \frac{\Delta Y_{os}}{\Delta T}$$

Output Noise vs. Denominator Figure 30 shows the relationship between the rms value of noise at the divider's output, in a constant bandwidth of 5Hz to 10kHz, and denominator magnitude. The total noise at the output is essentially

$$V_N = \sqrt{\left[E_{Nz}\frac{K}{V_x}\right]^2 + \left[E_{Nx}\frac{K}{V_x}\right]^2 + E_{No}^2}$$

where

E_{Nz} = equivalent numerator input noise: Vrms, 5Hz to 10kHz

E_{Nx} = equivalent denominator input noise: Vrms, 5Hz to 10kHz

E_{No} = equivalent output-stage noise: Vrms, 5Hz to 10kHz

K = scale factor = 10V

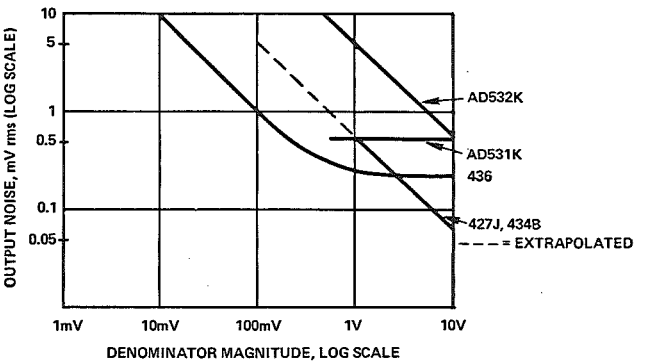


Figure 30. Output noise vs. denominator (5Hz to 10kHz bandwidth)

The 436 has the best overall noise performance, while the 427 and 434 are quieter for denominator voltage in the range 2V to 10V. As a general-purpose multiplier/divider, the AD532K is reasonably quiet; the AD531K output noise is almost independent of denominator level. If "peak-to-peak" noise is defined as 6X rms, 1mV rms = 6mV peak-to-peak.

Input Characteristics

These specifications define the input voltage range and errors at the numerator and denominator inputs.

Numerator (Z) Voltage Range is the maximum span of numerator voltage for which the error specifications apply. The numerator voltage is limited to a magnitude less than or equal to the denominator voltage for the dividers described here* (see Figures 2 and 3). The AD532K, AD531K, 427J and 436 will accept positive and negative numerator voltages (i.e., they are 2-quadrant devices), but the 434 is limited to positive numerators (1 quadrant).

Numerator: Maximum Safe Voltage is the maximum that can be applied to the divider input continuously without causing damage.

*But K may be scaled for <10V for the AD531 and the 434; and the numerator may exceed the denominator by the factor $E_{O_{max}}/K$.

Numerator: Input Resistance is the effective input resistance between the numerator input terminal(s) and power-supply common. The input resistance ranges from 10kΩ on the 436 to 10MΩ for the AD531K. The resistance of the signal source should be 0.1% or less of the numerator input resistance to minimize variation of scale factor.

Numerator Input Current is the bias current flowing into or out of the numerator terminal, with $V_Z = 0$. Usually, this is a negligible source of error, even for the AD532K, but it should be considered in the choice of the resistance-to-ground for applications where the inputs are to be capacitance-coupled.

Z-Input Offset Voltage: The numerator offset is not specified for general-purpose multiplier/dividers (427J, AD531K, and AD532K). The 100μV Z-offset of the 436 and 434B will cause an error of only 0.1% at 100mV input; the error can be further reduced by externally trimming.

Z-Input Offset-Voltage Drift characterizes the sensitivity of the Z-input offset to temperature. It is not usually specified (at this writing), but it is nevertheless a useful number, since the numerator offset drift is the primary source of output offset drift for values of denominator voltage substantially less than full-scale.

$$\text{Output offset drift} = \frac{K}{V_X}\frac{\Delta Z_{os}}{\Delta T} + \frac{\Delta E_{os}}{\Delta T}$$

Denominator, X, Voltage Range to Meet Specifications (Without External Trim) is the maximum span of denominator voltage for which the specified accuracy is maintained, with no external adjustment of offsets or scale factor. Since the AD531K, AD532K, and 427J require trimming for reasonable performance as dividers, no limit is specified for them. The 436 and 434B will operate over a range of denominator exceeding 100:1 with low error.

Denominator Range to Meet Specifications With External Trim: Trimming the offsets expands the dynamic range of the 436 and 434 to 2000:1, and provides a reasonable dynamic range for the 427, AD531K, and AD532K. Note that the 427 and AD532K

require negative denominators, while the 434B and 436 require positive denominators. The AD532K will accept positive denominator voltage if the input terminals (X_1 and X_2) are interchanged.

Maximum Safe Denominator Voltage is the maximum voltage that can be applied to the divider input continuously without causing damage.

Denominator Input Resistance: The AD532K has a very high input resistance (3MΩ), while the other three range between 25 and 100kΩ. All five types should be driven from sources with low resistance to minimize source-loading errors. The 3μA typical input current of the AD532K partially offsets the advantage of its high input resistance for source resistances of 10kΩ or more.

Denominator Input Current is the current flowing into or out of the denominator terminal with $V_x = 0V$.

Denominator Offset Voltage is a constant offset voltage effectively in series with the denominator input. The low offset of the 436 and 434 causes minimal change in apparent scale factor over a 100:1 denominator range:

$$\text{Error @ } V_x = 10V;\ \frac{10^{-4}}{10} \cdot 100\% = 0.001\%$$

$$\text{Error @ } V_x = 0.1V;\ \frac{10^{-4}}{0.1} \cdot 100\% = 0.1\%$$

Denominator Offset-Voltage Drift characterizes the sensitivity of the denominator offset drift to temperature. The specified $\Delta X_{os}/\Delta T$ of 15μV/°C for the 436 and 434B can cause a change in error of 0.7% over a 100:1 denominator range, and 0° to 70°C temperature range.

Output Characteristics

This group of specifications describe the output terminal properties of the divider.

Voltage and Current Range: The two-quadrant dividers, AD531K, AD532K, 427J, and 436 will supply a minimum of ±10V at ±5mA

at their outputs. The one-quadrant 434 swings a minimum of 0 to +10V at 5mA. Types requiring an external loop closure around the output amplifier can employ current boosters "inside the loop" to beef up the output for output current beyond 5mA.

Output Resistance: All five dividers have low-impedance outputs, resulting in minimal change in output voltage as load current is changed. However, since output impedance is affected by loop gain, the general-purpose multipliers used as "inverted-multiplier" dividers will suffer an increase of output impedance as denominator decreases.

Capacitive Load is the minimum amount of capacitance that can be connected directly between the divider output terminal and ground without causing the device to oscillate.

Power Supply

Specified Performance: The power-supply voltage and tolerance required for the divider to meet its accuracy specifications. The design-center power-supply voltage for all five types is ±15V.

Power Supply Operating Range is the range of power-supply voltage that the divider will accept and still operate as a divider. If external trims are used, the circuit can usually be adjusted to meet the same accuracy specifications as for ±15V supply.

Quiescent Current is the current drawn from the power supplies at zero output voltage and current. The quiescent current-drain will be augmented by the load current, since the output amplifiers have "Class B" output stages.

Physical Size: The IC's (AD531K, AD532K) are by far the smallest, and the pulse-modulation multiplier/divider, 427J, is the largest. IC types are available in hermetically-sealed ceramic 14-pin dual in-line packages, and the AD532 is also available in the hermetic TO-100 10-pin metal can; IC types may also be made available in chip form for applications requiring hybrid construction.

*Price** The IC's are the least expensive, but they offer the lowest performance (except for speed of the AD531K), and trims are required for reasonable performance. Surprisingly, the most-expensive multiplier/divider, 427J, does not offer the highest performance as a divider. The high-performance 436 and 434B outperform the 427, at lower cost, but are not as inexpensive as the IC types. If one considers the fact that the 436 and 434 have excellent performance without external adjustments, and even

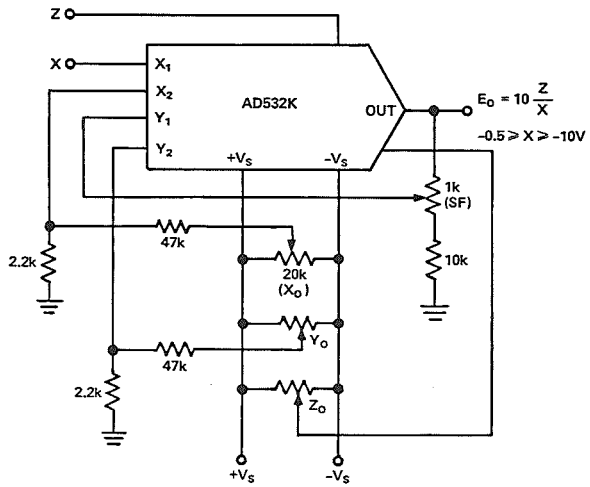


Figure 31. AD532K divider circuit (inverted multiplier)

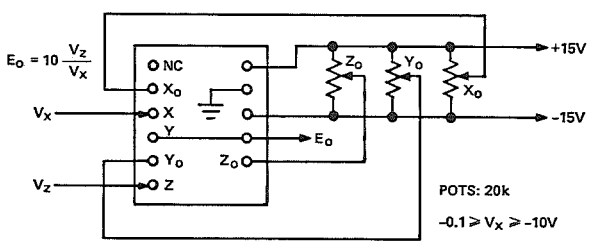


Figure 32. 427J divider pin connections (inverted multiplier), pinside view

*Summer, 1973. Price is listed as a measure of relative cost, not primarily as a commercial inducement. Those interested further should consult recent Product Guides or price lists, or the nearest Sales office, since (a) prices are subject to change, and (b) IC prices are more so.

better performance when "tweaked-up," and that the 434 multiplies and divides simultaneously, it may turn out that the 434 and 436 are less expensive to use than IC's in many applications.

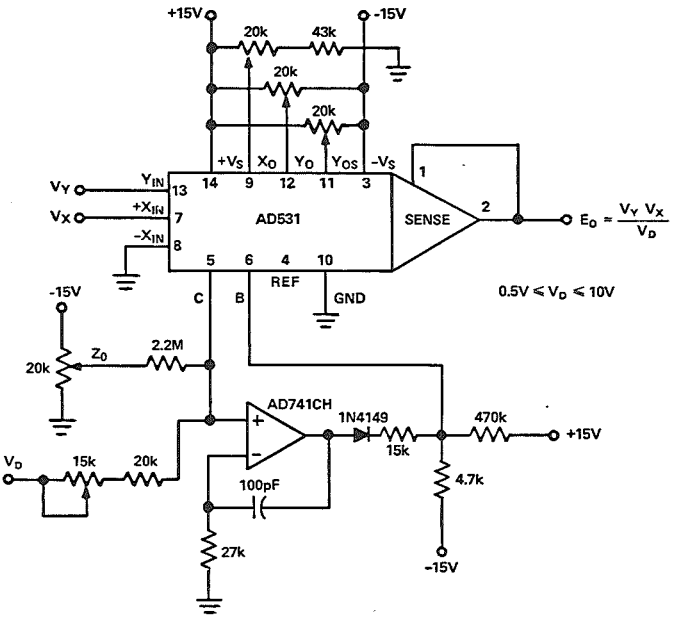


Figure 33. AD531K divider circuit — direct variable — transconductance (circuit for voltage input to denominator)

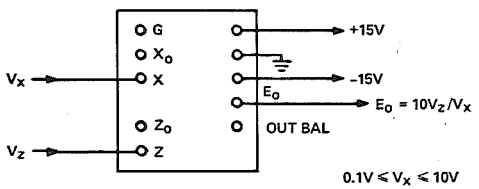


Figure 34. 436 divider connections, pinside view (high performance 2-quadrant variable transconductance)

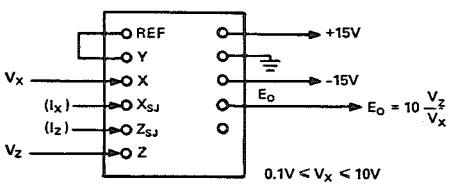


Figure 35. 434B divider pin connections (log-antilog), pinside view

TESTING AND ADJUSTING ANALOG DIVIDERS

Good test and adjustment procedures are exceptionally important for analog dividers, since their performance spans a wide range and is often critically dependent on adjustment. For example, a general-purpose "2%" multiplier-divider (e. g AD532J) can have a worst-case error of 2 volts, or 20%, when used as a self-contained divider with a 10:1 denominator range. In contrast, a specialized high-accuracy divider (e.g. 434B) can have a worst-case error of only 25mV under the same conditions – almost *100 times* less error than the general-purpose device! The accuracy of the "2%" divider can be improved by at least a factor of 3 by the adjustment procedure described in this section.

The tests for divider performance fall into the same three general categories as for multipliers

1. Static accuracy or error
   a. Total error
   b. Output offset
   c. Numerator and Denominator offsets
   d. Numerator and Denominator nonlinearity
   e. Scale-factor error
   f. Dependence of errors on denominator
   g. Dependence of errors on temperature and power-supply voltage
2. Dynamic errors
   a. Small-signal bandwidth
   b. Large-signal bandwidth
   c. Slewing rate
   d. Settling time
   e. Dependence of the above on denominator
3. Terminal or interface parameters
   a. Input resistance and voltage range
   b. Output voltage and current
   c. Power-supply voltage and current

In this section, the principal emphasis will be placed on tests for static and dynamic errors, since methods for measuring the terminal parameters are straightforward.

TEST EQUIPMENT FOR DIVIDER TESTING

Precision dc Reference: Accuracy to within 0.01% of setting, plus ±100μV, from ±10V to 0V in steps of 100mV or less.

Precision Decade Voltage Divider: 0.01% ratiometric "accuracy" with output buffer and inverter (see Figure 47). This is *essential* for accuracy measurements on wide-dynamic-range dividers, and quite useful for testing ordinary dividers.

Digital Voltmeter with at least 4½-digit resolution, 0.02% accuracy error. The 1V and 10V ranges will be the most-frequently used.

Sine-Wave or Function Generator: Frequency range 1Hz to 5MHz. Adjustable dc offset is handy for testing 1-quadrant divider and applying ac signals to denominator. Output amplitude range of 2mVp-p to 20Vp-p is the most useful. A calibrated output attenuator will facilitate measurements on wide-dynamic-range dividers.

Dual Power Supply with adjustable output voltage (±15V nominal) and adjustable current limit to prevent costly "accidents."

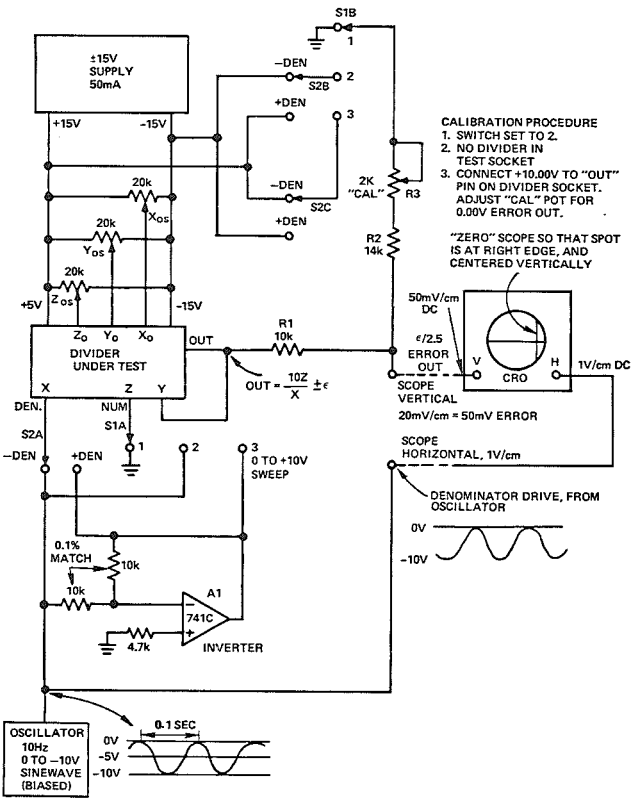
Oscilloscope with calibrated vertical *and horizontal* voltage inputs for cross-plot tests. Desirable sensitivity ranges are: Vertical, 10mV/cm to 5V/cm; Horizontal, 100mV/cm to 5V/cm. Bandwidth of 300kHz is adequate for crossplots. At least 5MHz vertical-axis bandwidth is required for dynamic tests.

Divider Test Socket, with all connections made and trimpots included, facilitates the test and adjustment of both modular and IC devices.

TEST AND ADJUSTMENT OF STATIC ERRORS

Cross-plotting the divider error against the denominator input is the most revealing, and also the most efficient method of testing the accuracy of an analog divider. This approach minimizes the ambiguity and lack-of-feel inherent in a dc point-by-point test or adjustment procedure.

The crossplot test setup, Figure 36, can be used for testing and adjusting any 1- or 2-quadrant divider. The most-important part of the setup is the low-frequency (10Hz or less) offset sine-wave generator that provides the sweep voltage for the divider and the horizontal axis of the oscilloscope. A unity-gain inverter, A1, provides a 0 to +10V sweep for dividers requiring positive inputs.



S1 Switch Position	Function	TEST CONDITIONS Numerator, Z	Denominator, X	Ideal Output	ADJUST
1	Numerator & Output Offset	0V	0 to –10V (or +10)	0V	Z_o = NUM, Y_o = OUTPUT OFFSET
2	Denominator Offset, $V_Z = V_X$	0 to -10V	0 to –10V (or +10)	+10V (–10V)	X_o = DEN OFFSET
3	Denominator Offset, $V_Z = -V_X$	0 to +10V	0 to -10V (or +10)	-10V (+10V)	X_o = DEN OFFSET

Figure 36. Divider error crossplot circuit

Since the output of the divider should ideally be constant (no slope or curvature) with the sweep-test conditions used in this setup, it is only necessary to subtract an ideal constant from the actual divider output to determine the error, as a deviation from zero on the display. The example given below is for devices requiring negative denominator voltage:

Test	Inputs	Ideal Output	Subtract
1. Numerator offset	$V_Z = 0$, $V_X = 0$ to $-10V$	0V	0V
2. Output offset	$V_Z = 0$, $V_X = 0$ to $-10V$	0V	0V
3. Denominator offset	$-\lvert V_Z \rvert = V_X = 0$ to $-10V$	+10V	+10V
4. Denominator offset (1st quadrant of 2-quadrant dividers)	$V_Z = -V_X$, $V_X = 0$ to $-10V$	$-10V$	$-10V$
5. Scale factor	$-\lvert V_X \rvert = V_X = 0$ to $-10V$	+10V	+10V

The subtraction is accomplished via a simple resistive divider R1 and R2, R3, referenced to the power supply. A more precise reference voltage, and a more sophisticated subtractor could be used, but the simple approach is adequate for testing the majority of general-purpose multiplier-dividers. If a good supply is used, and the R1-R2, R3 network carefully adjusted, the test circuit will be accurate enough for testing the specialized dividers, such as the 434.

Using the Divider Crossplot Tester

The easiest way to understand the operation of the crossplot tester is to follow through the adjustment of a typical two-quadrant divider, such as that illustrated in Figures 37 through 42. The procedure applies to any type of divider circuit, whether "inverted multiplier," log-antilog, transconductance, etc., and whether in modular or IC form. The sources of the errors, (for example, numerator offset) for the various divider types have been discussed earlier in this chapter. At any rate, these errors can be treated in a "black-box" fashion, as the procedure illustrates.

Proper adjustment of the "offset" errors dramatically reduces the divider's errors at room temperature, as Figures 37-38 and 40-41

illustrate. However, with changes in temperature, the errors can increase to values comparable to the untrimmed values, particularly for divider-connected general-purpose "multiplier/dividers." The temperature-drift effects can be easily monitored with the sweep-test circuit if the divider itself is placed in a temperature-test chamber (along with any adjustment circuitry that is to be subjected to ambient temperature variations). The circuit is adjusted for minimum error at 25°C, then the change in error over the temperature range of interest (say, 0° to 70°C) is observed.

(CONDITIONS: $V_Z = 0$, $V_X = 0$ to $-10V$, $\epsilon = V_{OUT}$
TEST SET FUNCTION SWITCH SET TO 1.)

The scope trace will be sharply curved up or down at the right edge of the screen, as the denominator, V_X, approaches zero. Notice that the total output offset is 400mV or 4% of Full Scale at a denominator of −2 volts.

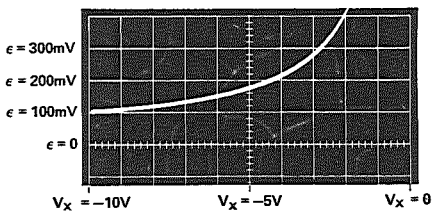


Figure 37. Total output offset vs. denominator test

CONDITIONS: $V_Z = 0$, $V_X = 0$ to $-10V$, $\epsilon = V_{out}$
TEST SET FUNCTION 1.

Adjust the Z_O potentiometer to flatten the scope trace -- note the dramatic reduction in offset as $V_X \rightarrow 0$. The error trace will not necessarily be centered on the "0" line -- this will be adjusted in the next step.

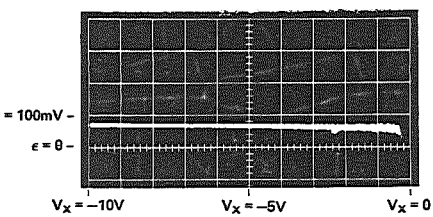


Figure 38. Numerator offset, Z_O, adjustment test

CONDITIONS $V_Z = 0$, $V_X = 0$ to $-10V$
TEST SET FUNCTION 1.

Adjust the Y_O potentiometer to align trace with center 0 error line. Note the increase in noise as $V_X \rightarrow 0$. This indicates the increased input-to-output gain of the divider, which approaches infinity as the denominator approaches zero. The total output offset is dramatically reduced from the initial value in Figure 37.

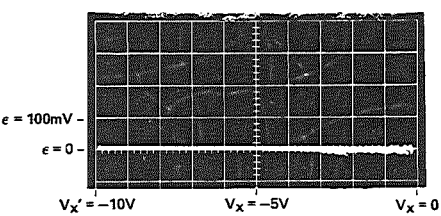


Figure 39. Output offset, Y_O, adjustment test

(CONDITIONS: $V_Z = V_X = 0$ to $-10V$
TEST SET FUNCTION 2.)

The scope trace will curve up or down as $V_X \rightarrow 0$. The increase in error is due primarily to denominator offset, since numerator offset was adjusted in Figure 38.

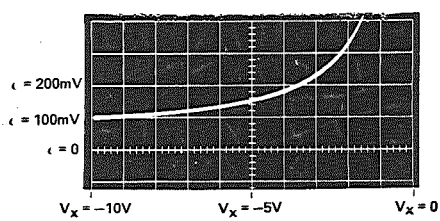


Figure 40. Total output error vs. denominator test

(CONDITIONS: $V_Z = V_X = 0$ to $-10V$ TEST SET FUNCTION 2.)

Adjust X_O potentiometer to flatten trace, which will usually not be aligned with "0" error line, due to scale factor error.

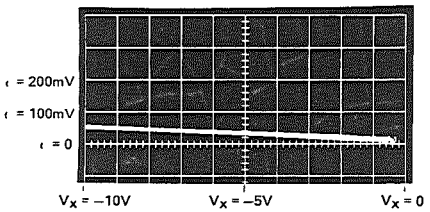


Figure 41. Denominator offset, X_O, adjustment test

(CONDITIONS: $V_Z = 0$ to $+10V$, $V_X = 0$ to 10V, TEST SET FUNCTION 3.)

Readjust X_O potentiometer if necessary to flatten trace; switch back to conditons of Figure 41 and check for best compromise in flatness as V_X - 0. If a scale factor trim is provided, adjust it for minimum difference between error trace and zero error line for input conditions of Figures 41 and 42.

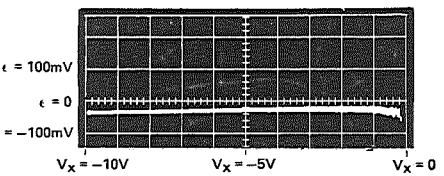


Figure 42. Denominator offset, X_O, and scale factor adjustment test

Measuring Denominator Frequency Response

Figure 43 shows a test setup for measuring the frequency response of the divider's denominator input as a function of denominator level. The denominator input of all commonly-available analog dividers is restricted to a single polarity: plus or minus (or, with differential inputs, either), so the signal generator must be offset to maintain V_{min} and V_{max} within the denominator input limits. The difference (i.e., p-p amplitude) may be maintained at a considerably smaller level (typically 10% of the offset) to minimize waveform distortion: if the ac test signal spans an appreciable fraction of the dc offset, the output will be noticeably distorted, since it is proportional to $K/(V_{DC} + V_{AC})$.

A square-wave can be used to determine denominator rise time, slewing rate, and settling time. In general, the time response will be slower for signals going toward zero denominator, and faster for signals approaching full-scale denominator.

Measuring dc Accuracy- and Temperature-Drift

While the sweep test, or crossplot technique, for measuring divider accuracy, is the fastest and the best way to get an overall picture

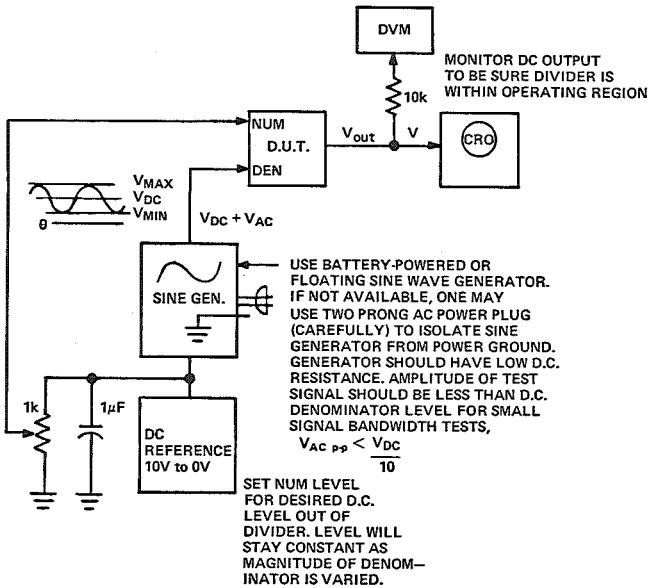


Figure 43. Test setup — denominator frequency response vs. denominator magnitude

of error as a function of denominator, it is difficult to measure the absolute error precisely (as necessary for calibration) with this technique. If the crossplot circuit is carefully calibrated, it can be used for absolute measurements. However, it tests the divider at a constant ratio of numerator to denominator, and so does not readily show numerator (constant-denominator) nonlinearity.

Furthermore, since the numerator and denominator are swept over their ranges, and spend a relatively-short time at low levels, errors due to thermal effects may not be visible. The sweep can be slowed, or a low-frequency square-wave can be used, but they are not as revealing as a dc test.

Measuring Numerator Nonlinearity

Numerator nonlinearity is measured by comparing the divider output with the numerator input at constant denominator voltage, with typical results as shown in Figure 44. Since the gain or attenuation through the divider is inversely dependent on the denominator level, the input or output must be linearly amplified

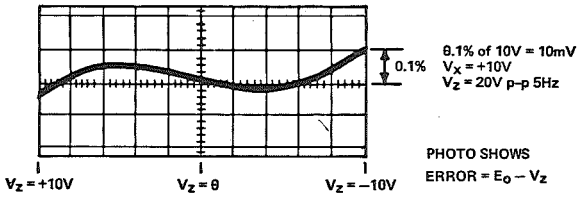


Figure 44. Two-quadrant divider, numerator nonlinearity

or attenuated to facilitate the input/output comparison. The easiest way to accomplish this for dividers with gains potentially greater than unity is to attenuate the numerator signal by a factor γ, equal to X/K, and then to compare the divider output to the input of the attenuator:

$$E_o - E_o(\text{ideal}) = K\frac{\gamma V_Z'}{V_X} - V_Z'$$

If a precision attenuator and an accurate dc reference are used, the denominator nonlinearity can be estimated from this test: the difference between the divider output and the numerator input will have an average slope equal to the "gain" error, or departure of the gain from the ideal value K/X. The scope photo, Figure 44, shows the nonlinearity of a 436 divider, measured with the test setup of Figure 45.

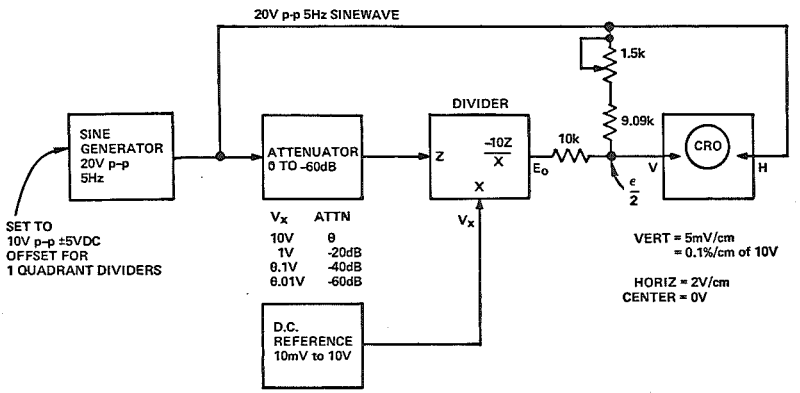


Figure 45. Test setup for numerator nonlinearity

DC Measurements of Accuracy and Temperature Drift

The dc error of the divider can be easily measured with the test setup of Figure 46. A precise voltage divider (e.g., Figure 47), is the most important piece of test equipment, since it provides a numerator voltage that is a precise fraction of the denominator voltage, independently of the absolute calibration of the dc voltage reference.

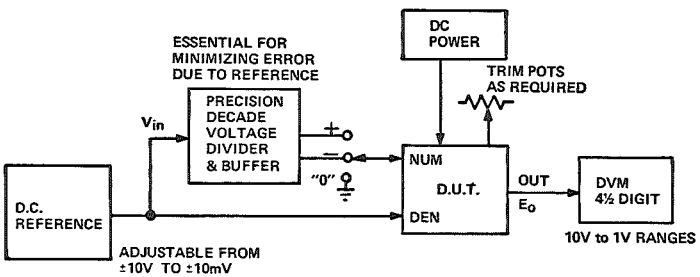


Figure 46. Divider DC accuracy test setup

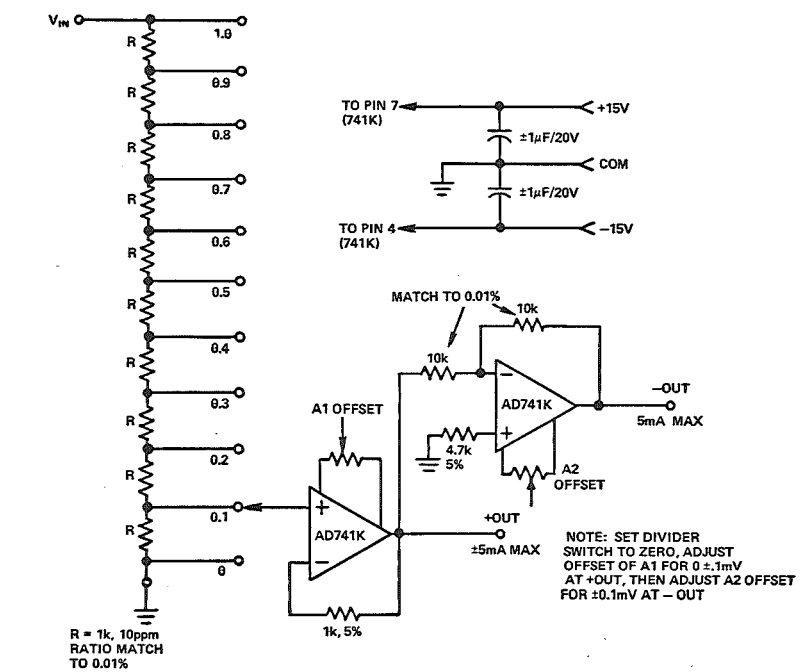


Figure 47. Decade divider and buffer

Since the divider (ideally) takes the ratio of the numerator and the denominator inputs, small errors (<1%) of setting) in the calibration of the absolute magnitude of the dc reference will have negligible effect on the accuracy of measurement if the numerator is a precisely-known fraction of the denominator. It is convenient (and desirable) to have available a dc reference with good resolution (e.g., 1mV steps); it is especially useful for testing the high-performance log-antilog dividers.

The dc error-test procedure is straightforward. For example, for a 2-quadrant divider (such as the 427), set the reference to the desired denominator voltage (e.g., -10V), then step the numerator voltage divider through 1-volt steps from -10V to 0V. Then, reverse the polarity of the numerator and step the attenuator to +10V. The divider output at each step can be read on the DVM, and then written down and compared to the theoretical value. The same procedure can be followed, with the divider operating at different ambient temperatures, to determine the temperature coefficient of divider error. Table 3 is a sample temperature-test form that includes the minimum number of measurements necessary to determine the offset and overall accuracy drift of a 2-quadrant divider over the 0° to 70°C operating range.

Measuring Numerator Frequency Response

This test is straightforward for a 2-quadrant divider, and is not very involved for a 1-quadrant divider. The test setup, Figure 48,

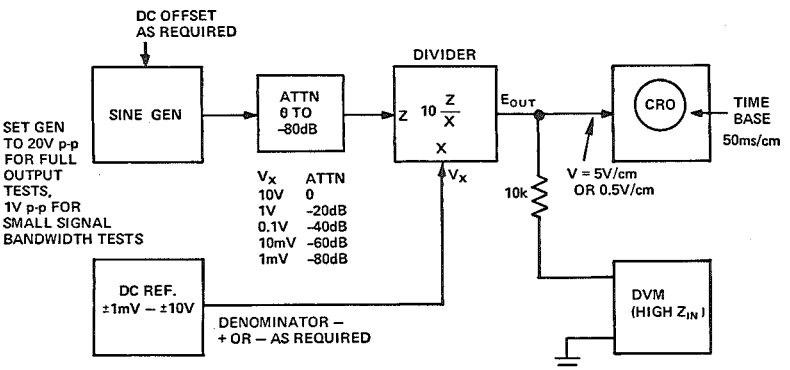


Figure 48. Test setup — numerator frequency response vs. denominator magnitude

TABLE 3. TEST CHART FOR ACCURACY AND OFFSET DRIFT VS. TEMPERATURE FOR A TWO QUADRANT DIVIDER

Denominator V_x	Numerator V_z	Theoretical E_o	E_o Measured 0°C	25°C	+70°C
−10.000V	−10.000V	+10.000			
−10.000V	+10.000V	−10.000V			
−10.000V	0.000V	0.000V (Offset)			
− 1.000V	− 1.000V	+10.000V			
− 1.000V	+ 1.000V	−10.000V			
− 1.000V	0.000V	0.000V			

Absolute Error = $V_{MEAS.} - V_{THEO.} = \delta$

% of Full Scale Error = $\frac{\delta}{10V} \cdot 100 = \%FS = 10\delta$

%/°C DRIFT = $\frac{\delta\% \text{ FS}}{T_2 - T_1}$

Measurements should be made at smallest expected denominator. 1V was picked for this example since it is the minimum useful denominator for most general–purpose two quadrant "inverted multiplier" dividers.

illustrates the basic scheme. A signal generator with a continuously-variable output-amplitude control may be used instead of the constant-amplitude source and calibrated attenuator. However, it is important to remember that the signal on the numerator input must have peak amplitude less than the magnitude of the denominator for dividers with a 10V scale factor (constant K or variable V_y). One-quadrant dividers require a dc offset for the numerator proportional to that of the denominator; so the numerator offset will have to be adjusted at each denominator level.

The bandwidth test procedure is

1. Set the dc reference to the desired denominator voltage.

2. Set the oscilloscope vertical sensitivity to 5V/cm for large-signal tests; use dc coupling so that the total output voltage is

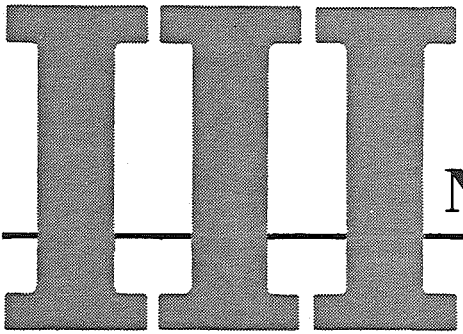
displayed – this will make saturation and offset effects more noticeable. Set the oscilloscope sensitivity to 0.5V/cm or less for small-signal tests. AC coupling will be required for 1-quadrant dividers, since their output will be "offset" due to the dc bias required on the numerator input.

3. Set the amplitude and offset of the signal generator so that the divider output, as displayed on the scope, is within the required limits, e.g., 1Vp-p, at a frequency at least a decade below the expected -3dB frequency.

(The numerator dc offset can be most easily adjusted by connecting a DVM to the divider output, as indicated in Figure 48. The offset is then adjusted so that the dc output is at the desired level within the operating range of the divider – for example, +5V for full-output frequency tests on a 434 one-quadrant divider.)

4. Sweep the generator up in frequency until the divider's output amplitude falls off – or peaks – to the 3dB (∓30%) point, or there is noticeable distortion at the output. Repeat this procedure at several denominator voltages within the expected operating range.

A square-wave input can be used to determine slewing rate, rise time, and settling time in the same manner as for a multiplier or an operational amplifier.



Nonlinear IC's

Chapter 4

> "The Analog Art shows no signs of yielding to the Dodo's fate. The emergence and maturation of monolithic processing finesse has perhaps lagged a bit behind the growth of the Binary Business. But whereas digital precision is forever bounded by bits, there is no limit excepting Universal Hiss to the ultimate accuracy and functional variety of simple analog circuits."
>
> Barrie Gilbert, January, 1973

Although a great majority of configurations and performance classes of the devices to which this book is devoted are principally available in the form of modular discrete-circuit assemblies, a sea-change is occurring.

Having thoroughly saturated the linear-function area of analog circuits with a plethora of general- (and special-) purpose operational amplifiers, integrated-circuit technology has now turned to the development of nonlinear-function circuits.

An increasing number of non-linear functions, previously available only in module form, are becoming available as integrated circuits. Except for comparators (which combine op-amp and digital characteristics), the greatest progress made by analog IC's to date has been in circuits that perform the basic functions of multiplication, division, squaring, rooting, and multiplying D/A conversion.

SIMILAR BUT DIFFERENT

For the most part, the similarities between the IC and the module approaches are straightforward: they both perform similar circuit

operations and can be generally applied to solve the same system-design problems. The differences fall into two categories: generic differences between IC's and modules, such as cost and size; and technological differences, which affect circuit design and performance, bringing both advantages and limitations.

The most salient difference is cost. Not only are costs of comparable IC devices competitive at the time they are introduced, but the trend is inexorably down, especially as usage increases to large quantities – a powerful incentive to the system designer to use them for new applications. Not long ago, modular multipliers with <2% overall error were sold in the $25 to $30 price range. Now, equivalent IC multipliers (AD533JH) sell for less than $6 in hundred lots! The next few years will see "garden-variety" IC multipliers selling at prices not much higher than those of today's general-purpose IC op amps.

Other generic differences are small size and high reliability. The small IC packages (both the hermetically-sealed ceramic dual in-line package and the hermetically-sealed TO-100 can) offer significant savings of space in all applications, some of which would not even be possible using the modular discrete-component package. (Such devices as the AD532, needing no external trims or other components, offer the ultimate in small size). The increased potential reliability of monolithic assembly techniques, relative to their equivalent modular functions, has been amply documented.

Because discrete-circuit modules are not limited in either circuit complexity, physical configuration, or package size, they continue to offer performance advantages over their IC counterparts, but the gap has already narrowed to negligible proportions for general-purpose moderate-bandwidth 1-2% devices. Where state-of-the-art accuracy, speed, stability, and/or ease-of-use must be obtained, modules are still (at this writing) the first – and perhaps the only – choice.

Modules using discrete circuitry can employ pulse-modulation circuits to obtain errors less than 0.1%, while *present* IC devices, using variable transconductance, are limited to ±0.5%, with external trim. ("Cross-feed" trims can reduce this by a factor of 2, as explained in Chapter 3-2.) The pulse-modulation technique, inher-

ently more accurate, is difficult to employ in integrated-circuit form, because of the stringent demands it imposes on circuit components produced on a monolithic chip. However, new approaches to IC multiplier designs hold considerable promise for the future.

Discrete designs can also take advantage of monolithic matching of selected elements as building blocks, providing combinations that are difficult to come by with reasonable yield on a single monolithic chip, at today's state-of-the-art. On the other hand, automatic laser trimming of IC multipliers, on the chip, can help make IC multipliers more competitive in price/performance/convenience.

In the area of dynamic performance, IC transconductance cells are inherently wideband (as incomplete current-to-current devices). Complete monolithic multipliers are generally limited to a few MHz of bandwidth because of limitations on the speed of lateral PNP transistors used in the level-shifting output amplifier. Incomplete current-output devices (so-called multipliers, but actually just current cells) require moderate numbers of external components, including a level-shifting amplifier, all of which tends to reduce speed, as well as to contribute additional errors that must be added to the errors of the basic monolithic device. The economic choice between basic transconductance cells, with considerable external circuitry, and modules or complete IC's with guaranteed performance, tends to favor the latter, except for specific non-precision high-speed application areas where the nature of the current cell is not a barrier to its use.

The IC multipliers discussed in this book are complete self-contained operational blocks, requiring only a power supply, trims (in some cases), and normal circuit-implementation techniques to obtain working circuits.

Finally, there are differences in testing philosophy that affect the performance of IC multipliers. The cost of production-testing module-type multipliers manually is not a large part of the cost of these devices. On the other hand, in order to realize the potential cost savings of IC multipliers, automated test procedures are an absolute necessity. The principal drawback of automated high-speed testing is that there is insufficient warmup time to allow all parameters to reach their final values. Consequently, both predic-

tive techniques and conservative safety margins must be used by the manufacturer (i.e., Analog Devices) to make sure that the user achieves the guaranteed specifications in a normal, fully-warmed-up circuit application. The bonus for the user is that quite often the devices he purchases from a conscientious IC manufacturer may be considerably better than the specifications would indicate.

DESIGNING IC MULTIPLIERS

It is only within the past five years that the basic circuit configurations were devised which made accurate monolithic multipliers possible. It took about two of these years for the industry to provide the means of fabricating devices having errors of a magnitude that would be competitive with discrete-component circuit modules.

The key technological factors that had to be awaited were:

1. Near-ideal NPN transistors exhibiting high current gains, close matching, and very close conformity to ideal logarithmic junction characteristics over wide current and temperature ranges.
2. Linear, stable, close-tolerance monolithic resistors.
3. An important factor that helped monolithic multipliers attain performance standards suitable for general-purpose applications is the better understanding of subtle sources of errors arising from the chip layout, such as thermal effects, non-negligible resistance of the aluminum metallization, non-matching of apparently identical transistors, etc.

Both the user and the designer of monolithic nonlinear circuits are faced with the need for compromises. Those problematic factors that concern the designer are:

1. The complete system, comprising input amplifier(s), the main functional core, the output amplifier, and all auxiliary circuits, such as reference-voltage and bias supplies, must be achieved with whatever devices can be concentrated on a chip no larger than, say, 80 mils (2mm) square.

2. All the power generated by the circuit has to be dissipated by a relatively small package, in contrast to the substantial size and mass of a discrete-circuit module. So the compromise between high load-driving capability, on the one hand, and negligible warmup and long-term drifts, is especially severe. In addition, the close thermal coupling between the power-dissipating output stage and the temperature-sensitive logarithmic devices calls for very careful layout to minimize thermal unbalances between critical transistor-pairs.

3. Some very useful components are just not available. Selected devices, such as computer-matched transistors, calibrated and guaranteed reference diodes, and fast, high-gain PNP transistors obviously cannot be incorporated into the design. The most serious problem is the bandwidth limitation caused by the use of lateral PNP transistors; most of the other problems can be satisfactorily dealt with.

4. The number of adjustments needed to get the device within its stated accuracy must be minimized. Apart from their inconvenience for the user and their adverse effect on production costs, each external adjustment requires a minimum of one bonding pad and one package pin, both of which are usually at a premium (one bonding pad consumes as much area as a typical NPN transistor, and an extra pin may make a low-cost 10-pin version of a device unobtainable). On-chip resistor trimming is feasible (and is used successfully in production of the AD532), but it does add to production cost. Thus, the considerations involved in minimizing worst-case tolerances take on an added importance in monolithic design.

But IC's pose opportunities as well as problems. The advantages for the user are low cost, small size, and high reliability. For the designer, they include:

1. Low incremental cost for adding useful circuit refinements. The addition of even a single matched transistor pair to a discrete design would require very careful consideration and would be expected to increase both the material- and the labor- cost of the module noticeably. In contrast, the inclusion of additional monolithic transistor pairs would not make

a substantial difference to the cost of either materials or labor; it could even lower the total cost by ensuring that a greater proportion of the chips (i.e., yield) performed properly. For example, quite complex circuits can be used to generate a precise voltage reference to replace the calibrated zener diode used by the module designer. In fact, there is every possibility that such circuits, pioneered by engineers battling with the apparent "limitations" of the monolithic medium, will become the preferred type of voltage reference for future discrete modules.

2. Another advantage of the monolithic approach is, ironically, a result of the very close proximity of components on a chip that also causes the difficulties listed under (2) above. It is the unexcelled matching and temperature-tracking of devices *as processed,* that is, without the need for selection. As the technology has matured, these factors are tending to become a secondary source of inaccuracies, rather than the dominant source that they once were. Thus, trimming and testing costs of the monolithic product will continue to decline, in relation to the available performance.

So much for the generalities. Let us now take a closer look at the way a monolithic circuit designer approaches the operational requirements.

COMPARING CIRCUITS

Suppose we wish to design a 4-quadrant multiplier of medium accuracy (say, 1%) having a small-signal bandwidth of about 1MHz. We might begin by listing some of the techniques available and consider their properties in relation to the feasibility of monolithic fabrication.

Quarter-Square. This method requires two precision squaring devices and several operational amplifiers to generate sums and differences. Once the classical approach to precise high-speed multiplication, it does not have much to commend it for monolithic implementation; in any event, the technique is practically obsolete, even for module designs. In fact, low-cost multipliers are now perhaps the best way of performing the squaring operation!

Pulse Modulation. This method would require very high carrier frequencies to achieve 1MHz signal bandwidth and is rather difficult to adapt to 4-quadrant operation. Also, several connections to external capacitors would probably be necessary to provide various timing and filtering functions.

The Hall Effect. It is possible to make Hall plates* with standard NPN processes, but they are not optimum, and the output product is a signal at the millivolt level ("The Hall Effect is a small effect"). A rather strong magnetic field that responds to one of the variables is a necessity; and the two input channels have greatly differing dynamics.

Antilog-of-sum-log (Chapter 3-2). This method can certainly be used in a 1-quadrant monolithic realization. Some objections, however, are that the full four-quadrant capability calls for a substantial increase in complexity over the 1-quadrant case, speed is a function of signal amplitude, and a relatively-large number of amplifiers are needed.

Current-ratio (*linearized variable-transconductance*). This method is uniquely suited to the medium and is used in practically all the monolithic multipliers on the market today. It is simple, basically temperature-insensitive, and operates on differential current signals to achieve four-quadrant operation directly. Bandwidth is inherently wide; it is limited in practice only by the output amplifier, which uses lateral PNP transistors to achieve level-shifting.

DESIGN CONSIDERATIONS

Let us now sit in the designer's chair and see how the monolithic aspects affect his approach to applying the current-ratio cell. The basic core has already been described (Chapter 3-2), but it is instructive to recast it slightly to emphasize certain points.

Figure 1 shows a typical monolithic version; many others are possible. Notice that the two "linearizing diodes" are actually only a

*The Hall Effect: If current flows through a conductor and a magnetic field is applied at a right angle to it, an orthogonal voltage will be developed across the conductor proportional to the product of the current and the flux density. The proportionality constant ("Hall Coefficient") is a function of the material and the conductor's configuration.

pair of emitters in a common collector-base region. This is one of the ways the designer reduces the chip area; an extra emitter can consume as little as 5% of the area required by a fully-isolated transistor. A similar conservation of space is possible by noticing that pairs of output transistors Q4-Q6 and Q3-Q5 share common-collector regions. Again, if separate transistors are replaced by putting two emitter-base structures in a single collector region, the area increase is only about 30%.

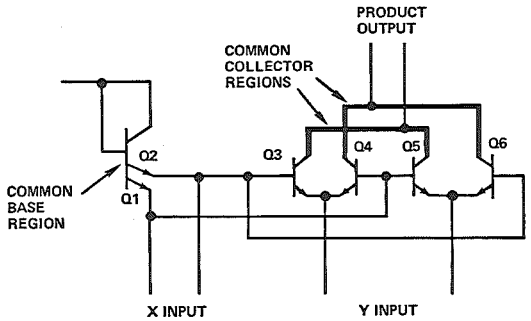


Figure 1. Circuit of monolithic multiplier cell. Compare this with Q1, Q2, Q3 in Figure 11, Chapter 3-2.

These six junctions are placed close together on the chip and must have exactly-matched emitter areas. Often, large emitters are used to reduce the effects of process tolerances. However, there is a need to compromise, because although isothermal matching may improve with emitter size, the larger devices become more widely separated, increasing the probability of increased sensitivity to thermal gradients on the chip; it can be shown that each centigrade degree between certain pairs can introduce 0.07% distortion. Another reason for limiting the emitter area is to maintain a reasonable cutoff frequency.

Area-matching in the multiplier core is of paramount importance, for two reasons. First, it can be shown that a 1mV offset between these junctions can cause a parabolic nonlinearity of about 1% of full scale to be superimposed on the product. Second, offsets introduce large zero-errors, referred to the inputs, because of the large amount of degeneration needed to handle ±10V signals; the ratio is about 200, so a 1mV transistor mismatch becomes 200mV at the X or the Y input (or both – it all depends on where the

mismatches arise). Furthermore, this zero-error has a kT/q kind of temperature dependence, amounting to nearly 0.7mV/°C in the example just given. High-quality processing and thoughtful layout have done much to take the sting out of these problems, and new circuit tricks are being added to the designer's repertoire which permit him to completely eliminate all but a trace of residual mismatch.

Another source of errors in this simple cell, which seldom confronts the module designer, arises out of the difficult topology and attendant interconnection problems of the circuit (try to connect everything up on paper without introducing any crossovers; and you must get all input- and output nodes outside the circuit). This is not the place to delve into the interesting ways of dealing with this problem; but as an example of the care that must be exercised, consider the consequences of using a rather circuitous route for one of the aluminum interconnects. At 50mΩ per square, a length difference of 20 mils (1/2mm) in a 0.5 mil (1/80mm) track amounts to a resistance inequality of 2Ω. If this conductor is carrying 1mA, a differential voltage of 2mV is generated. Inside the critical junction loop of Figure 1, such a mistake would ruin any chances of achieving distortion levels of even 1%.

Avoidance of excessive ohmic drops is also a contributing factor to the choice of sub-milliampere operating levels for these transistors. The effect of these drops on linearity explains why VHF multipliers, which need to operate at much higher currents to maintain bandwidth, usually exhibit inferior linearity to instrumentation circuits.

Compensation for errors introduced by finite current-gains (beta) provides another example of the way in which the monolithic designer can take advantage of the medium. In this case, it is that betas of devices all over the chip tend to match up and to track with temperature. It can be shown that the circuit of Figure 1 introduces a scale-factor error which is three times the α error. That is, if Q3 through Q6 had α's of 0.99 (Beta = 100), the overall gain error would be -3%. Although this could be initially trimmed out, any variation of beta, especially at low temperature, would introduce a scale-factor shift. Fortunately, state-of-the-art

processes consistently produce transistors having betas of several hundred, so this is not a severe problem. High-accuracy multipliers can take advantage of beta-tracking (and of the current-ratio principle) to employ compensation circuitry which maintains a very stable scale factor, even over the military (–55°C to +125°C) temperature range.

This has been just a brief look into some of the ways the design of monolithic multipliers differs from that of their discrete counterparts. A full treatment of the subject has never been published, and possibly never will, because of its highly-specialized nature. Most of the topics just discussed in relation to multipliers apply just as well to other nonlinear circuits based on logarithmic junctions, particularly those involved in ratio and power-function generation. The comparison with discrete circuitry is equally pertinent.

SPECIFICATIONS AND CHARACTERISTICS

Since both IC and modular nonlinear function circuits share common design principles and are used for the same kinds of applications, and since the operational guidelines for most IC nonlinear devices were set in terms of their modular forebears, it is not surprising that few differences exist in their specifications. In fact, if one bears in mind that (except for the AD532, at this writing) the IC device is specified under externally-trimmed conditions – usually the adjustment of four variable resistors (for those devices that include the output amplifier) – then the only differences are those that exist between any IC and the equivalent modular function (warmup time, power dissipation, size, cost, etc.) Therefore, the definitions, established in Chapter 3-2, of feedthrough, nonlinearity error, gain error, accuracy, etc., apply equally to both IC and modular function-circuits.

Modular circuits, using pulse-width/amplitude modulation principles, multiply with maximum errors below 0.1%; the best of IC's (at this writing – it is necessary to reiterate this *caveat*, because of the rapidly-expanding limits of the IC state-of-the-art), using the transconductance principle, guarantee that multiplying errors will

be less than 0.5%. However, the best IC has a typical accuracy (error) vs. temperature specification of 0.01%/°C, due to the excellent temperature tracking inherent in IC construction (a comparable number to that for modules). Modular multipliers offer small-signal bandwidths of 10MHz and minimum slewing rates of 120V/μs; the best performance of a current-output (incomplete) IC multiplier, over a limited range, is 6MHz and 30V/μs, and for voltage-output IC's 1MHz and 45V/μs.

There are on the market several nonlinear IC devices that essentially provide only the basic transconductance multiplying function, with a resulting low-level current output signal that requires the addition of an amplifier and a number of passive components to achieve a usable signal level. This externally-applied circuitry provides its own sources of error (as well as cost), the amount of which depends to a great extent on the choice of active and passive components and the circuit-design virtuosity of the user. In this case, then, the manufacturer cannot provide a guarantee of overall accuracy, but must limit himself (in a manner similar to that of general-purpose, many-degree-of-freedom devices, such as op amps) to specifying individual parameters. It is important to note that Analog Devices has principally chosen to opt for committed circuitry: all AD IC multipliers are complete-on-a-chip circuits, including the output amplifier, and are thus guaranteed for overall performance.

NONLINEAR IC'S vs. IC OP AMPS

Many readers of this book will reach this point with a background of experience in the applications of functional devices, whatever their mode of manufacture (from "bottles" to chips). But there are also many whose experience with analog ("linear") circuits is pretty much limited to IC op amps. It may be helpful for the latter to consider the following comparison of qualitative differences between nonlinear and "linear" analog integrated circuits.

In the vast majority of both nonlinear and linear (i.e., op amp) applications, accuracy of signal reproduction is the specification of greatest concern. Due to the many degrees of freedom of op amp circuits, however, it is rarely that the manufacturer can satisfy

this concern with a single specification that guarantees the user his required accuracy. The specifications that contribute to overall accuracy: input bias current, offset current, input voltage offset, voltage-offset drift, CMRR, etc., all add up to different errors, depending on the particular way (of many) in which the op amp is used. Thus, the very-general nature of IC op amps hinders the manufacturer in any attempt to guarantee an overall accuracy specification. He must constrain himself to specifying such parameters as I_b, E_{os}, Gain, CMR, etc., and leave the determination of overall accuracy to the user.

Nonlinear function IC's, on the other hand, perform rather specific tasks. Though their applicability is wide: automatic gain control, true rms, vector summation, absolute value, ratio measurement, etc., in almost all cases they are hooked-up in the same way, and perform the same function, be it multiplying, dividing, squaring, or square-rooting. The multiplicity of degrees-of-freedom, that prevents the IC manufacturer from providing a relevant overall accuracy specification for op amps, does not exist in the case of nonlinear-function IC's. Thus the user is freed from the often-laborious and sometimes confusing requirement that he calculate the circuit's worst-case accuracy error before considering the many parameters that must be traded-off. Except for instances where he is seeking performance levels considerably better than the overall specification, the need to understand, interpret, and calculate the effects of such partial specifications as feedthrough, nonlinearity, and scale-factor error (which are provided nevertheless) is eliminated by their measurement and inclusion in the guaranteed overall accuracy specification.

As noted earlier, though, overall accuracy can be truly guaranteed only when the signal that is the result of the particular nonlinear manipulation is received at the output of the device at a level that requires no further processing or amplification (excluding external trims, the effects of which are included in the specification). The point is that partial-multiplier circuits must be treated as many-degree-of-freedom devices, and the overall performance calculation must include the effects of components added externally, but not included in the manufacturer's specification.

TESTING AND SELECTION

The test circuits given for multipliers in Chapter 3-2 are universally applicable from a technical point of view. However, where multipliers are produced (or consumed) in volume, the integrated-circuit device, with its low cost and high production volume, has made it necessary to turn to computer-controlled automated testing systems, in order to keep the costs commensurate with manufacturing costs by less handling and higher throughput. The automated test system can make more measurements, in a shorter period of time, sort the devices into a number of different categories, and do it without the need for skilled test technicians in routine operation.

A typical bench test of a modular multiplier may involve the setting-up of three pieces of equipment, inserting the module into a socket, manipulating a number of switches (or interconnections), making (say) 10 measurements, and classifying the module (if that particular module has more than one classification) – a procedure which may consume one minute (or more) per device.

Temperature testing requires loading the modules onto boards, which are then put into an environmental chamber and adjusted at room temperature. The chamber ("oven") is then brought to each test temperature, and more measurements are made. Temperature testing thus requires an additional minute per device per temperature level, plus setup time and stabilization time.

On the other hand, the automated test system, after an initial investment in (equipment and) time for writing and debugging the program, can perform about 5 times as many measurements in as little as two-to-three *seconds* per device. When combined with an environmental chamber and data storage, such as magnetic tape, the temperature testing and drift testing (which involves calculating the differences between the same tests at two different temperatures) are also performed in a very short time (about 1 second). In addition to the critical parameters, the high rate of testing allows checking of less-important (but still guaranteed) parameters such as power consumption, bias currents, output swing into a load, and maximum ratings.

The use of automated handling equipment, interfaced to the test system, provides for more-efficient use of the test system by reducing insertion time to less than 1 second.

Automated testing, however, is not a panacea; it has its problems and limitations. One of these is that, with such fast testing, the device does not have enough time to reach its normal operating temperature. This can usually be compensated for by testing to a tighter limit than that which is guaranteed. This obviously necessitates discarding some devices which otherwise might meet all of the specifications (or placing potential premium types in a lower-price category), but the saving in test time far outweighs the yield loss caused by insufficient warmup time.

The major difficulty in testing multipliers is performing the three null adjustments and setting the scale factor ($1/V_T = 0.1/V$), in order to be able to perform the accuracy, linearity, and feedthrough measurements. The basic technique used with the automatic system is to vary each null voltage by means of a programmable dc source, in response to a successive-approximation routine written into the software, while the measurement system monitors the output. When the proper output level is reached, the null voltage is stored by a sample-hold, the programmable source is switched to the next null terminal, and the process is repeated.

For gain tests, rather than adjusting the scale-factor by setting an attenuator on the Y input (of the AD530 or AD533), as a user might do, the automatic system adjusts the programmable signal source to the Y input voltage required to give unity transfer from the X input to the output. This value of voltage is then used later to establish the Y input during the various tests that call for the full-scale value of Y.

To avoid an iterative null routine, where the nulls must be repeated, or fine-tuned, the adjustments are performed in the proper order, viz., Y feedthrough ($0 \times Y$, trim X_{OS}), X feedthrough ($X \times 0$, trim Y_{OS}), E_{OS} (0×0, trim V_{OS}), and scale factor.* It is accomplished by using a sample-and-difference technique to measure the output-voltage *changes* in response to the input signals, while ignoring the output magnitude (untrimmed offset voltage)

*This process straightforwardly zeroes the output, including the effects of both the Z_{OS} and $X_{OS}Y_{OS}$ terms in equation 13, Chapter 3-2.

during the adjustment of "linear" feedthrough (see Figures 34 and 35, Chapter 3-2).

For example (Figure 2), in nulling the Y feedthrough, the X_0 S-H is gated into the *track* condition, essentially connecting the programmable voltage source to the X_0 pin of the multiplier. At the same time, the X input is set to zero, and the Y input is alternately switched from +10 to -10V. The output (+Y) is subtracted from the output (-Y). When the difference is zero, the successive-approximation routine is stopped, and the X_0 S-H is put into *hold*. The differencing technique eliminates dc offsets and also prevents the untrimmable component of feedthrough, due to multiplier nonlinearity, from affecting the null.† The whole null procedure, involving all four adjustments, takes about 1 second to perform.

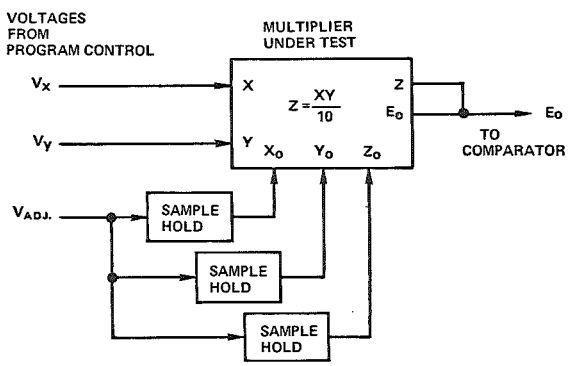


Figure 2. Connections to multiplier in automatic test circuit

For temperature testing, the measured 25°C null voltages are stored on magnetic tape and later played back to establish proper 25°C null conditions for each multiplier, as it is tested at the extremes of its rated temperature range. This technique closely simulates the user's circuit conditions (pots set at 25°C), while allowing the use of automatic handling equipment with resulting throughput of the order of 500 devices per hour. With this test setup, performance over the temperature range can be both guaranteed and verified by testing of 100% of the devices.

Test systems such as this, though few and far-between (at this writing, it is believed to be unique with Analog Devices), account

†Feedthrough nonlinearity is quadratic for these devices, as noted in Chapter 3-2.

for the excellent quality/price ratio of complete monolithic multipliers, and for the maintenance of applications-oriented specifications.

DYNAMIC TRIMMING

Until the introduction of the AD532, integrated-circuit multipliers required several external components to allow adjustment to within the specified tolerances. Such adjustments are costly for the user to implement (compared to the basic price of the device), and they introduce additional potential for thermal and accidental errors.

By the combination of the micro-machining capability of a laser with an automatic measuring and positioning system, it has become possible (and economically feasible) to adjust the multiplier offsets and scale factor by changing the values of on-chip thin-film resistors. The result is an integrated-circuit multiplier which can be plugged in and turned on, with no adjustments or external components required.

Figure 3 is a block diagram of an automated dynamic-trim system developed at Analog Devices. The coordinates of the starting- and stopping-point of each resistor to be trimmed are stored on a continuous loop of punched tape. The *device position control* reads the tape and positions the device under the laser beam by applying a number of pulses to digital stepping motors driving an X-Y table. The *power and control logic* module applies power and input voltages to the device in a sequence determined by the logic. It also conditions the output of the device and feeds it to the *measurement and trim control system,* which determines when the output of the device has reached the desired value; it then, via the control logic, turns off the laser beam. The measurement approach used is similar to that described above in relation to the automatic null and test system.

The laser beam, which is coherent light concentrated in a small area to generate a high energy density, oxidizes part of the resistor, causing its resistance to increase permanently.

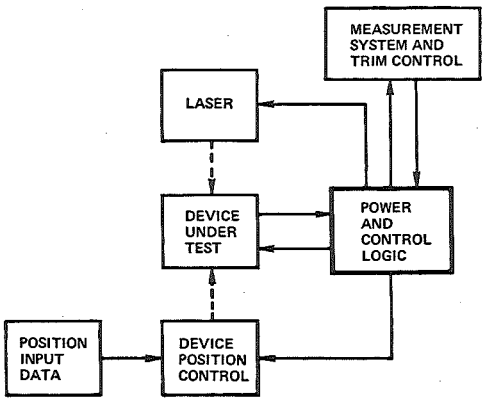


Figure 3. Laser-trimming system configuration

Figure 4 is a simplified schematic of a multiplier cell. In normal operation, a constant voltage is applied at the –X input to adjust the offset of the X-input transistor pair. In dynamic trimming, the X inputs are held at zero volts (so is the –Y input), while the +Y input is switched between a specified ± voltage-pair. The laser then increases the resistance of either R1 or R2, which adjusts the current balance in the stage for minimum linear feedthrough. This is measured by phase-sensitive chopping and filtering of the device's

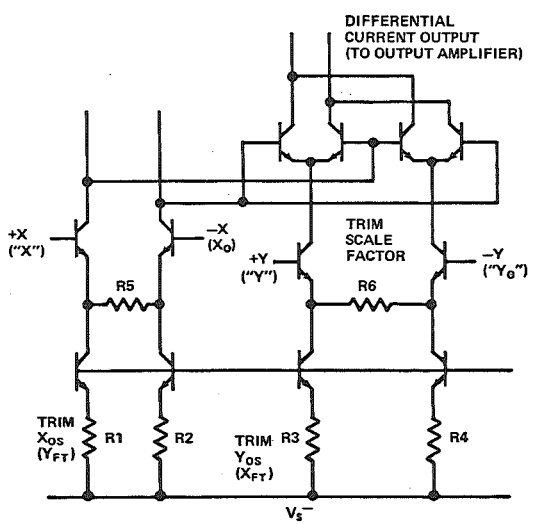


Figure 4. Simplified schematic of multiplier input circuit showing feedthrough and scale-factor trim resistors

output; the laser is turned off when the output of the filter is zero, indicating equal feedthrough at both input levels. The feedthrough for the +X input is adjusted in a similar manner by holding the Y inputs and –X at zero and increasing the resistance of either R3 or R4.

The offset voltage is zeroed by adjusting one of a pair of resistors in the on-chip output amplifier. All inputs are set to zero volts, and the resistance is increased until the output reaches zero volts. The scale factor is set by increasing R_6, which is deliberately made slightly low, while the errors are monitored for maximum input values in all four quadrants. The resistance is increased until the total four-quadrant error is minimized. Because this adjustment affects the offsets, it is necessary to repeat the offset trimming a second time (fine trim) in order to insure the best-possible yield vs. cost.

Once the device has been plugged in and aligned to the X-Y table, the trim procedure is completely automatic.

APPLYING: PRACTICAL USE OF IC'S FOR BEST RESULTS

HINTS

While especial attention is given to the accuracy, feedthrough, and linearity specifications, and their minimization, the best efforts of the manufacturer, and the cost paid by the user, may be wasted if the device is improperly scaled, interfaced-with, or adjusted.

Scaling. The effects of offset drift and cubic nonlinearity and feedthrough can be minimized by scaling inputs and outputs to give full-scale voltages at their respective peak values. Parabolic nonlinearity is the most-prevalent type in transconductance multipliers, and it can usually be greatly-reduced by the methods of Figures 14 and 15 in Chapter 3-2. Low-level input signals should be preamplified to, say, ±10V to insure best accuracy and dynamic range.* Figure 5 shows the use of op amps as followers-with-gain to provide both isolation and scaling of high-impedance low-level signals. Inverting amplifiers may be used to adjust gain in applica-

*Note that if both inputs are scaled to half-scale, instead of full-scale, 3/4 of the dynamic range is wasted. If the output of the circuit must be only 1/4-scale, it is better to use an additional attenuator following the multiplier's full-scale output.

tions where the polarity relationships require inversion, for example, if a divider requires negative denominator input from a positive signal.

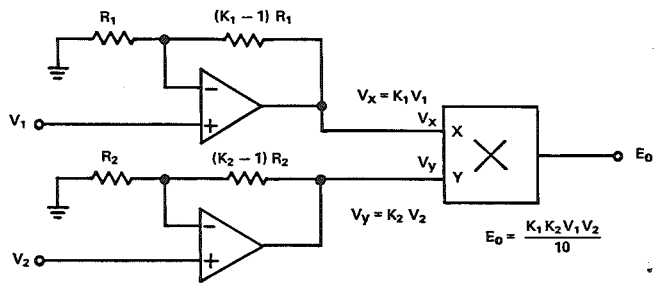


Figure 5. Op amps as followers-with-gain to scale multiplier inputs to ±10V

Buffering. If either signal source is at high impedance, the input impedance of a multiplier may result in significant loading error. This is composed of specified resistance levels, bias current (and its variation with time and temperature), and the added shunt resistance of any resistive voltage dividers introduced for scaling purposes. In such cases, the source should be buffered by a follower-connected op amp, especially if the amplifier can also provide needed amplification.

Trimming. Most multiplier data-sheets provide trim procedures for optimizing performance in various modes: multiplication, division, squaring, rooting, etc. For some modes, certain trim adjustments can be eliminated. Trims may even be incorporated into adjacent portions of the circuit, if appropriate, and the device trim-terminals grounded, to minimize overall error of a *circuit* containing the multiplier.

The use of cross-feedthrough trims has been mentioned early in the chapter, as a means of squeezing the best performance out of a low-cost device. Usually, only an X trim is necessary; Y feedthrough is close to the point of diminishing returns.

Since internally-trimmed devices are almost never exactly "on" the design-center setting, performance can be improved in critical cases by introducing external trims. Trimming may be used

preferentially to improve performance in those quadrants where accuracy is most important.

Finally, if the multiplier is a crucial element of a very high-precision circuit, calling for overall error less than 0.1%, it may be feasible to keep a high-accuracy multiplier at constant temperature, map out its error surface, and use several low-cost multipliers in a function-fitting configuration (Chapter 1-1) to simulate the error surface and subtract it from the output. In the past, such a suggestion could be considered a speculative fantasy, but with the low cost of today's multipliers and the availability of high-powered computing techniques to test conceptual models, the cost and time involved may be by no means prohibitive.

KINKS

Power-supply decoupling capacitors are often built into discrete-component modules; but it is not practical to include them on an IC chip. As in the case of IC operational amplifiers, it is good practice to use them routinely, especially for designs involving high overall gain in the circuit. Bypass capacitors, at each device, should be located as close to the device as practicable, but never through a switch or circuit-board edge connector, which can introduce undesirable series inductance. A typical configuration is a 0.01μF ceramic, in parallel with a 1-10μF tantalytic, from each side of the supply to common.

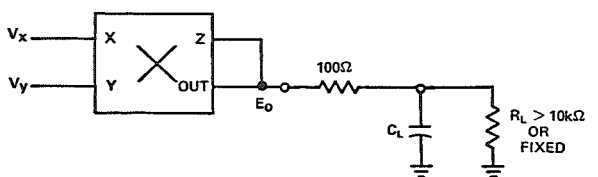
Some care may be necessary in locating offset-adjustment potentiometers. Since long lead lengths may introduce undesirable effects, the adjusting potentiometer should be as close to the device as feasible.

Integrated circuits can be particularly sensitive to capacitive loading. While good design dictates that general-purpose devices should be (and ADI's are) capable of driving 500 to 1000pF worth of capacitive loading at any output level without modification,* it may be wise to include some resistance in series with the load (Figure 6a) or to add a suitable buffer (Figure 6b) whenever

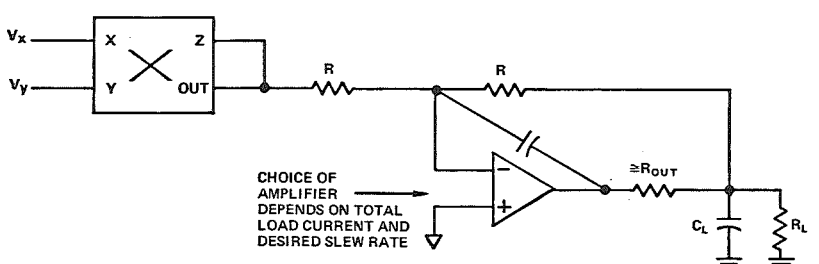
*Not all manufacturers see this in the same light

larger capacitive loads are anticipated. For the AD530, 531, 532, and 533, the series resistance should be of the order of 100Ω. (Caution: when the nonlinear function cell and its amplifier are connected in a feedback configuration to obtain the inverse function, for example, the square-root (AD530, 532, 533), the capacitive loading capability may be adversely affected because the loop gain is doubled at high levels.)

A word about warmup shifts! The large thermal mass and greater power-dissipation capability of modular function circuits generally results in cooler operation and smaller warmup shifts. IC function circuits, on the other hand, may have a large power-to-volume ratio, depending on the circuit complexity, and can run quite warm. Thus, the user should allow a 5-10 minute warmup time (in free air) before performing final trim adjustments or measurements of device accuracy to specifications. Warmup effects can be reduced by perhaps an order-of-magnitude if the device is mounted in a heat sink.



a. Isolating I.C. multiplier from large capacitive load by fixed resistance



b. Isolating multiplier from load by buffer op amp

Figure 6. Isolating large capacitive load to prevent multiplier from oscillating

PITFALLS

Unlike discrete modular devices, the inherently high reliability of integrated circuits can be easily compromised by applications abuses. As shown in Figure 7, the "circuit board" for IC's consists of a P-doped substrate with P-doped isolation barriers that are biased at the negative-supply voltage level to provide the necessary isolation between circuit elements. When the power supply is *off*, the isolation is reduced and the chip is left vulnerable to the voltage stresses present at its input(s) and output. It is for this reason that most IC manufacturers state that the absolute maximum input and output ratings are $\pm V_s$, which strongly implies 0V with $\pm V_s = 0$.

Some IC's, such as the AD531, incorporate input-circuit protection. Many don't. Worse than failing, unprotected input transistors may simply change their parameters, a change which can be manifested in terms of increased bias current (decreased beta) or voltage offset.

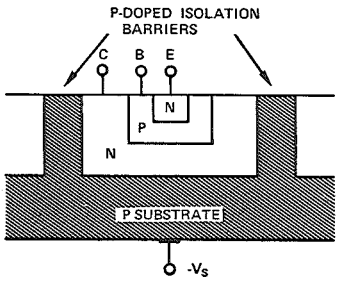


Figure 7. Bipolar I.C. construction, using junction isolation

Although failures are not generally a problem when the inputs are less than ±1V, and are never a problem when V_{IN} is less than $V_s \pm 0.5V$, higher input levels can be accommodated by using input/output protection circuits, such as those shown in Figure 8. While the 1kΩ series resistors alone will often suffice, the diode clamps to the supplies provide certain protection, except when the supplies have been switched off.

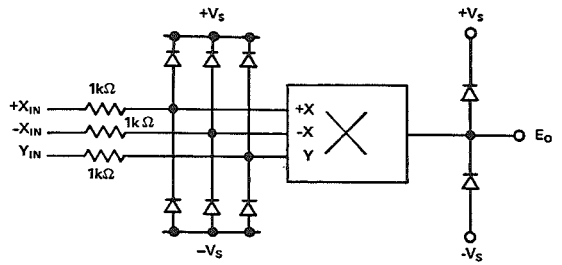


Figure 8. Protection of I.C. device against overvoltage. Diodes protect against voltage spikes, and resistors protect against power-off stresses.

ON THE HORIZON – AND BEYOND

The field of IC nonlinear devices is a largely virginal field within the rapidly-expanding analog ("linear") IC industry. As recently as one year ago, only one self-contained 4-quadrant multiplier[1,2] (AD530) and several multiplier cells had been introduced. It was noted earlier that while monolithic matched-transistor techniques are ideally suited to transconductance and log-antilog circuit techniques, the missing complement – on-chip precision resistors – have only been available for the last three years. The utilization of precision thin-film monolithic resistors, in conjunction with the superbly-matched devices that are characteristic of silicon semiconductor technology will in the long run make available scores of new circuits, both linear and nonlinear, in addition to the three basic families of multipliers (AD530, AD531. AD532) now available, and the AD7520 multiplying D/A converter. Laser trimming (exemplified by the AD532, which permits operation to rated accuracy without *any* additional components) adds a key capability to the nonlinear IC device-manufacturing process, *adjustability*. With effective utilization of this capability, the only deficiency that appears to pose fundamental limitations is speed.

Even the speed frontier can be crossed by going to dielectrically-isolated, dynamically-trimmed IC's. With such combined process-

[1]"Self-Contained I.C. Multiplier/Divider," by R.S. Burwen, *NEREM 1970 RECORD*, p. 56, Boston Section IEEE.

[2]"A Complete Multiplier/Divider on a Single Chip," by R.S. Burwen, *Analog Dialogue*, Vol. 5, No. 1, January, 1971.

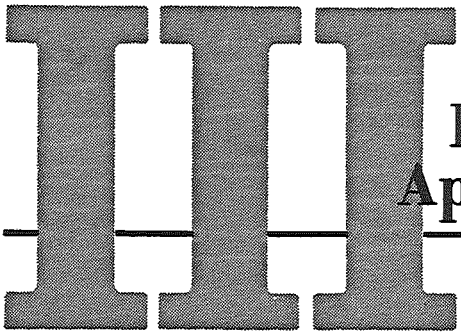
ing capabilities, 10MHz, dynamically-trimmed, <0.5% multipliers (complete-on-a-chip) become possible.

However, even before such combined techniques are ultimately exploited, circuit- and device-design ingenuity will make available a wide range of analog circuits that rely for precision on monolithically-matched active devices and dynamically-trimmed deposited thin-film resistors. For instance, it appears likely that careful exploitation of currently-available technology will soon make available multipliers with errors in the 0.1% range, using variable-transconductance techniques.

Other more-specialized multipliers will also appear for limited-polarity, wide-dynamic-range, high-accuracy applications. New IC device structures, not yet put into practice commercially (and which depart radically from conventional circuit concepts), hold out the prospect of marked improvement of one of the fundamental limitations of transconductance techniques – noise.

Along with refinements in the multiplier/divider art, IC's will soon provide high-accuracy log-antilog operations, with the potential of growth comparable to that witnessed by the industry in multiplier/dividers (and still in the accelerating stage). The first of such products will be available at the time this book sees the light of day. Such circuits are eminently integratable. Also, more-complex functions that depend on multiplication, division, or log operations, e.g., true-rms, vector-sum, and precision AGC loops, will soon appear as single chips.

Thus, the future of "nonlinear" "linear integrated-circuits" is exceptionally bright. A rough analogy can be established between the development of these basic nonlinear circuits and the history of op amps (the basic linear circuit) as follows: the "multiplier cell" techniques brought us to the 709 level, while the AD532 has brought us to the 741 stage of development, the point at which op amps became practical for widespread application. It is not unsafe to predict that the wave of op amp development that followed the 741 and led to hundreds of different IC amplifiers for virtually every application will be paralleled by a similar rapid growth in the usage and proliferation of nonlinear IC's.



Discontinuous Approximations

Chapter 5

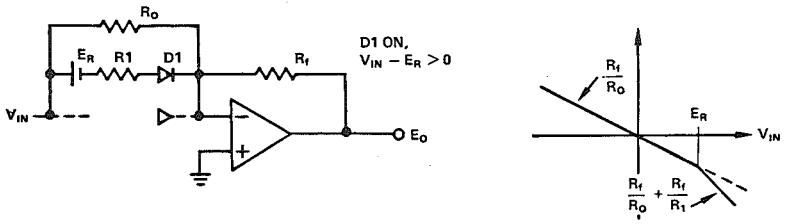
In this chapter, circuits used for obtaining piecewise-linear input-output relationships will be discussed. Examples of such relationships include piecewise-linear function fitting, absolute value, dual-mode linear responses, and sign-magnitude-to-bipolar conversion. There will also be a brief discussion of digital aids to analog function fitting.

Often, a nonlinear response can be conveniently simulated or linearized by a circuit with a response that is neither curvilinear nor linear, but is built up into an approximation of the desired response by changing the gain of the circuit as input (or output) thresholds are crossed.

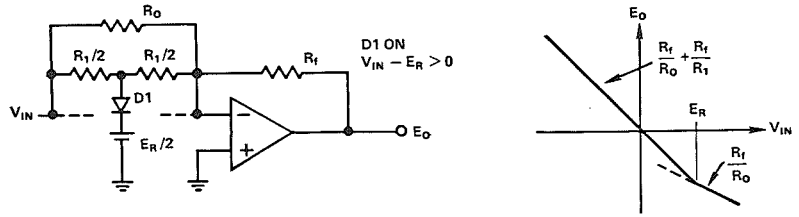
Piecewise-linear approximations to curvilinear functions were introduced in Chapter 2-1 (Figures 15 and 16), and an application to a linearization problem was plumbed in Chapter 2-3 (Figure 7). To ensure high accuracy and sharp breakpoints (the latter is not necessarily an advantage), operational amplifiers and diodes in an "ideal diode" configuration were suggested; but they are not the only way. This chapter considers the problem in a somewhat wider circuit perspective.

BREAKPOINTS

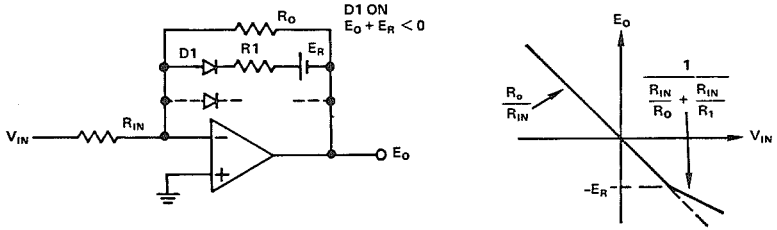
If a diode can ideally be considered as a polarity-sensitive switch having zero voltage drop when positive voltage is applied, and zero leakage current when negative voltage is applied, it can be used with bias voltages and resistance networks to construct an op-amp circuit with a controlled nonlinear response.



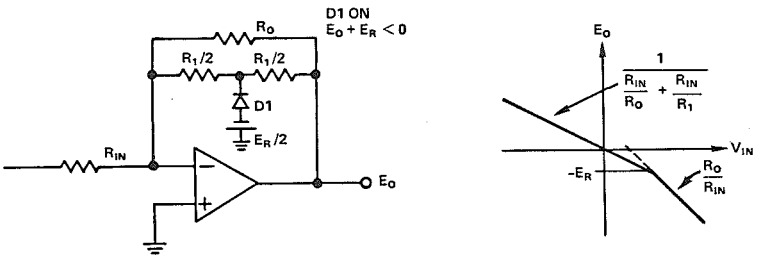
a. Series breakpoints — input



b. Shunt breakpoints — input



c. Series breakpoints — feedback



d. Shunt breakpoints — feedback

Figure 1. Series and shunt breakpoints generated in input and feedback circuits of single op amp

Figure 1 shows the input output-relationships for circuits having ideal series and shunt breakpoints, in the forward and the feedback paths. In all cases, the diode and reference are biased and circuited to cause the diode to conduct when the input has increased beyond the threshold.

The threshold, referred to the input, is equal to E_R for the diode in the forward path, and E_R, divided by the gain, for the feedback path (in the plots, it is simply referred to the output).

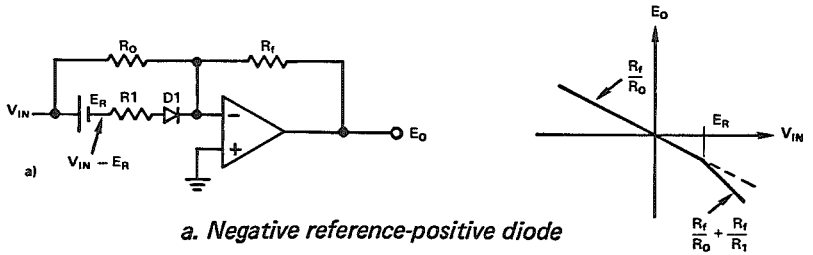
The degrees of freedom include: series vs. shunt circuits, choice of the input vs. the feedback path, and choice of polarity of both reference voltage and diode connections, as well as the choice of resistance ratios.

For additional breakpoints, similar circuits, with graduated values of E_{Ri}, are connected between the summing point and either the input or the output. The series connection is often preferred, because it is easier to get extremely high resistance in the *off* condition than negligibly low resistance in the *on* condition. However, the shunt circuit has the advantage that the reference source can be grounded (hence driven by an op amp output if a variable threshold is desired).

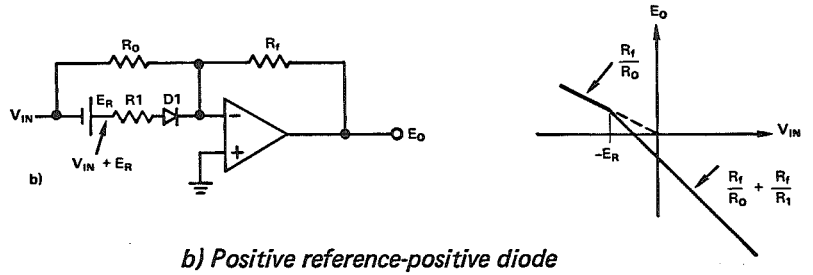
If the desired function does not go through the origin, an additive bias can be summed at the amplifier's summing point, via a resistor, to relocate it. Its effect can be viewed as a translation of the function along the input or the output axis, depending on the location of the breakpoints.

Additional monotonic shapes are available by changing the polarities of the reference and/or the diodes. Figure 2 shows the ideal responses available with different combinations of polarity in the series input case. Figure 3 shows the effect of reference polarity with multiple slopes. Note that zero output at the origin is obtained when the reference and the diode are of opposite polarity (input zero); if the reference and the diode are of the same polarity, the *extrapolated* R_f/R_o response passes through the origin, but the break occurs before it reaches zero. If zero output is desired, a bias can be added at the summing point, as mentioned

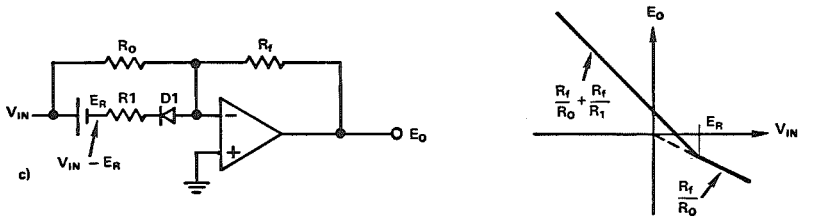
above. A complete array of shapes can be catalogued by considering all combinations of polarity, series vs. shunt, and input vs. feedback.



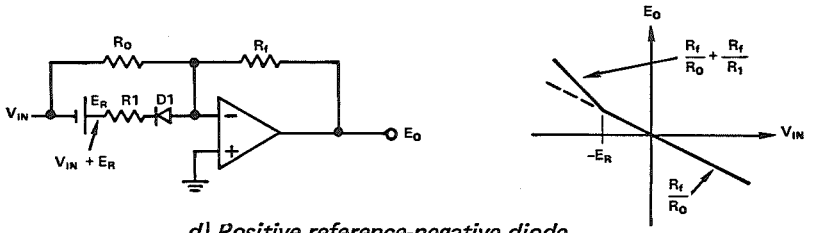
a. Negative reference-positive diode



b) Positive reference-positive diode



c) Negative reference-negative diode



d) Positive reference-negative diode

Figure 2. Effect of reference and diode polarity on input-output relationship; series breakpoints, input circuit

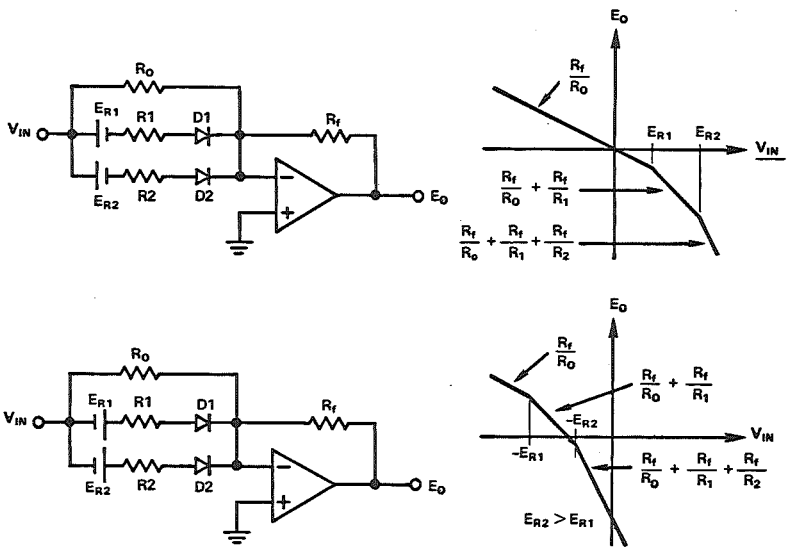


Figure 3. Effect of reference polarity on multiple slopes

The above-mentioned shapes all have monotonic derivatives, i.e., they are all concave-up or concave-down. However, by combining degrees of freedom, it is possible to obtain reversals (and ideally, many reversals, depending on the references and gains).* Figure 4 shows a single reversal, employing series input and feedback. Note that an input bias is employed to obtain zero output for zero input.

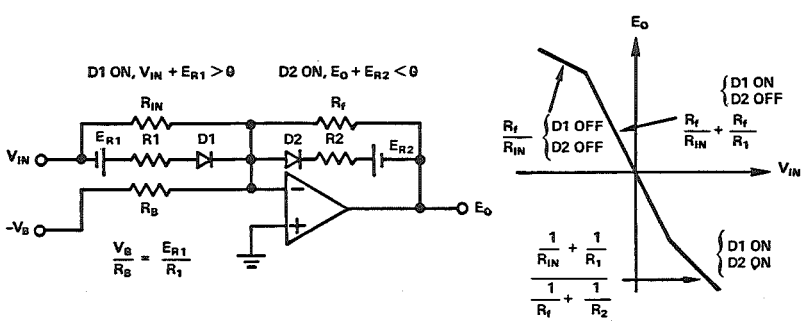


Figure 4. Use of input and feedback breakpoints to obtain reverse slopes with single amplifier

*But the incremental slope is always negative unless the + input is driven.

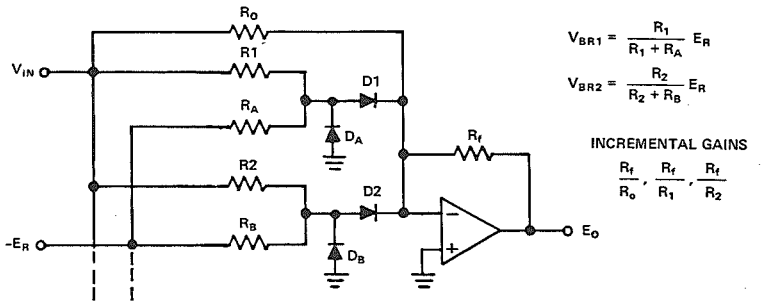
PRACTICAL CIRCUITRY

There are several problems in putting the ideal circuits mentioned earlier into practice:

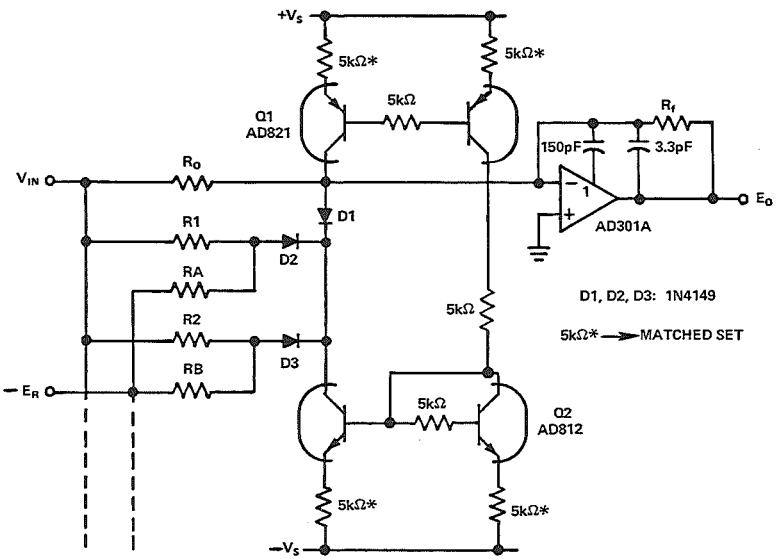
1. The references are shown floating. It would be desirable to have them derived via resistance networks, starting with a single (preferably grounded) reference. This would allow a good, stable power supply to also serve as the reference.

2. Diodes have appreciable voltage drop when conducting (about 0.5^+ V). Instead of their having a clear-cut threshold, the behavior is logarithmic. Over a 100:1 range of current variation, the threshold shifts by at least 120mV at 25°C, with a thermal shift of about 2mV/°C. From 1mA down to 10μA, series resistance increases from 25Ω to 2500Ω.

Figure 5a shows the basic elements of a circuit that can function in either the forward or the feedback path of an operational amplifier. It answers objection 1. The ideal threshold of conduction is at $V_{IN} = E_R \ R_1/(R_1 + R_A)$ for the first break, $V_{IN} = E_R \ R_2/(R_2 + R_B)$ for the second break, etc. The incremental gains are R_f/R_o, R_f/R_1, R_f/R_2, etc. Thus, the break points depend on the reference. Diodes D_A and D_B limit the reverse swing of D1, D2, etc.



a. Uncompensated-input circuit with grounded reference



b. Compensated high-speed piecewise-linear function fitter

Figure 5. Shunt-biased, series diode piecwise-linear function fitter a) in principle, b) with first-order temperature compensation

Figure 5b shows the same basic circuit, but with the added benefit of first-order compensation for the diode drops and their variation with temperature.

If the breakpoint must be sharp and located precisely, with near-zero drift, an "ideal diode" feedback circuit, employing diodes in the feedback path of an operational amplifier for polarity sensing only, may be used as a dual-mode circuit (Figure 6). In the circuit of Figure 6, if the net input current $V_{IN}/R_1 + V_R/R_4$ is positive, diode D1 is turned on, D2 is turned off, and the output (1) is

$$V_1 = -\frac{R_3}{R_1}V_{IN} - \frac{R_3}{R_4}V_R \qquad (1)$$

If output (2) is unloaded, or loaded only to common (or a virtual ground), its output is zero, since D2 is turned off and no current flows in R2.

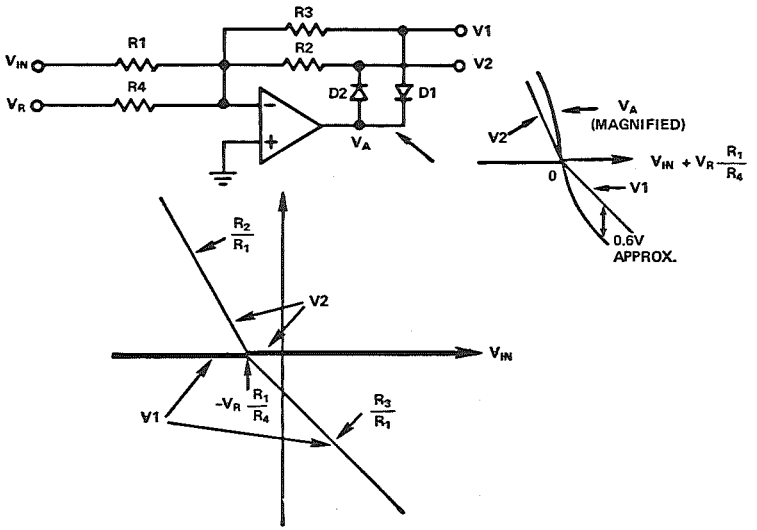


Figure 6. Ideal diode circuit

If the net input current is negative, D1 is turned off (output (1) = 0), D2 is turned on, and output (2) is

$$V_2 = -\frac{R_2}{R_1} V_{IN} - \frac{R_2}{R_4} V_R \qquad (2)$$

Thus, the output of the circuit at (1) is zero for all V_{IN} less than $-V_R (R_1/R_4)$ and proportional to positive values of the difference; output (2) is zero for all V_{IN} greater than $-V_R (R_1/R_4)$ and proportional to negative values.

Either output can be used as an incremental "ideal-diode" breakpoint in a system which sums a number of breakpoints;[1] the

[1] See Figures 15 and 16, Chapter 2-1 and Figure 7, Chapter 2-3.

two outputs ($R_2 \neq R_3$) summed together provide a two-slope response, with the break at $-V_R(R_1/R_4)$. A bias can be summed into the summing amplifier to offset the break point (Figure 7).

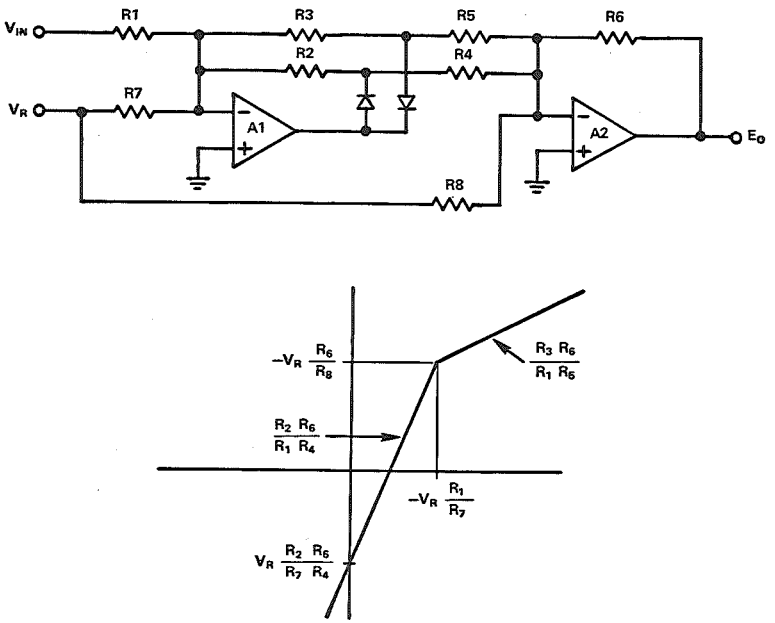


Figure 7. Ideal diode in high-accuracy dual-mode circuit

CURRENT SWITCHING

The circuit of Figure 8 is an "ideal diode" with current output. When V_{IN} is greater than V_R, the amplifier output drives the gate of the enhancement-mode FET with whatever voltage is necessary to maintain the voltage across R equal to $(V_{IN} - V_R) = I_R$. When V_{IN} is less than V_R, the FET shuts off, and the diode conducts away the reverse current from V_R through R to maintain the voltage at R equal to V_{IN}.

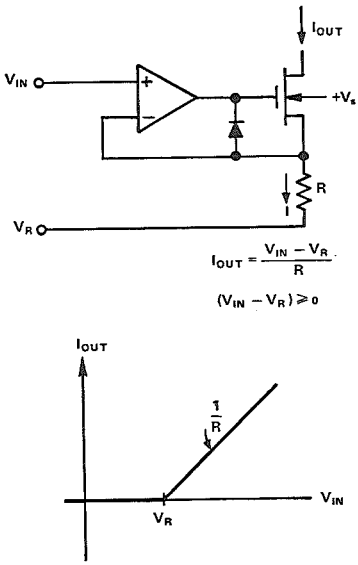


Figure 8. Unidirectional linear voltage-to-current switch

SPEED IMPROVEMENT

All of the above "ideal-diode" circuits are relatively slow: at the break point, the output must slew through a dead band of two diode drops; and charge stored in a capacitive load requires time to discharge through the feedback resistor in the *off* condition. Though the circuit has a low dynamic impedance while conducting, it must contend with greatly-reduced loop gain while switching at high speeds—first, because of the amplifier's reduced open-loop gain, second, because of the increased loop attenuation due to the high diode impedance near zero.

In the circuit of Figure 9, the switching diodes have been replaced by transistors Q2 and Q1, which saturate when the net input current becomes positive or negative, respectively, and maintain the output near ground. The circuit is considerably faster than the diode circuit, because the output impedance is always quite

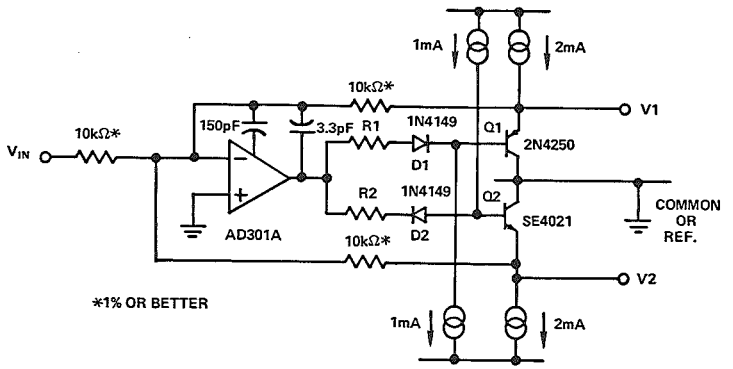


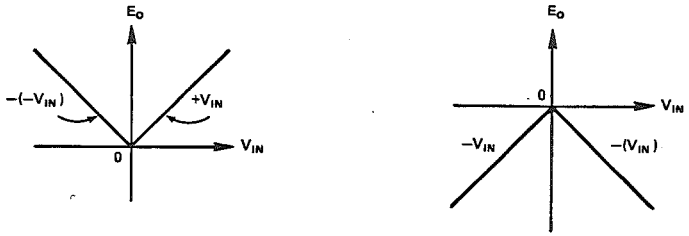
Figure 9. Low-output impedance "ideal-diode" circuit

low—in the saturated condition, it is about 5Ω, and in the active region, it is even lower, about 0.01Ω. D1, D2, R1, and R2 can be adjusted to minimize the dead zone. The output offsets of Q1 and Q2 in the saturated condition will be about 10mV.

This circuit can be connected as a full-wave mean-value circuit by connecting a differential low-pass (R-C-R) filter across the two outputs, and subtracting to obtain the average of the rectified input. It will provide reasonably accurate measurements at frequencies as high as 100kHz.

ABSOLUTE-VALUE CIRCUITS

Many uses of absolute-value circuits have been discussed in earlier chapters. They include measurements of magnitude, conditioning of signals for input to one-quadrant multipliers and other nonlinear devices, measurements of mean absolute deviation, full-wave rectification, vector computation, etc. Absolute-value voltages can be made available in either positive or negative polarity (Figure 10).



a) Positive absolute value + | V_{IN} | *b) Negative absolute value − | V_{IN} |*

Figure 10. Positive and negative absolute value

The circuit of Figure 11 is a typical absolute-value circuit. It comprises an ideal-diode and a differencing circuit. For positive input voltages, $V_B = 0$, $V_A = -V_{IN}(R_3/R_1)$, and the output is

$$E_o = \frac{R_3 R_5}{R_1 R_4} V_{IN} \tag{3}$$

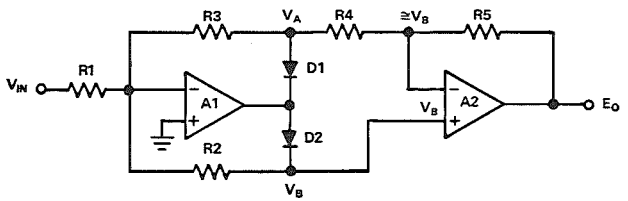


Figure 11. Practical absolute-value circuit

if all resistors are equal. For negative inputs, D1 is open, D2 conducts

$$-\frac{V_{IN}}{R_1} = \frac{V_B}{R_2} + \frac{V_B}{R_3 + R_4} \tag{4}$$

and

$$E_o = V_B \left(1 + \frac{R_5}{R_3 + R_4}\right) \tag{5}$$

Again, it can be seen that if all resistances are equal, the right-hand sides of both equations will be $1\frac{1}{2}V_B$ (multiplying (4) through by R_1); hence $E_o = -V_{IN}$. Therefore, the output will be equal to V_{IN} if positive and $-V_{IN}$ if negative, or $+|V_{IN}|$.

POLARITY DETECTION

Quite often, it is useful to have a polarity signal, as well as the absolute-value output. For example, to use a one-quadrant multiplier as a four-quadrant multiplier, it is possible to take the absolute-value of both inputs, and compare the polarities in an exclusive-or gate ("0", first and third quadrants (+), "1", second and fourth quadrants (–)). A sign-magnitude-to-bipolar circuit may be used to restore the polarity, if desired. Another application is in sign-magnitude A/D conversion, using a unipolar converter.

The circuit of Figure 11 may be followed by the polarity detection circuit shown in Figure 12, which makes use of the 2-diode-drop transition region at the output of A1 to derive a logic signal as a function of polarity. The output of the circuit will be positive-true "1" when the input signal is positive, and "0" when the input signal is negative.

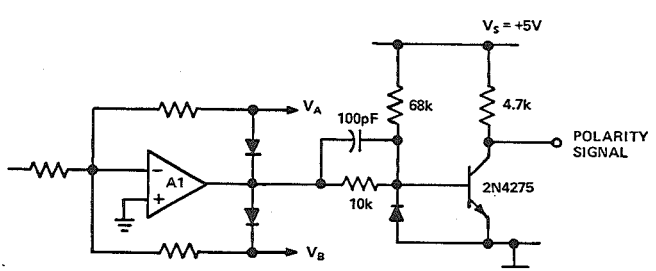


Figure 12. Polarity output signal from ideal-diode circuit

SPECIAL-PURPOSE ABSOLUTE-VALUE CIRCUITS

Figure 13 shows a high-input-impedance absolute-value circuit, making use of an ideal diode circuit and an adder-subtractor. The negative inputs of both amplifiers must follow the positive inputs.

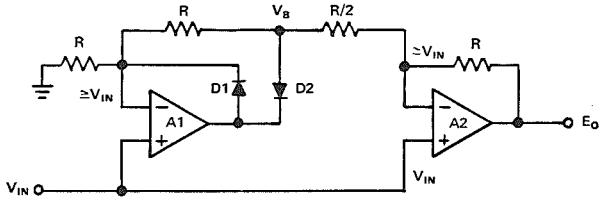


Figure 13. High-input-impedance absolute-value circuit

When V_{IN} is positive, the current V_{IN}/R to ground is supplied by D1; D2 is off; therefore no current flows through any of the other three resistors, and E_o must follow V_{IN}. When V_{IN} is negative, D2 conducts, D1 is off, and $V_B = 2V_{IN}$. The output is $(+3V_{IN} - 4V_{IN}) = -V_{IN}$, a positive voltage; therefore $E_o = |V_{IN}|$.

Figure 14 is a circuit that takes the absolute value of a differential input voltage and converts it to a current. It operates in similar fashion to the current-switching circuit of Figure 8, but responds to full-wave inputs. It is useful as an input to devices that call for current inputs, such as integrating meters and logarithmic multiplier/dividers.

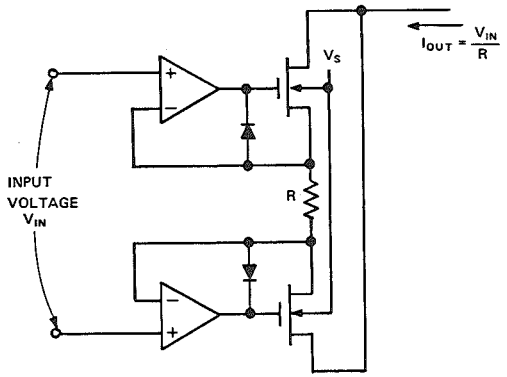


Figure 14. Differential high-input-impedance voltage-to-current absolute-value circuit

SIGN-MAGNITUDE TO BIPOLAR

Figure 15 depicts a circuit that will accept a positive *magnitude* signal and a negative-true *polarity* signal; at the output, it provides a bipolar signal with polarity determined by the inputs.

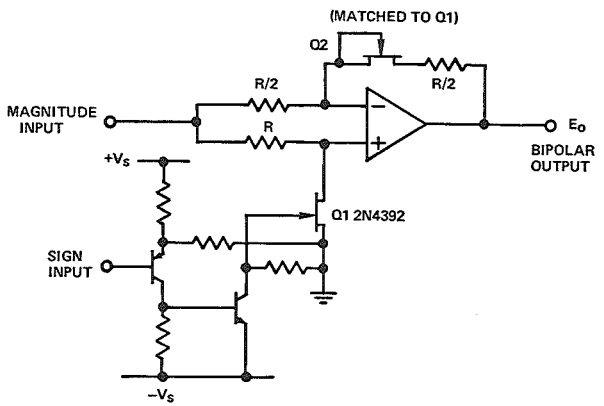


Figure 15. Sign-magnitude-to-bipolar circuit

When the FET switch, Q1, is *off*, the amplifier A1 operates as a unity-gain follower, with performance limited by the common-mode performance of the amplifier, and the impedance level of the input resistors (bias current and noise pickup). When the FET switch is *on*, the positive input signal is shunted to ground, and the amplifier functions as an inverter. Since Q1 does not have zero *on* resistance, there is some leakage of signal to the + input terminal. However, it is almost exactly compensated for (over a wide temperature range) by the resistance of Q2, the FET in series with R2. Improved accuracy can be obtained using 3 equal R's, and adding a second matched FET in series with Q2.

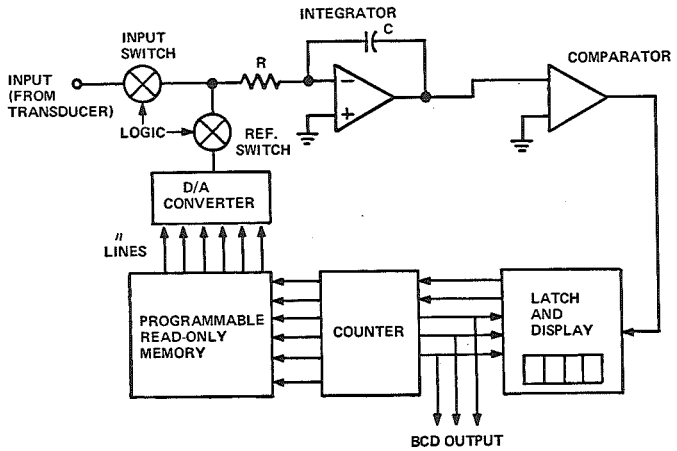
A NOTE ON DIGITAL TECHNIQUES

The read-only memory can be thought of as a "digital function fitter," since it can be programmed to fit (in pointwise fashion—2^n-1 points) an arbitrary function of an input digital number ("address").

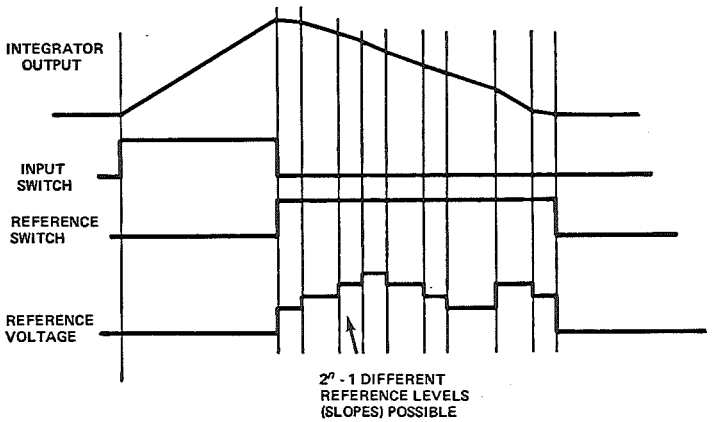
It is natural to consider the possibility of converting to digital, applying the digital number to a ROM, and (if necessary) converting the modified digital number occurring at the output of the ROM back to analog. It may (or may not) be more cumbersome than purely analog function fitting, and the discreteness of the fit may (or may not) be undesirable. Costs for both digital and analog techniques are coming down, and the issues are not clearly definable, since experience and inclination can weigh equally with marginal cost differences.

However, there are applications that involve conversion anyway, where consideration of a ROM for linearizing may be especially appropriate. For example, in a conventional dual-slope integrating system (used, typically, in digital panel meters), the signal input is integrated for a fixed number of counts. Then a reference voltage is applied to the integrator in the opposite polarity, and the number of counts required for the return to zero from the initial condition established by the integrated analog voltage, is a measure of the average value of the analog voltage.

For compensation and linearization of transducers, it is possible to use a D/A converter to adjust the reference-voltage level (Figure 16). The D/A converter is fed by a ROM, which has as its input



a. Block diagram of linearized dual-slope A/D converter



b. Waveforms of linearized dual-slope converter

Figure 16. Analog-digital transducer linearizing circuit and A/D converter

the counter output. As the count increases during integrator discharge, the "address" (i.e., input number) to the ROM changes. The ROM's programmed output changes, depending on the program, and feeds the D/A converter a number, which is converted to an analog reference level, which modulates the rate at which the integrator is discharged. Using this approach, there can be as many as $2^n - 1$ integrator rates, where n is the number of bits used by the ROM and the D/A converter.

With this technique, individual transducers can be linearized and gain-compensated. First, the transducer output can be calibrated, by feeding its output and the true measurements into a computer, which can generate a paper tape of the program needed by the ROM. The tape can then be used to program a field-programmable ROM. The ROM can then be shipped with the transducer (it can even bear the same serial number), much as calibration curves have been in the past. At the same time the transducer is installed, the ROM can be installed in a compatible A/D converter; in this way, the output of the A/D converter will be completely matched (linearized and gain-compensated) to the individual transducer to which it is committed (or multiplexed).

III Multifunctional Devices: Powers & Roots

Chapter 6

A perhaps unfamiliar, but nevertheless very useful, nonlinear device is the *multi-function circuit*. It combines multiplication and division with the ability to raise a voltage (or voltage ratio) to an arbitrary positive power or negative (reciprocal) power. The magnitude of the power may be greater than unity ("power") or less than unity ("root"). A good example of such a multifunction circuit (and the first to appear on the market) is the Analog Devices Model 433. Its transfer function is

$$E_o = \frac{10}{E_{REF}} V_y \cdot \left(\frac{V_z}{V_x}\right)^m \qquad (1)$$

where

E_o = Output voltage, $\geqslant 0$

V_y, V_z, V_x = Inputs, $\geqslant 0$

E_{REF} = Constant $\cong +9V$

m = Any number in the range 0.2 to 5, set by the ratio of two resistors, e.g., m = 2.72, or m = 0.318

A reference voltage, equal in magnitude to the constant, E_{REF}, is available as an input for operations involving only one or two variables, or for other purposes involving a reference voltage.

This combination of the three functions, multiplication, division, and exponentiation, within one small (38 X 38 X 16mm) module, yields computing power comparable to that of a small algebraic analog computer, or a log-log slide rule.

The multifunction circuit can be easily connected to perform many different functions, as determined by the choice of inputs, jumpers, and (for exponents) resistors. Among the available functions are:

1. Multiplication $E_o = K V_y V_z$

2. Division $E_o = K(V_z/V_x)$

3. Squaring $E_o = K V_y V_z \ (V_y = V_z)$

   or $E_o = K V_z^2$

4. Square-Rooting $E_o = K V_y/E_o$

   or $E_o = K V_z/E_o$

   or $E_o = K V_z^{0.5}$

5. Root of ratio $E_o = K V_y \left(\frac{V_z}{V_x}\right)^m \qquad m < 1$

6. Power of ratio $E_o = K V_y \left(\frac{V_z}{V_x}\right)^m \qquad m > 1$

7. Reciprocal power $E_o = K V_y \left(\frac{V_z}{V_x}\right)^m = K V_y \left(\frac{V_x}{V_z}\right)^{-m}$

In addition, there are other functions that can be performed by a single multifunction circuit and a modicum of external components

8. True rms (Chapters 2-3, 3-7) $E_o = \overline{K V_y V_z}/E_o = \sqrt{\overline{KV_{in}^2}}, \quad (V_y = V_z \geqslant 0)$

9. Vector sum (Chapter 2-3) $E_o = \sqrt{V_1^2 + V_2^2}$

$V_1, V_2 \geq 0$

10. Trignometric Functions (Chapters 2-1, 2-3, and 2-5) $E_o = K \tan^{-1} (V_2/V_1)$

$E_o = K \sin \theta$

Two factors account for the versatility of the multifunction circuit:

1. *Log-antilog operating principle*: Powers and roots can be easily generated by adjusting the gain of either the log or antilog portions of the circuit (or both). In the divider connection (m = 1, V_y constant), the log-ratio input section provides good accuracy over a much wider dynamic range than is possible with linear ratio circuits. A comparison of the multifunction circuit, as a divider, and a conventional "inverted-multiplier" divider circuit (Chapter 3-3) is shown in Figure 1.

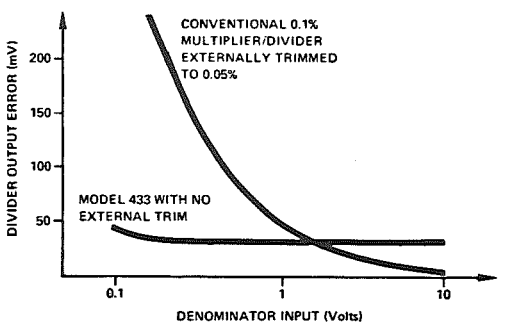


Figure 1. Divider error as a function of denominator level: multifunction circuit (m = 1) compared with an "inverted-multiplier" circuit.

2. *Three variable inputs are useful:* The ZY/X transfer function makes possible implicit solutions, through the use of feedback, of equations such as those for root-mean-square and vector addition. The additional variable also makes possible two-variable multiplication or division with voltage-adjustable scale factors, and direct implementation of such equations as the ideal gas relationship, involving pV/T.

CIRCUIT DESCRIPTION

The multifunction circuit is shown as a simplified schematic diagram in Figure 2 and an operational block diagram in Figure 3. It is in many ways similar to the log-antilog multiplier-divider circuits described in Chapter 3-2 (Figure 20) and Chapter 3-3 (Figure 20).

Amplifiers A1 and A2 and dual-transistor Q1 are connected so that the log of the ratio of input voltages V_Z and V_X (the difference of their logarithms) appears at the base of Q1B, multiplied by the usual kT/q. The antilog circuit is basically the log circuit in reverse: the input is applied at the base of Q2B, and the output, at A3, is proportional to the exponential of the input-times-the reference-current established by D1, R4, and A4. Since the argument of the exponential is multiplied by q/kT, the temperature effects are cancelled out.

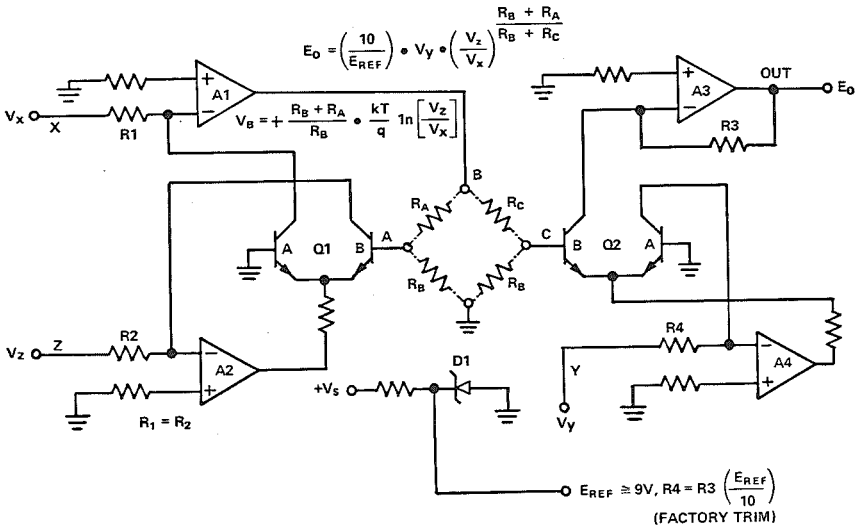


Figure 2. Simplified schematic of the multifunction circuit

The symmetrical arrangement of the circuit provides very low scale-factor and offset drift, independent of the denominator (V_X) input level. The scale-factor stability is limited primarily by the zener reference, D1, and the relative drifts of resistors R1 through R4.

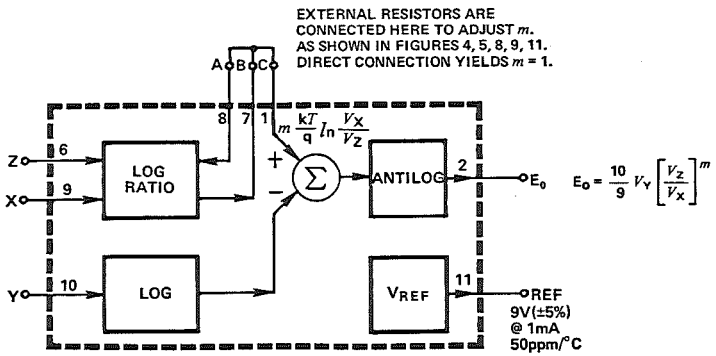


Figure 3. Functional block diagram of Model 433

POWERS AND ROOTS

The distinguishing feature of the multifunction circuit is its ability to take roots or powers of voltage ratios (with one or both voltages variable).

Any exponent between 1/5 and 5 (e.g. 1/4.73, 1/3, 1/2, 1/1.7, 1.05, 2.0, 2.1, etc.) can be obtained by attenuating or amplifying the log of the ratio of the Z and X inputs that appears at point "A" in the circuit of Figure 2. Negative exponents are obtained by interchanging the signals applied to the X and Z inputs.

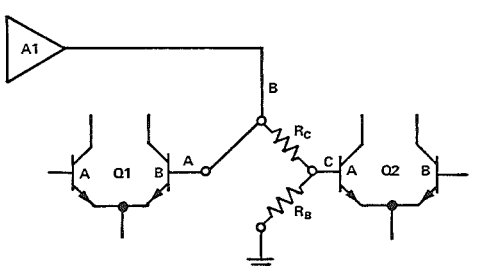


Figure 4. Connections for $1 > m = \dfrac{R_B}{R_C + R_B}$

Connections for the "root mode" (exponents less than unity) are shown in the partial circuit of Figure 4. The resistive divider R_C, R_B, attenuates the log of the ratio of Z and X before the antilog is taken in the output section. The exponent m is equal to the attenuation, $R_B/(R_B + R_C)$.

$$E_o = K\,V_y\,\epsilon^{m\ln(V_z/V_x)} \tag{2}$$

$$E_o = K\,V_y\left(\frac{V_z}{V_x}\right)^m = K\,V_y\left(\frac{V_z}{V_x}\right)^{\frac{R_B}{R_B+R_C}} \tag{3}$$

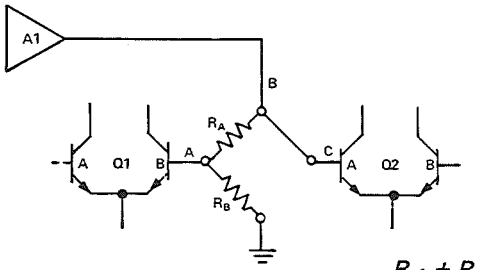


Figure 5. Connections for $1 < m = \dfrac{R_A + R_B}{R_B}$

Connections for the "power mode" (exponents greater than unity) are shown in the partial schematic of Figure 5. In this case, since the feedback voltage is attenuated by $R_B/(R_B + R_A)$, the gain, m, is $(1 + R_A/R_B)$. Therefore

$$E_o = K\,V_y\left(\frac{V_z}{V_x}\right)^m = K\,V_y\left(\frac{V_z}{V_x}\right)^{1+\frac{R_A}{R_B}} \tag{4}$$

Figure 6 shows normalized plots of the function for several representative values of m, $V_x = 10$, $V_y = E_{REF}$. As might be expected, for $m = 1$, the response is linear with a slope of unity. For $m > 1$, the slope increases from zero at $V_z = 0$ to m at $V_z = 10V$. For $m < 1$, the slope decreases from "infinity" at zero to m at $V_z = 10V$. Thus, while "powers" are quite stable, with a maximum gain of 5 at full scale, "roots" become less stable as the input approaches zero (resulting in greatly magnified noise and drift), but are quite stable for larger values of the input ratio. Fortunately, the multifunction circuit has very low noise and drift, referred to the input, so that over a 100:1 range of input ($V_z = V_x$), the errors at the extreme exponents (1/5 and 5) tend to be small. This can be seen in Figure 7, a plot of output noise vs. denominator at constant ratio.

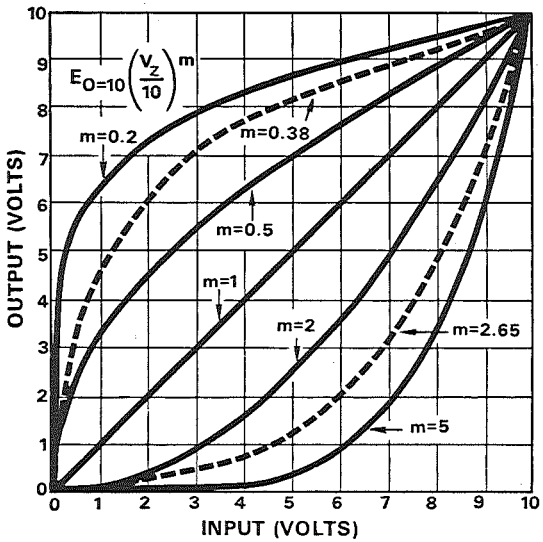


Figure 6. Output vs. input for several values of the exponent, m

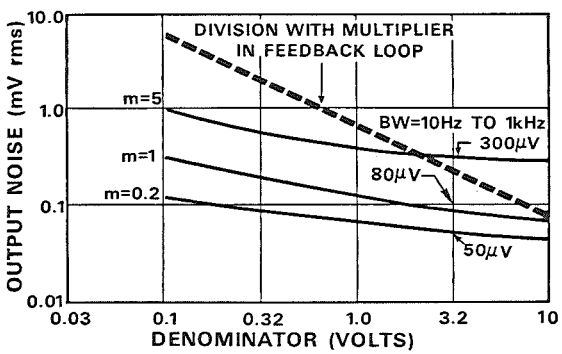


Figure 7. Output noise vs. denominator voltage (unity ratio) for the 433, compared with noise output of inverted-multiplier divider (log scales)

Since incremental input noise, referred to the output, is approximately proportional to the slope of the function, it is useful to know the input level at which a given slope (of the curve in Figure 6 corresponding to the desired m) occurs. This is determined by differentiating the exponential relationship, setting the derivative, dE_o/dz (where $z = V_z/V_x$), equal to a specific value of G (the slope or gain), and solving for the corresponding value of z, i.e., z(G), at which it occurs.

$$z(G) = \left(\frac{G}{m}\right)^{1/(m-1)} \tag{5}$$

The values of z corresponding to various orders-of-magnitude of G are listed below:

m	z(G=1)	z(G=10)	z(G=100)
1/5	0.134	0.008	0.0004
1/4	0.157	0.007	0.0003
1/3	0.192	0.006	0.0002
1/2	0.250	0.0025	0.00002
1	all values		
2	0.500	5.0	50.0
3	0.577	1.826	5.77
4	0.630	1.357	2.92
5	0.669	1.189	2.115

A convincing demonstration of the efficacy (and repeatability) of the multifunction circuit can be seen in Figure 8. Two 433 multifunction circuits are connected in cascade; the first is set for m = 1/5, the second is set for m = 5. The input to the first is a 0 to +10V 5Hz triangular wave. The output of the first, as expected, has the characteristic 5th-root relationship sketched in Figure 6; it is equal to $10(V_{in}/10)^{1/5}$.

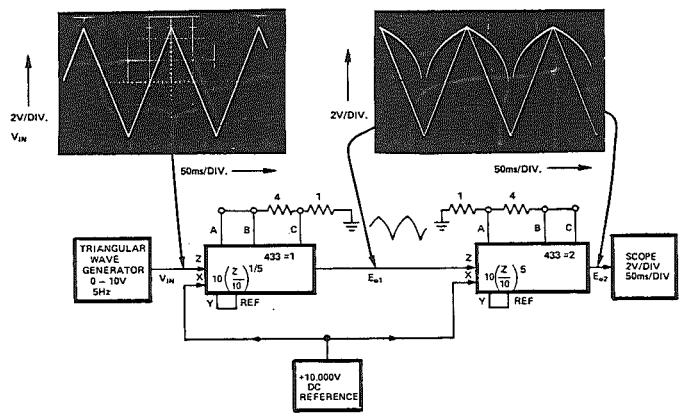


Figure 8. Fifth root and fifth power cascaded

The output of the second 433 is a triangular wave with little apparent distortion, except in the vicinity of zero. Its response of $10(E_{o_1}/10)^5$ inverts the fifth-root response of E_{o_1} to achieve a linear overall response.

Tailoring the Range of Exponent-Adjustment

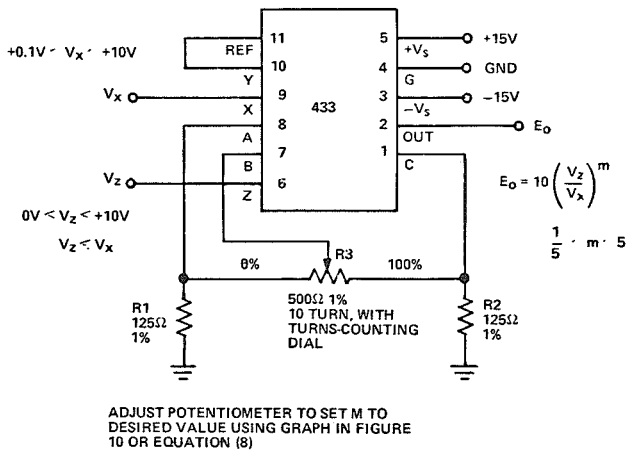


Figure 9a. 433 multifunction module computes continuously-adjustable power or root of ratio

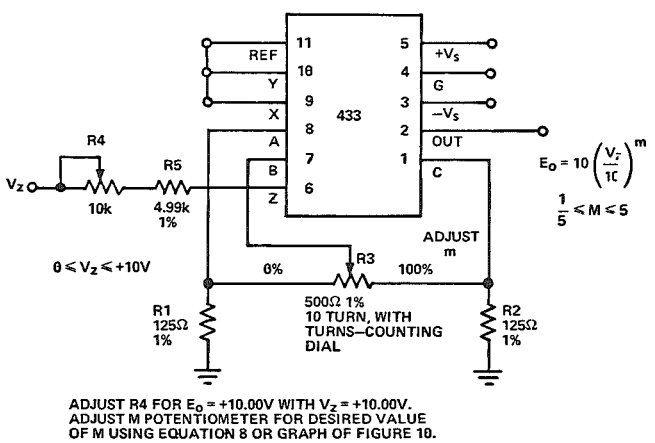


Figure 9b. 433 multifunction module takes continuously-adjustable power or root of single variable

Figure 9. Wide-range exponent adjustment

For some purposes, it is useful to allow the exponent to be adjusted through unity without rewiring or switching. This can be easily accomplished with a single potentiometer, connected as shown in Figure 9a (V_z and V_x both variable) or Figure 9b (V_z only variable), to allow a range of continuous variation of m from 1/5 to 5. Sucn an arrangement is especially useful for linearizing and curve-fitting, since the pot can be adjusted until the output waveform has the desired shape. The exponent may then be read to within ±5% (or better) by the use of the calibration curve (Figure 10).

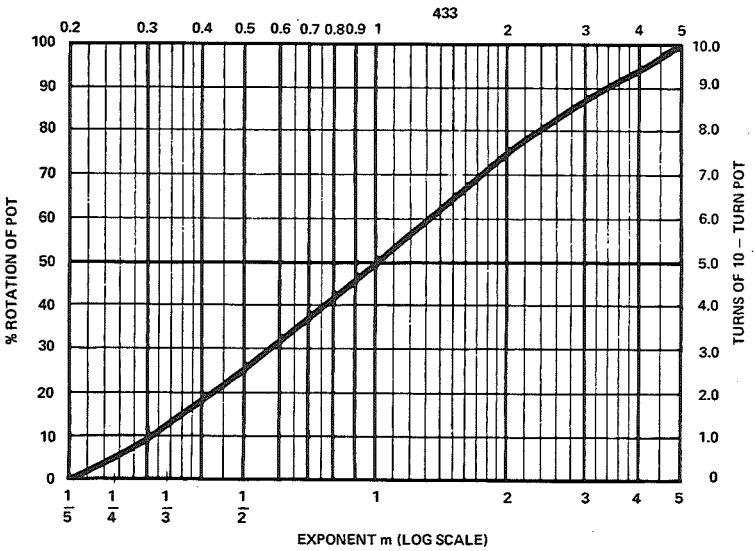


Figure 10. Potentiometer rotation as a function of exponent, m, for the circuits of Figure 9, using 433

For example, suppose that the setting of the pot that produces best linearity (in a linearizing application) is experimentally found to be 3.20 turns. Referring to Figure 10, one finds that for 32% rotation, the calibration curve shows an m of 0.6. Thus, the empirically-arrived-at optimum exponent turns out to be 0.6:

$$E_o = 10(V_z/V_x)^{0.6} \qquad (6)$$

The calibration curve can also be used to preset a desired exponent. Suppose, for example, that a transfer function of

$$E_o = 10(V_z/10)^{1.5} \tag{7}$$

is desired. First, set up the circuit of Figure 9b, then determine the setting of the exponent potentiometer from Figure 10. In this case, m = 1.5 corresponds to about 64%. Set the pot to 6.40 turns.

If an accurate calibration of m is desired, a high-quality 10-turn pot with less than 0.1% nonlinearity and an accurately-calibrated turns-counting dial should be used. Resistors R1 and R2 should be matched to 0.1%, and should exactly equal 1/4 of the total resistance of the pot. Under these conditions, if α is the fractional rotation of the pot, the relationship between α and m is

$$m = \frac{1 + 4\alpha}{5 - 4\alpha}, \qquad \alpha = \frac{5m - 1}{4(m + 1)} \tag{8}$$

as plotted in Figure 10.

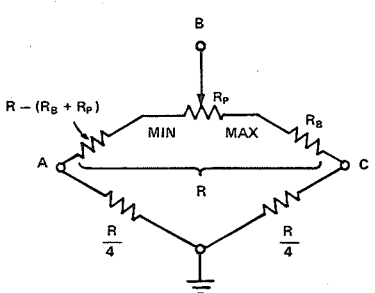


Figure 11. Configuration for arbitrary range of adjustment of the exponent, m

For smaller ranges of exponent adjustment, the potentiometer circuit may include resistances on either or both ends of the pot to tailor the range of adjustment to within the desired limits. Figure 11 shows how this may be accomplished. The design equations for R, R_B, and ($R - R_B - R_P$), in terms of the minimum

and maximum values of m and a chosen value of pot resistance are:

$$\frac{R_B}{R} = \frac{5 - m_{max}}{4(1 + m_{max})} \tag{9}$$

$$R = R_P \frac{1 + m_{min}}{\frac{5}{4} - \frac{R_B}{R} - m_{min}\left(\frac{1}{4} + \frac{R_B}{R}\right)} \tag{10}$$

The ratios R_B/R and R/R_P are calculated from the maximum and minimum values of m. Then, a suitable (low) value of R_P is chosen, R is computed, R_B is computed, and $(R - R_P - R_B)$ is established.

Table of Exponents and Ratios

Table 1 shows a set of calculated values of $(V_z/V_x)^m$, for the integral (and their reciprocal) powers from 1 to 5, to facilitate checks on the accuracy of the power/root setting.

TABLE 1

TABLE OF EXPONENTS AND RATIOS

$(V_z/V_x)^m$ as a function of V_z/V_x and m [in $E_o = KV_y(V_z/V_x)^m$]

$KV_{y_{max}} = 10V$, except as noted for values of $V_z/V_x > 1$

	V_z/V_x ↓ \ m →	1/5	1/4	1/3	1/2	1	2	3	4	5
$\frac{V_z}{V_x} < 1$	0.01	0.398	0.316	0.2155	0.100	0.010	0.0001	–	–	–
	0.025	0.478	0.3975	0.2925	0.158	0.025	0.0006	–	–	–
	0.05	0.5495	0.473	0.3685	0.2235	0.050	0.0025	0.0001		
	0.1	0.631	0.5625	0.464	0.316	0.100	0.0100	0.0010	0.0001	
	0.25	0.758	0.707	0.630	0.500	0.250	0.0625	0.0156	0.0039	0.0010
	0.5	0.8705	0.841	0.7935	0.707	0.500	0.250	0.125	0.0625	0.0312
	1.0	1.	1.	1.	1.	1.	1.	1.	1.	1.
$\frac{V_z}{V_x} > 1$	2.0	1.1485	1.189	1.260	1.414	2.000	4.000	8.000	16.000	32.000
	($KV_{y_{max}}$)	(8.706)	(8.409)	(7.937)	(7.071)	(5.000)	(2.500)	(1.250)	(0.625)	(0.312)
	5.0	1.3795	1.4955	1.710	2.236	5.000	25.000	125.00	625.00	3125
	($KV_{y_{max}}$)	(7.248)	(6.687)	(5.848)	(4.472)	(2.000)	(0.400)	(0.080)	(0.016)	(0.003)
	10.0	1.585	1.7785	2.1545	3.1625	10.000	100.00	1000.0	10,000	–
	($KV_{y_{max}}$)	(6.310)	(5.623)	(4.642)	(3.162)	(1.000)	(0.100)	(0.010)	(0.001)	–

Square-Root Circuit

While the square root may be computed by setting m = 1/2, it is also possible to compute the square root with m = 1, saving the cost of a precision resistor-pair. This is done by an implicit solution, with the output voltage fed back to the denominator input, as shown in Figure 12.

$$E_o = 10(V_z/V_x)^1 = 10(V_z/E_o) \quad (11)$$

$$E_o^2 = 10\,V_z \quad (12)$$

$$E_o = (10V_z)^{1/2} \quad (13)$$

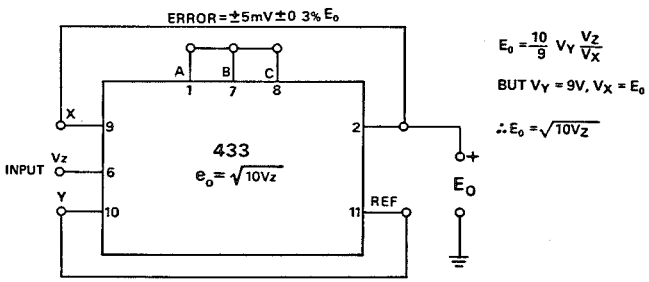


Figure 12. Square root circuit using divider with feedback

Figure 13 is a plot of the error of the 433 connected in this configuration, compared with the "inverted-multiplier" square-root circuit, using a conventional 0.1% multiplier/divider. For low values of input ($\leqslant 0.1$V), the multifunction circuit is considerably more accurate.

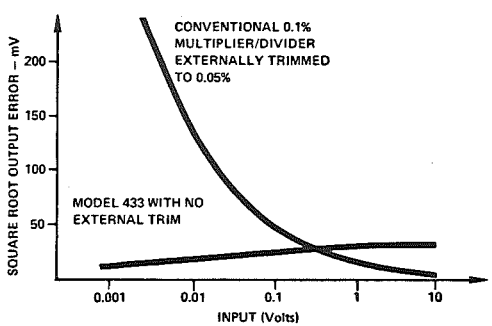


Figure 13. Square root error of 433 compared with square-root error of inverted-multiplier divider connected for square-rooting

In general, the multifunction circuit can obtain the m/(m + 1) power of V_z by this feedback technique, but its usefulness is limited, since it "uses up" the denominator input, and, in any event, requires a pair of resistors that could be used to implement the power $m' = m/(m + 1)$ directly.

SPECIFICATIONS

Specifications of a representative modular multifunction circuit, the Analog Devices Model 433J/B are listed in Table 2. The general format is similar to that shown for the multiplier and divider specifications discussed in Chapters 3-2 and 3-3; it will not be reviewed in detail here, except for specific pertinent comments.

General Expression: The transfer function is listed as

$$E_o = \frac{10}{9} V_y \left(\frac{V_z}{V_x}\right)^m \tag{14}$$

The coefficient "9" is initially set at 9.0V ±5% to match the reference output voltage V_{REF}. Thus, if the reference voltage (or a calibrated equivalent voltage) is applied to V_y,

$$E_o = 10\left(\frac{V_z}{V_x}\right)^m \tag{15}$$

The transfer gain may be trimmed to a value less than (10/9 ±5%) by adding resistance in series with the Y input; a 25kΩ variable resistor is the usual vehicle for settings near unity.

Input Range

The input signal range to the Y, Z, and X terminals is 0 to +10V, positive only; i.e., the 433 is a one-quadrant (I) device that will not respond to negative input voltages or produce negative output voltages. Nevertheless, the *Maximum Safe* input voltage rating is

TABLE 2. SPECIFICATIONS OF MULTIFUNCTION CIRCUITS (Typical @ +25°C Unless Otherwise Noted).

Model	433J	433B
General Expression	$E_O = +\frac{10}{V_{REF}} V_y \left(\frac{V_z}{V_x}\right)^m$	*
Rated Output[1]	+10.5V @ 5mA	*
Input		
Signal Range	$0 \leqslant V_x, V_y, V_z \leqslant +10V$,	*
Max Safe Input	$V_x, V_y, V_z \leqslant \pm 18V$	*
Resistance		
X Terminal	100kΩ ±1%	*
Y Terminal	90kΩ ±10%	*
Z Terminal	100kΩ ±1%	*
External Adjustment of the Exponent, m		
Range for m <1 (Root)	$1/5 \leqslant m < 1$, $m = \frac{R_B}{R_C + R_B}$	*
Range for m >1 (Power)	$1 < m \leqslant 5$, $m = 1 + \frac{R_A}{R_B}$	*
	$(R_1 + R_2) \leqslant 200\Omega$	*
Accuracy (Divide Mode)[2,3]		
Total Output Error @ +25°C (for specified input range)		
Typical (RTO)	±5mV ±0.3% of output	±1mV ±0.15% of output
Max Error (RTO)	±50mV	±25mV
Input Range ($V_z \leqslant V_x$)	0.01V to 10V, V_z	*
	0.1V to 10V, V_x	*
Over Specified Temp. Range	±1%	±1% max
Output Offset Voltage (Not Adjustable)		
Initial @ +25°C max	±5mV	±2mV max
Offset vs Temp.	±1mV/°C	±1mV/°C max
Noise, 10Hz to 1kHz		
V_x = +10V	100μV rms	*
V_x = +0.1V	300μV rms	*
Bandwidth, V_y, V_z Small Signal (-3dB), 10% of DC Level V_y or V_z		
$V_y = V_z = V_x$ = 10V	100kHz	*
$V_y = V_z = V_x$ = 1V	50kHz	*
$V_y = V_z = V_x$ = 0.1V	5kHz	*
$V_y = V_z = V_x$ = 0.01V	400Hz	*
Full Output (V_y or V_z = 5VDC ±5VAC)	(V_x) • (5kHz)	*
Reference Terminal Voltage[1]		
V_{ref} (Internal Source)	+9.0V ±5% @ 1mA	*
vs Temp (0 to +70°C)	±0.005%/°C	*
Power Supply Range		
Specified	±(14.7 to 15.3)VDC @ 10mA	*
Operating	±(12 to 18)VDC	*
Temperature Range		
Specified	0 to +70°C	-25°C to +85°C
Storage	-25°C to +85°C	-55°C to +100°C
Package Outline	FA-7	*
Case Dimensions	1½" x 1½" x 0.62" 38 x 38 x 16mm	*

*Same specifications as 433J.
[1] Terminals short circuit protected to ground only.
[2] Accuracy is specified in divide mode which is a worst case condition. Input range is 10mV to 10V for specified accuracy when connected as a multiplier.
[3] Error is defined as the difference between the measured output and the theoretical output for any given pair of specified input voltages.
Specifications subject to change without notice.

±18V; though voltages outside its normal range are computationally irrelevant, they will not harm the unit.

Accuracy, Divide Mode

Accuracy as a divider is specified in two ways,

1. as a worst-case, maximum error of ±50mV (0.5% of full scale output)
2. as a small fixed error, plus a fixed percentage of output; ±5 mV ±0.3% of actual output, typical

(2) is more closely descriptive of the actual error of the device. The worst-case ±50mV, or 0.5% of full-scale, the customary overall accuracy specification, is useful near full scale, but it is overly conservative at the lower levels.

TESTING THE MULTIFUNCTION CIRCUIT

In the multiplier and divider modes (m = 1), the multifunction circuit may be tested with the circuits and techniques described in Chapters 3-2 and 3-3, as they are applied to 1-quadrant devices. Figures 14 through 17 illustrate tests that are of particular interest for the multifunction circuit. They test, in this order: divider errors, multiplier errors, dynamic errors, and exponent errors.

The *divide mode* accuracy test, Figure 14 shows a single dc reference driving the denominator directly, and the numerator through

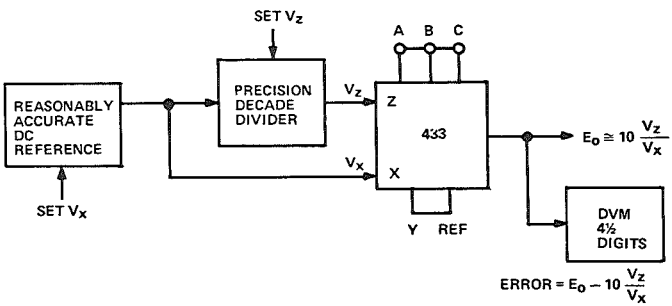


Figure 14. Measuring DC errors of multifunction circuit in divide mode

a precise voltage divider. This approach provides a true-ratio input, independent of the absolute accuracy of the dc reference. It is especially important that this approach be used for high-accuracy dividers, such as the 433, since the seemingly-negligible absolute errors that can exist between two independent dc references can cause large absolute errors at the divider output.

For example, suppose that we want to test the 433 at V_z = 10mV, V_x = 100mV, and that two separate references are used, both having reasonable accuracy — say, 0.01% of full scale. The theoretical output voltage should be

$$E_o = 10\frac{0.010}{0.100} = 0.1 \times 10V = 1V \qquad (16)$$

If the Z reference is high by 0.01% X 10V = 1mV, and the X reference is low by 0.01%, or 1mV, the actual test that is performed is

$$E_o = 10\frac{0.011}{0.099} = 10/9V = 1.11V \qquad (17)$$

This means that a perfect divider will indicate an output error of 11% (of reading) from the value that would be ideally given by two perfect references! The numerator is 10% (of setting) high and the denominator is 1% low, despite the 0.01% specification on the references.

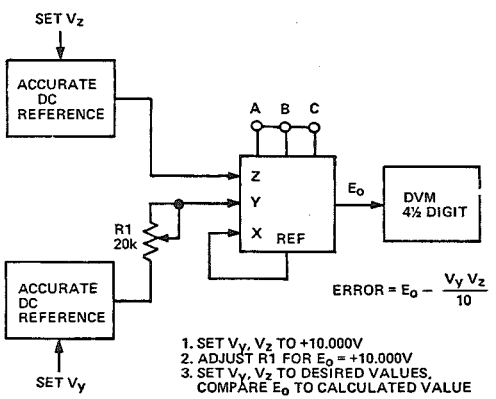


Figure 15. Measuring multiplication errors of multifunction circuit

The error due to imperfect references can be found and accounted for by measuring the X and Z inputs directly with a DVM with 100μV (or better) resolution and good linearity, but it is usually easier and more satisfactory to use a precise voltage-divider or very accurate (100μV-or-less absolute error) reference for the divider inputs.

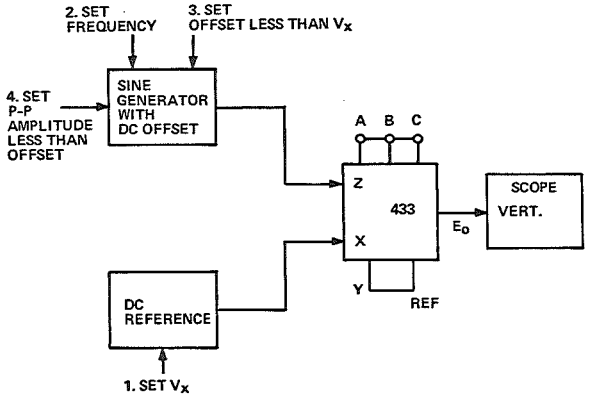


Figure 16. Measuring frequency response to numerator signals, as a function of V_X. Offset voltage keeps the AC signal in the first quadrant.

Accuracy as a Function of Exponent Setting (m). This is the most interesting (and difficult) test to perform, unless you have access to means of mechanizing the measurement, and an adequate table of ideal output values for comparison. The best non-mechanized approach is to measure the output as a function of the input (or input ratio V_Z/V_X), point by point, using the test setup of Figure 17. As noted above, the X and/or Z input voltages (or their ratio) must be known to an accuracy greater than that of the device under test. Assuming that the inputs are known, the actual output can be compared to the theoretical output at various values of the inputs, or their ratio.

Semi-automated testing, using analog waveforms, may be performed if a unit having greater accuracy than that specified for the units under test is available for comparison. A slow triangular wave is fed into the inputs of both devices and the outputs are compared via a difference amplifier. Another means of automating

the point-by-point error measurement is to apply the inputs via a D/A converter, programmed by a computer. The output of the unit at each point is compared with the computed theoretical value, after conversion to digital form.

The apparent dynamic range of the 433 depends greatly on the exponent, m, as discussed earlier and indicated in Table 1. For example, let $V_x = 10V$, $V_z = 1V$

$$\text{If } m = 1,\ E_o = 10\ (1/10) = 1V$$

$$\text{If } m = 2,\ E_o = 10\ (1/10)^2 = 0.1V$$

$$\text{If } m = 5,\ E_o = 10\ (1/10)^5 = 100\mu V!$$

At the other extreme, m = 1/5, the gain of the 433 $\rightarrow \infty$ as the ratio $V_z/V_x \rightarrow 0$. For the above values,

$$\text{If } m = 1/2,\ E_o = 10(1/10)^{1/2} = 3.16V$$

$$\text{If } m = 1/5,\ E_o = 10(1/10)^{1/5} = 6.31V$$

From these examples, it is evident that forethought and care should be employed when measuring (and interpreting) the errors of the 433 in the power and root modes, especially for very low values of V_z/V_x. Careful testing will show that multifunction devices based on logarithmic circuitry can give surprisingly good results, even at such outlandish powers as Z^5 and $Z^{1/5}$.

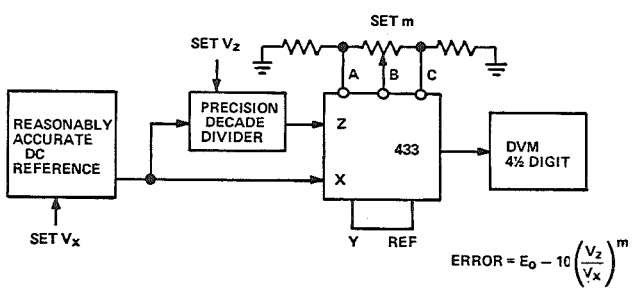
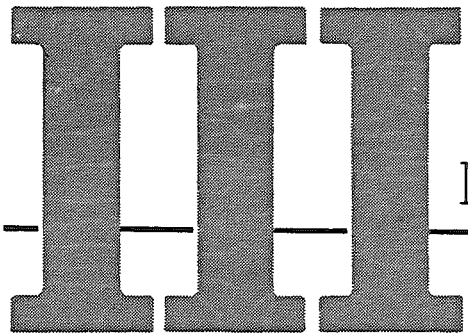


Figure 17. Measuring DC error of multifunction circuit in power or root mode.



Root Mean-Square

Chapter 7

In the introductory chapter and in Chapter 2-3, there were brief discussions of some properties and applications of the root mean-square, and typical circuits for implementing the function. This chapter, after a brief review of the nature of rms measurement, provides an in-depth discussion of the circuitry used by manufacturers of modular rms devices, errors and specifications of rms circuits, and configurations for testing rms devices.

The root mean-square of any voltage over an interval T is

$$\text{rms} = \sqrt{\frac{1}{T}\int_0^T [f(t)]^2\, dt} \qquad (1)$$

The computing process is to square the voltage, $f(t)$, instant by instant, integrate it over the period T, divide by T to obtain the mean, and compute the square root. The integration indicated here is a true time integration, starting with initial conditions at $t = 0$, and ending with a measurement at $t = T$ (or after T, if the final value is retained in the *hold* condition). The desired initial conditions must be reset (e.g., to zero) before another measurement is made.

While this measurement gives a reading of true rms, it is somewhat cumbersome for all but one-shot phenomena. More typically, the waveform being measured is random or periodic and has stationary properties (including, among other things, a constant rms). If the

rms is reasonably constant, the mean (of the squared signal) may be measured by a circuit that responds to the running average. In its simplest form, it is a low-pass filter consisting of a simple RC unit-lag circuit, with the RC time constant chosen to be considerably longer than the longest period present in the signal, but short enough to follow variations in the signal's rms value without introducing excessive delay errors.

Three fundamental properties of rms quantities are important to the instrument designer:

1. The rms is a measure of the heating value of a voltage or current applied to a resistor; over the interval, T, all waveforms having the same rms voltage or current will dissipate exactly the same amount of energy in the resistor, irrespective of their variation with time. This is true whether the waveform is constant, sinusoidal, biased-ac, random, or a train of pulses. The rms is a fundamental physical measurement.

2. The rms value of any stationary zero-mean random process is equal to the standard deviation of that process.* Whether the distribution measured by the electrical waveform involves electrical random noise or the size of apples on a conveyor belt, the rms measurement is a valid measurement of the standard deviation for large sample size. The rms is a fundamental statistical parameter.

3. If orthogonal or uncorrelated quantities are summed, the rms of their sum is equal to the square-root of the sum of the squares of their individual rms values.

The standard deviation is the square-root of the *variance* from the *mean value* of a set of samples. For an infinitely large sampling,

$$\sigma = \sqrt{\int_{-\infty}^{\infty} (X - m)^2 p(X)\,dX},$$

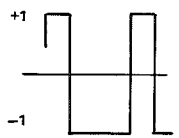
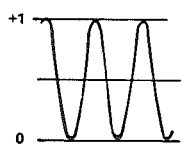
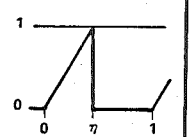
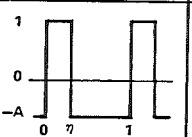
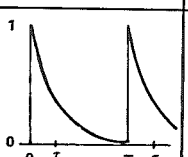
where the mean,

$$m = \int_{-\infty}^{\infty} X p(X)\,dX$$

and p(X) is the probability that X has a given value.

Until recently, accurate rms instrumentation was not feasible for compact, wideband, low-cost applications. A widely-used substitute was the mean absolute value (or statistically, the mean absolute deviation). The mav, or mad, is obtained by simply full-wave-rectifying a signal and averaging the resulting waveform. The table of Figure 14 in Chapter 2-3 lists a number of waveforms, their rms and mad values. Table 1 shows similar data for several other waveforms.

TABLE 1. CHARACTERISTICS OF SOME COMMON WAVEFORMS.
See Chapter 2-3, Figure 14 for Sine, Square, Triangle, Sawtooth, Gaussian Noise, Zero-Based Rectangular Pulse Train.

WAVEFORM		RMS	MAD	$\frac{\text{RMS}}{\text{MAD}}$	CREST FACTOR
	AMPLITUDE–SYMMETRICAL RECTANGULAR	1	1	1	1
	SINE–SQUARED (RAISED COSINE)	$\sqrt{\frac{3}{8}}$ $\doteq 0.6124$	$\frac{1}{2}$	1.225	1.633
	SAWTOOTH PULSE	$\sqrt{\frac{\eta}{3}}$	$\frac{\eta}{2}$	$\sqrt{\frac{4}{3\eta}}$	$\sqrt{\frac{3}{\eta}}$
	OFFSET PULSE $\left(\text{IF AVE} = 0,\ \eta = A(1-\eta)\right)$	$\sqrt{\eta(1-A^2)+A^2}$ $\sqrt{A}$	$\eta(1-A)+A$ $\frac{2A}{1+A}$	$\frac{\text{RMS}}{\text{MAD}}$ $\frac{1+A}{2\sqrt{A}}$	$\frac{1}{\text{RMS}}$ $\frac{1}{\sqrt{A}}$
	EXPONENTIAL PULSE	$\sqrt{\frac{\tau}{2T}\left(1-\epsilon^{-2T/\tau}\right)}$ $\cong \sqrt{\frac{\tau}{2T}}$	$\frac{\tau}{T}\left(1-\epsilon^{-T/\tau}\right)$ $\cong \frac{\tau}{T}$	$\sqrt{\frac{T}{2\tau}}$	$\sqrt{\frac{2T}{\tau}}$

Because measurements on sine waves were widely used, meters were calibrated to read the rms value of a sine wave, while the mad was the actual voltage that was measured. Thus, such meters would read $\pi/2\sqrt{2}$ (= 1.111) times the mean absolute value. For waveforms other than undistorted sine waves, this ratio could be greatly in error: for dc or symmetrical square waves, the error is 11% high; for triangular or sawtooth waves, the error is 4% low; for Gaussian noise, it is 11.3% low. But these waveforms could be calibrated, if their nature was known. Much worse is the inability of such devices to measure waveforms of unknown form or of variable "duty cycle." For example, for a train of zero-based rectangular pulses, the ratio of rms/mad is 2 for a 25% duty cycle, and *10* for a 1% duty cycle. Figure 1 shows the error of measurement of rms over one-half cycle of a sinusoidal waveform as a function of firing angle in a SCR circuit, if 1.111 times the mean is used.

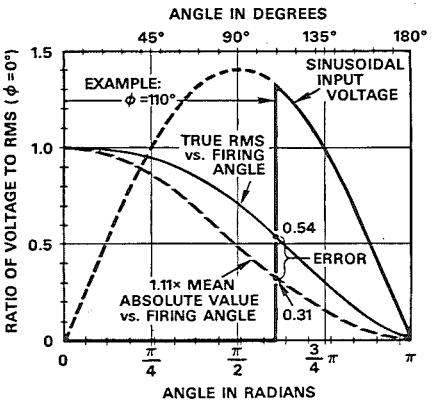


Figure 1. RMS and mean value of ideal full-wave SCR output as a function of firing angle ϕ

Since the mean square (hence the rms) measures, with accuracy and consistency, the power in a signal of known or unknown shape, averaged over a given time interval, it provides valid, universal, and repeatable measurements of the intensity of random phenomena, such as acoustic noise, mechanical vibration, and electrical noise, as well as phenomena characterized by waveforms with more determinate shapes.

Although, surprisingly, even some of today's "better" voltmeters still use rms-calibrated mad, a pronounced and rapid swing toward true-rms instrumentation is now in process. This swing is a result of two trends: the increased use of time-domain measurements, and the greatly decreased cost and increased availability of compact true-rms instruments. One can buy rms-to-dc converter modules with accuracy (errors) in the 0.1% to 0.5% class for about $50. Previously, the cost of classical thermal rms-to-dc converters (of the order of $1000) had restricted their use to the most-expensive digital voltmeters or specialized true-rms analog meters.

This restriction to expensive laboratory meters will vanish during the next few years. The growing market for low-cost portable digital multimeters and ac transfer standards will undoubtedly stimulate the demand for accurate and reliable ac measurements. Users of digital instruments naturally expect good accuracy and resolution, and they will want the ac-measurement capability of an instrument to be as good as its dc capability. Portable meters are generally used to measure complex waveforms in locations where auxiliary instruments (oscilloscopes and laboratory DVM's) are not available; therefore the ac accuracy must be independent of the waveform.

As noted earlier, rms converters are useful in industrial measurement and control: SCR waveforms, noise and vibration analysis, and power dissipation in fixed resistors are but a few applications. However, for variable or reactive loads, average power measurement is performed by instant-by-instant multiplication, followed by averaging, to obtain the average power (Chapter 2-3, Figure 17). (In such applications multiplication of rms values can lead to wrong answers.)

RMS-to-DC CONVERTER CIRCUITS

There are, today, three electrical techniques in common use for performing rms measurements:

1. *Thermal*, based on the conversion of an unknown voltage or current to heat in a known value of resistance.

2. *Direct computing*: the use of analog-computing techniques to straightforwardly compute the rms value of an input waveform by squaring, averaging, and rooting in an open-loop configuration,

3. *Implicit computing*: a variation of (2) in which the square-root operation is performed implicitly (i.e., by feedback).

Of these three techniques, the thermal converter is satisfyingly basic by its nature, but it is difficult to realize. Computing types, especially those employing implicit square-rooting, can provide accuracies and bandwidths equalling the best of the thermal converters, usually at lower cost.

THERMAL RMS-DC CONVERTER CIRCUITS

The simplest thermal RMS-dc converter circuit that is useful for low-frequency (<10MHz) measurements is the fixed-gain, variable-temperature converter, shown in Figure 2. The input, applied to

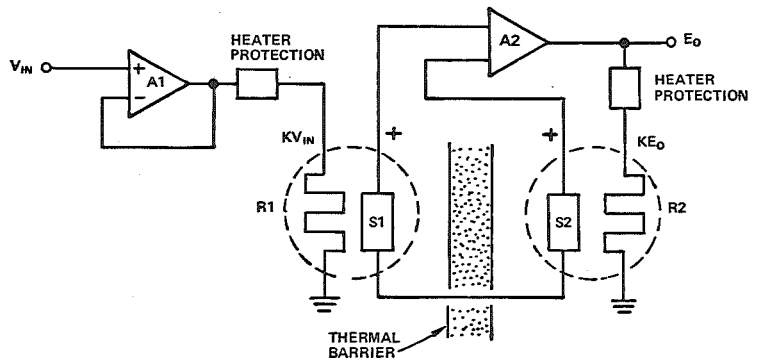


Figure 2. Thermal true rms-to-dc converter (fixed gain)

resistor R1, causes it to heat up. The circuit applies a dc voltage to R2, sufficient to cause it to heat up to the same temperature as R1, and continuously adjusts it to maintain the temperature difference at zero, as measured by the sensors S1 and S2. If both R1 and R2 have identical thermal paths to the environment, the power dissipated in both is identical, and, since $(KV_{IN})^2/R_1 = (KE_o)^2/R_2$, the output

$$E_o = \sqrt{\frac{R_2}{R_1}} \cdot (V_{RMS}) \qquad (2)$$

The input buffer amplifier, A1, should provide a high impedance for the input signal, sufficient output current to drive the low-resistance (10 to 100Ω) heater, R1, and adequate bandwidth (the amplifier is usually the limiting factor on input bandwidth in thermal converters, but thermal lag causes settling of the rms to new values to be slow, especially for decreasing input.

The structure of the heater-sensor assemblies is critical to the accuracy and bandwidth of the thermal rms converter. Until recently, the best converters used vacuum-sealed resistor-sensor assemblies, containing thin-wire-wound resistors and thermocouples. It is essential that the wire maintain constant resistance as a function of temperature, so that the voltage across R2 will vary *linearly* with the rms value of V_{IN}. It is also important that R1-S1 and R2-S2 be thermally isolated from one another. If a significant amount of heat from R1 reaches S2 (or S1 from R2), then the sensitivity of the converter will be diminished, and nonlinearities may be introduced.

If thermocouples are used for S1 and S2, then A2 must be quite stable – perhaps chopper-stabilized – because of the low (e.g., 40μV/°C) sensitivity of thermocouples. Some detectors use several thermocouples in series, but the signal levels are still submillivolt.

Recently, balanced thermal detectors have been developed that use thin-film resistors for the heaters, and transistors for the sensors. Since the base-to-emitter voltage of a transistor has approximately a -2mV/°C temperature coefficient at 25°C, it is nearly two orders of magnitude better as a sensor than a thermocouple. While this reduces the performance requirements for A2, the thermal balance, input amplifier, and settling time problems still remain.

Performance of the "Fixed-Gain" Thermal Converter

Errors can be quite low – typically less than 0.1% of reading for input signals over a narrow range of amplitudes (usually less than 3:1). Since the power dissipated in the heater, R1, is proportional to the square of the input rms, a 3.2:1 change of input amplitude will change the power dissipation by 10:1, which can result in a comparable temperature rise. If the input amplitude is increased too

much, R1 may be burned out. On the other hand, if the signal level is too low, the temperature rise of R1 will be too small for satisfactory operation.

The bandwidth of the thermal converter (in terms of input-signal response) is limited by the bandwidth of the input amplifier A1 at the upper end, and by the thermal time constant of R1-S1 and R2-S2 at low frequencies (i.e., 1Hz to 10Hz). The converter works perfectly at dc, since no averaging is required. The thermal converter can therefore be calibrated against an accurate dc reference, and then used to measure an ac signal (within its bandwidth) of about the same rms level (within ±50%) as the reference.

The limited dynamic range implies a limitation on crest factor (the ratio of peak input to rms). Since the heaters must be operated in the upper portion of their dynamic ranges under steady-state low-crest-factor conditions (such as sinewave inputs, c.f. = $\sqrt{2}$), there is little "headroom" for peaks. For instance, if a heater-detector works best with 10mA to 30mA into the heater, and a crest-factor capability of 3 is required, the input buffer amplifier must be able to supply 30-90mA linearly. At a crest factor of 5, the requirement is 50mA to 100mA. Even if the amplifier can supply the current, the heater might burn out if its instantaneous power rating is exceeded (power is proportional to the *square* of voltage or current).

Variable-gain thermal rms-dc converter: The limited dynamic range and crest factor, and long settling time of the fixed-gain thermal converter can be substantially bettered by operating the heaters, R1 and R2, at constant power (temperature). As shown in Figure 3, the gain of the input buffer-amplifier is manipulated by the null-sensing amplifier A2 to bring the power in R1 into equilibrium with the power in R2, which is driven from a constant voltage V_{REF}. If the input amplifier has a gain that is inversely proportional to the control voltage, E_o, then the control voltage will be proportional to the rms of the input voltage. At null,

$$\overline{\left(K \frac{V_{IN}}{E_o}\right)^2} \frac{1}{R_1} = \frac{{V_{REF}}^2}{R_2} \qquad (3)$$

Therefore,

$$E_o = \sqrt{K \frac{R_2}{R_1} \frac{\overline{V_{IN}^2}}{V_{REF}^2}} = K' \sqrt{\overline{V_{IN}^2}} \qquad (4)$$

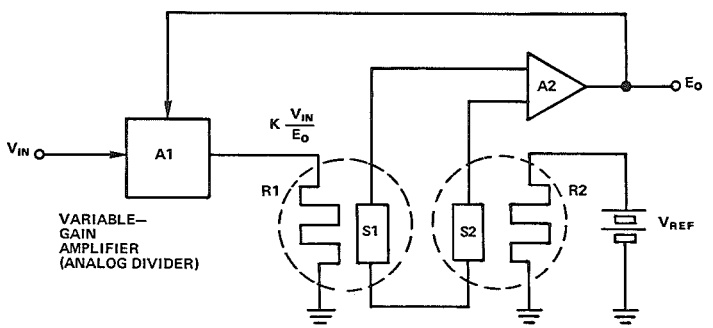


Figure 3. Variable-gain thermal rms-to-dc converter

The variable-gain thermal rms-dc converter has better dynamic range and accuracy than the fixed-gain converter, but it shares some of the same weaknesses. Since it requires fairly large (10mA to 100mA) currents in the heater resistors, good ground-return practices should be followed to avoid causing significant voltage drops in the ground paths.

Since the heater-sensor pairs operate above ambient temperature, a significant warmup time (5 minutes or more) is usually required for a thermal converter to reach usable accuracy. The thermal time constant determines the averaging time, and thus the lowest frequency (excluding dc) for which rms can be measured accurately. The averaging time cannot be increased by the use of low-pass filters (as is the case for computing-type converters). For this reason, thermal converters do not usually work well at frequencies below 10Hz.

DIRECT COMPUTATION

Computing the root mean-square of a waveform requires three mathematical operations: squaring, averaging, and square-rooting. They can be implemented in a straightforward fashion, using multipliers and operational amplifiers, as shown in Figure 4.

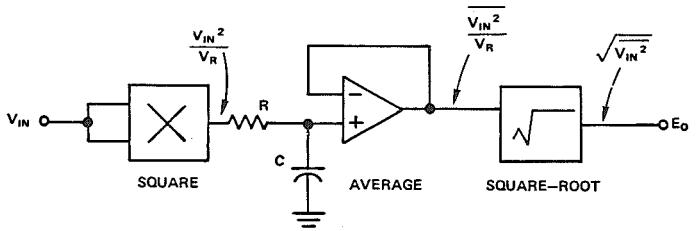


Figure 4. Explicit RMS circuit

This scheme, which embodies explicit computation is unsatisfactory, for several reasons.

1. Cost and complexity: It requires two multipliers, or a square-rooter, plus an op amp.

2. Limited dynamic range: The output of the squarer will vary over a 10,000:1 dynamic range (1mV to 10V) for a 100:1 instantaneous-input range (0.1V to 10V). Since the input multiplier will have errors greater than 1mV, the error will strongly depend on signal level, resulting in an overall dynamic range less than 100:1, probably only 10:1. In this respect, the direct-computing rms circuit shares similar dynamic-range limitations with the fixed-gain thermal converter. Despite these limitations, the direct computation of the rms value can be made quite accurate over a 10:1 range of input. If a 0.1% multiplier is used as the squarer, and a high-accuracy square-rooter (e.g., 434B) is used, an error level of ±0.1% of full scale can be achieved.

IMPLICIT COMPUTATION

Perhaps the best approach to computing the rms value of a signal is to use a circuit that implements an implicit solution to the rms equation:

$$V_{RMS}^2 = \overline{V_{IN}^2} \tag{5}$$

by the use of the identity

$$V_{RMS} = \frac{\overline{V_{IN}^2}}{V_{RMS}} \tag{6}$$

Figure 5 is a block diagram of a circuit that performs the indicated operations of squaring, averaging, then dividing by the output. Since the output is essentially constant over the period of the signal being averaged, it may perform the division *before* the average is taken.

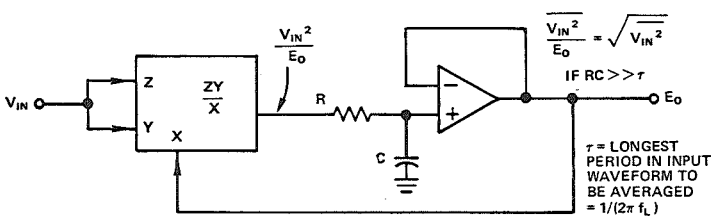


Figure 5. Implicit RMS-computing circuit

This scheme overcomes all the limitations of the direct computing approach, and it has much greater dynamic range than the variable-gain thermal converter. Also, it can be designed to handle very slow waveforms, because the choice of RC is essentially arbitrary, within the constraints that it be much longer than the longest period to be measured, and short enough to provide adequate settling time.

There are two ways in which the scheme can be implemented: direct multiplication-division, and via a specially-designed true-rms module employing log-antilog operations.

Direct multiplication-division with implicit feedback can be implemented using such 3-variable devices as the AD531 IC multiplier-divider (see Figure 15, Chapter 2-3), the 433 multifunction

module, or the 434 multiplier-divider. The AD531, used in the rms-circuit, requires careful trimming, plus at least 1 external amplifier. The circuit is accurate to within only 1% or 2%, because of device limitations. The 433 or 434 can be used to make a very high accuracy (within 0.1%), wide-dynamic-range (1000:1) rms circuit. However, it is a 1-quadrant device and must be driven by a high-precision rectifier if the rms of bipolar signals is required. Neither the 433 nor the AD531, with external circuitry, can compete with specialized rms modules on the basis of price or performance.

Special-purpose log-antilog rms-dc conversion combines logarithmic and implicit computing techniques to achieve overall errors of less than 15mV + 0.2% of expected value over a 1000:1 dynamic range. It consists of a log-antilog squarer-divider, with an absolute-

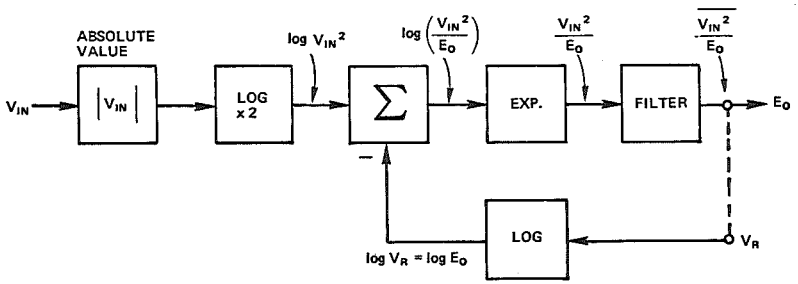


Figure 6. Log-antilog RMS-to-DC converter

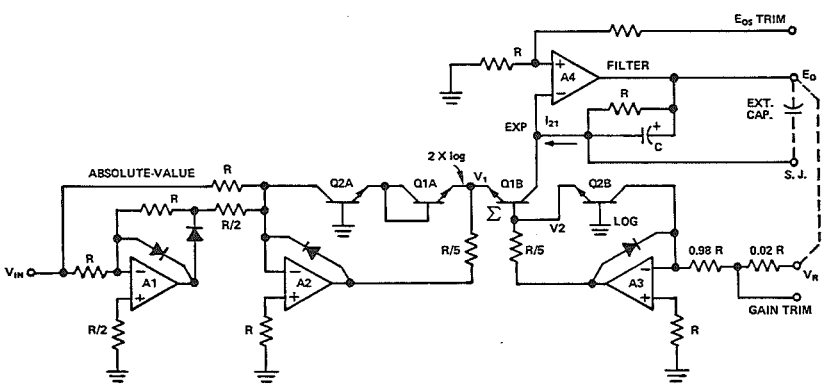


Figure 7. Schematic diagram of log-antilog RMS-to-DC converter

value (full-wave rectifier) front end, and an internally-connected filter. A block diagram of the circuit is shown in Figure 6, and a schematic appears in Figure 7.

The bipolar input signal, V_{IN}, is converted to a current representing the magnitude by an absolute-value circuit (amplifier A1 and the associated components). The unipolar current is transformed into a voltage proportional to twice the logarithm of the input (i.e., $2 \log x = \log\{x^2\}$) by two junctions in series (A2, Q1A, and Q2A). The log of the *output* is obtained by A3 and Q2B and subtracted from the log-of-the-square-of-the-input; the result is antilogged by Q1B and A4, averaged by the filter RC, in the feedback path of R4, and transformed to the output voltage by R.

The derivation shows how the temperature-sensitive terms are cancelled, if the transistors are matched and isothermal.

$$V_1 = -2\frac{kT}{q}\ln\left(\frac{V_{IN}}{RI_{ES}}\right) \tag{7}$$

$$V_2 = -\frac{kT}{q}\ln\left(\frac{E_o}{RI_{ES}}\right) \tag{8}$$

$$I_{21} = I_{ES}\,\epsilon^{q(V_2 - V_1)/kT} \tag{9}$$

$$\begin{aligned} V_2 - V_1 &= \frac{kT}{q}\left(2\ln\frac{V_{IN}}{RI_{ES}} - \ln\frac{E_o}{RI_{ES}}\right) \\ &= \frac{kT}{q}\ln\left(\frac{V_{IN}^{\,2}}{E_o RI_{ES}}\right) \end{aligned} \tag{10}$$

$$I_{21} = I_{ES}\frac{V_{IN}^{\,2}}{E_o RI_{ES}} = \frac{V_{IN}^{\,2}}{RE_o} \tag{11}$$

$$E_o = \overline{I_{21} R}\Big|_{RC} = \left(\frac{\overline{V_{IN}^2}}{E_o}\right) \qquad (12)$$

For signal frequencies that are high compared to $1/2\pi RC$ $\overline{E_o} \cong E_o$; hence

$$E_o = \sqrt{\overline{V_{IN}^2}} \qquad \text{(cf. (5) and (6))} \qquad (13)$$

Thus, the output voltage is equal to the rms of the input voltage assuming that the corner frequency of the low-pass filter is much lower than the lowest-frequency component of the input signal. The circuit responds accurately to dc inputs, which require no averaging. Because it can respond to dc, this rms-dc converter can be calibrated with ease, since a dc reference can be used for comparison. The circuit can also be used for *mean-square* output if the denominator input, which controls the scale factor, is supplied by a constant voltage instead of feedback from the output.

For dc and low-frequency inputs, errors can be trimmed to very low values (~ 0.02%). The primary sources of static errors are the voltage and current offsets of the operational amplifiers. At high crest factors (3 to 5), log-conformity error of the transistors introduces nonlinearity; even so, the error of the circuit will increase by only 5%-of-reading for c.f. = 10.

The dynamic response of the rms circuit depends on the signal level. In the 440, at 20Vp-p input level, the slewing rate of A1 limits the overall -3dB sine-wave bandwidth to 500kHz and the 1%-of-reading error-bandwidth to 50kHz. At 2Vp-p, the 1%-of-reading error bandwidth is typically about 150kHz. However, the bandwidth decreases as the signal level is reduced further, because of the reduction of current through the log transistors Q1A and Q2B. The bandwidth for signals in the range of 1 to 2Vrms can be increased to the order of 5MHz by using fast amplifiers for A1 and A2.

The offset and scale-factor drift with temperature or power-supply variations are negligible sources of error. The symmetrical arrange-

ment of the log and antilog transistors results in complete cancellation of the temperature-dependent terms, kT/q and I_{ES} The result is that the scale-factor drift is determined primarily by the temperature coefficient of the resistors, which can be 10ppm/°C or less. The major source of output drift is the offset voltage- and current-drift of the output amplifier, A4, and the feedback amplifier, A3. The input offset is 1mV or less, and the drift is about 20μV/°C.

RMS-TO-DC CONVERTER SPECIFICATIONS

The most salient feature of a true-rms-to-dc converter is that it ideally has no error due to an indirect approximation to the rms. Static errors are due only to scale factor, linearity, and offset errors: dynamic errors are due to insufficient bandwidth at the high end of the frequency range, insufficient averaging time at the low end, and linearity errors that affect crest factor in midband.

Salient specifications of rms modules are summarized in an example: the set of specifications for the Model 440 general-purpose (low-cost) rms module (Table 2). Employing a circuit similar to that of Figure 7, it has provisions for output-offset adjustment, scale-factor trim, and for the addition of external capacitance to increase the averaging time. The Appendix to this chapter illustrates means of reducing the ripple by the use of an external filter, and of obtaining a better approximation to a true time-average over any time period through the use of gated integration and sampling, and incremental summation.

The specifications can be interpreted as follows:

Maximum Error

A catchall specification for quick reference, this is the maximum deviation of the dc component of the output voltage from the theoretical output value at full-scale output.

Accuracy

Maximum error, no adjustment is the amount by which the output will differ from the theoretical value. It is the sum of a fixed error and a component proportional to the theoretical output.

TABLE 2. SPECIFICATIONS OF A TYPICAL GENERAL-PURPOSE RMS-TO-DC CONVERTER

(typical at 25°C unless noted otherwise)

Parameter	Model →	440J	440K
MAXIMUM ERROR		0.35%	0.15%
ACCURACY			
Maximum Error, No Adjustment		±15mV±0.2%	±5mV±0.1%
Maximum Error, Externally Adjusted		±10mV±0.1%	±2mV±0.05%
Typical Error, Externally Adjusted		5mV±0.05%	1mV±0.05%
TEMPERATURE COEFFICIENTS			
Output Offset, maximum		0.2mV/°C	0.2mV/°C
Scale Factor, maximum		0.02%/°C	0.02%/°C
DYNAMICS			
Frequency for Specified Error, Minimum		10kHz	10kHz
Frequency for 1%-of-Reading Error			
Sine Wave, 20Vp-p, minimum		50kHz	50kHz
Sine Wave, 2Vp-p, minimum		100kHz	100kHz
Sine Wave, 0.2Vp-p		8kHz	8kHz
-3dB Bandwidth			
Sine Wave, 20Vp-p		500kHz	500kHz
Sine Wave, 2Vp-p		500kHz	500kHz
Sine Wave, 0.2Vp-p		100kHz	100kHz
CREST FACTOR @ 1Vrms Output			
For Specified Error		2	2
For 1% Additional Error		3	3
FILTER			
Time Constant (internal)		10ms	10ms
Time Constant Increase vs. External		50ms/μF	50ms/μF
INPUT			
Voltage Range, Specified Operation		±10V	±10V
Voltage Range, Maximum		$\pm V_s$	$\pm V_s$
Resistance		10kΩ	10kΩ
OUTPUT			
Voltage Range, Specified Operation		0 to +10V	0 to +10V
Current, minimum available		10mA	10mA
POWER SUPPLY			
Error Sensitivity		0.2mV/V	0.2mV/V
Range for Specified Performance		±14V-±16V	±14V-±16V
Operating Voltage Range		±6V-±18V	±6V-±18V
Quiescent Current		±10mA	±10mA
TEMPERATURE RANGE		0°-70°C	0°-70°C

Maximum error, externally adjusted is the amount by which the output will differ from the theoretical value when the output offset and scale factor have been trimmed.

Temperature Coefficients

Output offset: the maximum sensitivity of the output to temperature with zero input, or the maximum displacement of the average error vs. output plot over a temperature range, divided by the temperature range.

Scale factor: the maximum sensitivity of the slope of the output-vs.-input (dc) to temperature

Dynamics

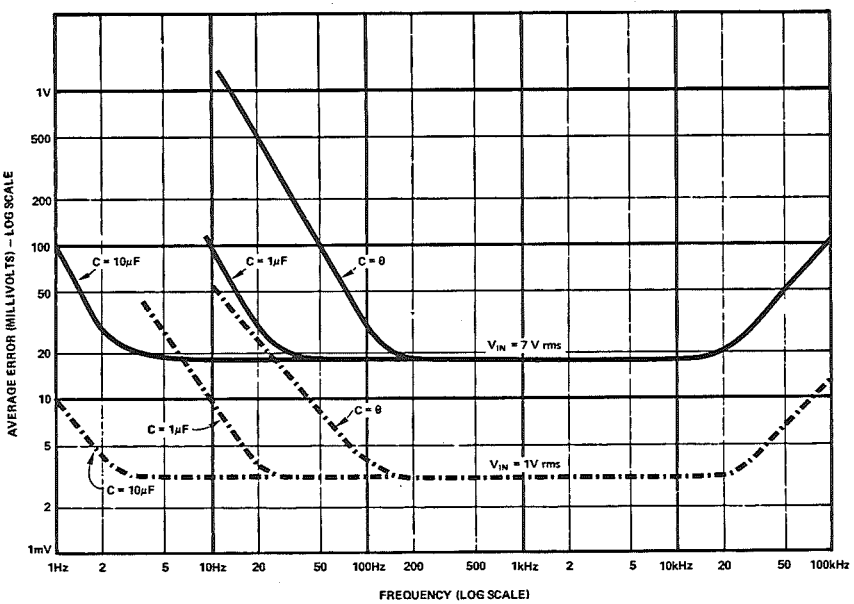
Frequency for specified error is the minimum value of frequency (at the high-frequency end) at which the error is guaranteed to be equal to or less than the specified midband value (sine-wave input). Error at the low-frequency end is governed by the choice of filter, both internal and external. Figure 8 shows a typical error-vs.-frequency plot. Low-end error behavior is shown with no added capacitance, and with 1 and 10μF added (60 and 510ms filter time constants). At very low frequencies, the output of the circuit follows the instantaneous (→ dc) value of the input.

Frequency for 1%-of-reading error is the minimum value of frequency (at the high end) at which the error (except for offset) is guaranteed to be equal to or less than 1% of reading. It is a function of peak-to-peak amplitude.*

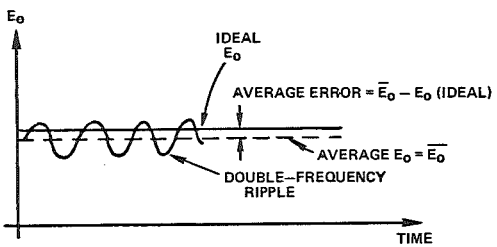
-3dB Bandwidth is the minimum value of frequency (at the high end) at which the error is guaranteed to be equal to or less than 30%.

Crest Factor: (a property of the signal) the ratio of peak signal voltage to the ideal value of rms; the value of crest factor for which the error is maintained within specified limits at a given level of

*For non-sinusoidal waveforms, the attenuation of harmonics increases dynamic errors at lower fundamental frequencies than are specified here. Since square waves and pulses are familiar waveforms and, at the same time, rich in harmonics, Figure 9 shows the error (for such inputs) caused by frequency-response rolloff in the input stages, as a function of pulse width (seconds) and the specified -3dB bandwidth (Hz).



a. Average error of the 440J RMS-to-DC converter as a function of input amplitude, frequency (sine waves), and externally-connected capacitance



b. Average and ripple components of error of rms-to-dc converter at low frequencies (sinusoidal input). The finite averaging time of the filter produces both a double-frequency ripple component and an offset of the average output value (see Appendix A to this chapter).

Figure 8. Output error of rms-to-dc converter as a function of frequency. The error values plotted are the average errors measured after filtering out the ripple.

rms for a midband-frequency signal. Crest factor, rms, and average are plotted in Figure 10 as a function of duty cycle, for rectangular pulses.

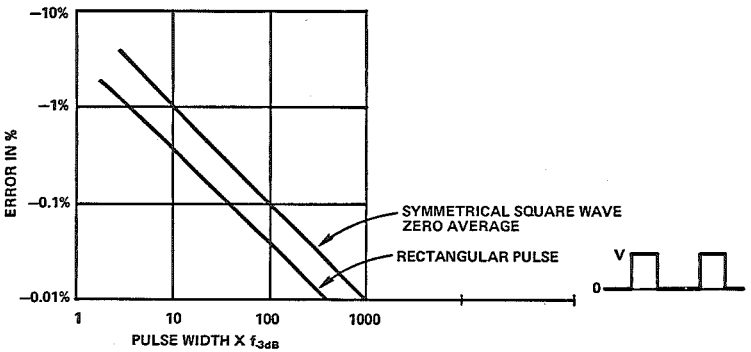


Figure 9. Error of rms-to-dc converter due to finite bandwidth, for pulse and square-wave inputs.[1]

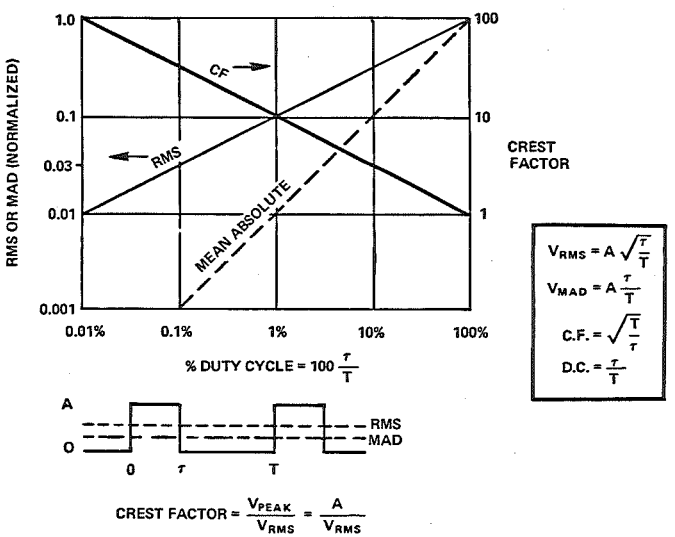


Figure 10. RMS, average and crest factor for rectangular pulse train

[1] Source: "RMS Voltage Measurements — Which Method Works Best?" by Roy Chapel, *Electronic Products Magazine*, January 15, 1973, p. 36.

Filter time constant and Ext. Cap. The time constant of the internal averaging filter, and the increase of time constant per μF of added external capacitance.

Input: the voltage range over which specified operation is obtained, the absolute-maximum voltage, and the effective input resistance.

Output: the maximum output range for rated performance, the minimum current guaranteed available at full-scale output voltage, and the source resistance of the output.

Power Supply: Output-error sensitivity to supply voltage, power-supply range for specified performance, power-supply range for operation, and quiescent current drain.

Temperature Range: the range of temperature variation for operation within specifications. Temperature coefficients are determined by 3-point measurements ($T_H - 25°C$), ($25°C - T_L$), when measured.

TESTING THE RMS-TO-DC CONVERTER

USEFUL EQUIPMENT

The following equipment is useful for testing and calibrating rms-to-dc converters. Starred items (*) are essential.

1. * Accurate dc reference: ±1mV (or less) absolute error, adjustable from 0V to ±10V in ±10mV steps

2. * Accurate ac reference: 0.05% (or less) absolute error, rms output 1 to 2V from 100Hz to 10kHz

3. High-prevision voltage divider with buffered output, adjustable from 1:1 to 100:1

4. * Digital voltmeter, dc-reading, 4½ or 5½ digits, 0.01% error

5. * Digital voltmeter, ac-reading, 4½-digit resolution; can respond to either mean-absolute value or true rms; used for monitoring signal-generator amplitude and making comparative accuracy tests for (clean) sinewaves

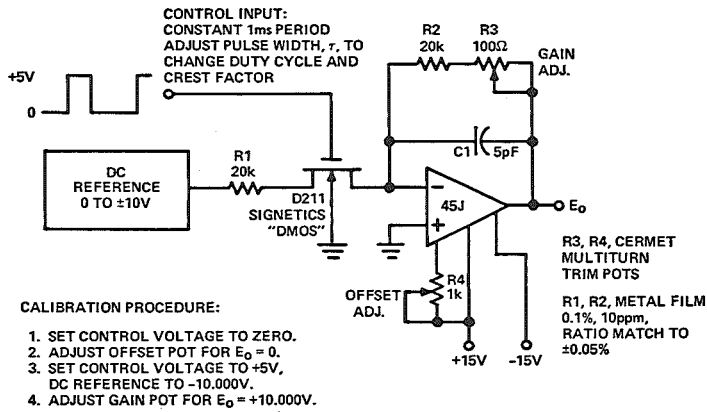


Figure 11. Pulse generator with accurate, adjustable amplitude

6. Accurate pulse generator (see Figure 11)

7. True-rms digital voltmeter, capable of responding to ac and ac + dc signals, 4½ digit

8. Oscilloscope, 5MHz bandwidth

9. * Sine-wave generator with low distortion (< 0.1%), 10mVrms to 7Vrms, 10Hz to 5MHz

TEST PHILOSOPHY AND PROCEDURES

The primary objective in testing an rms converter is to determine how accurately it can convert an ac signal (sine-wave or complex, *including* a dc component) to a dc voltage that is equal to the rms value of the input waveform.

The basic test method is to apply a signal of known rms value to the input, as illustrated in Figures 12 through 17, and measure the resulting dc output with an accurate meter.

This sounds easy, but it isn't all that easy in practice. First, the error of the rms converter depends on the properties of the input

waveform: amplitude, frequency, wave shape (crest factor); second, it is difficult to obtain an ac signal, for example a sine wave, of accurately-known rms value.

For these two reasons, it is usually easier to calibrate the rms converter with an accurate dc reference (assuming that the converter responds to dc), as illustrated in Figure 12. (It will also be found useful to calibrate the input signal waveforms with an accurate rms-to-dc converter.)

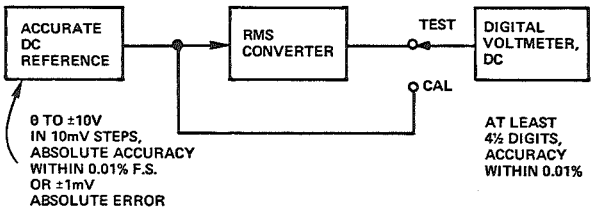


Figure 12. Measurement of absolute accuracy at DC

TABLE 3. TEST CONDITIONS FOR CHECKING DC ACCURACY OF RMS-TO-DC CONVERTER

	V_{IN}	E_o (IDEAL)	Description of Test
1.	0V	0V	Total zero offset, referred to output
2.	+10mV	+10mV	Input offset: + offset will cause output to read > 10mV; – offset vice versa
3.	-10mV	+10mV	Input offset: + offset will cause output to read < 10mV; – offset vice versa
4.	+100mV	+100mV	Low-end accuracy
5.	-100mV	+100mV	Low-end accuracy
6.	+1.00V	+1.00V	Mid-scale accuracy, check for agreement with specification
7.	-1.00V	+1.00V	Mid-scale accuracy, check for agreement with specification
8.	+10.00V*	+10.00V	Full-scale accuracy and symmetry (compare + and – readings)
9.	-10.00V*	+10.00V	Full-scale accuracy and symmetry (compare readings)

*Or ± specified full-scale input for the device under test

The input voltages listed in Table 3 include the most critical points on the dc response function. Other intermediate voltages may be used, as desired, to obtain more-detailed information for a plot of the rms converter's error.

The dc measurements provide information for adjusting the scale factor, the output offset, and (externally, if not available internally) the input offset, which affects symmetry.

AC Measurements

After the converter has been tested for dc errors, and any necessary adjustments have been performed, the ac error may be checked, using a sine wave as the input source. If an ac standard, with 0 offset, is available, the configuration of Figure 13 may be employed. If an ac standard is not available, but a good ac DVM is instead, Figure 14 may be used. The response to ac signals should be tested at a number of different input levels and frequencies to check for nonlinearity, bandwidth limits, and limitations at the low end due to the averaging time of the device (including the intended value of externally-connected capacitance).

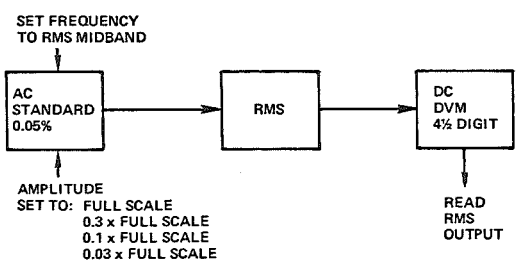


Figure 13. Measurement of absolute accuracy relative to an AC standard

Figure 15 shows a configuration for testing the linearity of the converter over a range of input amplitudes. The amplitude and frequency of the source are set once. Then a low-distortion precision attenuator is used for amplitude adjustment (a) to ensure that the shape does not change, and (b) to obtain precisely-calibrated ratios of input to full-scale.

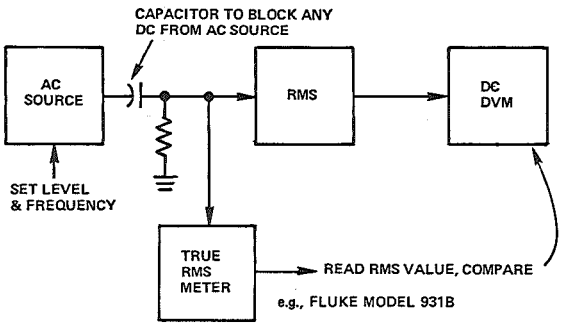


Figure 14. Measurement of absolute accuracy of RMS-to-DC converter relative to accuracy of true RMS meter

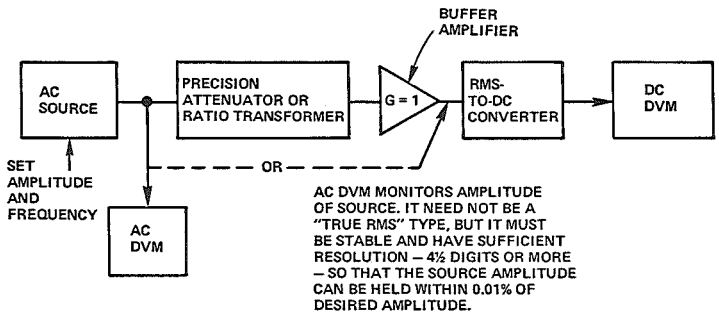


Figure 15. Measurement of nonlinearity for AC input

Figure 16 shows a configuration for measuring error as a function of crest factor, employing a precision pulse source, such as that illustrated in Figure 11. It is easiest to check the crest-factor handling capability with a rectangular pulse of known amplitude and duty cycle. The relationship between crest factor and duty cycle is shown graphically, and in equation form, in Figure 10. Crest factor can be set in terms of the output rms or the input amplitude (which should be less than rated peak input).

The minimum pulse repetition rate, and therefore the frequency at which the crest factor –for rectangular pulses– (for a given accuracy) decreases in terms of the midband value, will be determined by the averaging time-constant. As a rule, the error of the rms-to-dc converter will increase in direct proportion to the crest factor, if the pulse width and repetition rate are within the high and low bandwidth limits of the converter.

Figure 17 shows how the frequency response of the rms-to-dc converter may be measured.

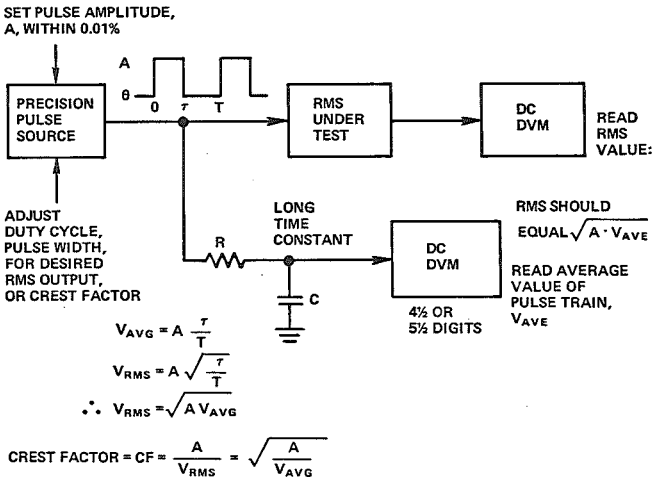


Figure 16. Measuring accuracy of the rms-to-dc converter as a function of crest factor and pulse width (duty cycle)

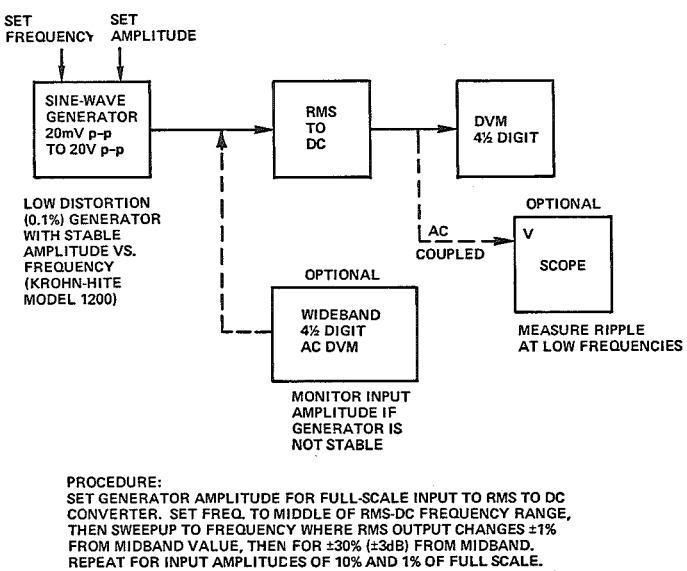
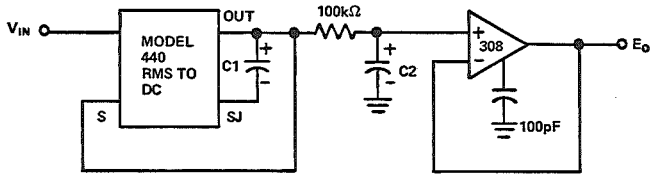


Figure 17. Measuring frequency response of rms-to-dc converter function of crest factor and pulse width (duty cycle)

APPENDIX TO CHAPTER 3-7

A. Use of a Low-Pass Filter to Reduce Ripple at Low Frequencies

With externally-connected capacitance, the 440 can be used to compute accurately the rms of signals having components at quite low frequencies. While the ripple content is not important if the output is read on an analog meter (which provides mechanical averaging) or "eyeballed" on an oscilloscope, it can lead to errors if the output is converted to digital form, and to annoyance if a digital panel meter is used for observations. A low-pass filter may be used following the rms circuit, to add an additional stage of averaging and attenuate ripple components.* The illustration shows a low-cost circuit configuration for accomplishing this.



C1 & C2 = LOW LEAKAGE TANTALUM, 20VDC OR GREATER

LOWEST USEFUL FREQUENCY, F_L	APPLICATION	C1	C2	ERROR OF AVERAGE VALUE OF E_o
50Hz	Power Line	1μF	4.7μF	0.5% $\overline{E_o}$
20Hz	Audio	2μF	4.7μF	0.5% $\overline{E_o}$
3Hz	Low Frequency Vibration, Noise	10μF	20μF	0.5% $\overline{E_o}$

A) Adding a low-pass filter to reduce ripple at low frequencies

B. Use of Controlled Integration and Digital Averaging to Shorten the Averaging Time

For many applications, the running average provided by an RC low-pass filter (or thermal time constants) does not conveniently provide a close-enough approach to the mathematical average over

*Since this averaging is outside the loop, it is only useful for removing ripple components. It is not a substitute for an increased *inside-the-loop* time constant to reduce low-frequency errors. If the inside-the-loop time constant is insufficient, the *average level* of the output will be seen to be in error when the ripple has been satisfactorily filtered out. As a rough guide, if the p-p ripple is less than 10% of the output level, the average error component will be negligible, and external filtering may be used to reduce the ripple to the desired level. If the ripple is greater, it is likely to be accompanied by significant average error; an increased value of C1 may be necessary, in addition to the external filter.

a fixed time period, especially if that period is *very* long, because of the long settling time (many cycles) and the difficulty of obtaining stable capacitances and resistances of adequate magnitude.

The running average is also inadequate if the mean square changes at a rate comparable to the averaging time constant required to smooth out the ripples in the signal (for example, in the case of an amplitude-modulated waveform).

For such cases, controlled integration, sample-hold, and even the use of digital averaging can greatly improve the accuracy of the rms- or mean-square-to-dc conversion and provide an effective averaging time that is arbitrary, ranging from seconds to hours, or even days.

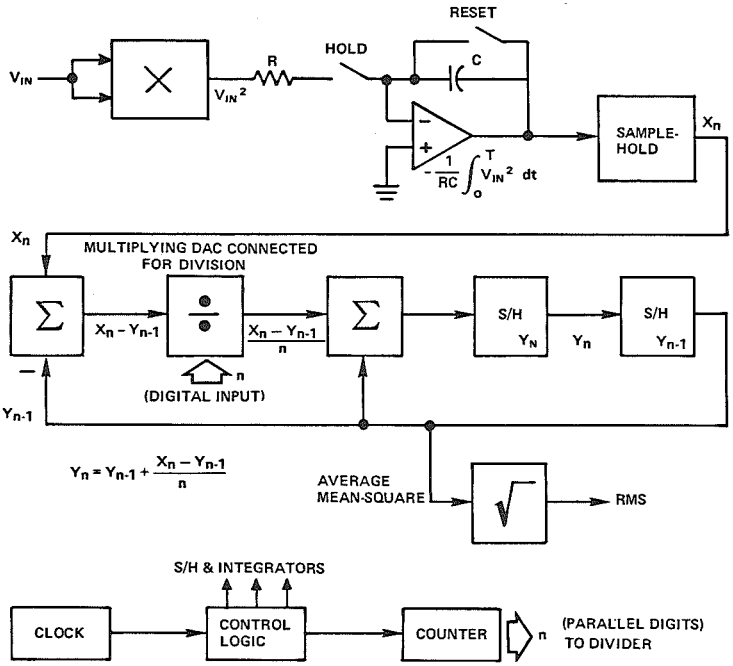
A direct computation scheme, employing all of the above, is shown in illustration (B). The input signal is squared and integrated repeatedly over an interval T, with a characteristic time (RC) equal to T. Thus, the output of the integrator after interval n is the mean square of the nth interval.

At the end of each interval, the integrator output is acquired and held by a sample-hold. Its value (X_n) is compared with the average of the mean-squares up to that time, Y_{n-1}. The difference, divided by n, is added to Y_{n-1} to produce the new average, Y_n, which is stored in a sample-hold for use in computing the next value of Y, Y_{n+1}. The formula for the average over n intervals is

$$Y_n = Y_{n-1} + \frac{X_n - Y_{n-1}}{n} \qquad (14)$$

The average of the mean-squares is then square-rooted to compute the true rms over the entire period. For example, if each integration period is 15 minutes, 1000 counts will provide the rms over a 10-day period.

The division by n can be performed by a multiplying DAC, such as the AD7520, connected as a divider, with the digital input, n, supplied by a clock-driven counter, at the appropriate rate. (The count should start with a preset count of 1, to avoid the possibility of dividing by zero. The divider is scaled for unity gain at n = 1, decreasing for higher values.)



B) Long-term rms computation

The integrator and sample-holds are sequenced by control logic signals derived from the basic clock pulses. During the computing interval, the Y_{n-1} sample-hold is in *hold* and both the X_n and Y_n sample-holds are in *sample*, tracking the integral and continuously computing the next value of Y (count = n) right up to the end of the interval. At the end of the interval, the following events ensue: X_n switches to *hold;* the integrator is quickly reset and immediately starts integrating over the next interval; Y_n switches to *hold*; Y_{n-1} samples the final value of Y_n and returns to *hold*; then, X_n and Y_n revert to *sample*, the counter is incremented to n + 1, and the next value of Y is continuously computed right up to the end of the next interval.

The Y_{n-1} sample-hold, which is quite critical, since its errors, including drift, are cumulative, is perhaps a "sample-infinite-hold" circuit (an A/D converter with output taken from its internal DAC).