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## **SECTION IV**

### **ADCs FOR DSP APPLICATIONS**

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## **ADCs FOR DSP APPLICATIONS**

- **SUCCESSIVE APPROXIMATION ADCs**
- **FLASH ADCs**
- **SUBRANGING ADCs**
- **INTEGRATING (DUAL SLOPE) ADCs**

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## SECTION IV

### ADCs FOR DSP APPLICATIONS

The trend in ADCs for DSP applications is to integrate the sample-and-hold function with the ADC, thus producing what is commonly referred to as a *sampling* converter. This greatly simplifies system designs by eliminating the need for interfacing the SHA to the ADC, a process which involves tricky timing issues as well as a certain amount of

optimization for best performance. A sampling ADC can be completely specified not only in terms of traditional dc parameters, but also in terms of ac performance parameters such as SNR, effective bits, THD, etc. In the following section, we examine several popular architectures used to implement the ADC function.

#### ADCs for DSP APPLICATIONS

- Most are *Sampling* ADCs Containing on-chip SHA, or
- Sigma-Delta Converters
- No Need for Customer to Interface SHA to ADC Encoder
- Complete DC and AC Specifications Provided

Figure 4.1

#### SUCCESSIVE APPROXIMATION ADCs

The successive approximation architecture shown in Figure 4.2 has been extremely popular in the industry primarily because it combines relatively high resolution and speed with low cost. The building blocks for the encoder portion of the successive approximation ADC consist of a comparator, DAC, and control logic (successive approximation register, or SAR). The overall static accuracy is primarily determined by the DAC which can be laser trimmed at the wafer level.

The analog input drives one input of the comparator, while the DAC output is connected to the other input. The conversion technique consists of comparing the unknown input against a precise voltage or current generated by the DAC. The input of the DAC is the digital number at the ADC's output. The conversion process is strikingly similar to a weighing process using a chemist's balance, with a set of  $N$  binary weights (e.g., 1/2 lb, 1/4 lb, 1/8 lb, 1/16 lb, etc.) for unknowns up to 1 lb.

After the conversion command is applied, and the converter has been cleared, the DAC's MSB output (1/2 fullscale) is compared with the input. If the input is greater than the MSB, it remains ON (i.e., "1" in the output register), and the next bit (1/4 FS) is tried. If the input is less than the MSB, it is turned OFF (i.e., "0" in the output register), and the next bit is tried. If the second bit doesn't add enough weight to exceed the input, it is left ON ("1") and the third bit is tried. The process continues in order of descending bit weight until the last bit has been tried. When this process is completed, the conversion complete line changes state to indicate that the contents of the output register now constitute a valid conversion. The contents of the output register form a binary word corresponding to the input signal's magnitude. In most successive approximation ADCs, the output data is also available in serial format.

## SUCCESSIVE APPROXIMATION A/D CONVERTER ENCODER

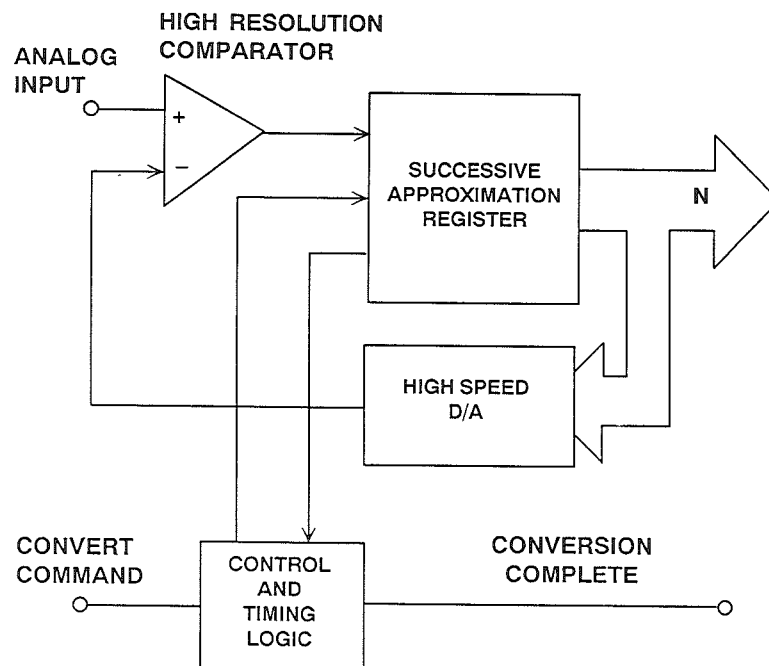


Figure 4.2

## SAR ADC WITH SHA

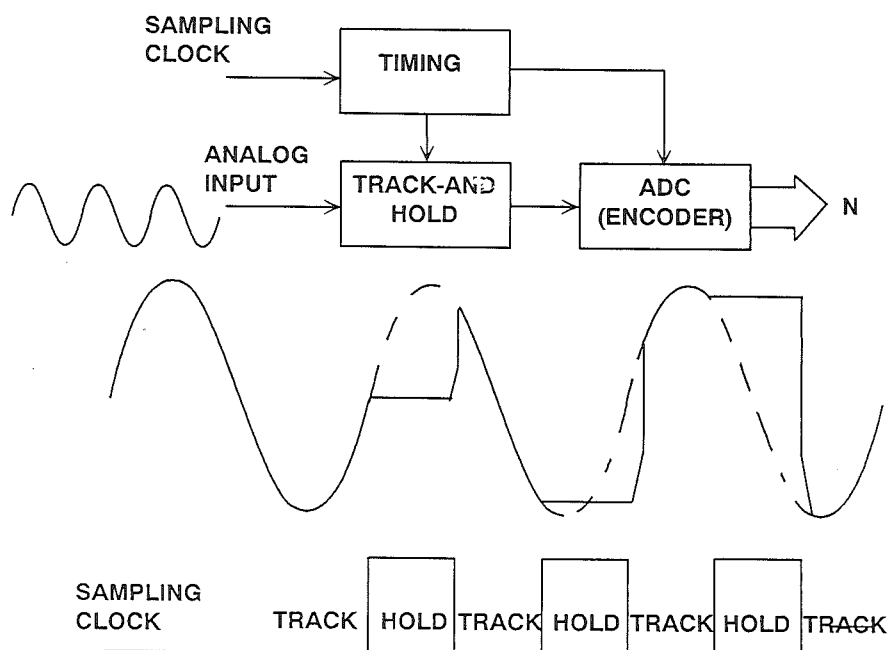


Figure 4.3

Each of the bit decisions requires a clock period. An N-Bit converter will have N clock periods (plus an initialization period). Thus, the minimum conversion time of the ADC will be determined by the maximum allowable clock frequency and the number of bits. This frequency is limited by several factors: SAR clock-to-data-output delay, DAC settling time, and SAR input data setup time.

During the conversion time, it is important that the analog input signal be held constant to avoid errors. This usually requires that a SAR ADC encoder be preceded by an appropriate SHA if dynamic signals

are to be digitized. Sampling ADCs integrate the entire function shown in Figure 4.3 on a single chip. An example of this integration is the AD1674, a 12 bit 100kSPS ADC with on-chip SHA. This device is packaged with industry-standard AD574 pinouts and has complete dc and ac specifications. The AD7870/AD7875/AD7876 is a family of 12 bit 100kSPS low-power CMOS ADCs which also has the on-chip SHA. These devices offer complete ac and dc specifications as well as flexible input voltage ranges and easy parallel or serial interfacing to popular DSP processors.

## FLASH ADCs

Recent advances in VLSI process technology and design techniques have made flash ADCs with up to 10-bits of resolution practical. As well as offering high sampling rates for digitizing video signals (usually without requiring a SHA), flash converters are often used as building blocks for higher resolution ADCs. A block diagram of a typical flash converter is shown in Figure 4.4. The analog

input signal to be digitized is applied simultaneously to  $2^N - 1$  latched comparators, where N is the number of bits. The reference voltage input for each comparator is derived from a resistive voltage divider string. The reference voltage for each comparator is one LSB (least significant bit) higher than the comparator immediately below it.

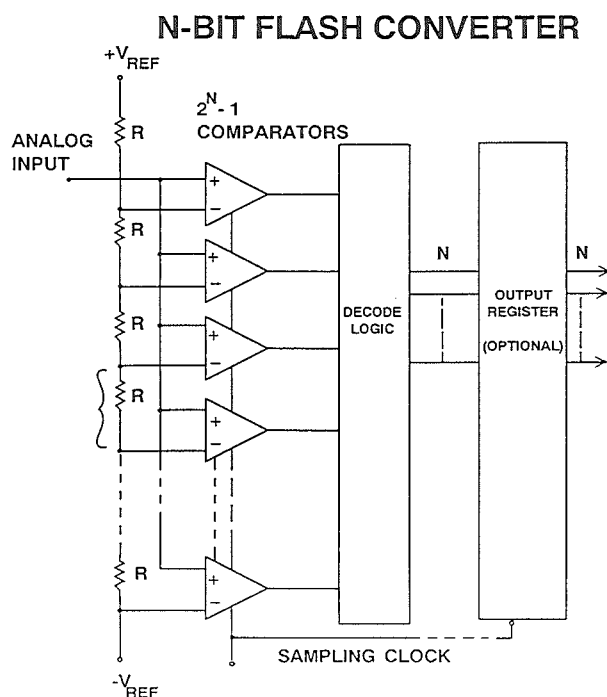


Figure 4.4

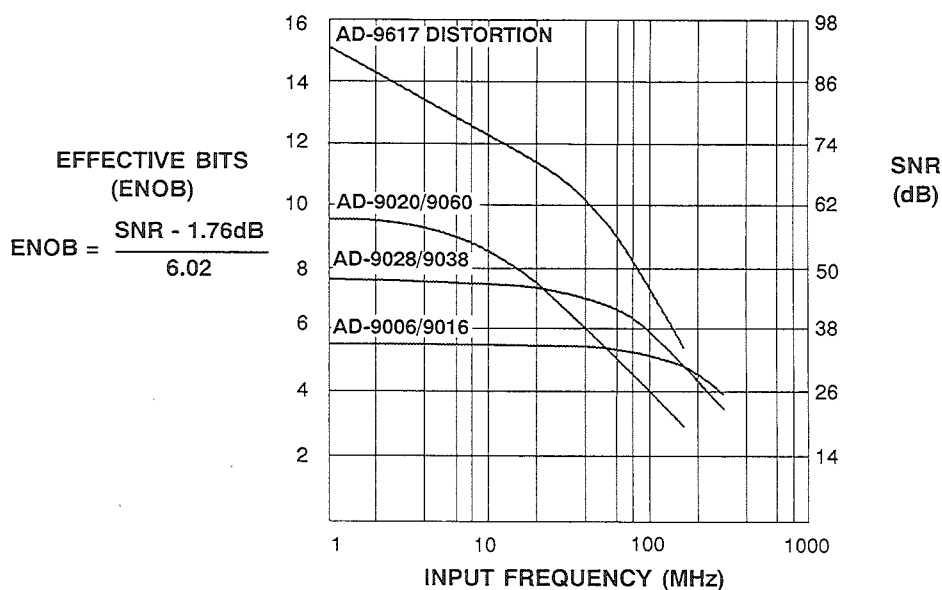
When an analog signal is present at the input of the comparator bank, all comparators which have a reference voltage below the level of the input signal will assume a logic "1" output. The comparators which have their reference voltage above the input signal will assume a logic "0" output. The result is often referred to as a *thermometer* code, and is applied to a stage of decoding logic. This decoding can be accomplished in a variety of ways (such as a simple priority encoder) and ultimately results in the formation of the digital output word. As shown in the diagram, the binary output of the decoding logic often drives an on-chip output latch.

Flash converters are inherently sampling ADCs and usually require no SHA, but they do require careful selection of the drive

amplifier because of their low input resistance, high bandwidth and rather large (and non-linear) input capacitance. Typical effective bit performance of several flash converters is shown in Figure 4.5 along with the harmonic distortion performance of an appropriate drive amplifier.

The AD9060 10 bit, 75MSPS flash converter meets the exacting requirements of HDTV systems as well as other instrumentation applications. The AD9038 8 bit, 300MSPS converter provides a demultiplexed output to simplify the interface with high speed memories. The AD9058 dual 8 bit 50MSPS ADC offers an effective solution where matching is important (In-phase and quadrature radar receivers, and ultrasound imaging) or PC board space is at premium.

## FLASH ADC AND OP AMP DYNAMIC PERFORMANCE



FLASH ADC	RESOLUTION	SAMPLING RATE
AD9020	10 BITS	40 MSPS
AD9060	10 BITS	60 MSPS
AD9028/9038	8 BITS	250 MSPS
AD9006/9016	6 BITS	400 MSPS

Figure 4.5



## SUBRANGING ADCs

A block diagram of an 8-bit subranging ADC based upon two 4-bit flash converters is shown in Figure 4.6. Although 8-bit flash converters are readily available at high sampling rates, this example will be used to illustrate the theory. The conversion process is done in two steps. The first four significant bits (MSBs) are digitized by the first flash (to better than 8-bits accuracy), and the 4-bit binary output is applied to a 4-bit DAC (better than 8-bit accurate). The DAC output is subtracted from the held analog input, and the resulting residue signal is amplified and applied to the second 4-bit flash converter by the summing amplifier. The outputs of the two 4-bit flash converters are then combined into a single 8-bit binary output word. If the residue signal doesn't exactly fill the range of the second flash converter, non-linearities and missing codes will result.

Modern subranging ADCs use a technique called *digital correction* to eliminate problems associated with the architecture of Figure 4.6. A block diagram of a 12-bit digitally corrected subranging (DCS) ADC is shown in Figure 4.7. Note that a 5-bit and an 8-bit flash converter have been used to achieve an overall 12-bit output. If there were no errors, the 5-bit "residue" signal applied to the 8-bit flash converter by the summing amplifier would never exceed one-half of the range of the 8-bit flash. The extra range in the second flash converter is used in conjunction with the error correction logic (usually just an adder) to correct the output data for most of the errors inherent in the traditional uncorrected subranging converter architecture previously discussed.

### 8-BIT SUBRANGING A/D CONVERTER

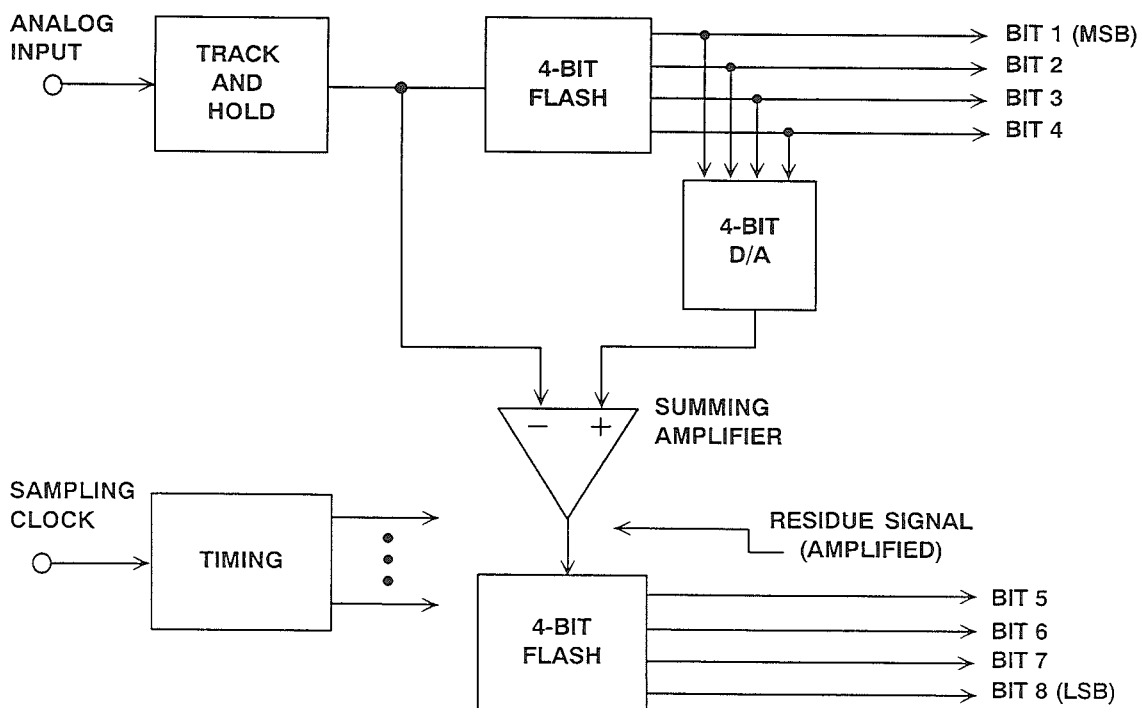


Figure 4.6

## 12-BIT SUBRANGING A/D CONVERTER - DCS

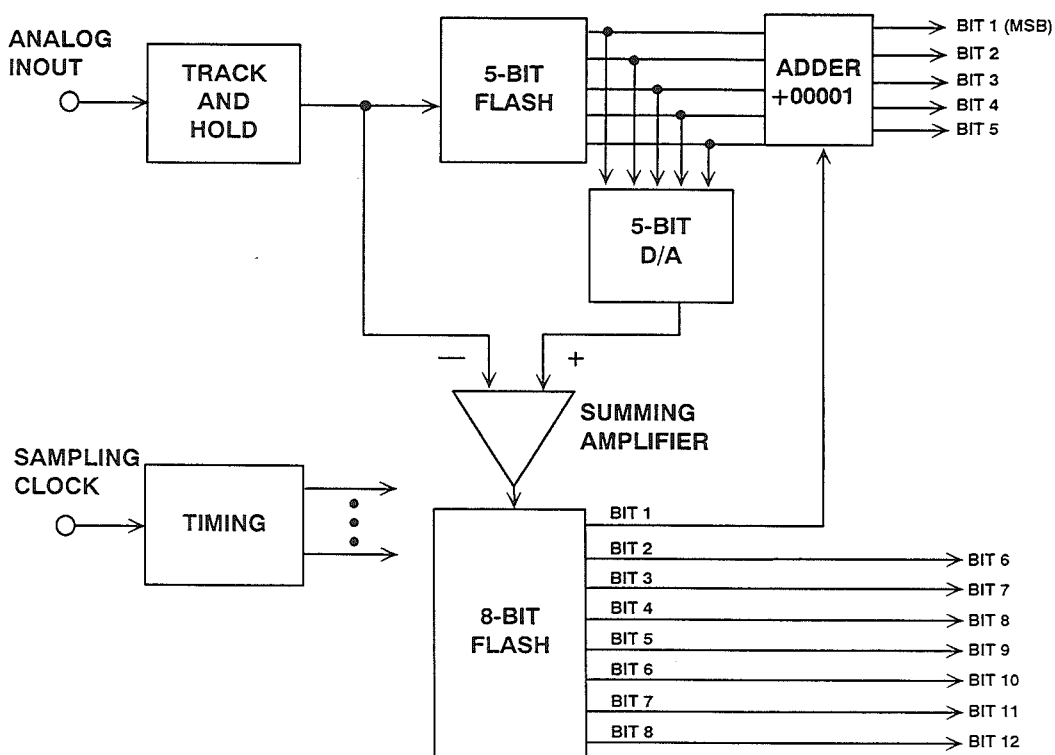


Figure 4.7

## AD1671 12-BIT, 1 MSPS DIGITALLY CORRECTED SUBRANGING ADC

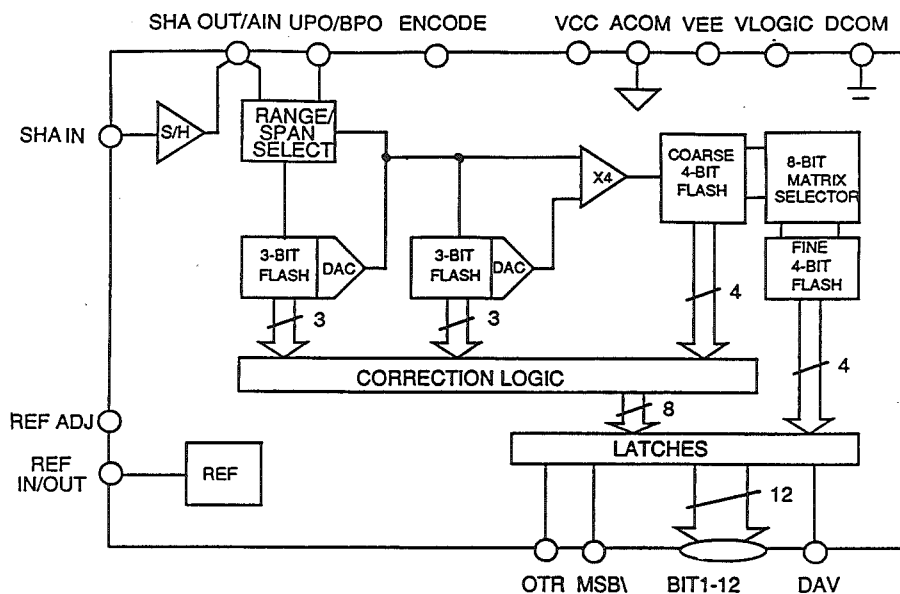


Figure 4.8

The AD1671 ADC uses a four-step DCS architecture as shown in Figure 4.8. Upon receipt of an ENCODE command, the SHA goes into the hold mode. After sufficient time for settling has elapsed, the first 3-bit flash converts the analog input voltage. The 3-bit residue is passed to a correction logic register and a segmented current output DAC. The DAC output is connected through a resistor (within the Range/Span Select Block) to AIN. A residue voltage is created by subtracting the DAC output from AIN, which is less than one-eighth of the fullscale analog input. The second flash has an input range that is configured with one bit of overlap with the previous DAC. The overlap allows for errors during the flash conversion. The first residue voltage is connected to the second 3-bit flash and to the noninverting input of a high speed, differential, gain-of-four amplifier. The second flash result is passed to the correction logic register and to the second segmented current output DAC. The output of the second DAC is connected to the inverting input of the differential amplifier. The differential amplifier output is connected to a two-step backend 8-bit flash. This 8-bit flash consists of coarse and fine flash converters. The result of the coarse 4-bit flash converter,

also configured to overlap one bit of DAC 2, is connected to the correction logic register and selects one of 16 resistors from which the fine 4-bit flash will establish its span voltage. The fine 4-bit flash is connected directly to the output latches.

The AD679 14-bit 100kSPS ADC shown in Figure 4.9 uses a *recursive subranging* architecture which makes multiple passes through a single 4-bit flash converter. The 4-bit flash first produces a 4-bit representation of the analog input. This value is reconstructed through the DAC, and the difference between this and the actual input is then amplified (to take full advantage of the dynamic range of the 4-bit flash), and the whole cycle then repeats itself. After 5 cycles, the result is presented at the digital output. A 1-bit overlap between cycles serves as error-correction.

The AD7886 is a 12 bit, 650kSPS low-power CMOS subranging ADC with on-chip SHA which is completely specified for both dc and ac performance. The AD9014 is a 12 bit, 10MSPS converter optimized for use in broadband receiver applications where spurious-free dynamic range is a key specification.

AD679 14-BIT, 100 kSPS  
RECURSIVE SUBRANGING ADC

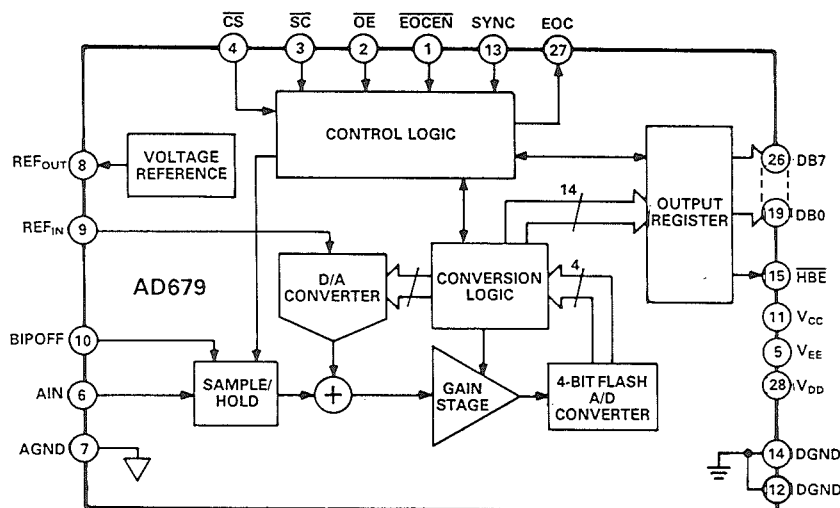


Figure 4.9

## INTEGRATING (DUAL SLOPE) ADCs

Integrating ADCs are used for slow, precise measurements such as in digital voltmeters and many applications involving slow transducers, especially when they drive a display. An example of this type of converter is the high performance AD1175 22-bit 10, 20HZ ADC. The basic integrating ADC block diagram is shown in Figure 4.10 and consists of an integrator, a comparator, an up/down counter, a clock, and control logic.

Before the conversion starts, the integrator is held in the discharged state, i.e. R is connected to ground via S1 and C is shorted by S2. At the start of the conversion, R is connected to the unknown input voltage via S1, and S2 opens, allowing C to charge. The fixed integration time is controlled by the clock and the counter. At the end of the

integration period, S1 connects a known reference voltage to R, and the capacitor is discharged. The amount of time required for the capacitor to discharge is measured by the counter. Since the integrating capacitor, the resistor, and the clock frequency are unchanged during the charge and discharge cycles, the ratio of the charge and discharge times is equal to the ratio of the reference voltage to the unknown input voltage. The conversion accuracy is unaffected by the absolute values of R, C, or the clock frequency, and any noise on the input signal is integrated for the whole sampling period. A diagram showing the charging and discharging action of the integrating ADC is shown in Figure 4.11.

### INTEGRATING (DUAL SLOPE) ADC

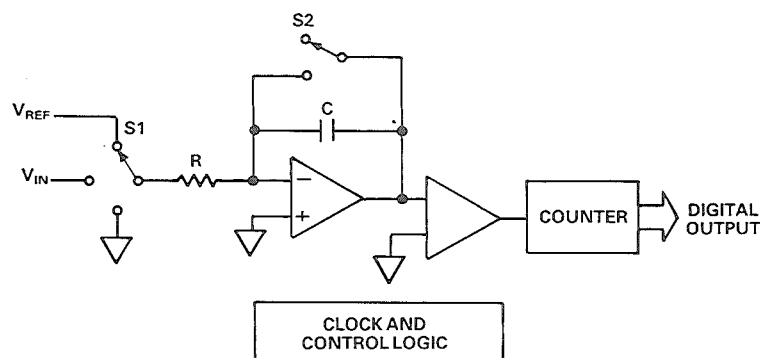


Figure 4.10

## CHARGE/DISCHARGE WAVEFORM OF INTEGRATING ADC

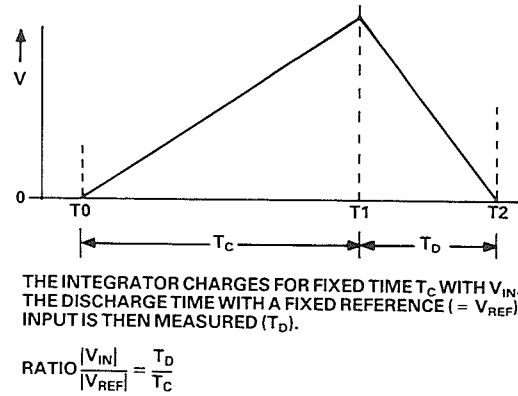


Figure 4.11

Leakage and offset in the integrator and hysteresis and offset in the comparator affect the conversion accuracy, and most practical integrating ADCs perform a conversion with the integrator input grounded to compute the errors due to these effects. These errors are then subtracted from the result of an actual conversion. The nature of an integrating ADC is such that there is virtually no differential nonlinearity, and it does not suffer from missing codes.

The sampling period,  $T$ , of an integrating ADC is fixed. If the frequency of any ripple on the input to the ADC is an integral multiple of  $1/T$ , a whole number of cycles will occur during each integration period, and the

net contribution to the charge in the integrator due to ripple will be zero. Thus, an integrating ADC has near infinite rejection of input frequencies  $n/T$ , where  $n$  is an integer. By selecting  $T$  to be the period of the power line frequency (16.667ms for 60Hz and 20ms for 50Hz), line ripple on the input signal will be disregarded. The normal mode response for the integrating ADC with a conversion period  $T$  is shown in Figure 4.12.

As will be discussed in Section VI, sigma-delta ADC technology offers an attractive alternative to the integrating ADC, especially if the function is to be implemented in VLSI technology.

## NORMAL MODE RESPONSE OF INTEGRATING ADC

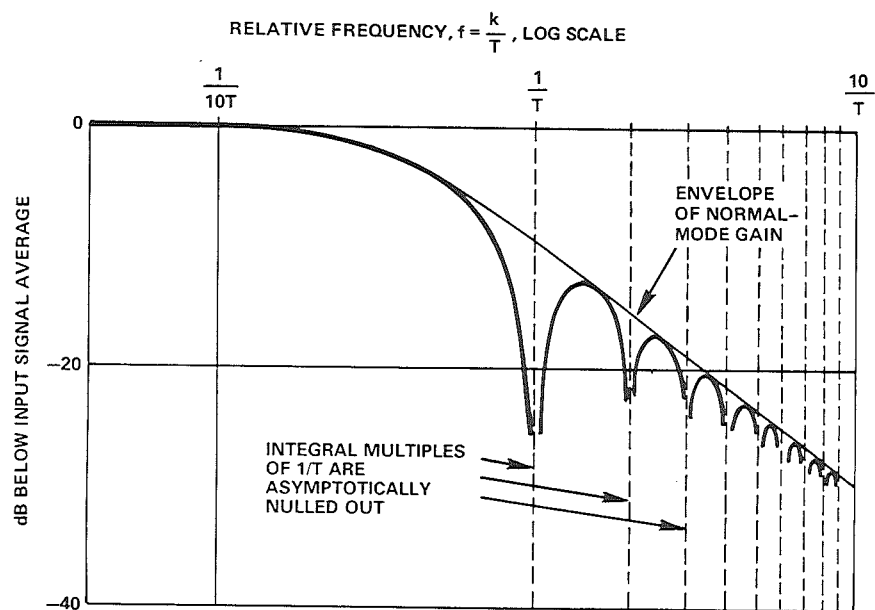


Figure 4.12