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SECTION IX

NON-LINEAR CIRCUIT APPLICATIONS

Barrie Gilbert, Bob Clarke

9.1 INTRODUCTION TO DYNAMIC RANGE COMPRESSION

In real-world signal-processing systems the signal of interest often exhibits a wide range of amplitudes. Familiar examples are: radio and radar receivers, where the dynamic range of an electromagnetic signal may be as high as 120 dB; analytical instruments such as gas chromatographs, where the output current of a photodetector may vary from picoamps to milliamps; sonar and ultrasound systems, where the attenuation of an acoustic signal varies rapidly with the path length; and so on. In terms of the signal voltage,

$$\text{Dynamic range (dB)} = 20\ lgt \frac{\text{Largest signal voltage}}{\text{Smallest signal voltage}}.$$

where *lgt* here, and throughout this section, means $\log_{10}$, or "logarithm to base 10".

Note that in a *linear-impedance* system, power is proportional to the voltage (or current) squared. Therefore, a 10,000:1 *voltage* ratio – that is, an 80 dB dynamic range – corresponds to a 100,000,000:1 *power* ratio. Accordingly:

$$\text{Dynamic range (dB)} = 10\ lgt \frac{\text{Largest signal power}}{\text{Smallest signal power}}.$$

We have chosen to use voltage ratios throughout this section because the majority of signal-processing circuits respond to purely voltage-mode signals, and occasionally operate on purely current-mode signals. Of course, at any branch in a real circuit there are both voltage- and current-mode components of the signal, hence finite power. On the other hand, the miniscule power "consumed" at the gate input of an MOS amplifier is not a very good indicator of the available dynamic range . This is because the voltage noise at this node of the circuit might be quite high, from microvolts to millivolts depending on the noise bandwidth and allowing for the possibility of 1/f noise, while the largest signal voltage might only be a volt or two. Power ratios are more useful in fixed-impedance systems, such as RF amplifiers operating between a resistively-matched source and load, usually 50 Ω.

At this point, we should differentiate between the dynamic range of the *signal* and that of the processing *system*:

$$\text{Signal dynamic range (dB)} = 20\ lgt \frac{\text{Largest actual signal voltage}}{\text{Smallest actual signal voltage}}$$

$$\text{System dynamic range (dB)} = 20\ lgt \frac{\text{Largest permissible signal voltage}}{\text{Smallest detectable signal voltage}}$$

We are solely concerned in this Section with the *system* dynamic range, in particular, with methods for maximizing this range, preferably matching or somewhat exceeding that of the signal. We will present the theoretical foundations as well as fully-tested practical circuits for dealing with many commonly-encountered situations in which signals of unusually wide dynamic range must be compressed to a more manageable level.

In dealing with such signals the need invariably arises for amplifiers which, on the one hand, can provide high gain with low noise levels when the signal is weak, in order to drive high-level processing circuits (such as A/D converters) while, on the other hand, being able to cope with large signals with minimum degradation. This Section also provides guidelines in the selection of suitable amplifiers for use in wide dynamic range systems.

DYNAMIC RANGE DEFINITIONS

$$\text{Dynamic range (dB)} = 20\ lgt \frac{\text{Largest signal voltage}}{\text{Smallest signal voltage}}$$

$$\text{Dynamic range (dB)} = 10\ lgt \frac{\text{Largest signal power}}{\text{Smallest signal power}}$$

$$\text{Signal dynamic range (dB)} = 20\ lgt \frac{\text{Largest actual signal voltage}}{\text{Smallest actual signal voltage}}$$

$$\text{System dynamic range (dB)} = 20\ lgt \frac{\text{Largest permissible signal voltage}}{\text{Smallest detectable signal voltage}}$$

Figure 9.1.1

9.1.1 NOISE LIMITATIONS

The dynamic range of all signal-processing systems is limited by random noise, which sets a fundamental bound on the smallest signal that can be detected or otherwise utilized with adequate signal-to-noise ratio (SNR). This noise may be generated by numerous mechanisms, including those associated with the source itself (e.g., antenna, photomultiplier, piezoelectric transducer, etc.) as well as by the active and passive devices in the amplifier.

Noise cannot be discussed without reference to bandwidth, which will be unavoidably limited by the type of amplifier(s) used. Deliberate filtering is often included in a signal-processing channel to reduce noise, as well as to improve the separation of wanted from unwanted signals. This may take the form of band-pass, low-pass or high-pass functions, or combinations of these, depending on the situation. Nonlinear filtering may also be used, for example, in order to minimize the disturbance of the signal path in the presence of impulsive noise. In some case, adaptive filtering is effective: a "lock-in amplifier" seeks a periodic (and often extremely weak) component in a noisy signal and automatically tunes a narrow-band filter to track its frequency (Reference 9.1.1). A key element of such a system is a synchronous detector.

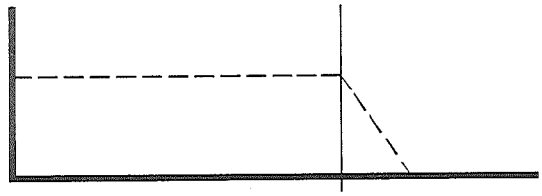
The noise powers of uncorrelated sources add, so noise voltages (or currents) must be added using a root-sum-of-squares (RSS) calculation. This leads to some rather startling consequences. Suppose a system has a major voltage noise source of magnitude E_a and several minor noise sources which RSS sum to a magnitude of E_b. Then, for the major source to contribute almost 90 % of the total system noise, E_a needs to be only twice E_b. When $E_a/E_b = 5$, fully 98 % of the noise is due to E_a.

It follows that the overall noise performance of a practical system can benefit greatly by (1) minimizing the input-referred noise of the first stage and (2) using the highest possible gain in this stage. However, the second of these objectives is frequently unrealizable in systems that must handle signals of large dynamic range, because the high gain would then preclude distortion-free operation at maximum signal levels.

Noise is frequently specified in terms of "noise spectral density", or NSD. This term reflects the fact that the total noise power is directly proportional to the system's noise bandwidth, B_N (in Hertz). The NSD is therefore usually of interest in specifying a channel's *input-noise* limitations. Note that the noise bandwidth is not, in general, equal to the –3dB bandwidth. B_N can be viewed as the bandwidth of an equivalent system with a "brick-wall" cessation of response at that frequency. A system with a single-pole low-pass corner at $f_o = 1/2\pi T$ has a B_N equal to $\pi f_o/2$, or $1.57 f_o$, while for two such real-pole low-pass sections in cascade B_N is $\pi f_o/4$. (See Figure 9.1.2).

FILTER NOISE BANDWIDTHS

Single-Pole Low-Pass Filter: $B_N = \pi f_o/2 = 1.57 f_o$



Two Single-Pole Low-Pass Filter sections in cascade: $B_N = \pi f_o/4 = 0.785 f_o$

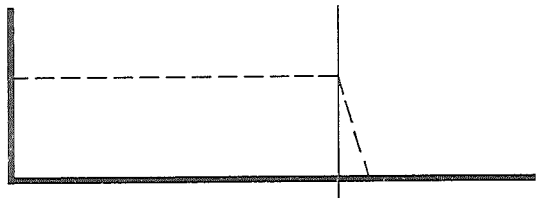


Figure 9.1.2

The total NSD will have both voltage- and current-components. We will use the symbol S_E to refer to the *voltage* noise spectral density and the symbol S_I to refer to the *current* noise spectral density. Since the noise power is proportional to the square of either the voltage or current, S_E and S_I have the dimensions of Volts per Root-Hertz and Amps per Root-Hertz, respectively. Noise signals are usually small, and therefore nonlinear effects are often negligible; in such circumstances, it is permissible to use superposition methods to evaluate each contributing source independently, followed by an RSS calculation to calculate the total noise. A notable exception is the logarithmic amplifier, where even very small noise voltages at the input can cause later stages in the amplifier to be in heavy limiting. Special approaches to both noise analysis and noise specification are required in such cases.

9.1.1.1 NOISE GENERATORS

We will only briefly review some of the most basic aspects of noise generation. The topic is well-covered in many fine standard texts; see, for example, Reference 9.1.2. The thermal (Johnson) noise voltage of an ideal resistor has an open-circuit magnitude of

$$S_E = (4kTR)^{0.5} \qquad \text{Eq. 9.1.1}$$

where T is the absolute temperature in Kelvins, k is Boltzmann's constant (1.38×10^{-23} Joules/Kelvin) and R is the resistance in Ohms. This evaluates to 0.129 nV/$\sqrt{\text{Hz}}$ per root-ohm at

a temperature of 300 K (about 27 °C). We will refer to this constant as the *standard temperature ohm-normalized noise-spectral density*, and assign it the symbol S_Ω.

A 100 Ω resistor generates 10S_Ω or 1.29 nV/√Hz at T = 300 K.

It is sometimes more useful to consider the resistor to be noise-free and then represent the noise as an equivalent current-source in shunt with it; of course, this has the same value as the short-circuit current-noise, $S_I = (4kT/R)^{0.5}$.

Some real resistors exhibit excess noise, which is a function of the current flowing in the resistor. This occurs whenever there are grain boundaries in the resistive material. Monolithic diffused and thin-film resistors do not have significant excess noise. The contact-related artifacts which were troublesome in thin-film resistors many years ago are nowadays eliminated through the use of one or more intermediate conductive layers.

The incremental channel resistance of a junction-FET or strongly-inverted MOS transistor behaves as a simple ohmic resistance, as far as noise is concerned, but has a value of $3/2gm$. The transconductance, *gm*, is proportional to the width-to-length (W/L) ratio of the channel and the channel current (I_{DS}). Low-noise MOS stages demand the use of large interdigitated devices (large W) operating at high values of I_{DS}. Field-effect transistors, and in particular, MOS types, suffer from significant amounts of flicker noise. This noise increases with decreasing frequency, f, roughly with a $1/f^{\alpha}$ form, where α is often taken to be unity; thus, it is called "1/f noise". The topic is complex and even controversial (see, for example, Reference 9.1.3). However, as a guideline, 1/f noise can only be reduced by increasing the channel *area*, WL.

The base-emitter voltage, V_{BE}, of an ideal bipolar junction transistor (BJT) operating at a constant collector current I_C is not noise-free. There is unavoidable "granularity" in this current, expressed as the shot noise, which has a current noise spectral density of

$$S_I = (2qI_C)^{0.5} \qquad \text{Eq. 9.1.2}$$

This noise current operates on the transistor's (noiseless) incremental emitter resistance

$$re = kT/qI_C \qquad \text{Eq. 9.1.3}$$

to generate a voltage-noise spectral density of

$$S_E = (2qI_C)^{0.5}\, kT/qI_C$$

$$= kT\,(2/q)^{0.5}(1/I_C)^{0.5} \qquad \text{Eq. 9.1.4}$$

The shot-noise-induced voltage which effective appears in series with base-emitter path is thus inversely proportional to the square-root of the collector current and *totally independent of the transistor geometry or process technology.*

The V_{BE} noise for a BJT is 0.476 nV/√Hz per root-milliamp of I_C at T = 300 K.

It is interesting to note in passing that this noise is √2 times *smaller* than the noise in a real resistance of the same value as *re*.

NOISE GENERATORS

$$S_E = (4kTR)^{0.5} \qquad \text{Eq. 9.1.1}$$

A 100 Ω resistor generates $10S_\Omega$ or 1.29 nV/√Hz at T = 300 K.

$$S_I = (2qI_C)^{0.5} \qquad \text{Eq. 9.1.2}$$

$$re = kT/qI_C \qquad \text{Eq. 9.1.3}$$

$$S_E = (2qI_C)^{0.5}\, kT/qI_C \qquad \text{Eq. 9.1.4}$$

$$= kT\,(2/q)^{0.5}(1/I_C)^{0.5}$$

The V_{BE} noise for a BJT is 0.476 nV/√Hz per root-milliamp of IC at T = 300 K.

$$R_N = \frac{S_E^2}{4kT} \qquad \text{Eq. 9.1.5}$$

Figure 9.1.3

9.1.1.2 NOISE OF TYPICAL INPUTS STAGES

When dealing with signal sources which have relatively low resistance, the input stage should be chosen to exhibit a low value of S_E. After all the noise generators have been RSS-added, the resulting S_E can be expressed as an equivalent noise resistance

$$R_N = \frac{S_E^2}{4kT} \qquad \text{Eq. 9.1.5}$$

An input-noise resistance of one quarter that of the source would contribute only 10% of the total noise. For bipolar input stages, the dominant noise-voltage generator is typically the base resistance, $r_{bb'}$. The channel resistances of field-effect transistors used in input stages exhibit the same noise behavior as simple resistors.

9.1.1.3 PRACTICAL AMPLIFIER NOISE SPECIFICATIONS

We can define the absolute lower limit of the system's dynamic range as simply being equal to its noise referred to the input, when driven from some specified source impedance, and in a specified bandwidth. This is commonly referred to as the "noise floor". A signal of the same magnitude presented to the input would result in a SNR of 0 dB, by definition. While this clearly represents the fundamental lower limit on the system dynamic range, it may be more meaningful to specify this limit in terms of some acceptable SNR, say, 20 dB. In analog channels handling digital data, this limit may be specified in terms of the maximum allowable bit-error-rate (BER).

In low-frequency applications, it is customary to specify the noise at the input of an amplifier in terms of separate voltage and noise components. The voltage noise spectral density is that noise which appears to be present at the input when this input is short-circuited. The best of contemporary op-amps exhibit values of the order of 1 to 5nV/√Hz. The bipolar-input AD797, optimized for this specification, has an NSD of 0.9 nV/√Hz. The generic workhorse "741", on the other hand, has a typical NSD of 15nV/√Hz due to the use of a four-transistor input stage operating at only ~10μA. As previously noted, there is a fundamental limit to what can be achieved at any given bias level. It is quite unrealistic to expect a micropower amplifier to have a low voltage-NSD. An ideal bipolar differential pair operating at a 1 μA cannot have a NSD lower than 30 nV/√Hz at room temperature.

In high-frequency circuits, it is common to specify the *noise-figure* of amplifiers. Noise Figure (NF) is often computed using the formula

$$NF = 10\ lgt\ \frac{e_n^2 + I_n^2 R_s^2 + 4kTR_sB_N}{4kTR_sB_N} \qquad \text{Eq. 9.1.6}$$

In the formula, e_n is the voltage noise, I_n is the current noise, B_N is the bandwidth in Hz, T is the absolute temperature in Kelvins, k is Boltzmann's constant (1.38×10^{-23} Joules/Kelvin) and R_S is the source resistance in Ohms.

9.1.2 DYNAMIC-RANGE LIMITATIONS

While noise limits the lower end of a system's dynamic range, performance at the upper end of the signal range is always degraded by the increasing importance of nonlinear aspects of circuit behavior. Thus, one way to specify the upper limit to the system's dynamic range is by determining the magnitude of the signal at which the *total harmonic distortion* reaches some maximum acceptable level, say 1 %. Alternatively, it may be specified as that signal level which causes the system's incremental gain to fall by 1 dB; this is called the *1 dB compression point* as shown in Figure 9.1.4.

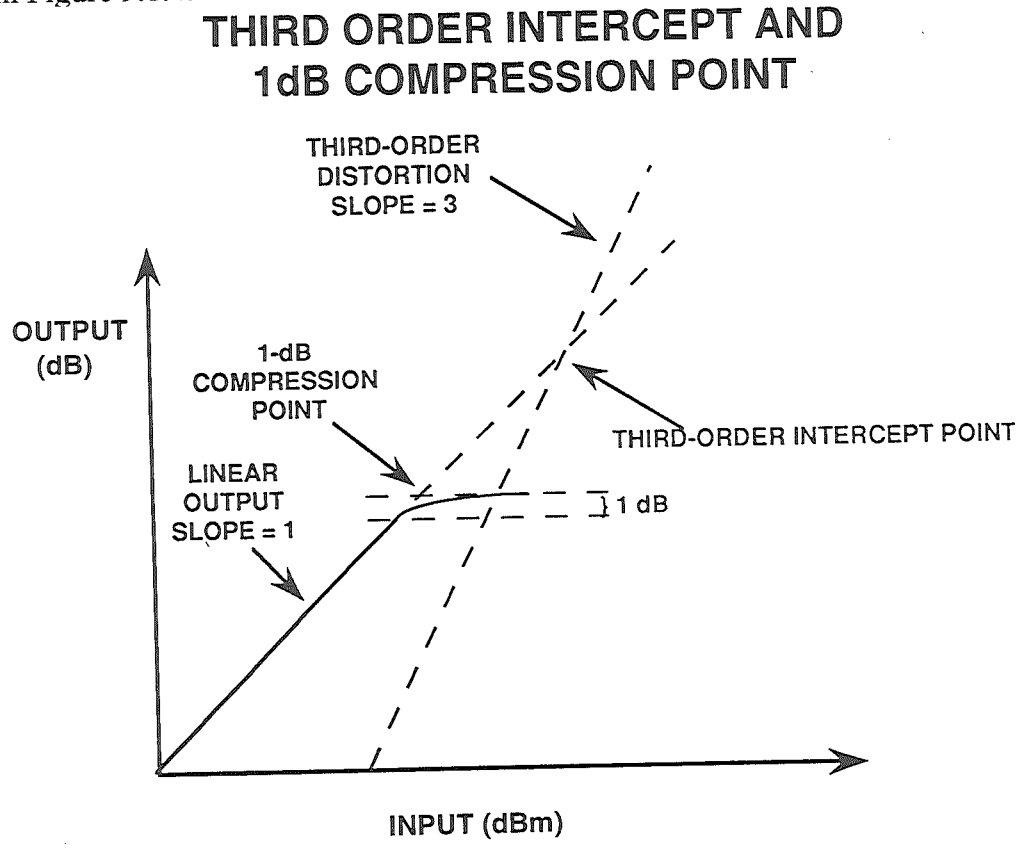


Figure 9.1.4

The term "spurious-free dynamic range", sometimes used in this context, is a little misleading because of course the distortion of any real amplifier is always finite, and a continuous function of signal level. In systems involving frequency-translation using mixers, distortion generates spurious signal components in the intermediate (IF) output spectrum, which are usually troublesome. The term *third-order intercept* is often used to specify the signal-handling capacity of the mixer; this can be defined as the extrapolated single-tone input level which would generate equal fundamental and third-harmonic outputs.

In some cases (such as the gas chromatograph) it may be more appropriate to characterize the entire dynamic range in "DC" terms, limited at the low end by such things as finite offset and input bias current of the input stage, and at the upper end by the onset of unacceptable nonlinearity or even clipping. In other words, the dynamic range in these cases is that range over which the measurement *accuracy* is held to within defined limits (for example, ±1 % of

reading). In such cases, flicker noise (both voltage and current), which dominates the performance of many such low-bandwidth systems, may impose a serious limitation on the available dynamic range.

From these considerations, it will be apparent that the precise method for defining the "dynamic range" of a given system clearly depends on the nature of the signal and the type of processing invoked. No single standard can be applied to adequately define the dynamic range of all systems. In fact, the central challenge of the design of a signal-processing system is ultimately that of optimizing each section so as to recover the maximum possible information (in digital systems, to achieve the lowest possible bit-error rate).

9.1.3 SIGNAL COMPRESSION

In some cases, a wide dynamic range is an essential aspect of the signal, something to be preserved at all costs. This is true, for example, in the high-quality reproduction of music. However, it is often necessary to compress the signal down to a smaller range without any significant loss of information. Compression is often used in magnetic recording, where the upper end of the dynamic range is limited by tape saturation and the lower end by the granularity of the medium. In professional noise-reduction systems, compression is "undone" by precisely-matched nonlinear expansion during reproduction. Similar techniques are often used in conveying speech over noisy channels, where the performance is more likely to be measured in terms of word-intelligibility than audio fidelity. The reciprocal processes of compressing and expanding are implemented using "compandors"; many schemes have been devised to achieve this function.

In radio systems, the received energy exhibits a large dynamic range due to the variability of the propagation path, requiring dynamic-range compression in the receiver. In this case, the wanted information is in the modulation envelope (whatever the modulation mode), not in the absolute magnitude of the carrier. For example, a 1 MHz carrier modulated at 1 kHz to a 30 % modulation depth would convey the same information whether the received carrier level is at 0 dBm or –120 dBm. Some type of automatic gain control (AGC) in the receiver is invariably utilized to restore the carrier amplitude to some normalized reference level in the presence of large input fluctuations. AGC circuits are dynamic-range compressors which respond to some metric of the signal – often its mean amplitude – acquired over an interval corresponding to many periods of the carrier. Consequently, they require time to adjust to variations in received signal level. The time required to respond to a sudden increase in signal level can be reduced by using peak detection methods, but with some loss of robustness, since impulsive noise can now activate the AGC detection circuits. Nonlinear filtering and the concept of "delayed AGC" can be useful in optimizing an AGC system. Many tradeoffs are found in practice; Figure 9.1.5. shows a basic system.

A TYPICAL AGC SYSTEM

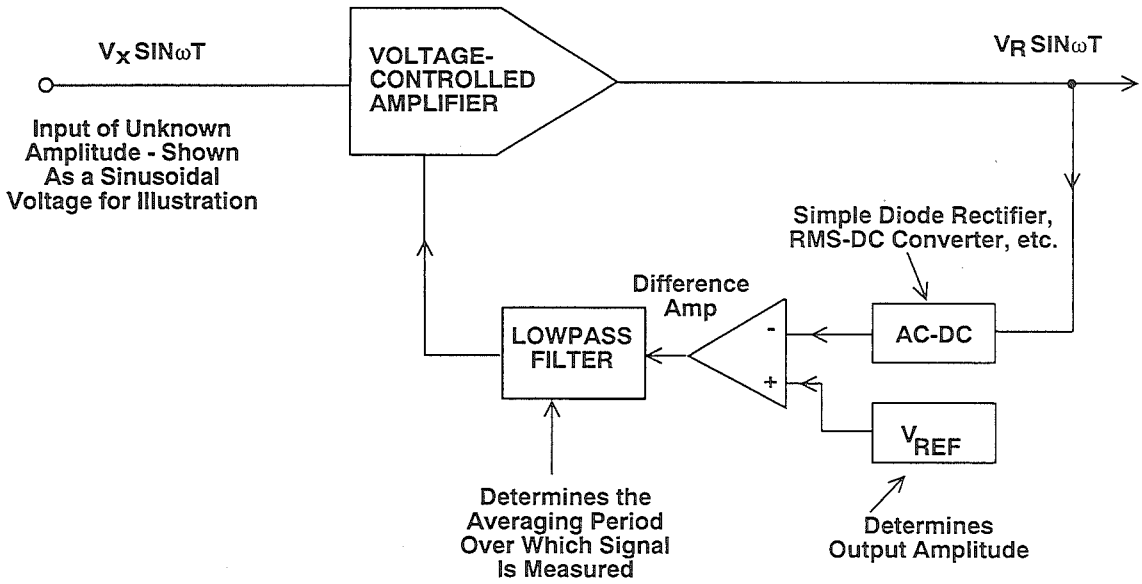


Figure 9.1.5

In other cases, the system is required to respond almost instantaneously to the signal. For example, the waveshape of the pulse output of a microwave radar detector must be preserved over many decades of amplitude, which requires that each value of voltage on the input waveform maps uniquely to a value of the output, with essentially the same response for signals of some arbitrarily low frequency (often DC) up to the maximum bandwidth of the channel. The most common mapping functions are the logarithm (or its near-neighbor, the inverse hyperbolic sine) and square-root.

In this section a variety of practical circuit solutions will be presented for compressing signals of large dynamic range. Because of their extensive scope, we will not discuss signal-path filtering techniques, except where they arise incidentally.

9.1.4 LINEAR VS NONLINEAR COMPRESSION

We can divide dynamic range compression systems into "linear" and "nonlinear". In the first category, the gain of the amplifier(s) in the processing chain is independent of the magnitude of the signal but is arranged to vary such a way as to render the output (that is, its peak, mean or RMS value) essentially constant. The harmonic distortion is relatively low.

These systems use what are often called variable-gain amplifiers. While correct, this lacks precision, because *nonlinear* amplifiers (such as log-amps) also exhibit variable gain, but in direct response to the signal magnitude. The term voltage-controlled amplifier (VCA) is preferred in this context; it clearly describes the way in which the gain-control is implemented while allowing latitude in regard to the actual circuit means used to achieve the function. In fact, the gain may be controlled by a *current* within the circuit, but usually by conversion from a voltage at the control interface.

Analog multipliers and dividers are sometimes used as VCAs, but far more optimal circuit topologies are available.

AGC systems use one or more VCAs in conjunction with a level detector and low-pass filter (LPF), usually driven by the output. Occasionally, an analog divider will be used, in which case the input level is extracted and used as the denominator; unlike conventional (feedback) AGC systems, this approach makes use of *feedforward* control.

Any voltage-controlled amplifier may be converted to digital control by the inclusion of a DAC. There are relatively few amplifier products available which provide direct digital control, for reasons explained in the following section.

A special type of VCA is used in "swept-gain" applications. This is an amplifier whose gain is controlled without measurement of the actual signal level; instead, it utilizes the predictable magnitude of the signal as a function of time (or occasionally some other parameter). For example, in medical ultrasound systems the attenuation varies with the depth of the tissue layer being imaged. Similar circumstances arise in sonar and short-range radar.

By contrast, nonlinear dynamic-range compression is used in circumstances where low harmonic distortion is not a requirement. Log-amps provide the best example of this type of compression. All types of log-amps produce a low-dynamic-range output without the need to first acquire some measure of the signal amplitude for use in controlling gain. As we shall see later, these can be basically divided into baseband and demodulating types. Baseband log-amps produce an output with minimal time delay and do not employ rectification (that is, signal detection). Demodulating log-amps provide the detection function, and produce a baseband output from a higher-frequency input; filtering is employed on the detected output only to remove the unwanted high-frequency components. In special cases, VCAs of the type used for AGC or swept-gain applications can be used for nonlinear compression; some examples will be presented. In all such cases, an A/D converter of moderate resolution (say, 8 bits) can be made to handle a signal of large dynamic range (say, 16 bits, or 96 dB) while preserving equal incremental resolution over the whole range.

REFERENCES

9.1.1 See , for example, **Lock-In Amplifiers: Principles and Applications** by M. L. Meade, Peter Peregnius, Ltd., 1983

9.1.2 **Low Noise Electronic Design** by C. D. Motchenbacher and F. C. Fitchen, John Wiley Inc., 1973.

9.1.3 **The MOS Transistor** by Y.P. Tsividis, McGraw-Hill, Inc., 1987.

9.2 VOLTAGE CONTROLLED AMPLIFIERS (VCAS)

There are many ways to build voltage-controlled amplifiers. The literature goes back to the earliest days of electronics, amounting to thousands of papers and hundreds of patents. This section will review some of the most important contemporary techniques and show several practical applications.

Such digitally-controlled circuits as software-programmable-gain amplifiers or multiplying D/A converters (MDACs) provide discrete-gain steps. The Analog Devices LOGDAC™ AD7111 is a development of the MDAC approach to gain control. This special-purpose CMOS D/A converter emulates an attenuator with a range of 0 to –88.5 dB and resolution of 0.375 dB (a 4.4 % gain change per step) using an 8-bit control input.

Often, much finer gain-control is necessary, which requires the use of a larger control word. This is not of itself a basic problem: if one wished to achieve the above range of 88.5 dB with the resolution increased to 0.086 dB (a 1 % gain change per step), it would require a 10-bit word. However, important practical issues arise. In applications where the dynamic range is wide (88.5 dB corresponds to a voltage ratio of about 27,000:1), it follows that at the low end of the gain-control range the channel must process very small signals.

The complete separation of the digital control inputs from these weak signals is difficult, at both the silicon level and the board level. For example, this problem becomes severe when it is necessary to update the gain quickly – over a period of a few microseconds or less – in which case the feedthrough of rapidly-changing binary data edges ("glitching") becomes intolerable.

Furthermore, the use of MOS switches, such as those found in MDACs and their derivatives, is not conducive to low-noise, wideband design: the Johnson noise of the FET channel resistance can be reduced only by the use of large-geometry devices, and these in turn exhibit significant parasitic capacitances, leading to problems in controlling both the phase and the amplitude of the system response under all conditions, but particularly at high attenuation levels.

Consequently, in applications where (a) the signal to be compressed covers a wide dynamic range, (b) the required accuracy of the AC gain and phase response is high, and (c) the gain must be swept rapidly, digital control techniques are not attractive and in the most critical applications cannot be used at all. In these cases, a voltage-controlled amplifier (VCA) is indispensable.

It must also be remembered that there remain numerous applications where direct analog control is still the preferred approach from other considerations. For instance, it is inconvenient to distribute the control data on a wide digital bus to a large number of parallel signal-processing channels, as in an ultrasound system. It is also simpler to implement AGC systems using VCAs.

9.2.1 A COMMON VCA STRUCTURE

A popular approach to the design of a VCA is to use the reliable exponential relationship between collector current and base-emitter voltage in a bipolar junction transistor, through which means it is possible to achieve a gain-control range of several decades. A very widely-used

circuit is shown in Figure 9.2.1. The signal voltage V_Y is first converted to a complementary pair of currents, which are here denoted as $(1+Y)I_Y$ and $(1-Y)I_Y$, by a voltage-to-current (V/I) converter formed by Q1, Q2 and R_Y. The "modulation index" Y has a maximum range of ±1; in practice, it will have a peak value of about 0.75, to minimize distortion due to the nonlinear V_{BE} of the transistors. To a good approximation, $Y = V_Y/I_YR_Y$ (true when $I_YR_Y \geq 100$ kT/q).

A COMMON VARIABLE -GAIN CELL: THE "CONTROLLED CASCODE"

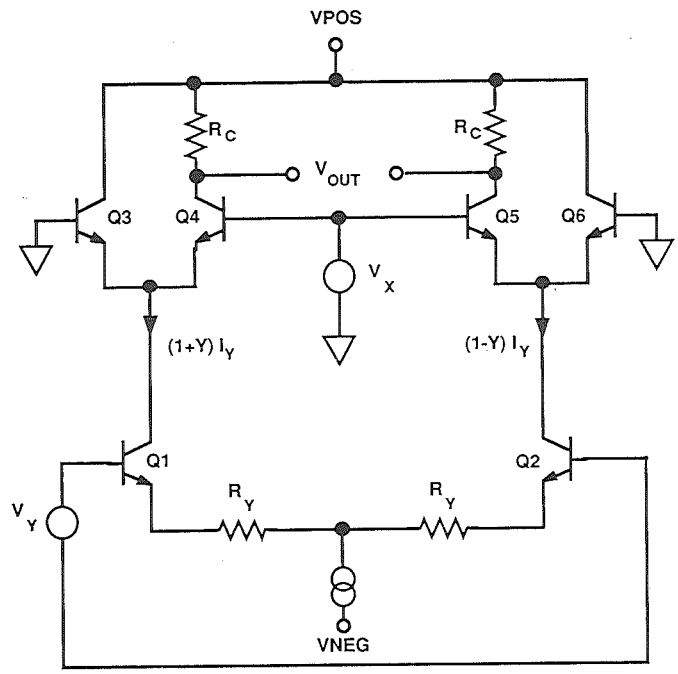


Figure 9.2.1

The signal-plus-bias currents are then applied to a "current-fork", comprising Q3 through Q6, that steers some fraction, $0 \leq X \leq 1$, of the signal currents to the output load resistors, and dumps the remainder to the positive supply. These transistors also act as a cascode stage, which extends the frequency range of the amplifier; because of this feature, we will refer to this cell as a "controlled cascode".

The parameter X is determined by the gain-control voltage V_X. It is readily shown that

$$X = \frac{exp(V_X/V_T)}{1 + exp(V_X/V_T)} \qquad \text{Eq. 9.2.1}$$

where V_T is the thermal voltage kT/q, which has a value of 25.85 mV at T = 300 K (about 27°C). At this temperature, X is 0.99 when V_X = 120 mV and 0.01 when V_X = –118 mV. If the

system gain is normalized to 0 dB when X = 1, the loss is 6 dB for $V_X = 0$; Figure 9.2.2 shows the decibel value of gain as a function of V_X at three temperatures.

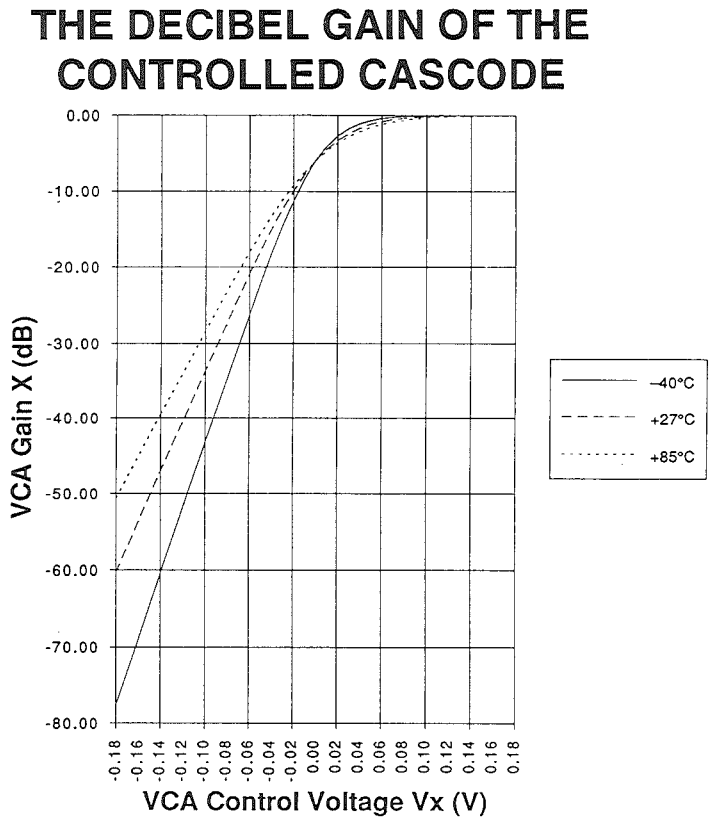


Figure 9.2.2

Several potential problems are immediately apparent from this graph. First, the circuit's control function is not "linear in decibels"; it approaches this condition only for very high attenuation. Second, the attenuation is a strong function of temperature; this, and the nonlinear control function, may not matter too much in closed-loop AGC systems, but both would be troublesome in "swept-gain" VCA applications, or in feed-forward AGC systems. The temperature-sensitivity can be addressed using special resistors to form an attenuator between the actual gain-control voltage and the base nodes.

Apart from these obvious weaknesses, this cell has additional problems. Notice that the lower end of the input dynamic range is fundamentally limited by the Johnson noise of R_Y. If this resistor is reduced to the point where acceptable noise performance is achieved, the upper end of the dynamic range will also be reduced, due to the onset of distortion, unless very large values of bias current I_Y are used.

For example, suppose we wish to achieve a short-circuited input noise spectral density of 1.5 nV/√Hz at 300 K (which corresponds to 15 μV in a 100 MHz bandwidth) then R_Y can be no more than 135 Ω. This assumes that Q1 and Q2 have no ohmic resistances; in practice, the $r_{bb'}$

of both transistors must be subtracted from R_Y to maintain the desired total resistance. Even well-optimized monolithic transistors may have $r_{bb'}$ values of 15 Ω, typically requiring R_Y to be 100 Ω.

Now postulate that a maximum input of 1 V RMS must be handled with a total harmonic distortion of less than –60 dBc. (At moderate frequencies the distortion will be third-order, but there will be increasing odd- and even-order components at high frequencies.) To meet this last requirement when R_Y = 100 Ω, it can be shown that the two currents I_Y must each be at least 23 mA; using typical ±5V supplies, this would correspond to an expenditure of almost half a watt in just the voltage-to-current converter! Such high power consumption is unwelcome where a very large number of VCAs are used, as in ultrasound imaging applications, and would be intolerable in most battery-operated systems.

So far, we have assumed that the noise due to the second stage is negligible, but that can only be true if the controlled-cascode cell has a maximum voltage gain (when X = 1) that is much greater than one. This gain is at most $2R_C/R_Y$. Let the noise at the input (due to $2r_{bb'} + R_Y$) be E_a, and that in the load circuit (at best, due to $2R_C$ alone) be E_b. The total noise at the output, E_{no}, for the maximum gain condition, where noise performance is critical, is

$$E_{no} = \{ (2R_C/ R_Y)^2 E_a^2 + E_b^2 \}^{0.5} \qquad \text{Eq. 9.2.2}$$

Referred to the input, this is equivalent to a noise of

$$E_{ni} = \frac{\{ (2R_C/ R_Y)^2 E_a^2 + E_b^2 \}^{0.5}}{2R_C/ R_Y} \qquad \text{Eq. 9.2.3}$$

Noting that $E_a = S_\Omega(2r_{bb'} + R_Y)^{0.5}$ and $E_b = S_\Omega(2R_C)^{0.5}$, where S_Ω is the ohm-normalized noise-spectral density (see Section 9.1.1.1) and setting $r_{bb'}$=0 for simplicity and also to show the fundamental limitations more clearly, we can write

$$E_{ni} = S_\Omega R_Y^{0.5} (1 + R_Y/2R_C)^{0.5} \qquad \text{Eq. 9.2.4}$$

The first part of this expression is simply the Johnson noise of R_Y. E_{ni} is increased in direct proportion to the second factor, requiring that $2R_C$ be much greater than R_Y. When $R_C = 2 R_Y$, the noise is increased by about 12 % or 1 dB. In our example, therefore, we might use R_C = 400Ω. But this raises a practical problem: if a value of I_Y = 23 mA were used to maintain acceptable distortion levels, the maximum voltage drop across the load resistors R_C would be nearly 15 V at full gain and full signal, requiring an inordinately high supply voltage. Further noise and distortion is generated by the base resistances and capacitances of the cascode transistors. At low gains, HF signal feedthrough occurs via the T-network formed by the $C_{je}/r_{bb'}/C_{jc}$ of these transistors, causing aberrations in the AC response.

In numerous ways this type of VCA fails to meet the exacting requirements of modern systems. Nevertheless, the approach remains appealing where some concessions to noise, distortion and gain-accuracy can be made. It is a simple cell for use in embedded applications, and provides the highest possible bandwidth for a given technology. Variable-gain amplifiers built along these lines are available for use up to about 1 GHz.

9.2.2 USING ANALOG MULTIPLIER/DIVIDERS TO BUILD VCAS

Analog multipliers and dividers can also be used in gain-control applications. These circuits are invariably based on the translinear principle, which exploits the precise proportionality of transconductance to collector current in a bipolar transistor.

Voltage-controlled amplifiers (VCAs) built from analog multipliers take one of two forms. In the first, the multiplier acts as a voltage-controlled attenuator ahead of a fixed-gain amplifier. This type of VCA is used in applications where not only a moderate maximum gain is needed but also a fairly high maximum loss. In the second, the variable attenuation is placed in the feedback path around an op amp, which in fact implements an analog divider. Analog dividers are more suitable for applications requiring high gains.

Products available from Analog Devices include the low-cost AD633, the high-accuracy AD734, and the high speed AD834 (useful to 500 MHz). These are four-quadrant multipliers. For gain-control applications, a two-quadrant circuit is more useful, such as the dual-channel AD539, which provides a signal bandwidth of about 60 MHz.

VCAs and multipliers based on the nonlinear properties of transistors inevitably exhibit various types of spurious nonlinearity, caused by non-ideal aspects of transistor behavior and the necessity for "open-loop" design. Nevertheless, with care in design and the use of distortion-nulling laser-trimming techniques in manufacturing, exceptionally low levels can be achieved. For example, the AD734 Multiplier/Divider exhibits nonlinearities of only 0.02 % from either the X- or Y-input, and provides a gain-bandwidth product of 200 MHz in its two-quadrant divider mode, implemented by direct control of the denominator voltage (rather than by putting a multiplier in a feedback path) over a 1000:1 range (10 mV to 10V).

Many practical circuits can be built using multipliers. We begin with a discussion of the AD539 and its use in conjunction with such transimpedance amplifiers as the AD844, because the AD539's basic structure is similar to that of the cell described in the last section, but the means have been included to provide accurate *linear* gain control, rather than the roughly-exponential, temperature-dependent gain control function of the basic cell. Figure 9.2.3 shows the essential pieces of the AD539. Note that there are two nominally identical channels whose gains are simultaneously controlled by a common voltage, V_X. These may be used separately, or in simple parallel to improve bandwidth and noise performance, or in a differential mode with appropriate support circuits.

SIMPLIFIED SCHEMATIC OF THE AD539 ANALOG MULTIPLIER

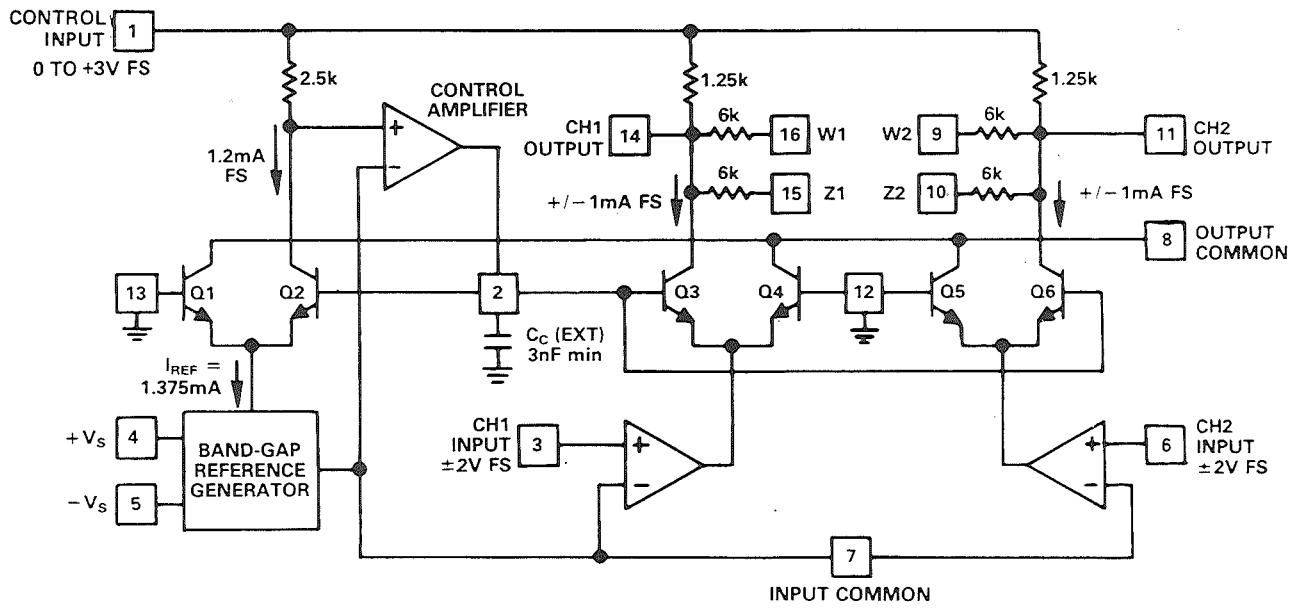


Figure 9.2.3

Two applications are shown. In Figure 9.2.4, the two sections of the AD539 are connected in simple parallel to double the output current. An AD844 transimpedance amplifier provides current-to-voltage conversion. The transfer function of this circuit is

$$V_W = \frac{-V_X V_Y}{2V} \qquad \text{Eq. 9.2.4}$$

where V_X is the gain-control voltage, a positive input from 0 V to 3.2 V , and V_Y is the signal input voltage, nominally ±2V full scale but capable of operating up to ±4.2 V. Connecting all four of the feedback resistors provided on the AD539 in parallel results in a feedback resistance of 1.5 kΩ, at which value the bandwidth of the AD844 is about 22 MHz, independent of V_X. The gain at V_X = 3.16V is +4 dB. Figure 9.2.5 shows the small signal response for a 50 dB gain-control range (V_X = +10 mV to +3.16 V). At small values of V_X, capacitive feedthrough on the PC board becomes troublesome, and careful layout techniques are needed.

In Figure 9.2.6, The AD827 dual high-speed op amp is used to provide output current-to-voltage conversion and the two sections of the AD539 are connected in series to provide a VCA with a square-law response. The transfer function of this circuit (measured at the reverse-terminated load) is

$$\frac{V_{OUT}}{V_{IN}} = \frac{V_X^2}{8V^2} \qquad \text{Eq. 9.2.5}$$

Alternately, the two sections may be operated in parallel with linear gain control. The frequency response of this circuit is about 8 MHz using the AD827 op amp. The AD811 high-speed op amp may be substituted in these circuits for increased performance.

For wider bandwidths, the AD834 multiplier (Figure 9.2.7) may be used with a variety of op amps to build VCAs with small-signal bandwidths as high as 480 MHz. In each case, the op amp converts the differential-current outputs of the AD834 into a voltage.

A 20MHz VCA USING THE AD539 AND THE AD844

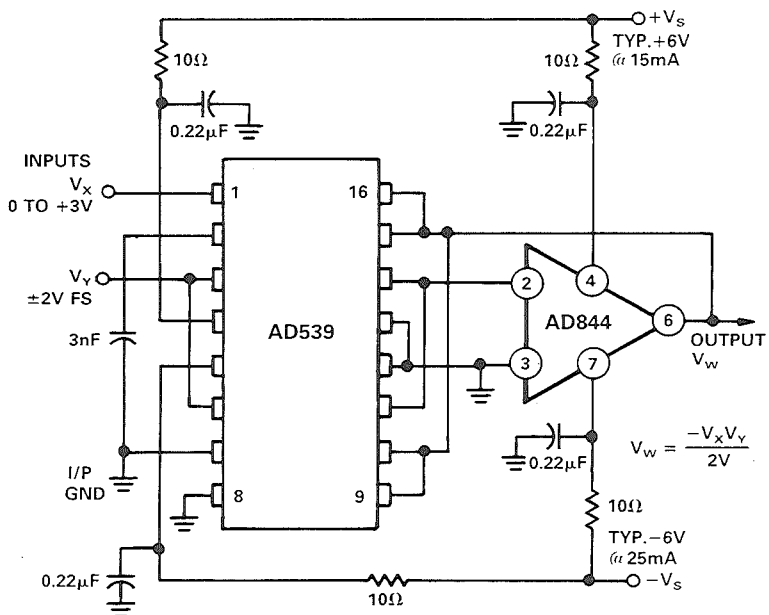


Figure 9.2.4

FREQUENCY RESPONSE OF THE 20MHz VCA

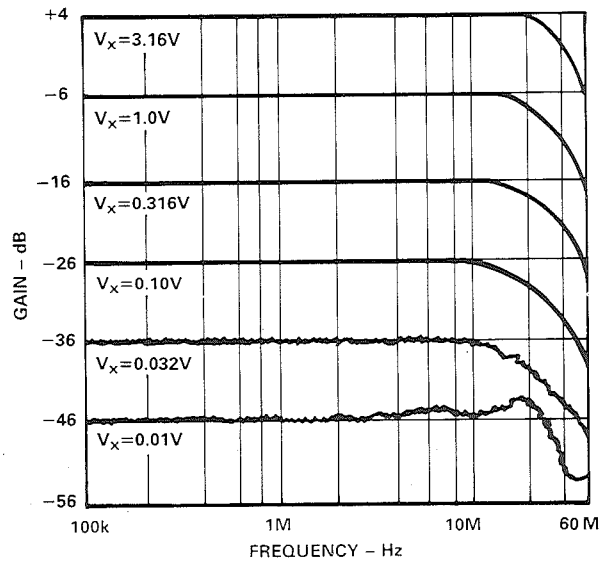
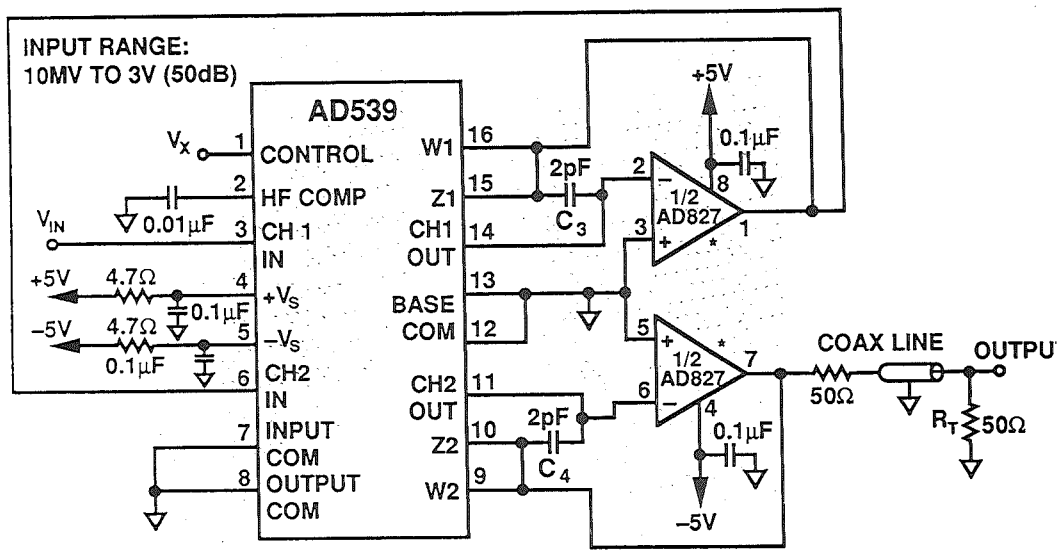


Figure 9.2.5

VCA WITH SQUARE LAW GAIN CONTROL USING THE AD539 MULTIPLIER



*PINOUT SHOWN IS FOR MINI-DIP PACKAGE

V_{out} AT TERMINATION RESISTOR, $R_T = V_x^2 V_{in}/8V^2$

V_{out} AT PIN 7 OF AD827 = $V_x^2 V_{in}/4V^2$

Figure 9.2.6

SIMPLIFIED BLOCK DIAGRAM OF THE AD834 MULTIPLIER

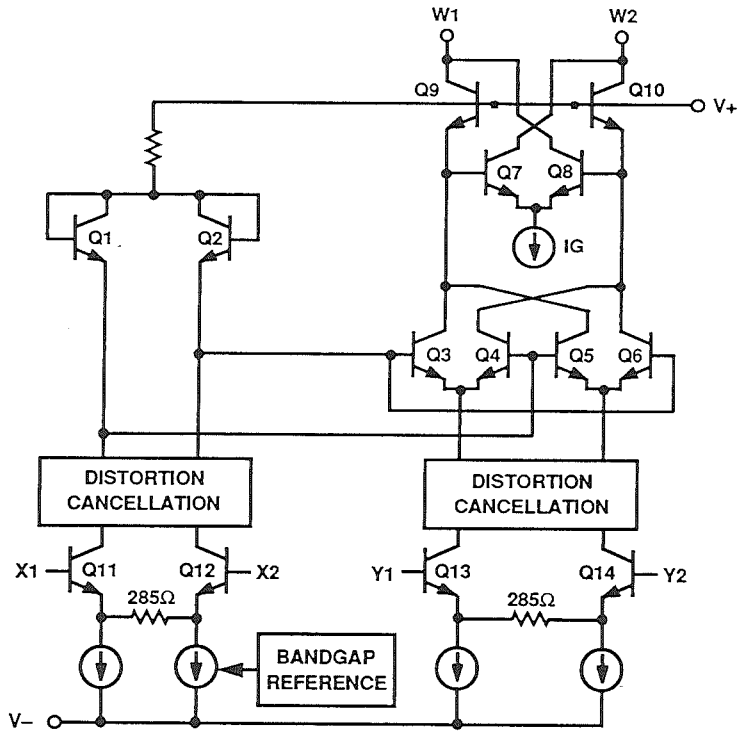


Figure 9.2.7

A 60MHz VCA USING THE AD834 AND THE AD5539

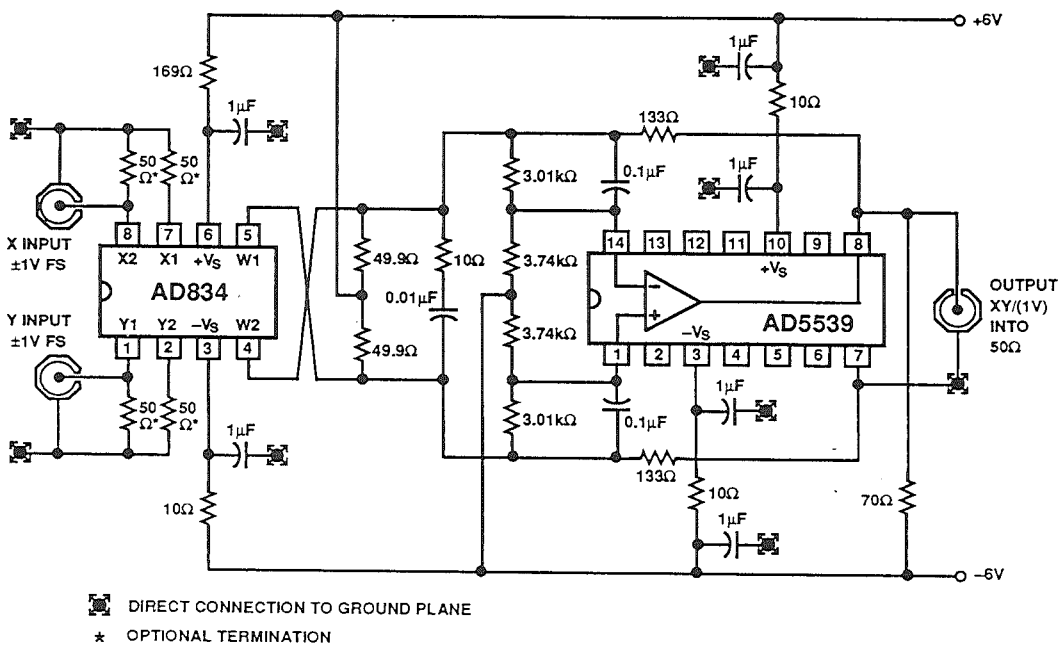


Figure 9.2.8

PULSE RESPONSE OF THE 60MHz VCA

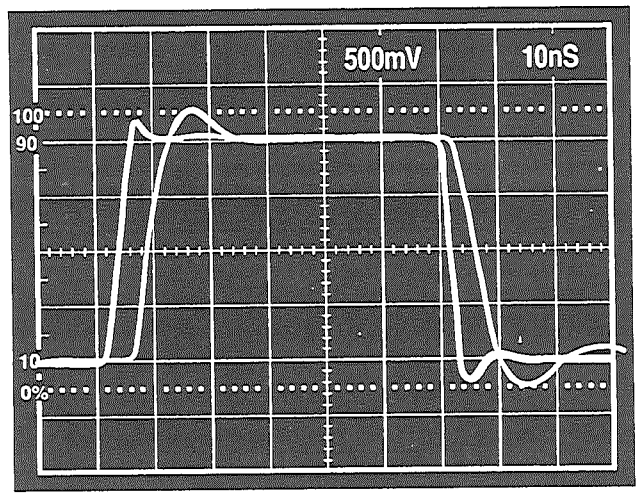


Figure 9.2.9

A 90MHz VCA is shown in Figure 9.2.10. The AD834's outputs are in the form of differential currents from a pair of open collectors, ensuring that the full bandwidth of the multiplier (which exceeds 500 MHz) is available. In this case, more moderate bandwidth is obtained using current-to-voltage conversion provided by the AD811 op amp, to realize a practical amplifier with a single-sided ground-referenced output. Using feedback resistors R8 and R9 of 511 Ω the overall gain ranges from -70 dB for $V_G \sim 0$ to +12 dB (a numerical gain of four) when $V_G = +1$ V.

The exact transfer function for the AD834 would show that the differential voltage inputs at X1, X2 and Y1, Y2 are first multiplied together, divided by the scaling voltage of 1 V (determined by the on-chip bandgap reference) and the resulting voltage is then divided by an accurate 250 Ω resistor to generate the output current. A simplified form of this transfer function is

$$I_W = (X_1 - X_2)(Y_1 - Y_2)\ 4\ \text{mA} \qquad \text{Eq. 9.2.6}$$

where I_W is the differential current output from W1 to W2 and it is understood that the inputs X_1, X_2, Y_1, and Y_2 are *expressed in Volts*. Thus, when both differential inputs are 1 V, I_W is 4 mA; this current is laser-calibrated to close tolerance, which simplifies the use of the AD834 in many applications. Note the direction of this current in determining the correct polarity of the output connections.

A 90MHz VCA USING THE AD834 AND THE AD811

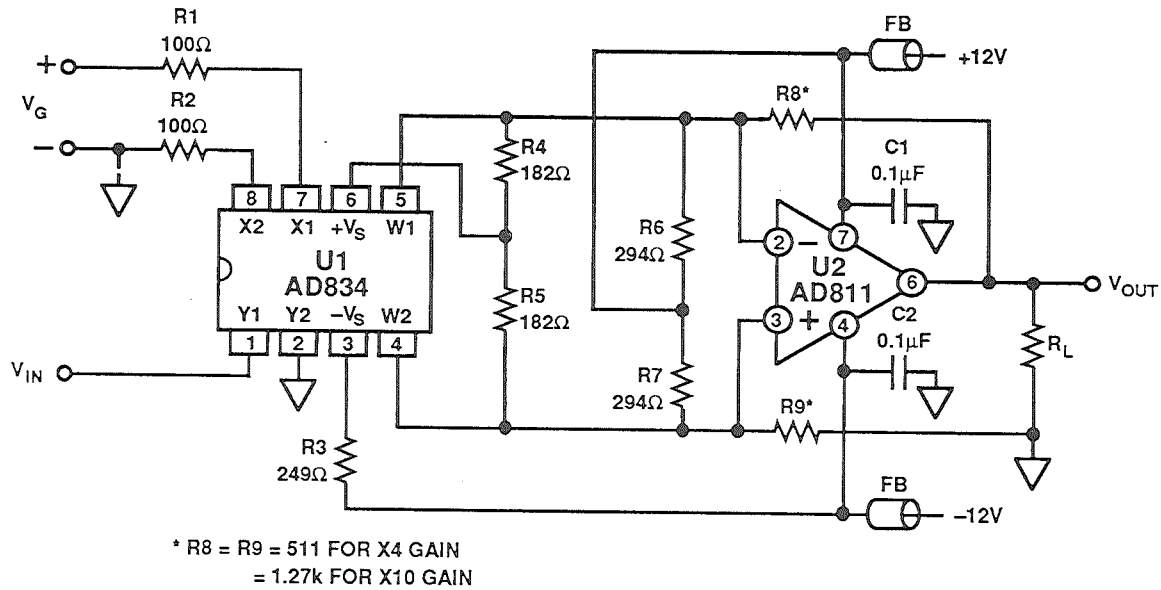


Figure 9.2.10

It is easy to show that the output of the AD811 is

$$V_{OUT} = 2 \times I_W \times R_F \qquad \text{Eq. 9.2.7}$$

where R_F is the feedback resistor. For $R_F = 500\ \Omega$ the overall transfer function of the VCA becomes

$$V_{OUT} = 4\,(X_1 - X_2)\,(Y_1 - Y_2) \qquad \text{Eq. 9.2.8}$$

which reduces to $V_{OUT} = 4\ V_G\ V_{IN}$ using the labeling conventions shown in Figure 9.2.10. As noted, the phase of the output reverses when V_G is negative. A slightly higher value of R_F compensates for the finite gain of the AD811.

The -3 dB bandwidth is 90 MHz (Figure 9.2.11) and independent of gain. The response can be maintained flat to within ±0.1 dB from DC to 40 MHz at full gain with the addition of a 0.3 pF capacitor across the feedback resistor R8. The circuit produces a full-scale output of ±4 V for a ±1 V input, and can drive a reverse-terminated load of 50 Ω or 75 Ω to ±2 V. Figure 9.2.12 shows the typical pulse response.

FREQUENCY RESPONSE OF THE 90MHz VCA

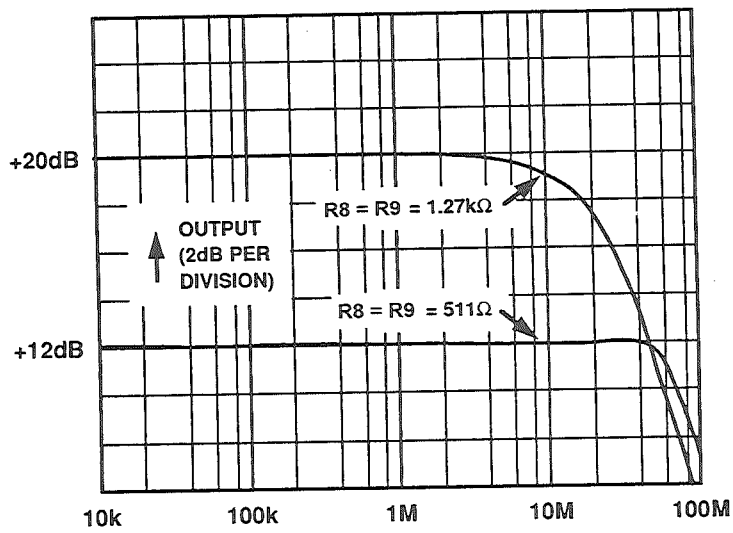


Figure 9.2.11

PULSE RESPONSE OF THE 90MHz VCA

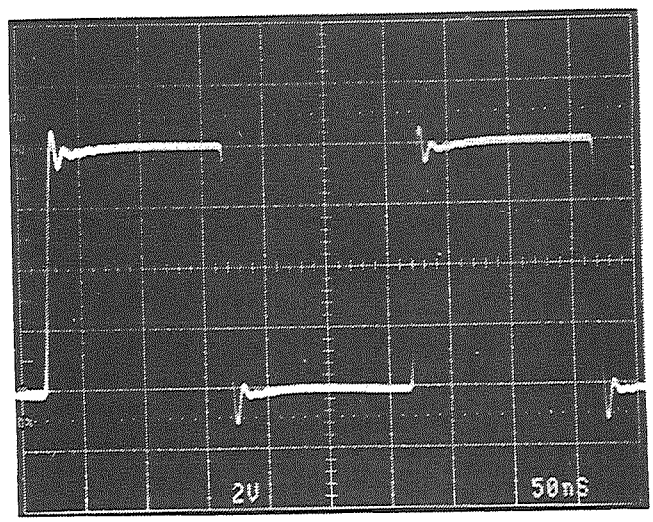


Figure 9.2.12

The gain can be increased to 20 dB (10) by increasing the values of R8 and R9 to 1.27 kΩ; this also reduces the -3 dB bandwidth to about 25 MHz and produces a maximum output voltage of ±9 V using ±12 V supplies. It is not necessary to alter the values of R6 and R7 for the high-gain version of the amplifier, although an optimized design would increase these slightly to restore the common-mode voltage at the input of the AD811 to +5 V.

Figure 9.2.13 shows a DC to 480 MHz VCA using a PNP transistor as a common base stage or cascode. The transistor's base is tied to +5 V, ensuring that the emitter potential stays at 5.7 V and provides a steady voltage drop across the emitter resistors. In this circuit, the AD9617 op amp's inputs are 350 mV below ground and within their common mode range.

A 480MHz VCA USING THE AD834 AND THE AD9617

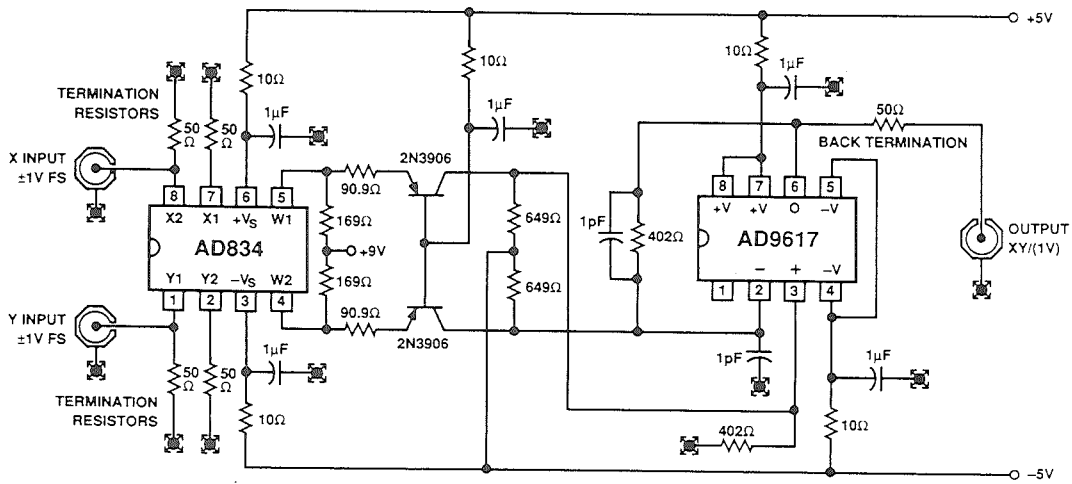


Figure 9.2.13

The bandwidth of a transistor configured as a cascode is approximately the unity gain frequency (f_t) of the transistor, provided that the user does not create any spurious poles. Choosing emitter resistors which are too large for the transistor's parasitic emitter-base capacitance or collector resistors too large for the transistor's parasitic collector-base capacitance will create unwanted poles that lower the frequency response of the circuit.

Another potential pitfall when using the active PNP level shifter is oscillations at the cascode's emitter. The input impedance of a bipolar junction transistor's emitter is inductive at frequencies approaching f_t, while the AD834's output is capacitive. These conditions can lead to oscillations.

To prevent such oscillations, the PNP's emitters in Figure 9.2.13 have been isolated from the AD834's output by the 90.9Ω resistors. These dampen any tendency to oscillate and provide signal attenuation. The 2N3906s and their accompanying network has proven to provide wideband level shifting without resonance or oscillation. Care must be taken when specifying alternative transistors.

The signal currents at the 2N3906s' collectors are now fed to an AD9617 op amp in a differential current-to-voltage converter configuration. This configuration is similar to the op-amp driven current-to-voltage converter that typically follows a current-output multiplying digital-to-analog converter.

The AD9617's inputs are connected to the collectors of the 2N3906s. The op amp creates a virtual short between the input nodes, forcing all the signal current to flow in the feedback paths. The differential transresistance of the converter is 400 Ω. The full scale gain of the circuit (X=Y=1V) at the AD9617's output is calculated as:

$$\text{Maximum Gain} = 2 \times 2.6\ \text{mA} \times 400\ \Omega = 2.08 \qquad \text{Eq. 9.2.9}$$

or 1.04 at the load after the reverse termination resistor. The actual circuit shows a full scale gain closer to unity. Figure 9.2.14 shows the pulse response. The small signal bandwidth is 480 MHz.

PULSE RESPONSE OF THE 480MHz VCA

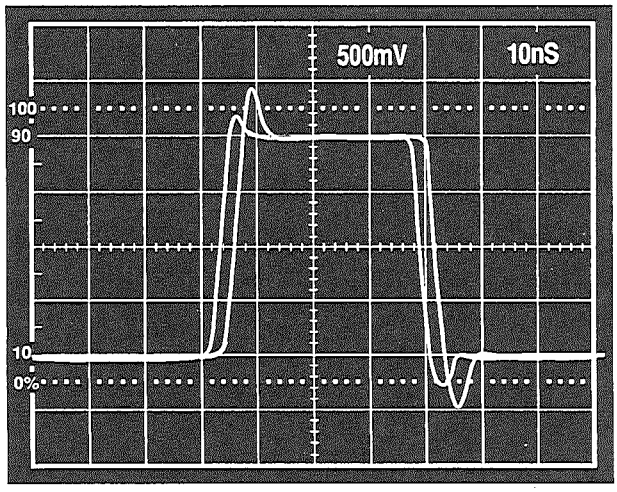


Figure 9.2.14

9.2.2.1 VIDEO KEYER

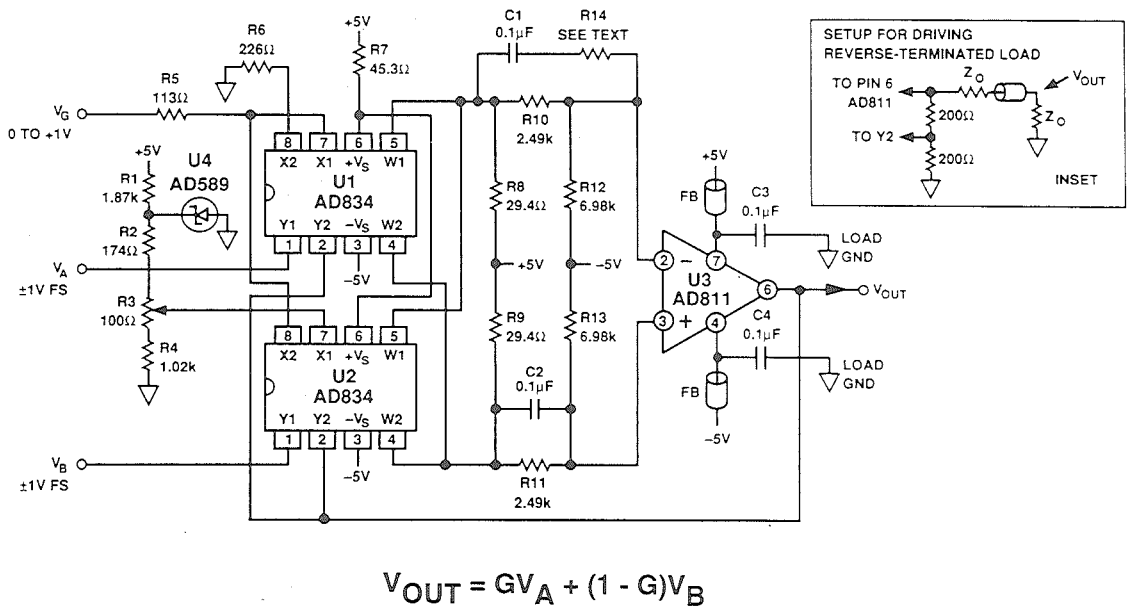
The AD834 also lends itself to a special form of a VCA called a video keyer. Keying is the term used in reference to blending two or more video sources under the control of a further signal or signals to create such special effects as dissolves and overlays. The circuit described here is a two-input keyer, with video inputs V_A and V_B, and a control input V_G.

The output at the load is given by

$$V_{OUT} = G\,V_A + (1-G)\,V_B \qquad \text{Eq. 9.2.10}$$

where G is a dimensionless variable (actually, just the gain of the "A" signal path) that ranges from 0 when $V_G = 0$, to 1 when $V_G = +1$ V. Thus, V_{OUT} varies continuously between V_A and V_B as G varies from 0 to 1.

A 2-INPUT VIDEO KEYER



$$V_{OUT} = GV_A + (1 - G)V_B$$

Figure 9.2.15

Figure 9.2.15 shows the circuit. Note first that V_{OUT} is returned to the inverting inputs Y2 of the multipliers and that their outputs are added. The sum is forced to zero by the assumed high open-loop gain of the op amp. Multiplier U1 produces an output $G(V_A - V_{OUT})$, while U2 produces an output $(1-G)(V_B-V_{OUT})$, where G is $V_G/(1\text{ V})$ and ranges from 0 to 1. Therefore, the complete system is described by the limiting condition

$$G(V_A - V_{OUT}) + (1-G)(V_B - V_{OUT}) \rightarrow 0 \qquad \text{Eq. 9.2.11}$$

which requires that

$$V_{OUT} = GV_A + (1-G)V_B \qquad \text{Eq. 9.2.12}$$

exactly as required for a two-input keyer. The summation of the differential current-mode outputs of the two AD834s is achieved by connecting together their respective W1 and W2 nodes. The resulting signal — essentially the loop error represented by the left-hand-side of Equation 9.2.11 — is forced to zero by the high gain of an AD811 op amp.

The operation is straightforward. Consider first the signal path through U1, which handles video input V_A. Its gain is zero when $V_G = 0$ and the scaling we have chosen ensures that it is unity when $V_G = +1$ V; this takes care of the first term in Equation 9.2.12. On the other hand, the V_G input to U2 is taken to the *inverting* input X2 while X1 is biased at an accurate +1 V. Thus, when $V_G = 0$, the response to video input V_B is already at its full-scale value of unity, whereas when $V_G = +1$ V, the differential input $X_1 - X_2$ is zero. This generates the second term in Equation 9.2.12. Figure 9.2.16 shows the AC response and Figure 9.2.17 shows the pulse response.

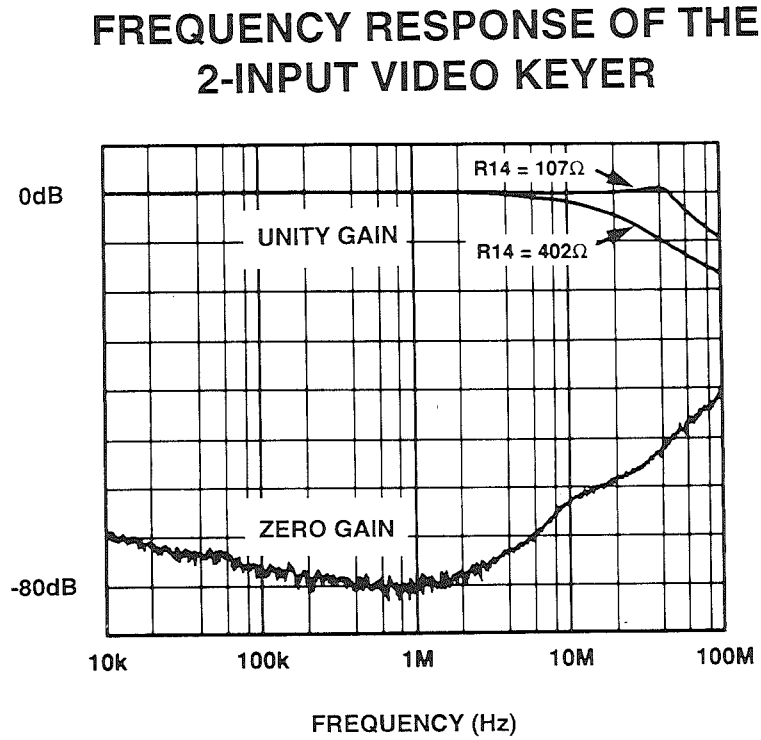
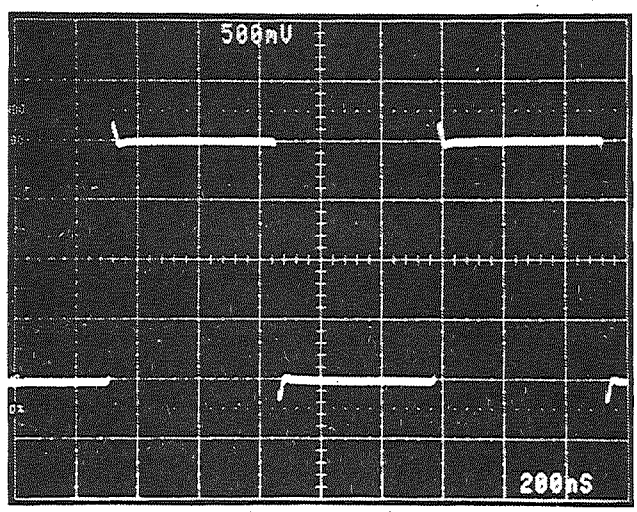


Figure 9.2.16

PULSE RESPONSE OF THE 2-INPUT VIDEO KEYER



R14 = 107Ω

Figure 9.2.17

To generate the 1 V DC needed for the "1–G" term, an AD589 reference supplies 1.225V±25mV to a voltage divider consisting of resistors R2 through R4. Potentiometer R3 should be adjusted to provide +1 V at the X1 input.

The bias currents required at the output of the multipliers are provided by R8 and R9. A DC-level-shifting network comprising R10/R12 and R11/R13 ensures that the input nodes of the AD811 are positioned within an acceptable common-mode range for this IC. At high frequencies, C1 and C2 bypass R10 and R11, respectively.

9.2.3 THE X-AMP

Two new dual-channel voltage-controlled amplifiers, the AD600 and AD602, have recently been introduced by Analog Devices. They differ from the multipliers just discussed in that the signal passes only through circuits that are linear: specifically a resistive ladder attenuator and a fixed-gain amplifier that uses negative feedback to enhance linearity. The term "X-AMP", coined to apply to this proprietary architecture, is a reference to the *exponential* gain function which they provide.

The X-AMP was developed for medical ultrasound applications. It provides the unusual combination of low noise (1.4 nV/√Hz), good signal-handling capabilities (1 V RMS at the input, 2 V RMS at the output), a constant 3 dB bandwidth of DC to 35 MHz, constant phase and group-delay characteristics, low distortion (–60 dBc to 10 MHz) and low power consumption (125 mW maximum per channel). The gain is an exponential function of the control voltage, V_G, which means it is "linear in dB", calibrated to 32 dB/Volt (31.25 mV/dB).

The two channels are independent and may be cascaded for a gain range of up to 80 dB in one package. Separate high-impedance, differential gain-control interfaces are provided. In the AD600 the gain for each section is 0 dB for V_G = –625 mV, 20 dB for 0 V, and 40 dB for +625 mV. When V_G exceeds these values, the minimum gain becomes –1.07 dB and the maximum is 41.07 dB. The AD602 is similar, except that each VCA provides a gain of –11.07 dB to 31.07 dB.

These precise over-range values will later be important in understanding the gain-sequencing scheme used in one of the circuits presented. The sections can also be operated in parallel, to achieve a noise spectral density of 1 nV/√Hz with no compromise in other aspect of performance.

As we will show, by adding an RMS converter to two series-connected VCA sections (a single AD600), a circuit can be built which provides both accurate automatic gain control (AGC) and an accurately-calibrated output voltage proportional to the decibel value of the RMS input over an 80 dB range.

9.2.3.1 X-AMP BASICS

The key idea behind these amplifiers is the use of a low-noise *fixed-gain* amplifier, which employs negative feedback to achieve low distortion and high gain-accuracy, preceded by a broadband *passive* R-2R attenuator network.

The new technique allows the attenuator to be *continuously* interpolated, thus providing the smooth decibel-scaled gain function. The fixed-gain amplifier (Figure 9.2.18) uses classical negative feedback to achieve accurate gain. Since it never has to cope with large input signals it can be optimized for low noise and low distortion. The overall bandwidth is constant. The resulting amplifier comes very close to the ideal VCA.

When a correctly-terminated regular ladder network is used for this attenuator, a "linear-dB" control law is *automatically guaranteed*, because the signals between adjacent tap-points bear a constant ratio, diminishing in an exponential fashion from input to termination. Using the familiar R-2R network the voltage ratio from left to right is exactly two, or about 6.02 dB. Using an R-R network, the attenuation would be 8.36 dB. Obviously, any desired ratio can be used; in practice, the use of integer resistor multiples ensures excellent attenuation accuracy without the need for trimming.

THE STARTING POINT IN THE SYNTHESIS OF THE X-AMP

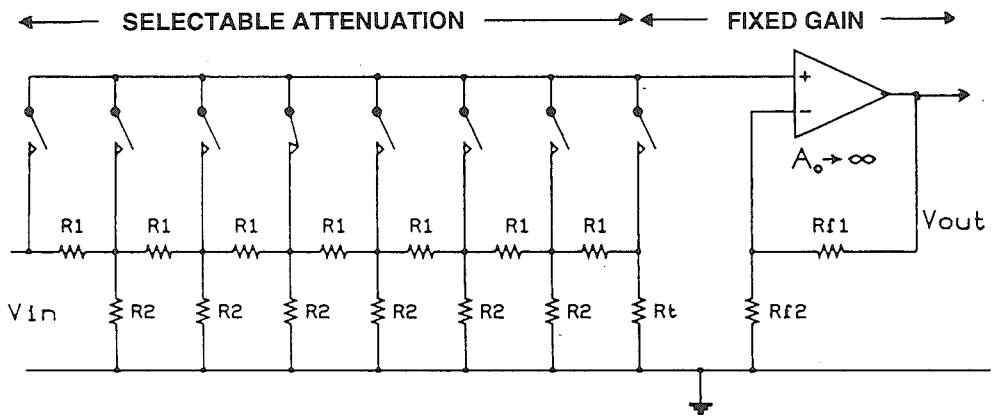


Figure 9.2.18

A seven-section R-2R attenuator provides a total attenuation of 42.14 dB (corresponding to an overall voltage ratio of 128). For the moment, assume that the taps on this attenuator are selected by a simple rotary switch, to provide eight discrete values of gain, separated by constant decibel steps of 6.02 dB. When a large input is to be handled, the full attenuation is used: a 1V input is reduced to 7.8 mV, easily handled by the main amplifier stage.

On the other hand, for small signals, the amplifier's input can be *directly* connected to the source, with essentially no extra thermal noise. In this condition, the noise generation mechanisms can be reduced to those fundamentally attributable to shot noise in the input stage of the amplifier and the combined Johnson noise of the source and feedback resistors. This is a distinct and unique advantage of the technique.

In an IC realization, the rotary switch might be replaced by eight digitally-selected MOS transistors. However, these would introduce significant amounts of extra noise due to their channel resistance, unless they were made very large, in which case parasitic capacitances would cause very undesirable feedthrough effects at high frequencies. They would still only provide discrete gain steps; any attempt to increase the resolution by using more attenuator sections with closer tap points, adding correspondingly more switches, would only exacerbate the feedthrough problem.

The key step in the development of the X-AMP concept is to replace the switches with controllable *gm* stages, as shown in Figure 9.2.19. These are bipolar differential pairs having a set of tail currents that are in the form of overlapping Gaussian sections. In this way, the effective input of the amplifier can be moved *continuously* from the source to the last tap on the attenuator. By correctly proportioning the interpolation currents, excellent gain linearity can be achieved: for the AD600 and AD602 it is about ±0.1 dB. Further development of the X-AMP showing the bipolar differential pairs is shown in Figure 9.2.20.

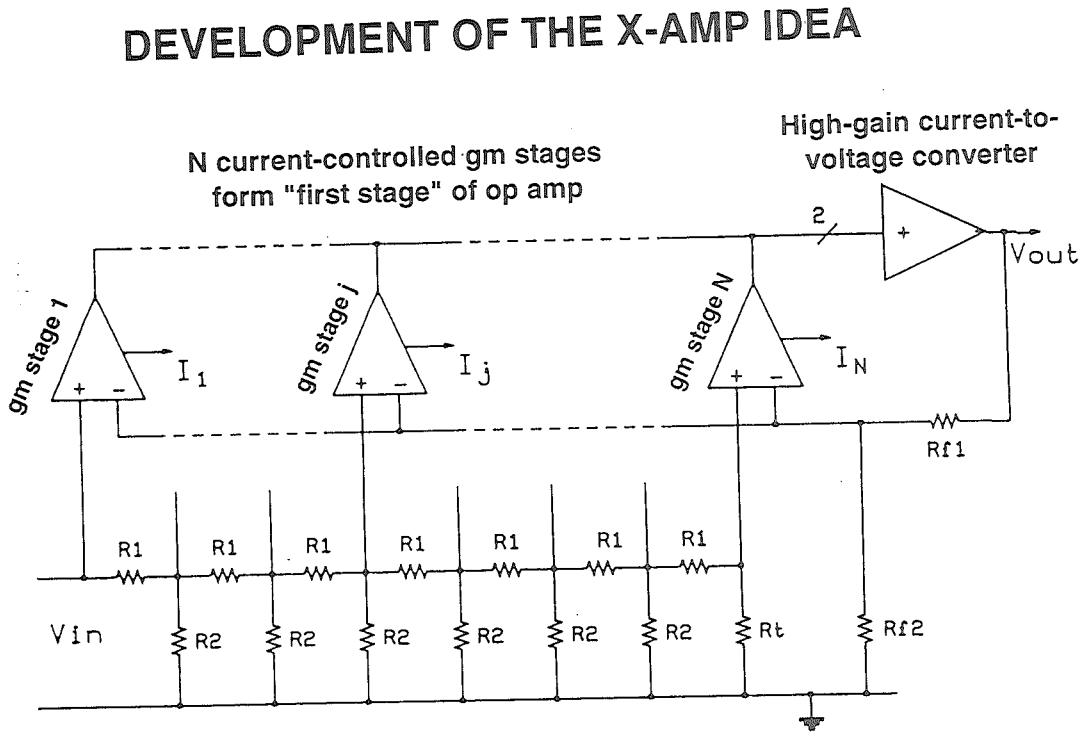


Figure 9.2.19

FURTHER DEVELOPMENT OF THE X-AMP IDEA

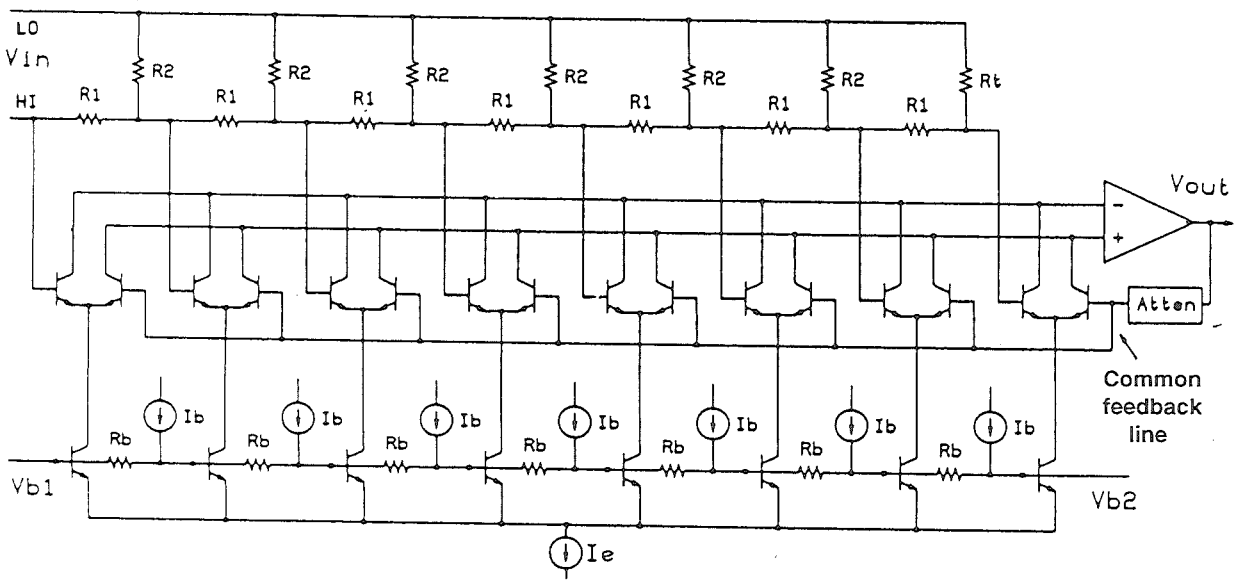


Figure 9.2.20

The fundamental noise floor for a differential bipolar transconductance (*gm*) stage, limited by shot-noise, is

$$S_I = \frac{0.926\text{nV}/\sqrt{\text{Hz}}}{\sqrt{I_T}} \qquad \text{Eq. 9.2.13}$$

at 300 K (27°C) where I_T is the differential amplifier "tail" current expressed in milliamps. In the AD600 and AD602, I_T is 2.4 mA, producing a theoretical noise-spectral-density (NSD) of 0.6 nV/√Hz. In addition, there will be Johnson noise in the resistances associated with the source, input stage and attenuators; at 300 K this evaluates to

$$S_\Omega = 0.129\sqrt{R_T} \quad \text{nV}/\sqrt{\text{Hz}}, \qquad \text{Eq. 9.2.14}$$

where R_T is the total ohmic resistance associated with the input system, that is, the sum of the source or tap resistance, the feedback resistor R_{F1} and the two base resistances of the input

transistors, $r_{bb'}$. For the AD600 and AD602, R_T is about 80 Ω, producing a NSD of 1.15nV/√Hz. The RMS sum of the shot noise S_I and Johnson noise S_Ω is 1.3 nV/√Hz. Some second-stage noise contributions and base-current noise raise this to 1.4 nV/√Hz.

Note that the *output* noise of the X-AMP is constant as the gain is varied. For the AD600, with a gain of 41.07 dB, or X113, the NSD is simply 1.4 nV/√Hz × 113 or 158 nV/√Hz. In a 1 MHz bandwidth this amounts to 158 μV RMS. Relative to a 1 V RMS output, this amounts to a signal-noise-ratio (S/N ratio) of 76 dB. For the AD602, having a gain which is 10 dB lower, the S/N ratio is 86 dB in a 1 MHz bandwidth.

Each gain control voltage V_G is applied to differential inputs (Figure 9.2.21), which have a scale factor of 32 dB per Volt; thus, a change of 31.25 mV always changes the gain by 1 dB. For the AD600, the gain for $V_G = 0$ is at the midpoint, that is, 20 dB. It is reduced to 0 dB when $V_G = -625$ mV and raised to 40 dB when $V_G = +625$ mV. Over this 0 to 40 dB range the gain is closely-specified. When V_G exceeds these values, the minimum gain is –1.07 dB and the maximum is 41.07 dB. The AD602 is very similar, but each fixed-gain amplifier now provides a gain of 31.07 dB, so each VCA section spans –10 dB to 30 dB (–11.07 dB to 31.07 dB max). The lower gain of the fixed amplifier in the AD602 improves the *output* signal-to-noise ratio by 10 dB; however, the input noise remains 1.4 nV√Hz.

BLOCK DIAGRAM OF THE AD600 AND AD602

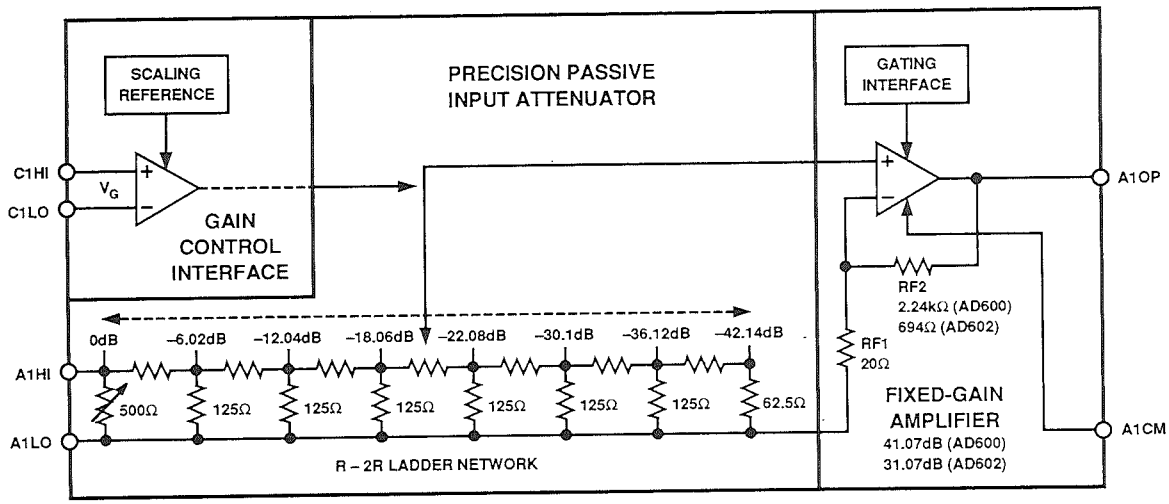


Figure 9.2.21

Since the AD600 and AD602 each provide two independent VCAs, A1 and A2, gain ranges of over 80 dB can be achieved. In the simplest case, their individual gain-control inputs are connected in parallel, and the gain varies by 64 dB per Volt. However, in order to optimize the signal-to-noise performance over the entire gain range, a sequential arrangement of the A1 and A2 gain control voltages can be used, in which the gain of A1 is first varied over its 40 dB range, while A2 operates at minimum gain (thus, with the lowest coupling of the output noise of A1); thereafter, only the gain of A2 is varied to provide the second 40 dB segment of the overall gain range. This "sequential-gain" function can be achieved by including an offset voltage (corresponding to about 40 dB) between the A1 and A2 gain-control inputs. We shall later show another modification to the gain-control function, using a small control offsets (3 dB in the case of two cascaded VCAs, 2 dB in the case of three sections) to achieve exceptionally accurate gain and excellent logarithmic linearity. Figure 9.2.22 lists the highlights of the X-AMP.

HIGHLIGHTS OF THE X-AMP

- Precise Decibel-Scaled Gain Control
- Accurate Absolute Gain Calibration
- Low Noise (1.4nV/ √Hz)
- Constant Bandwidth (dc to 35MHz)
- Stable Group Delay (±2ns over gain range)
- Low Distortion -- Uses Negative Feedback
- Low Power (125mW per channel maximum)

Figure 9.2.22

9.2.4 APPLYING THE X-AMP

The X-AMP is simple to apply. However, as for all wideband, high-gain amplifiers, careful PC board layout and adequate supply decoupling are important. This is particularly true when the amplifier sections are used in cascade. To simplify the following explanation, references to pin labels will be for amplifier A1, the connections for which are shown in Figure 9.2.23.

CHANNEL A1 OF THE AD600 OR AD602

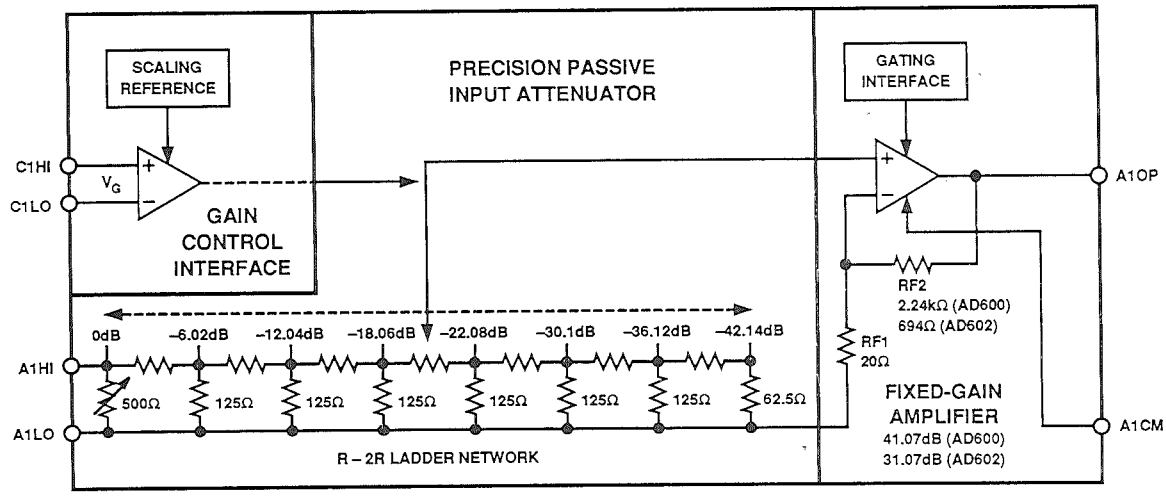


Figure 9.2.23

The input is applied to pins A1HI and A1LO, and may have a maximum value of 1 V RMS (±1.4 V peak), ultimately limited by the common-mode range of the eight g_m stages. The resistance from A1HI to A1LO is trimmed to 100 Ω ± 2 Ω, which allows the introduction of accurate external attenuation by the simple expedient of adding a series resistor. However, it is important to note that these pins do *not* form a fully differential input pair, as a glance at Figure 9.2.23 will show. In fact, A1LO must be always be very *well grounded*, since it carries not only the current in the ladder network but also the current in the feedback resistor RF1, which is about five times lower. Thus, the resistance which would be seen looking into A1LO if A1HI were grounded would be 100 Ω in parallel with 20 Ω, or 16.7 Ω. (Internally, A1LO is connected by multiple bond-wires to lower the impedance in this path.)

The output appears at pin A1OP but is referenced to an independent output ground, A1CM ("common"). A small common-mode voltage can exist between A1LO and A1CM, and this voltage will be rejected by the amplifier. (The details of the circuitry providing this feature are not shown explicitly in Figure 9.2.23.). Thus, if we denote the numerical gain of the amplifier by G, the output can be expressed as

$$V_{A1OP} = G(V_{A1HI} - V_{A1LO}) + V_{A1CM} \qquad \text{Eq. 9.2.15}$$

For the AD600, G is accurately controlled from X1 to X100 while for the AD602 the specified range is X0.316 to X31.6.

The peak output voltage into resistive loads greater than 500 Ω, such as a flash A/D converter, is specified as ±3 V when using the recommended ±5 V supplies. For a 200 Ω load, an output of ±1.5V can be supported while still meeting the distortion specifications. Even lower load resistances can be driven if an external pull-down resistor is added between the output and the negative supply; for example, a 1 kΩ resistor would provide an extra current of 5 mA. Considerable load current can occur at high frequencies when the load is purely capacitive; in these cases, a small series resistor (5 to 50 Ω) will improve the overall stability, often with little loss of bandwidth. In most cases, the output will be AC-coupled to the load.

The gain is controlled by the voltage V_G applied to the fully-differential pins C1HI and C1LO, which exhibit an input resistance of about 15 MΩ in shunt with 2 pF. This high resistance makes it an easy matter to control a large number of X-AMPs operating in parallel, as in the ultrasound application. Thus,

$$V_G = V_{C1HI} - V_{C1LO} \qquad \text{Eq. 9.2.16}$$

and has a maximum specified range of ±625 mV.

The decibel gain is simply

$$G_{dB} = 32\,V_G + 20 \quad \text{for the AD600} \qquad \text{Eq. 9.2.17}$$

or

$$G_{dB} = 32\,V_G + 10 \quad \text{for the AD602} \qquad \text{Eq. 9.2.18}$$

where V_G is in Volts.

The differential gain-control interface allows a variety of control schemes to be employed. In the simplest example, the gain can be made to either increase or decrease with a positive voltage, depending on whether C1HI or C1LO is connected to the control voltage. Because these inputs are essentially non-loading, it is a simple matter to provide an offset voltage to shift the control voltage to a particular range, using a resistor network across the supply. Thus, if the control input is connected to C1HI, while C1LO is offset to +625 mV, the control range now runs from 0 to +1.25 V.

If A1 and A2 are used in cascade and the same gain voltage is applied to both control interfaces in simple parallel, the gain factor is doubled to 64 dB/V, because the gains of both amplifiers vary simultaneously. However, if one of the control interfaces is offset by the appropriate

voltage we can arrange for the gain of A1 and A2 to vary sequentially, which keeps the scaling at 32 dB/V but now requires 2.5 V for the full 80 dB range, conveniently supplied by an inexpensive 8-bit DAC, such as the AD558. An example is shown in the next section.

The AD600 and AD602 also provide a TTL-compatible gating feature. When the pin GAT1 (or GAT2) is HI, the channel is shut down, and the output is set to within a few millivolts of the voltage on A1CM (or A2CM) with an attendant large reduction in output noise. This feature is useful in multi-channel synthetic-aperture or beam-forming systems, where channels having a weighting below some threshold can be switched off and their noise contribution to the summed signal thus minimized.

The gain-control range of the last circuit can be extended to 100 dB by using a further VCA section. Fully–tested implementations are shown later; in both, precise gain offsets are used to achieve either (1) a very high gain linearity of ±0.1 dB over the full 100 dB range, or (2) the optimal signal-to-noise ratio at any gain.

9.2.5 A LOW-NOISE AGC AMPLIFIER

Figure 9.2.24 provides an example of the ease with which the AD600 can be connected as an AGC amplifier. A1 and A2 are cascaded, with 6 dB of attenuation introduced by the 100 Ω resistor R1, while a time- constant of 5 ns is formed by C1 and the 50 Ω of net resistance at the input of A2. This introduces a single-pole low-pass filter at about 32 MHz,to ensure stability at maximum gain It also lowers the overall gain range to -6dB to 74dB. C4 blocks the small DC offset voltage at the output of A1 (which might otherwise saturate A2 at its maximum gain) and introduces a high-pass corner at about 8 kHz, eliminating low-frequency noise and spurious signals which may be present at the input.

A half-wave detector is used, based on Q1 and R2. The current into capacitor C2 is just the difference between the current provided by the AD590 (300 μA at 300 K, 27 °C) and the collector current of Q1. In turn, the control voltage V_G is the time-integral of this *error* current. In order for V_G (and thus the gain) to remain stable, the rectified current in Q1 must, on average, exactly balance the current in the AD590. If the output of A2 is too small to do this, V_G will ramp up, causing the gain to increase, until Q1 conducts sufficiently.

First consider the particular case where *R2 is zero* and the output voltage V_{OUT} is a squarewave at, say, 100 kHz, that is, well above the corner frequency of the control loop. During the time V_{OUT} is negative, Q1 conducts; when V_{OUT} is positive, it is cut off. Since the *average* collector current is forced to be 300 μA, and the squarewave has a duty-cycle of 1:1, the current when conducting must be 600 μA. With R2 omitted, the peak value of V_{OUT} is forced to be just the V_{BE} of Q1 at 600 μA, typically about 700 mV, or $2V_{BE}$ peak-to-peak. This voltage, hence the amplitude at which the output stabilizes, has a strong negative temperature coefficient (TC), typically –1.7 mV/°C. While this may not be troublesome in some applications, the addition of R2 will render the output stable with temperature.

A SIMPLE BUT ACCURATE AGC AMPLIFIER

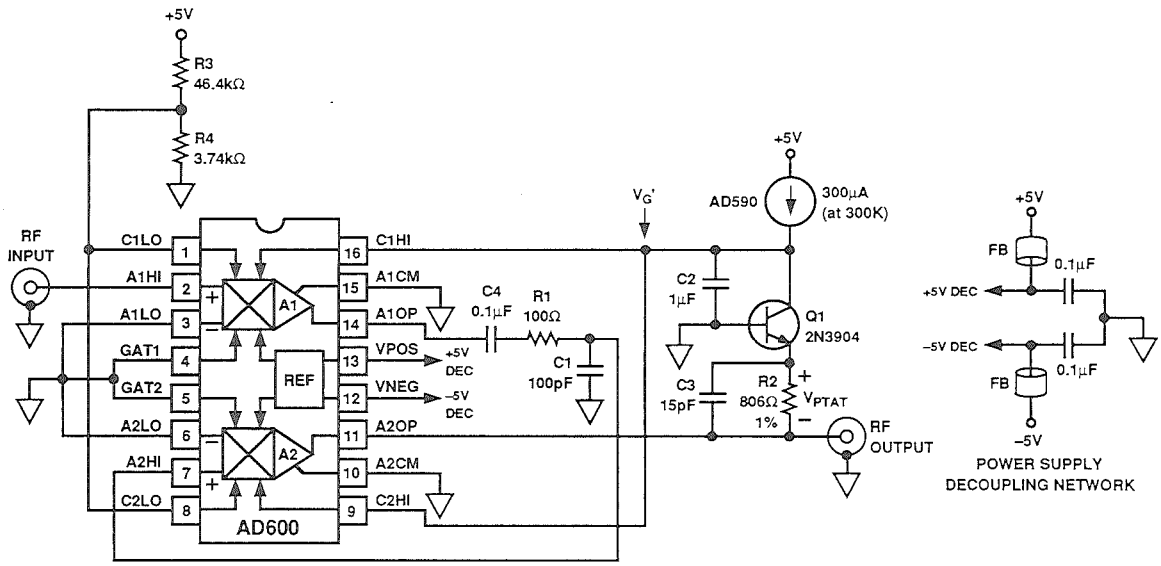


Figure 9.2.24

To understand this, first note that the current in the AD590 is proportional to absolute temperature (PTAT). (The AD590 is a temperature-dependent current source with a 1 μA/K temperature coefficient. At T = 300 K, its output is 300 μA.) For the moment, continue to assume that the signal is a squarewave. When Q1 is conducting, V_{OUT} is now the *sum* of V_{BE} and a voltage which is PTAT and which can be chosen to have an equal but opposite TC to that of the V_{BE}. This is actually nothing more than an application of the "bandgap voltage reference" principle. When R2 is chosen such that the sum of the voltage across it and the V_{BE} of Q1 is close to the bandgap voltage of about 1.2 V, V_{OUT} will be stable over a wide range of temperatures, provided, of course, that Q1 and the AD590 share the same thermal environment.

Since the average emitter current is 600 μA during each half-cycle of the squarewave a resistor of 833 Ω would add a PTAT voltage of 500 mV at 300 K, increasing by 1.66 mV/°C. In practice, the optimum value will depend on the type of transistor used, and, to a lesser extent, on the waveform for which the temperature stability is to be optimized; for the inexpensive 2N3904 and sinewave signals, the recommended value is 806 Ω. This resistor also serves to lower the peak current in Q1 when more typical signals (usually, sinusoidal) are involved, and the 200-Hz LP filter it forms with C2 helps to minimize distortion due to ripple in V_G. Note that the output amplitude under sinewave conditions will be higher than for a squarewave, since the average value of the current *for an ideal rectifier* would be 0.637 times as large, causing the output

amplitude to be 1.88 (=1.2/0.637) V, or 1.33 V RMS. In practice, the somewhat non-ideal rectifier results in the sinewave output being regulated to about 1.275 V RMS.

An offset of +375 mV is applied to the inverting gain-control inputs C1LO and C2LO. Thus the nominal –625 mV to +625 mV range for V_G is translated upwards (at the node labeled V_G') to –0.25 V for minimum gain to +1 V for maximum gain. This prevents Q1 from going into heavy saturation at low gains and leaves sufficient "headroom" of 4 V for the AD590 to operate correctly at high gains when using a +5V supply.

In fact, the 6 dB interstage attenuator means that the overall gain of this AGC system actually runs from –6 dB to +74 dB. Thus, an input of 2 V RMS would be required to produce a 1 V RMS output at the minimum gain, which exceeds the 1 V RMS maximum input specification of the AD600. The *available* gain range is therefore 0 to 74 dB (or, X1 to X5000). Since the gain scaling is 15.625 mV/dB (because of the cascaded stages) the minimum value of V_G' is actually increased by 6 X 15.625 mV, or about 94 mV, to –156 mV, so the risk of saturation in Q1 is further reduced.

The emitter circuit of Q1 is somewhat inductive (due its finite f_t and base resistance). Consequently, the effective value of R2 increases with frequency. This would result in an increase in the stabilized output amplitude at high frequencies, but for the addition of C3, determined experimentally to be 15 pF for the 2N3904 for maximum response flatness. Alternatively, a faster transistor can be used here to reduce HF peaking. Figure 9.2.25 shows the AC response at the stabilized output level of about 1.3 V RMS. Figure 9.2.26 demonstrates the output stabilization for sinewave inputs of 1 mV to 1V RMS at frequencies of 100 kHz, 1 MHz and 10 MHz.

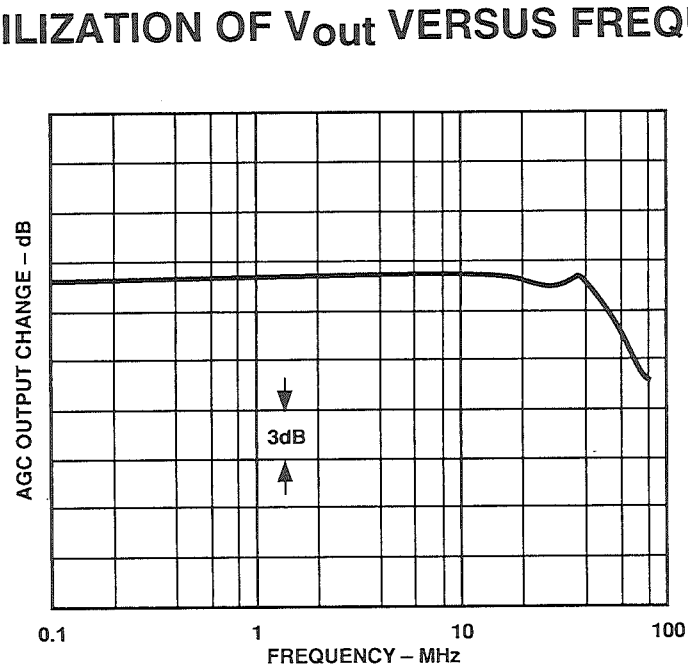


Figure 9.2.25

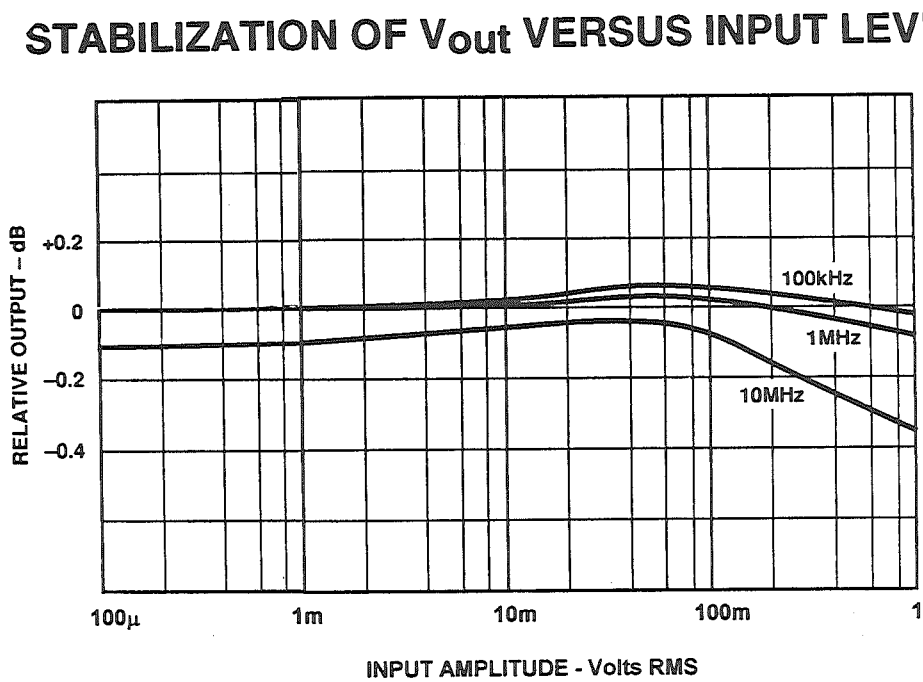


Figure 9.2.26

While the "bandgap" principle used here sets the output amplitude to 1.2 V (for the squarewave case), the stabilization point can be set to any higher amplitude, up to the maximum output of $\pm(V_S - 2)$ V which the AD600 can support. It is only necessary to split R2 into two components of appropriate ratio whose parallel sum remains close to the zero-TC value of 806 Ω. For example, using R2a = 1.62 kΩ from the emitter of Q1 to V_{OUT} and R2b = 1.62 kΩ from the emitter node to ground, the output can be raised to 2 V RMS for sinewave signals, without altering the temperature stability.

9.2.7 AN 80 dB RMS-LINEAR-dB MEASUREMENT SYSTEM

Monolithic RMS-DC converters provide an inexpensive means to measure the RMS value of a signal of arbitrary waveform. They also may provide a low-accuracy logarithmic ("decibel-scaled") output. However, they have a fairly small dynamic range – typically only 50 dB. More troublesome is that the bandwidth is roughly proportional to the signal level; for example, the AD636 provides a 3 dB bandwidth of 900 kHz for an input of 100 mV RMS, but only a 100kHz bandwidth for an input of 10 mV RMS. Its "raw" logarithmic output is unbuffered, uncalibrated and not stable over temperature requiring considerable support circuitry, including at least two adjustments and a special high-TC resistor.

All of these problems can be eliminated using an AD636 as *merely the detector element* in an AGC loop, in which the difference between the RMS output of the amplifier and a fixed DC reference are nulled in a loop integrator. The dynamic range and the accuracy with which the signal can be determined are now entirely dependent on the amplifier used in the AGC system. Since the input to the RMS-DC converter is forced to a constant amplitude, close to its maximum input capability, the bandwidth is no longer signal-dependent. If the amplifier has an exactly-exponential ("linear-dB") gain-control law its control voltage is forced by the AGC loop to have the general form

$$V_{LOG} = V_S \; lgt \; \frac{V_{IN\,(RMS)}}{V_Z} \qquad \text{Eq. 9.2.19}$$

where V_S is the logarithmic slope and V_Z is the logarithmic intercept, that is, the value of V_{IN} for which V_{LOG} is zero. (Compare this with Equation 9.3.1 in the section to follow on logarithmic amplifiers).

Figure 9.2.27 shows a practical wide-dynamic-range RMS-responding measurement system using the AD600. It can handle inputs of from 100 µV to 1 V RMS with a constant measurement bandwidth of 20 Hz to 2 MHz, limited primarily by the AD636 RMS converter. Its logarithmic output is a loadable voltage, accurately-calibrated to 100 mV/dB, or 2V per decade, which simplifies the interpretation of the reading when using a DVM, and is arranged to be –4 V for an input of 100 µV RMS input, zero for 10 mV, and +4 V for a 1V RMS input. In terms of Eq. 9.2.19, V_S is 2 V and V_Z is 10 mV.

A COMPLETE 80dB RMS-LINEAR-dB MEASUREMENT SYSTEM

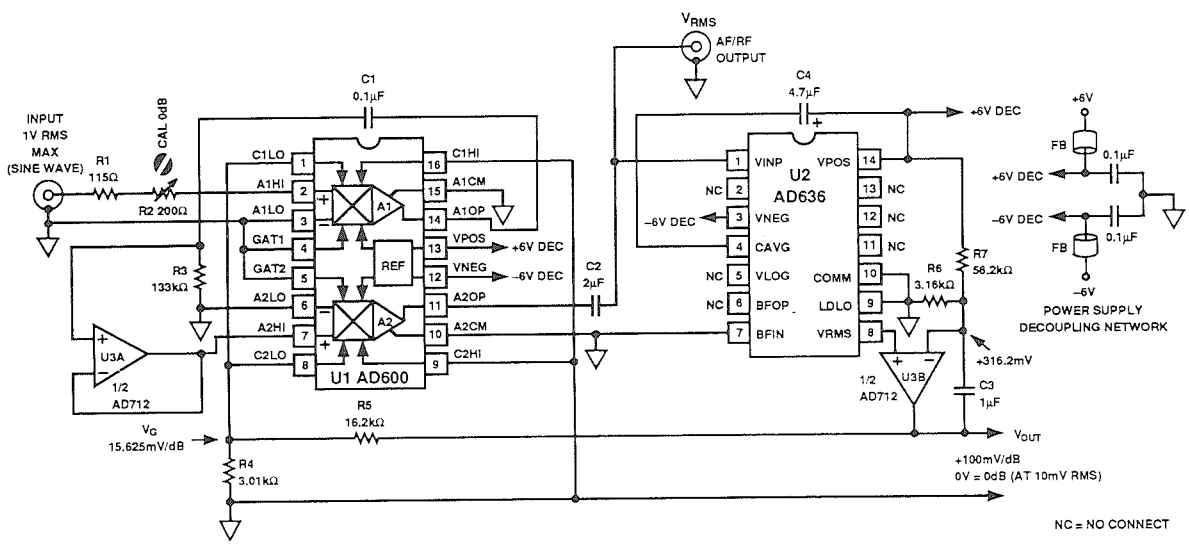


Figure 9.2.27

Note that the peak "log-output" of ±4 V requires the use of ±6 V supplies for the dual op-amp U3 (AD712) although lower supplies would suffice for the AD600 and AD636. If only ±5 V supplies are available it will be either necessary to use a reduced value for V_S (say, 1 V, in which case the peak output would be only ±2 V) or restrict the dynamic range of the signal to about 60 dB.

As in the previous case, the two amplifiers of the AD600 are used in cascade. However, the 6 dB attenuator and low-pass filter found in Figure 9.2.24 are replaced by a unity-gain buffer amplifier U3A, whose modest bandwidth eliminates the risk of instability at the highest gains. The buffer also allows the use of a high-impedance coupling network (C1/R3) which introduces a high-pass corner at about 12 Hz. An input attenuator of 10 dB (X 0.316) is now provided by R1 + R2 operating in conjunction with the AD600's input resistance of 100 Ω. The adjustment provides exact calibration of V_Z in critical applications, but R1 and R2 may be replaced by a fixed resistor of 215 Ω if very close calibration is not needed, since the input resistance of the AD600 (and all other key parameters of it and the AD636) are already laser-trimmed for accurate operation. This attenuator allows inputs as large as ±4 V to be accepted, that is, signals with an RMS value of 1 V combined with a crest-factor of up to 4.

The output of A2 is AC-coupled via another 12 Hz high-pass filter formed by C2 and the 6.7 kΩ input resistance of the AD636. The averaging time-constant for the RMS-DC converter is determined by C4. The unbuffered output of the AD636 (at pin 8) is compared with a fixed voltage of +316 mV set by the positive supply voltage of +6 V and resistors R6 and R7. (V_Z is proportional to this voltage and systems requiring greater calibration accuracy should replace the supply-dependent reference with a more stable source. However, V_S is independent of the supply voltages, being determined by the on-chip band-gap reference in the X-AMP.) Any difference in these voltages is integrated by the op-amp U3B, with a time-constant of 3 ms formed by the parallel sum of R6/R7 and C3.

Now, if the gain of the AD600 is too high, V_{OUT} will be greater than the "set-point" of 316 mV, causing the output of U3B – that is, V_{LOG} – to ramp up (note that the integrator is non-inverting). A fraction of V_{LOG} is connected to the *inverting* gain-control inputs of the AD600, so causing the gain to be reduced, as required, until V_{OUT} is exactly equal to 316 mV (DC), at which time the AC voltage at the output of A2 is forced to be exactly 316 mV (RMS). This fraction is set by R4 and R5 such that a 15.625 mV change in the control voltages of A1 and A2 – which would change the gain of the two cascaded amplifiers by 1 dB – requires a change of 100mV at V_{LOG}. Notice here that since A2 is forced to operate at an output level well below its capacity, waveforms of high crest-factor can be tolerated throughout the amplifier.

To verify the operation, assume an input of 10 mV RMS is applied to the input, which results in a voltage of 3.16 mV RMS at the input to A1, due to the 10 dB loss in the attenuator. If the system performs as claimed, V_{LOG} (and hence V_G) should be zero. This being the case, the gain of both A1 and A2 will be 20 dB and the output of the AD600 will therefore be 100 times (40dB) greater than its input, which evaluates to 316 mV RMS. This is the input required at the AD636 to balance the loop, confirming the basic operation. Note that unlike most AGC circuits,

(which often have a high temperature-coefficient of gain due to the internal "kT/q" scaling – see Eq. 9.2.1) these voltages, and thus the output, of this measurement system is very stable over temperature. This behavior arises directly from the fundamental and exact exponential calibration of the ladder attenuator.

Typical results are presented for a sinewave input at 100 kHz. Figure 9.2.28 shows that the output is held very close to the set-point of 316 mV RMS over an input range in excess of 80dB.

Figure 9.2.29 shows the "decibel" output voltage, V_{LOG}, and Figure 9.2.30 shows that the *deviation* from the ideal output predicted by Eq. 9.2.19 is within ±1 dB for the 80 dB range from 80 μV to 800 mV.

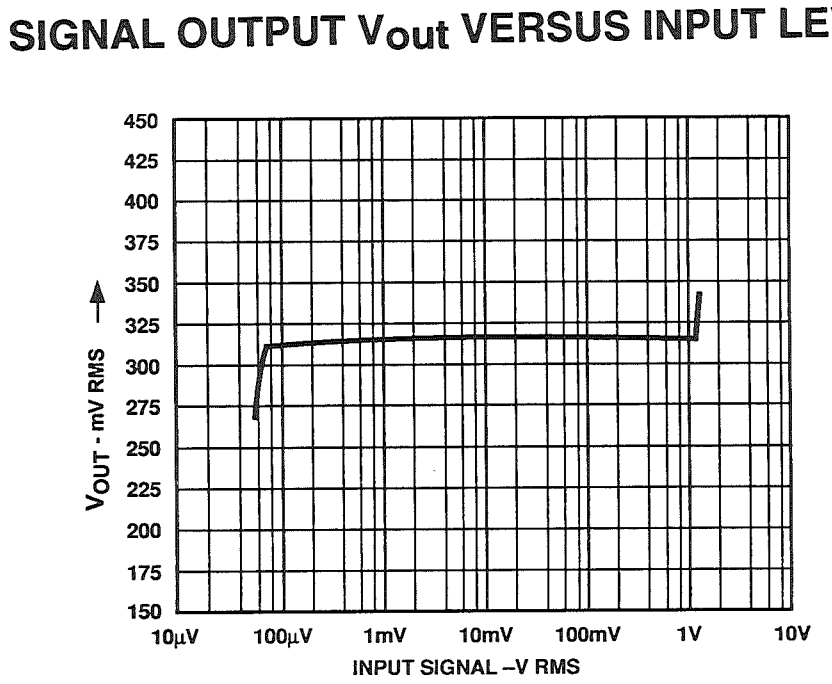


Figure 9.2.28

THE LOGARITHMIC OUTPUT V_{LOG} VERSUS INPUT LEVEL

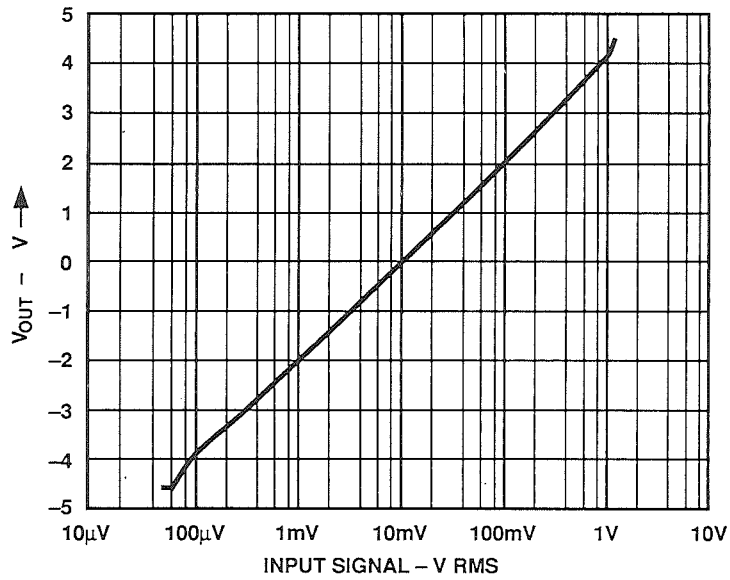


Figure 9.2.29

DEVIATION FROM THE IDEAL LOGARITHMIC OUTPUT

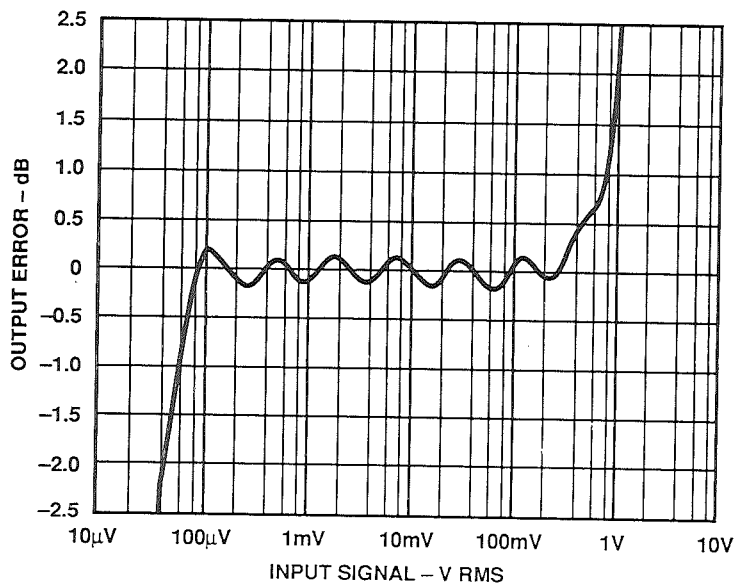


Figure 9.2.30

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By suitable choice of the input attenuator R1+R2, this could be centered to cover any range from 25 μV to 250 mV to, say, 1 mV to 10 V, with appropriate correction to the value of V_Z. (Note that V_S is not affected by the changes in the range). The gain ripple of ±0.2 dB seen in this curve is the result of the finite interpolation error of the X-AMP. Note that it occurs with a periodicity of 12 dB – twice the separation between the tap points in each amplifier section.

This ripple can be canceled whenever the X-AMP stages are cascaded by introducing a 3 dB offset between the two pairs of control voltages. A simple means to achieve this is shown in Figure 9.2.31: the voltages at C1HI and C2HI are "split" by ±46.875 mV, or ±1.5 dB. Alternatively, either one of these pins can be individually offset by 3 dB and a 1.5 dB gain adjustment made at the input attenuator (R1+R2). The error curve shown in Figure 9.2.32 demonstrates that over the central portion of the range the output voltage can be maintained very close to the ideal value. The penalty for this modification is the higher errors at the extremities of the range.

METHOD FOR CANCELING THE GAIN-CONTROL RIPPLE

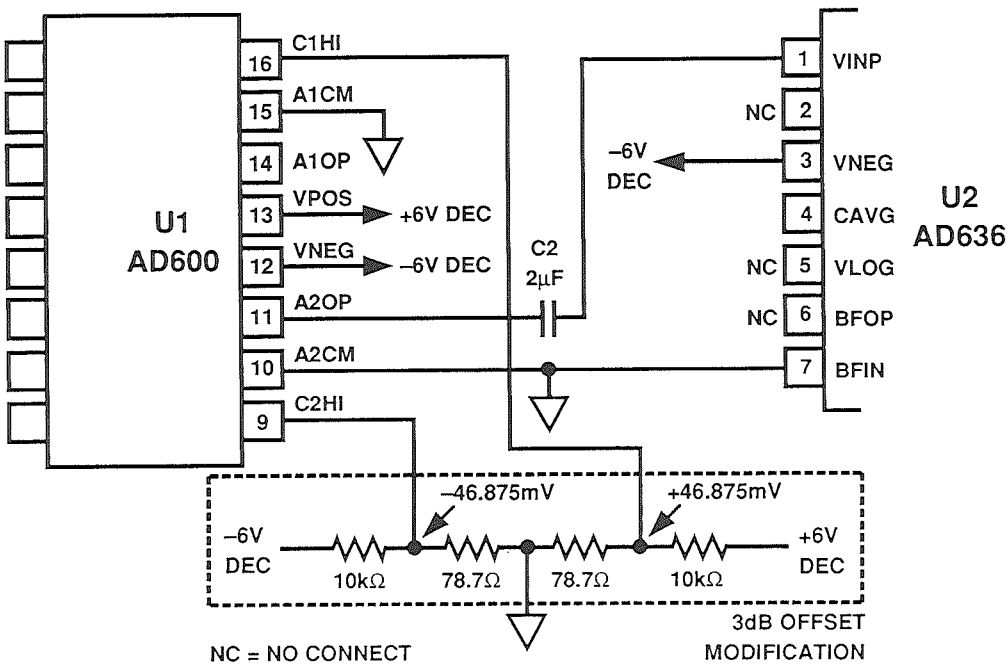

Figure 9.2.31

LOGARITHMIC ERROR USING THE PREVIOUS CIRCUIT MODIFICATION

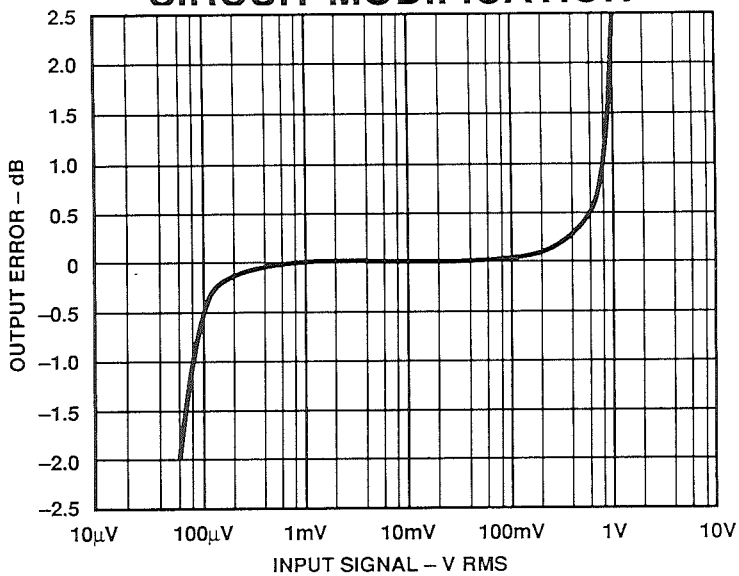

Figure 9.2.32

9.2.8 100 dB RMS/AGC SYSTEM WITH MINIMAL GAIN ERROR

Using three VCA sections, the measurement or AGC range can be extended still further. Figure 9.2.33 shows an RMS-responding AGC circuit which accepts inputs of 10 µV to 1 V RMS (–100dBV to 0 dBV) with generous over-range.

RMS/AGC SYSTEM WITH 100dB RANGE AND MINIMUM ERROR IN V_{LOG}

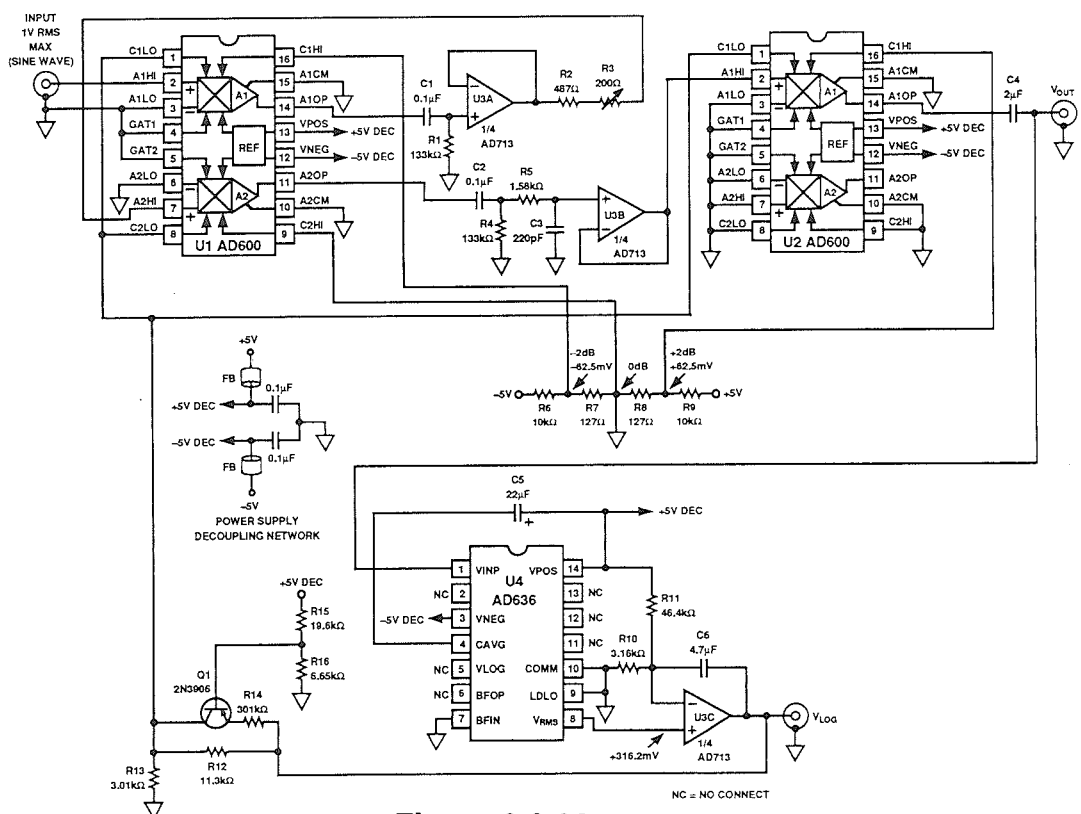

Figure 9.2.33

Figure 9.2.34 shows the measured AC output at V_{OUT}; the amplitude is linear within ±0.2 dB over the full input range. Figure 9.2.34 shows the measured logarithmic output, V_{LOG}, which is accurately-scaled 1 V per decade with an intercept (V_{LOG} = 0) at 3.16 mV RMS (–50 dBV). Gain offsets of –2 dB and +2 dB are provided by the ±62.5 mV introduced by R6–R9. These offsets eliminate the small gain ripple which arises in the X-AMP from its finite interpolation error, and has a period of 18 dB for the three cascaded VCA sections.

The gain ripple *without* this offset (in which case the gain errors simply add) is shown in Figure 9.2.35; it is still a remarkably low ±0.25 dB over the 108 dB range from 6 µV to 1.5 V RMS. With the gain offsets connected, the gain linearity remains under ±0.1 dB over the specified 100 dB range, as shown in Figure 9.2.36.

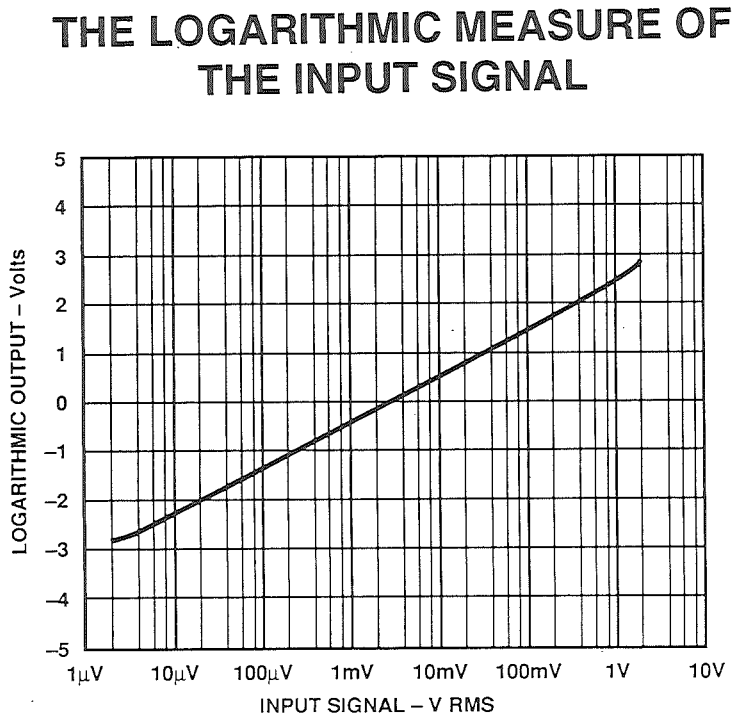

Figure 9.2.34

THE ABSOLUTE ERROR IN V_{LOG} WITHOUT RIPPLE CANCELLATION

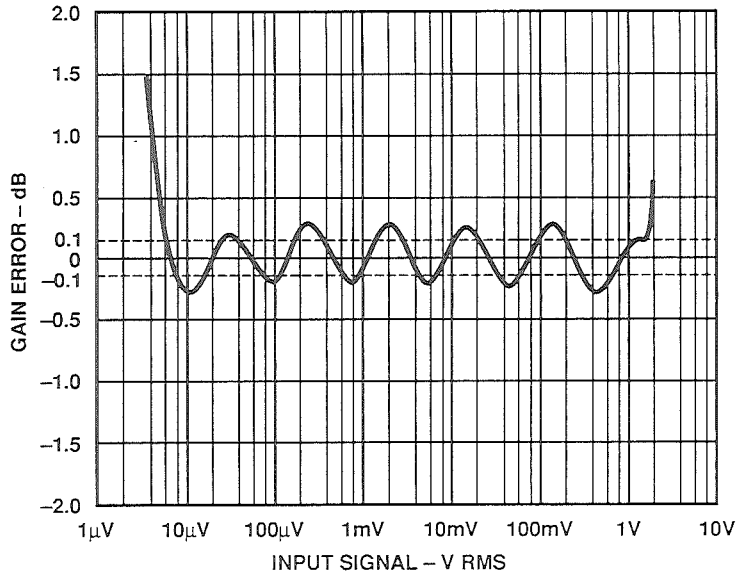

Figure 9.2.35

THE ABSOLUTE ERROR IN V_{LOG} WITH RIPPLE CANCELLATION

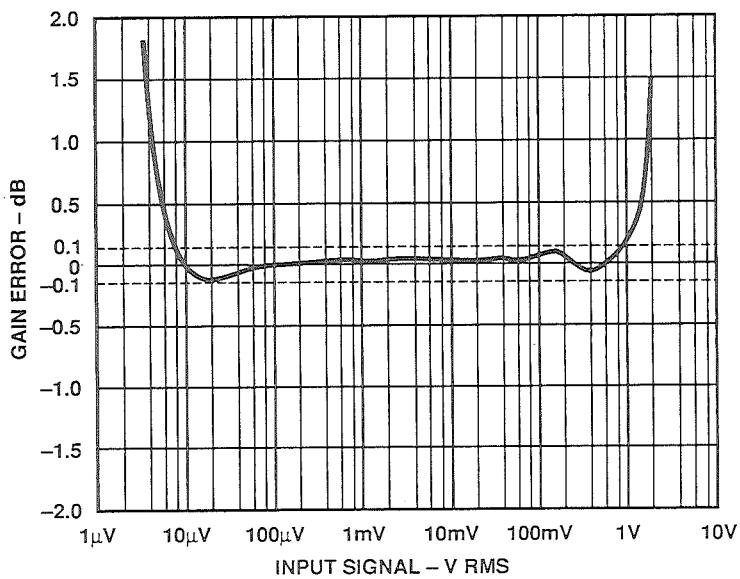

Figure 9.2.36

The maximum gain of the three cascaded amplifiers is 120 dB (one million). If no filtering were used, the noise-spectral-density of the first VCA (1.4 nV/√Hz), which amounts to an input-referred noise of 8.28 μV RMS in the full bandwidth (35 MHz), would amount to over 20 V pk-pk at the output (if the AD600 could generate that large of an output). Consequently, some reduction of bandwidth is mandatory, and in the circuit of Figure 9.2.33 this is provided by a single-pole low-pass filter R5/C3, which has a corner frequency of 458 kHz. This reduces the output noise to about 100 mV at a gain of 100 dB. Of course, the bandwidth (and hence output noise) could be easily reduced further, for example, in audio applications, merely by increasing C3.

The AD600 provides a DC-coupled signal path, but even minuscule offset voltages at the input would overload the output at high gains, so high-pass filtering is also needed. This is provided by R1/C1 and R4/C2; the corner frequency of both of these networks is at 12 Hz, providing operation down to sub-audio frequencies. Op-amp sections U3A and U3B (AD713) provide impedance buffering, since the input resistance of the AD600 is only 100 Ω. A further high-pass section at 12 Hz is provided by C4 and the 6.7 kΩ input resistance of the AD636 RMS converter.

The RMS value of V_{LOG} is generated at pin 8 of the AD636; the averaging time for this process is determined by C5, and the value shown results in less than 1 % RMS error at 20 Hz. The slowly-varying V_{RMS} is compared with a fixed DC reference of 316 mV, derived from the positive supply by R10/R11. Any difference between these two voltages is integrated in C6, in conjunction with op-amp U3C, the output of which is V_{LOG}. A fraction of this voltage, determined by R12 and R13, is returned to the gain-control inputs of all AD600 sections. An increase in V_{LOG} lowers the gain, because this voltage is connected to the *inverting-polarity* control inputs.

Now, since the gains of all three VCA sections are being varied simultaneously, the scaling is not 32 dB/V but 96 dB/V, or 10.42 mV/dB. The fraction of V_{LOG} required to set its scaling to 50 mV/dB is therefore 10.42/50, or 0.208. The resulting full-scale range of V_{LOG} is nominally ±2.5 V. This scaling was chosen to allow the circuit to operate from ±5V supplies. Optionally, the scaling could be altered to 100 mV/dB, which would be more easily interpreted when V_{LOG} is displayed on a DVM, by increasing R12 to 25.5 kΩ. The full-scale output of ±5V then requires the use of supply voltages of at least ±7.5 V; note that any changes to the supply voltages require an adjustment to the value of R11 if V_{OUT} is to remain 316 mV RMS.

A simple adjustable attenuator of 16.6 ± 1.25 dB is formed by R2/R3 and the 100 Ω input resistance of the AD600. This allows the reference level of the decibel output to be precisely set to zero for an input of 3.16 mV RMS, and thus center the 100 dB range between 10 μV and 1 V. In many applications R2/R3 may be replaced by a fixed resistor of 590 Ω. For example, in AGC applications, neither the slope nor the intercept of the logarithmic output is important.

A few additional components are added (R14–R16 and Q1) to improve the accuracy of V_{LOG} at the top end of the signal range (that is, for small gains). The gain starts rolling off when the

input to the first amplifier, U1A, reaches 0 dB. To compensate for this nonlinearity, Q1 turns on when V_{LOG} is approximately +1.5 V and increases the feedback to the control inputs of the AD600s, thereby needing a smaller voltage at V_{LOG} to maintain the input to the AD636 at the set-point of 316 mV RMS.

9.2.9 120 dB RMS/AGC SYSTEM WITH OPTIMAL S/N RATIO

In the last case, all gains were adjusted *simultaneously*, resulting in an output S/N ratio that is always less than optimal. The use of *sequential* gain-control results in a major improvement in S/N ratio, with only a slight penalty in the accuracy of V_{LOG}, and no penalty at all in the stabilization accuracy of V_{OUT}. The idea is simply to increase the gain of the three VCA sections one at a time as the signal level decreases, beginning with the first stage. Thus, the highest possible S/N ratio is maintained throughout the amplifier chain. This can be easily achieved with the AD600 because its gain remains accurate even when the control input is overdriven; that is, each gain-control "window" of 1.25 V is used fully before moving to the next amplifier to the right.

Figure 9.2.37 shows the circuit for the sequential control scheme which is only slightly changed from Figure 9.2.33. R6–R9 with R16 provide offsets of 42.14 dB between the individual amplifiers to ensure smooth transitions between the gain of each successive X-AMP, with the sequence of gain increase being U1A first, then U1B and lastly U2A.

RMS/AGC SYSTEM WITH 120dB RANGE AND OPTIMAL S/N RATIO PROFILE

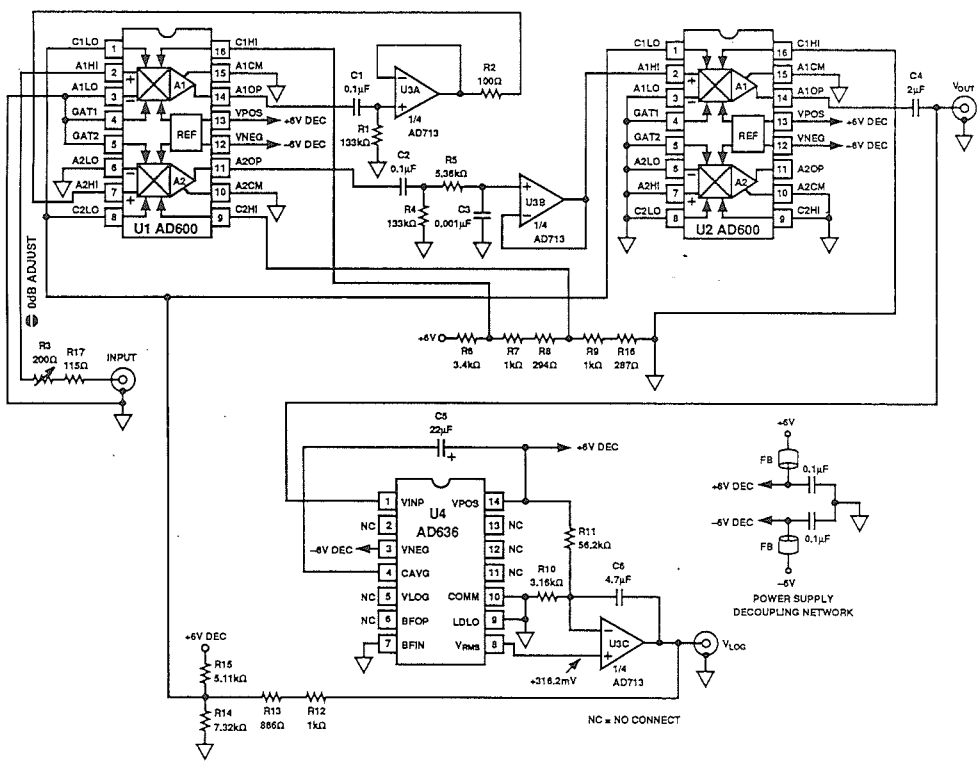

Figure 9.2.37

The precise value of the offset voltages is critical if maximum accuracy is to be maintained.. The adjustable attenuator provided by R3+R17 and the 100 Ω input resistance of U1A, plus the fixed 6dB attenuator provided by R2 and the input resistance of U1B, are included to set V_{LOG} to read 0 dB when V_{IN} is.3.16 mV RMS (–50 dBV) and thus center the 100 dB range between 10 μV and 1 V. R5 and C3 provide a 3 dB bandwidth of 30 kHz. R12–R15 change the scaling from 625 mV/decade at the AD600 gain-control inputs to the more convenient 1 V/decade at the logarithmic output. The increased range of the control voltage (compared to the previous circuit) requires the use of ±6 V supplies. Figure 9.2.38 shows V_{LOG} to be essentially linear over a full 120 dB range.

Figure 9.2.39 shows that the composite error ripple due to the individual gain functions is within ±0.2 dB (dotted lines) from 6 μV to 2 V. The small perturbations at about 200 μV and 20 mV, caused by the impracticality of matching the gain functions perfectly, are the only sign that the gains are now sequential. V_{OUT} remains within less than 1 mV of its set-point value of 316 mV RMS (that is, –10 dBV) for all input levels.

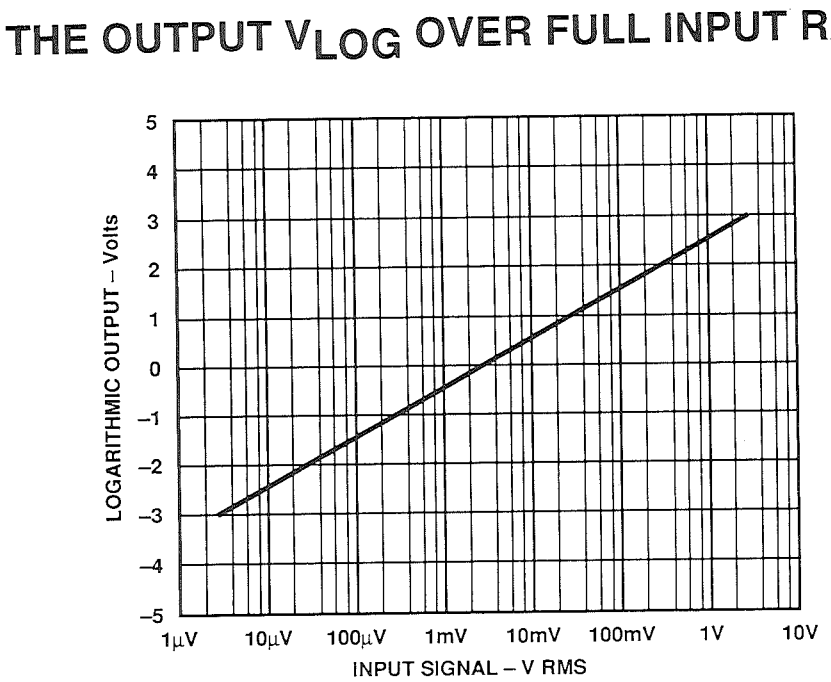

Figure 9.2.38

THE ERROR IN THE LOGARITHMIC OUTPUT V_{LOG}

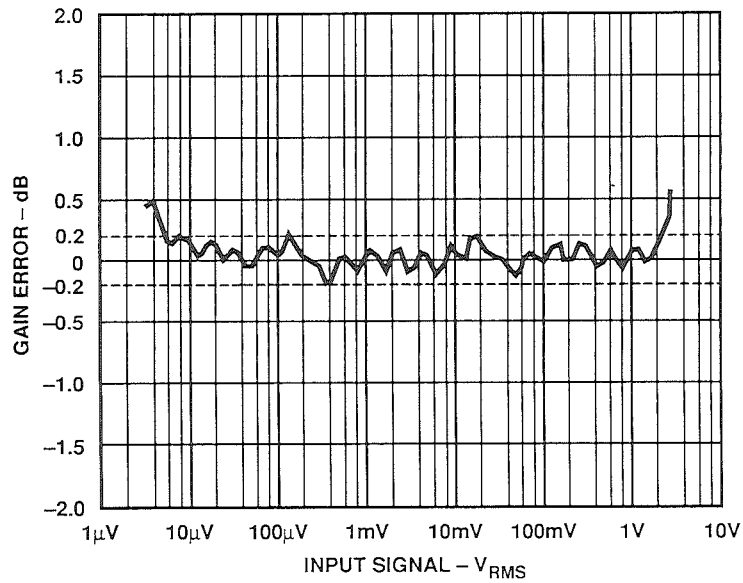

Figure 9.2.39

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To more directly compare the signal-to-noise performance in the "simultaneous" and "sequential" modes of operation, all interstage attenuation was eliminated (R2 and R3 in Figure 9.2.33; R2 in Figure 9.2.37), the input of U1A was shorted, R5 was selected to provide a 3 dB bandwidth of 20 kHz (R5 = 7.87 kΩ), and the gain control voltage was varied, using an external source. The RMS value of the noise was then measured at V_{OUT} and expressed as an S/N ratio relative to 0 dBV, this being almost the maximum output capability of the AD600. Results for the simultaneous mode can be seen in Figure 9.2.40. The S/N ratio degrades uniformly as the gain is increased. Note that since the inverting gain control inputs C1LO and C2LO are used, the gain decreases for more positive values of the gain-control voltage.

THE OUTPUT S/N RATIO VERSUS GAIN FOR THE "SIMULTANEOUS" MODE

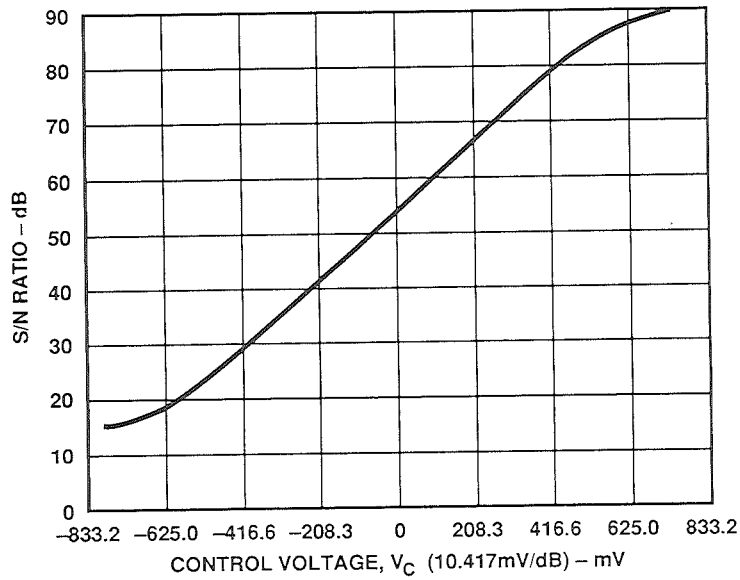

Figure 9.2.40

By contrast, the S/N ratio for the sequential mode is shown In Figure 9.2.41. In this case, U1A always acts as a fixed noise source; varying its gain has no effect on its output noise. (Recall that this is a feature of the X-AMP technique.) Thus, for the first 40 dB of control range (actually slightly more) when only this VCA section is having its gain varied, the S/N ratio remains constant. In this interval, the gains of U1B and U2A are at their minimum value of –1.07 dB. For the next 40 dB, the gain of U1A remains at its maximum value of 41.07 dB while only the gain of U1B is varied and that of U2A remains at its minimum value of –1.07 dB. In this interval, the fixed output noise of U1A is amplified by the increasing gain of U1B and the S/N ratio progressively worsens.

THE OUTPUT S/N RATIO VERSUS GAIN FOR THE "SEQUENTIAL" MODE

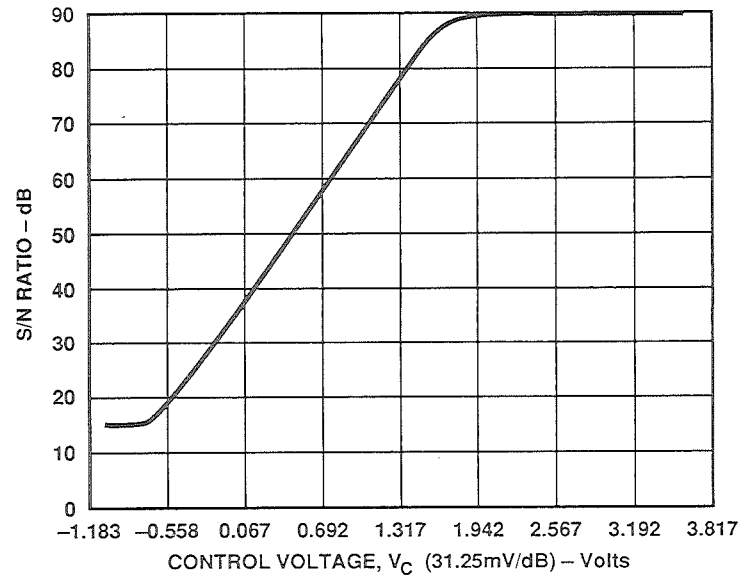

Figure 9.2.41

Once U1B reaches its maximum gain of 41.07 dB its output also becomes a gain-independent noise source. This noise is presented to U2A. As the control voltage is further increased, the gains of both U1A and U1B remain fixed at their maximum value while that of U2A varies from –1.07 dB to 41.07 dB and the S/N ratio continues to worsen, Figure 9.2.41 shows that the S/N ratio remains constant at 90 dB for the first 40 dB of gain range.

This arrangement of staggered gains can be easily implemented because when the control inputs of the AD600 are over-driven, the gain limits to its minimum or maximum value, without side-effects. This avoids the need for awkward nonlinear shaping circuits. It is the somewhat peculiar value of the gain in these over-driven states (–1.07 dB and 41.07 dB, not 0 dB and 40 dB) that explains the rather odd values needed for the offset voltages.

The optimization of the output S/N ratio is of obvious value in AGC systems. However, in applications where these circuits are considered for their wide-range logarithmic measurement capabilities, the inevitable degradation of S/N ratio at high gains need not seriously impair their utility. In fact, the bandwidth of the circuit shown in Figure 9.2.37 was specifically chosen so as to improve measurement accuracy, by using the system noise to alter the shape of the log-error curve at low signal levels.

9.2.10 AN ULTRA-LOW NOISE VCA

The two channels of an AD600 or AD602 may be operated in parallel to achieve a 3 dB improvement in noise level, providing 1 nV/√Hz without any loss of gain-accuracy or bandwidth. This is possible because the noise voltages of the two channels are, of course, uncorrelated.

In the simplest case, shown in Figure 9.2.42, the signal inputs A1HI and A2HI are tied directly together, the outputs A1OP and A2OP are summed via R1 and R2 (100 Ω each) and the control inputs C1HI/C2HI and C1LO/C2LO operate in parallel. Using these connections, both the input and output resistances are 50 Ω. Thus, when driven from a 50 Ω source and terminated in a 50 Ω load, the gain is reduced by 12 dB, so the gain range becomes –12 dB to 28 dB for the AD600 and –22 dB to 18 dB for the AD602. The peak input capability remains unaffected (1V RMS at the IC pins, or 2V RMS from an unloaded 50 Ω source). The loading on each channel, with a 50 Ω load, is effectively 200 Ω (because the load current is shared between the two channels) so the overall amplifier still meets its specified maximum output and distortion levels for a 200 Ω load. This amplifier can deliver a maximum sinewave power of +10 dBm to the load.

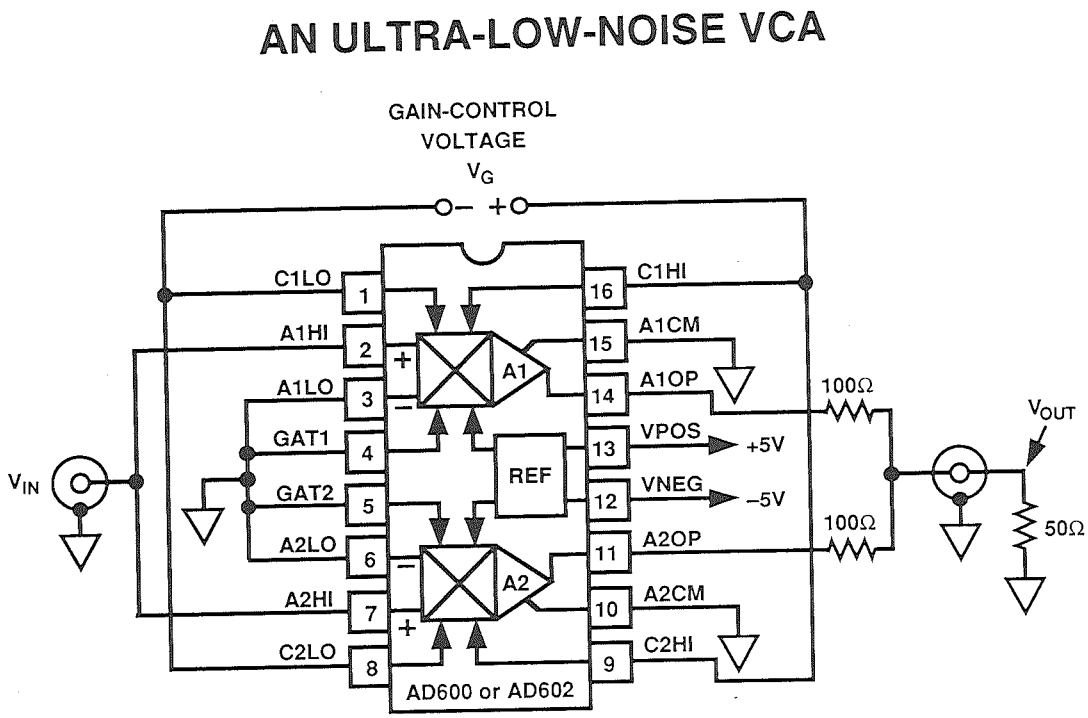

Figure 9.2.42

Figure 9.2.43 shows a couple of modifications. The outputs are now summed actively using the AD844 op-amp, resulting incidentally in a sign-reversal at the final output. Using the minimum feedback resistance of R3 = 806 Ω, the bandwidth is not impaired by the inclusion of this amplifier, and the overall gain may now be altered by R1 and R2. In the example shown, we have included a 50 Ω reverse-termination resistor, and have again assumed a 50 Ω source impedance, so the initial gain deficit is 12 dB. Thus, by using R1 = R2 = 402 Ω, the overall gain, from loaded 50 Ω source to a 50 Ω load, is restored to that of the AD600 or AD602 alone. Note, however, that using these values the AD844 may clip at full gain, unless it is provided with adequate supply voltages. Many useful variants of this arrangement can be devised, providing a near-universal low-noise 35 MHz variable-gain block.

AN ELABORATION OF FIGURE 9.2.42

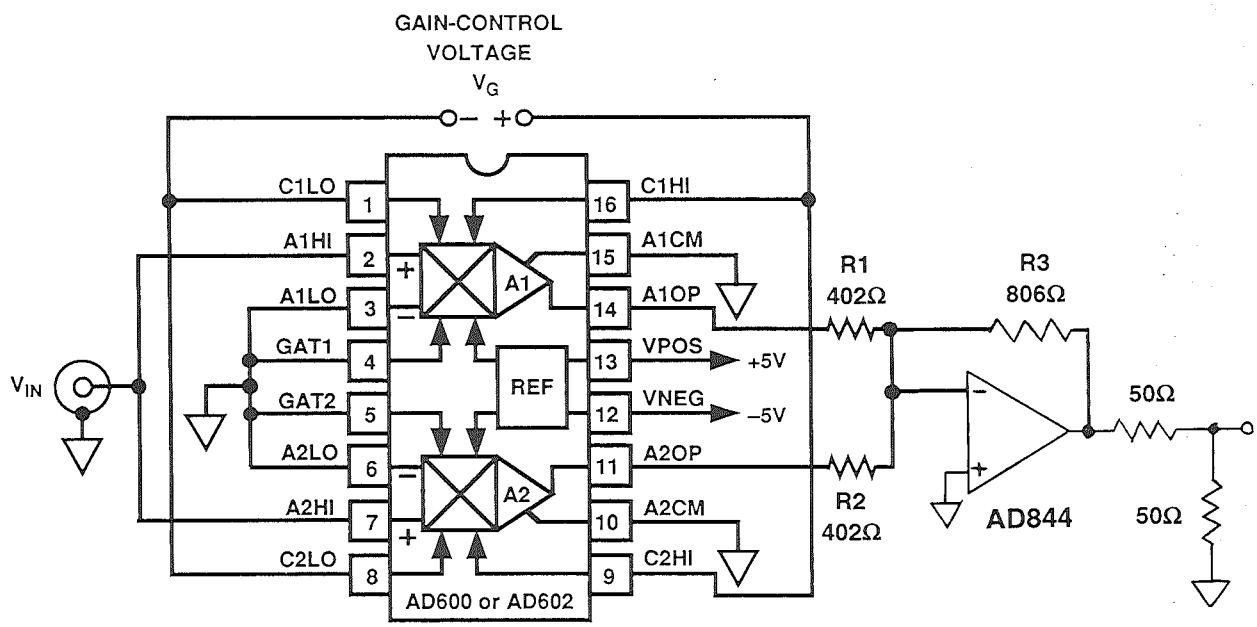

Figure 9.2.43

9.3 LOGARITHMIC AMPLIFIERS

Logarithmic amplifiers are used wherever a signal of large dynamic range must be compressed down to a signal of substantially smaller dynamic range, without the intervention of an AGC loop. The transfer function need not be logarithmic to achieve useful compression. However, the logarithmic function is valuable because it provides an output which changes by the same amount between application of any given ratio of input amplitudes, rendering the output easy to interpret. The scaling of might be 1 V/decade, in which case the output changes by 1 V for any ten-fold increase of the input.

Specifying logarithmic circuit performance requires care in defining terms. The literature abounds with poorly written explanations of fundamental issues, beginning with the naming of such devices. By calling these circuits "amplifiers" their nonlinear nature is in danger of being obscured. It is even unwise to view them as a special kind of amplifier. They may provide needed amplification (as in the case of Log Amps used in RF and IF strips) or *incidentally* exhibit small-signal gain under some conditions, but the true objective should be seen as implementing a precise mathematical transformation. This requires diligent attention to matters of scaling, without which the accuracy of the system will suffer.

Strictly speaking, these circuits ought to be called "logarithmic converters", but the name "logarithmic amplifier" or just "Log Amp" has become popular, and will probably always be used. Manufacturers of Log Amps who might wish to establish more exact terminology are obliged to bow to popular usage in naming them, or risk having the nature and utility of their products misunderstood. Accordingly, we use the term "Log Amp" in conformance with current usage.

9.3.1 CLASSIFICATION OF TYPES

Over the years, logarithmic amplifiers have accumulated a confusing assortment of terms, some quite misleading. We will attempt here to classify Log Amps into three broad groups (Figure 9.3.1), according to *structure* and *application domain*, and endeavor to be consistent in matters of terminology and nomenclature.

Translinear Log Amps provide a very wide dynamic range in response to a quasi-DC input, that is, one which is static or slowly varying. The design challenge here is to achieve excellent DC accuracy, with little emphasis on dynamic behavior. They are usually based on the *direct* invocation of the logarithmic (or "Translinear") properties of the bipolar transistor, explained later, and such Log Amps will be discussed in depth later. The widest dynamic range is achieved in this case when the input is in the form of a current. Practical translinear Log Amps can be designed to provide dynamic ranges approaching 180 dB. There are basic reasons why the dynamic behavior of such Log Amps is poor, as we shall see later, although the principle can be optimized for use at moderate (a few MHz) frequencies.

Baseband Log Amps, also known as "Video Log Amps" (although they are rarely used in video-display-related applications) respond to the *instantaneous* value of some rapidly-changing input (usually a voltage). This is often achieved using a technique which is best described as

"progressive compression", in which the logarithmic response can be approximated, to any arbitrary accuracy, through the use of cascaded amplifier stages having signal-dependent gain.

Most baseband Log Amps accept inputs having only one polarity and are usually DC-coupled. They are commonly used to compress pulse signals in which the "baseline" must be accurately preserved. When used *after* a microwave detector, (a backward diode), the combination is referred to as a "Detector-Log-Video-Amplifier", or DLVA. In these applications, the smallest input to the Log Amp may be only a few microvolts, calling for extremely low input offset voltages; this is sometimes achieved through some form of auto-nulling or DC restoration technique. Dynamic ranges of typical video Log Amps range from about 40 dB to 85 dB. DLVAs frequently include some deliberate deviation from a strictly-logarithmic response to first-order compensate for nonlinearities in a specific detector.

A special type of baseband Log Amp, called a *True Log Amp*, can accept inputs of *either polarity* and generate an output whose sign follows that of the input. Here, we are faced with typical misnomer, since a "true log" response would require the output to have a singularity of $\pm\infty$ as the input passes through zero, and anyway the log function has no simple meaning for negative arguments. In fact, the output of a practical amplifier of this type passes through zero when the input does, just as for any amplifier providing a bipolar response.

TYPES OF LOG AMPS

- Translinear Log Amps:
  - Based on Logarithmic (or translinear) Properties of Bipolar Transistors
  - Wide Dynamic Range, Poor ac Performance
- Baseband Log Amps:
  - Respond to Instantaneous Value of Rapidly Changing Input
  - "Progressive Compression" Technique Often Used
  - Sometimes Called "Video Log Amps"
  - "True Log Amp" Accepts Bipolar Inputs Sign of Output Follows Input
- Demodulating Log Amps:
  - AC Input Signal is Rectified
  - Output is the Modulated Envelope of the Input
  - Often Called "Successive Detection Log Amp"

Figure 9.3.1

Demodulating Log Amps rectify the AC signals applied to the input and use low-pass filtering to extract the running average – that is – a baseband signal corresponding to the modulated envelope of the input. In a similar fashion to the baseband Log Amp, multiple cascaded amplifier/limiter stages are used to realize this function, which is then called a "Successive Detection Log Amp" (sometimes abbreviated to SDLA). The signal frequency may be at the low megahertz to as high as several gigahertz. The low-frequency limit is invariably determined by AC-coupling components used to block DC bias and offset voltages from preceding gain stages and sometimes to reduce the effects of 1/f noise in the early stages. The resulting high-pass corner frequency is typically between a few tens of kilohertz and several megahertz.

In high-frequency Log Amps, the management of noise poses a major challenge. Bandpass filters are sometimes inserted between stages to limit the noise bandwidth. A bandpass response may also be desirable as part of the overall system function, for example, in the IF amplifier of a spectrum analyzer. However, the design of bandpass Log Amps needs care, since the scaling parameters, which define the logarithmic response, are now unavoidably frequency-dependent. Practical demodulating Log Amps provide dynamic ranges of from 40 dB to as high as 120 dB.

Although demodulating Log Amps were developed primarily for demanding military applications, there is no fundamental reason why they should be either expensive or incapable of operation down to low frequencies, for example, the audio range. One technique which we will discuss later is the use of DC-coupling throughout a monolithic chain of amplifier stages, augmented by a low-pass feedback network around the entire chain to effect a high-pass closed-loop response, whose corner frequency can be arbitrarily low. In fact, the continuous-time filter can be replaced by a sample/hold to correct for offset-induced errors on an occasional basis.

Demodulating Log Amps respond to a voltage input. Note that such amplifiers do *not* respond directly to input power, even though their input may be specified in these terms. In a fixed-impedance system any input voltage will correspond to a certain input power level, and a Log Amp *can be characterized* in terms of its output for this input. But it is important to realize that it is the input *voltage* that determines the output. For example, an RMS voltage of 223.6 mV represents a power of 1 mW when applied to a 50 Ω load, which is conventionally written 0dBm (meaning 0 dB relative to 1 mW). At this input level, a Log Amp would respond with some output, say 1 V. Now, if we were simply to alter the reference impedance at the input to 100 Ω, the input power would halve, but the Log Amp response would be unchanged.

While this classification has tried to avoid excessive mention of techniques, we need to briefly mention a special type of Log Amp, which may be of increasing importance as the integrated circuits needed to implement this approach become available. The key element is a *linear* amplifier whose gain may be controlled in a "direct-decibel" fashion, that is, whose gain is an exponential function of a control input, such as the X-AMP described in the previous section. In that section, we showed how an X-AMP may be used to implement demodulating logarithmic conversion, with the important property that the system may now be RMS-responding and independent of waveform.

9.3.2 SCALING OF LOG AMPS

Logarithmic circuits bring about a profound transformation of the signal, that goes far beyond "compression", and close attention to the details of the scaling of this function is necessary. The need for care in defining the Log Amp transfer function and its scaling parameters is not simply a matter of mathematical rigor. By viewing the device as a precision nonlinear element the designer is forced to think carefully about the source of these scaling voltages. If they cannot be defined with precision it is quite possible, even likely, that the circuit will not be stable with variations in supply voltage and temperature. Indeed, the main reason why commercially-available Log Amps have had such notoriously poor stability in the past is that in the traditional approach to their design was to view them first as amplifiers, second as having some kind of general compressive behavior, and only lastly being made to fit a logarithmic form to an acceptable level of accuracy.

We will therefore try to put the design of *all* types of Log Amps on a firm foundation, beginning with a clear formulation for the function. For all voltage-input, voltage-output logarithmic converters, this function *must* have the form

$$V_W = V_Y \, log\,(V_X / V_Z) \qquad \text{Eq. 9.3.1}$$

where V_W is the output, V_X is the primary signal input, which for now is assumed to be a varying DC voltage, V_Y is the slope voltage and V_Z is the intercept voltage, defined below. This formulation and terminology is consistent with that used in connection with other nonlinear circuits from Analog Devices, such as the multiplier family. Note in this connection that V_Y and V_Z are normally fixed voltages but can, in the most general case, also be signal inputs. The logarithm may be to any base, but in the context of practical Log Amps, whose input levels will often be expressed in decibels, base-ten logarithms are universally assumed. Changing the base of the logarithm in Eq 9.3.1 simply alters the effective value of V_Y. At this point, the function *log* means " logarithm to any base"; later, we will switch to *ln*, that is, natural (base-*e*) logarithms, in order to find certain integrals, and *lgt* will be used where we wish to specifically to refer to logarithms to base ten.

In general, V_W increases by an amount V_Y for each unit increase in the quantity $log(V_X / V_Z)$. When the logarithm is to base ten, that statement translates to "for each decade increase in V_X ", so in that case V_Y has the meaning of "Volts per decade". Figure 9.3.2 shows this function. The dotted regions correspond to those input levels for which the actual transfer function may be in error due to practical limitations. For example, at low input levels, noise and offset voltages will cause major errors, while at high input levels the finite signal-handling capability of the circuit will reach its limit.

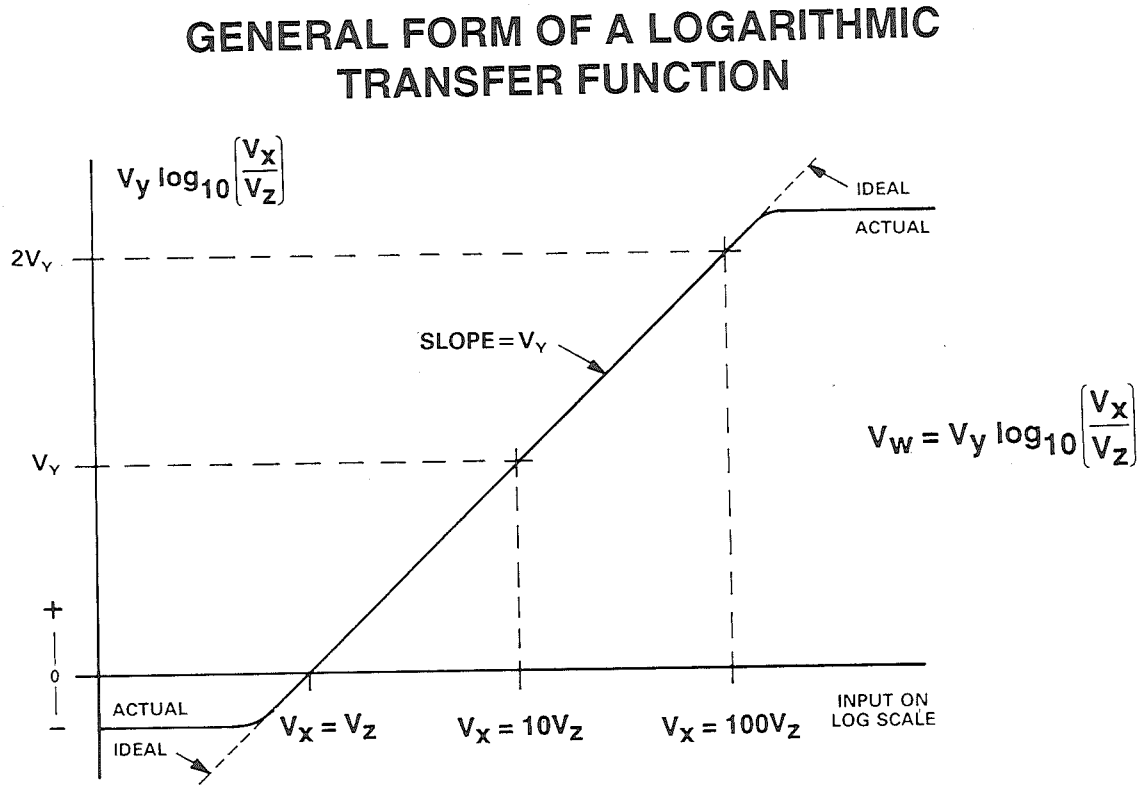

Figure 9.3.2

Eq. 9.3.1 is completely general and dimensionally consistent. V_W would be zero when $V_X = V_Z$, that is, V_Z defines the intercept of the transfer function on the horizontal axis. Note that we say "would be", because this may not actually occur, that is, V_Z may be the *extrapolated* intercept, and for reasons of design its value may be so small that the lower boundary on V_W will be first limited by noise or offsets. In fact, it is quite easy to set the intercept of a Log Amp to have *any* desired value of V_Z. This voltage need not be physically realizable; it could, for example, be as low as 1 nV. This can be readily appreciated by the following expansion:

$$V_W = V_Y \log (V_X V_X / V_Z V_Z)$$

$$= V_Y \log (V_X / V_Z) + V_A \qquad \text{Eq. 9.3.2}$$

where V_Z is the new value of the intercept achieved by adding some constant V_A to the output of the log-converter, having the value

$$V_A = V_Y \log (V_X / V_Z) \qquad \text{Eq. 9.3.3}$$

Clearly, V_A, and therefore V_Z, can have any value we wish.

A well-designed Log Amp has at least one high-accuracy DC reference source, from which both V_Y and V_Z are derived. A good example of a Log Amp designed with attention to the matter of calibration accuracy is the Analog Devices AD640. It actually has two laser-trimmed reference generators, one of which (a full band-gap circuit) sets V_Y and the other (a PTAT cell) which determines the accuracy of both V_Y and V_Z. These reference generators play a role every bit as important as those in an A/D converter, V/F converter, or analog multiplier.

We can just as easily cast Eq. 9.3.1 in terms of a current-input and voltage-output device:

$$V_W = V_Y \, log\,(I_X / I_Z) \qquad \text{Eq. 9.3.1a}$$

where V_Y, I_X and I_Z have equivalent specifications. This is the case for the translinear Log Amp, described in the next section. Alternatively, *all* signals may be in current form:

$$I_W = I_Y \, log\,(I_X / I_Z) \qquad \text{Eq. 9.3.1b}$$

This is less common, but certainly quite practical. Finally, the function may be in the form of voltage-input/current-output:

$$I_W = I_Y \, log\,(V_X / V_Z) \qquad \text{Eq. 9.3.1c}$$

This is the form found in RF Log Amps which use transconductance cells for demodulation; in these cases, the intermediate output current is converted back to a voltage.

9.3.3 SMALL-SIGNAL BEHAVIOR

Note that the above equations predict that V_W approaches $-\infty$ as V_X approaches zero. Of course, quite apart from the impracticality of this, there will be other limitations, particularly DC offsets at the input in the case of a baseband Log Amp, which limit the low-level accuracy. If we differentiate Eq. 9.3.1, using in this case base-*e* logarithms, with appropriate modification to V_Y, we find that the *incremental gain* of a Log Amp approaches $+\infty$ as V_{IN} approaches zero:

$$\frac{dV_W}{dV_X} = \frac{d}{dV_X} V_Y' \left\{ ln\,(V_X) + ln\,(V_Z) \right\}$$

$$= \frac{V_Y'}{V_X} \qquad \text{Eq. 9.3.4}$$

Thus, V_Z does not enter into the expression for incremental gain; this is consistent with the fact that we can arbitrarily alter V_Z after logarithmic conversion by the addition or subtraction of a

DC term at the output, as already shown. The notion that the gain must be infinite for zero-amplitude inputs should lead us to realize that the low-level accuracy of a demodulating Log Amp will be ultimately limited by (a) its maximum small-signal gain (determined in part by the number of stages) and (b) the noise level of the first stage. Of course, when the amplifier stages are DC-coupled the first stage offset might also be a limiting factor, but this can always be reduced by adjustment or the use of automatic offset control, as will be discussed later. Figure 9.3.3 shows the actual gain (from simulation) as a function of V_X for a high-performance multi-stage RF Log Amp. The reduction in gain for very small inputs is an artifact, due to an imperfection of the detectors: they are not exact absolute-value circuits with an "infinitely sharp" vertex, but become parabolic in this region, thus having zero gain. The tremendous variation in the incremental gain of a Log Amp should also serve as a reminder of the need for great caution in using small-signal analysis and simulation methods when dealing with Log Amps. Note in passing that the incremental gain is unity when the input voltage is equal to the scaling voltage.

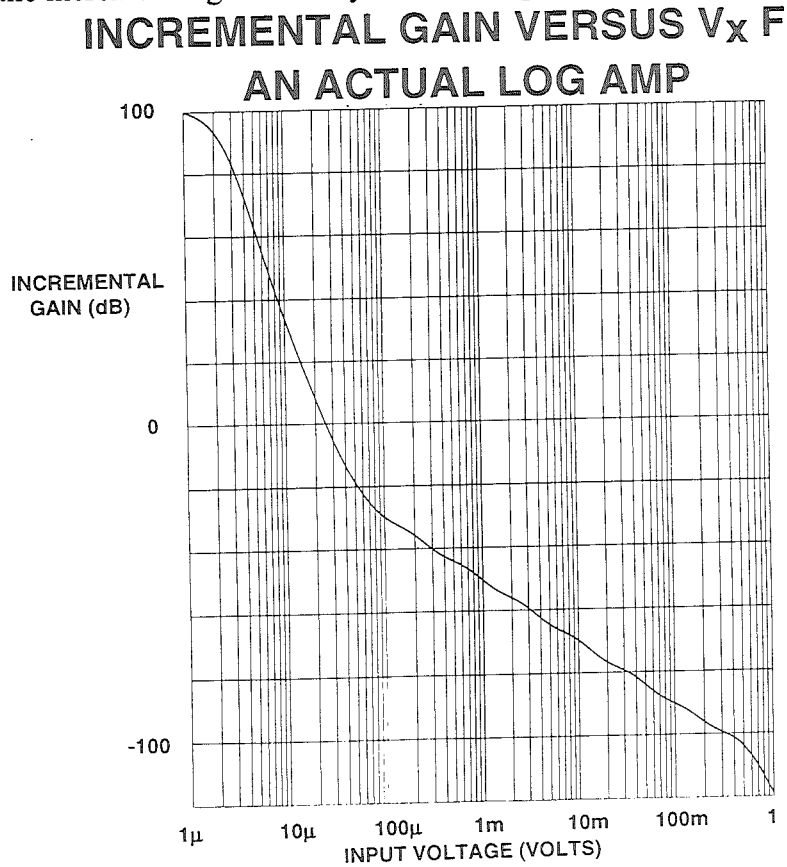

Figure 9.3.3

In discussing the scaling of Log Amps, the form of V_X is rarely mentioned. In the case of baseband converters this will often be a unipolar DC or quasi-DC (pulse) input, so Eq. 9.3.1 can be used without further consideration. But what happens when V_X becomes negative? There is no simple meaning to the log function when its argument is negative. Fortunately, we do not have to consider the mathematical consequences of this, because practical baseband Log Amps can be easily designed to handle inputs of either polarity with similar response. We can adapt Eq. 9.3.1 to handle this situation, by assuming that the circuit is arranged in some way to respond only to the magnitude of V_X and then restore its sign at the output:

$$V_W = sgn(V_X)\, V_Y\, ln(|V_X| / V_Z) \qquad \text{Eq. 9.3.5}$$

This is still not practical, however, because it requires that the output undergoes a transition from $-\infty$ to $+\infty$ as V_X diminishes and passes through zero. In fact, it is most likely in practical amplifiers intended to handle bipolar inputs that V_W will pass through *zero* when $V_X = 0$, because of the finite gain of its component sections. The situation described in Eq. 9.3.5 and its practical limitations can be handled by replacing the logarithmic function by the inverse hyperbolic sine function $sinh^{-1}$:

$$sinh^{-1}(u) = ln\ \{u + \sqrt{(u^2 + 1)}\} \qquad \text{Eq. 9.3.6}$$

$$= ln\ (2u) \quad \text{for } u >> 1$$

and

$$sinh^{-1}(-u) = -sinh^{-1}(u) \qquad \text{Eq.9.3.7}$$

Therefore, the "AC log" function may be written as

$$V_W = V_Y\, sinh^{-1}(V_X / 2V_Z) \qquad \text{Eq. 9.3.8}$$

Note the factor of two in the denominator of the argument. Figure 9.3.4 compares the ideal logarithmic transfer function with the hyperbolic sine in the region near $V_{IN} = 0$.

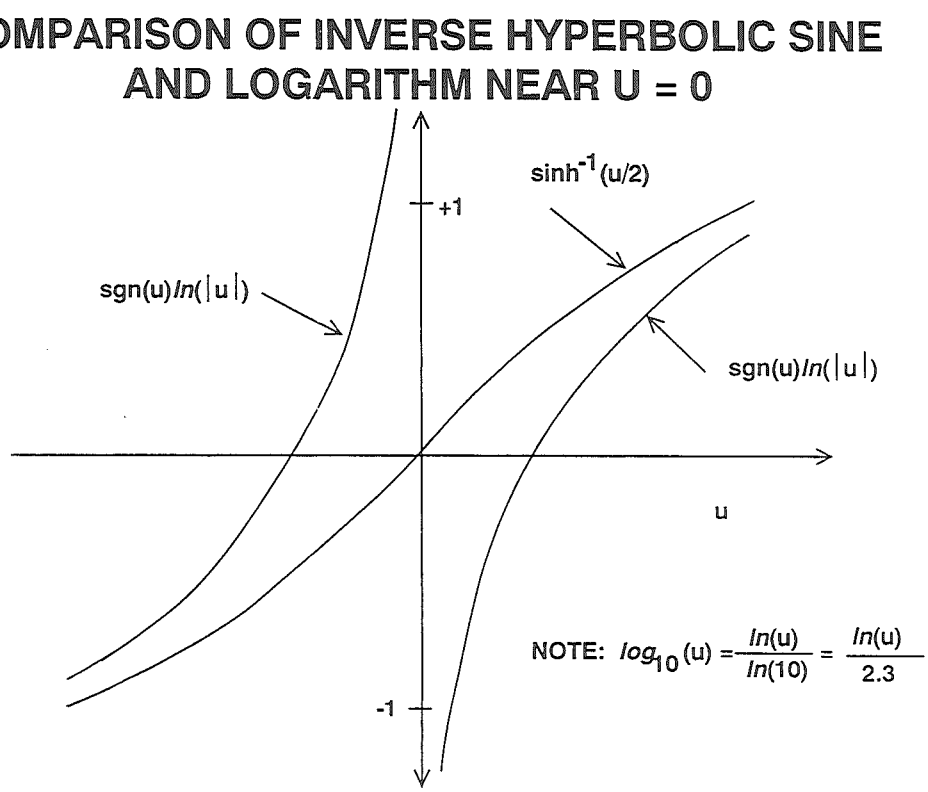

Figure 9.3.4

9.3.4 EFFECT OF WAVEFORM ON INTERCEPT

For the case of a demodulating Log Amp, having some kind of AC input, we must consider not just the amplitude of V_X , but its waveform, which has important practical consequences. In the performance specifications for a RF Log Amp, the signal is invariably presumed to be sinusoidal, and the intercept, usually specified in dBm (see above), applies to that implied operational mode. But for all other waveforms, the effective value of the intercept will be different. Note that the waveform has no effect on the slope (V_Y or I_Y).

For the case where the input is an amplitude-symmetric square wave, the rectification inherent in this type of Log Amp results in a response which is the same as that for a DC level. For a sinusoidal input where V_X is specified as the sine amplitude (not the RMS value), it will be exactly double this value. For an amplitude-symmetric triangle wave V_Z will be effectively increased by a factor of 2.718 (*e*). For a noise input with some prescribed probability density function (PDF) it will have a value dependent on the PDF: when this is Gaussian, V_Z is increased by a factor of 1.887.

These issues only became of interest with the advent of a fully-calibrated demodulating Log Amp (the Analog Devices AD640). Prior to that time, the intercept (often misleadingly called "log offset") had to be adjusted by the user, and most RF Log Amps could not be used at low enough frequencies where the response to a precise waveshape would be a matter of concern. Of course, the waveform-dependence of intercept does not arise in the case of video (baseband) Log Amps because it is a consequence of the signal rectification and averaging behavior of the post-demodulation low-pass filter, neither of which are present in a baseband Log Amp.

The proofs for above assertions are given here for completeness; to our knowledge they have not been previously published. For the sine case, we can write Eq. 9.3.1 in the form

$$V_W = V_Y \, lgt \{(E \sin \theta)/V_Z\} \qquad \text{Eq. 9.3.9}$$

where V_W remains the *instantaneous* value of the output, E is the amplitude of the sine input and θ is the angle, more usually written as a time function ωt. However, for a demodulating Log Amp, we are concerned with the *average value* of V_W , that is, the output of the post-demodulation filter.

We can avoid the mathematical nuisance of dealing with negative logarithmic arguments by just considering the behavior of Eq. 9.3.9 over the range for which sin θ is positive; in fact, we need only concern ourselves with the range $0 \le \theta \le \pi/2$, since the average over a full period will be simply four times the average over this range. (This assumes the use of exact full-wave rectification in the demodulator parts of the Log Amp. The theory is unchanged for half-wave operation, but will be modified by the inexact behavior of typical demodulation circuits, particularly at low signal levels. We will return to this topic when discussing specific Log Amp circuits in detail.)

The demodulated and filtered output is

$$AVE\,(V_W) = \frac{2}{\pi}\int_0^{\pi/2} V_Y\ lgt\ \{(E \sin\theta)/V_Z\}\,d\theta \qquad \text{Eq. 9.3.10}$$

$$= \frac{2V_Y}{\pi}\int_0^{\pi/2} \{lgt\,(\sin\theta) + lgt\,(E/V_Z)\}\,d\theta$$

$$= \frac{2V_Y}{\pi\ ln(10)}\int_0^{\pi/2} \{ln\,(\sin\theta) + ln\,(E/V_Z)\}\,d\theta$$

The definite integral of $ln(\sin\theta)$ over the range of interest is $-(\pi/2)\ ln\ 2$ and the complete integral yields

$$AVE\,(V_W) = \frac{2V_Y}{\pi\ ln(10)}\{-(\pi/2)\ ln\ 2 + (\pi/2)\ ln\,(E/V_Z)\}$$

$$= \frac{V_Y}{ln(10)}\{ln\,(E/V_Z) - ln\ 2\} \qquad \text{Eq. 9.3.11}$$

$$= V_Y\ lgt\,(E/2V_Z) \qquad \text{Eq. 9.3.12}$$

Simply stated, the response to a sine *amplitude* of E would be the same as for a *constant* DC input of E/2, that is, the entire logarithmic transfer function (Figure 9.3.1) is shifted to the right by 6.02 dB. The form of Eq. 9.3.11 deserves further attention. Inside the brackets we have the difference between a log term with the "standard argument" E/V_Z and a second term, in this

case *ln*(2), which is a function of the waveform, in the case, sinusoidal. This term can be viewed as a *waveform signature.*

Using a similar approach for the triwave input, we can write

$$V_W = V_Y \; lgt \{ (E / V_Z)(4t / T) \} \qquad \text{Eq. 9.3.13}$$

to describe the instantaneous output, where E is the amplitude of a triwave of period T. The demodulated and filtered output is now

$$AVE\,(V_W) = \frac{4}{T} \int_0^{T/4} V_Y \; lgt\,(4E\,t / V_Z\,T)\,dt \qquad \text{Eq. 9.3.14}$$

$$= \frac{4V_Y}{T} \int_0^{T/4} \{ lgt\,(t) + lgt\,(4E / V_Z\,T) \}\,dt$$

$$= \frac{4V_Y}{T\,ln(10)} \int_0^{T/4} \{ ln\,(t) + \ln\,(4E / V_Z\,T) \}\,dt$$

The integral of *ln*(t) is simply $t\,ln(t) - t$ and the complete integral yields

$$AVE\,(V_W) = \frac{4V_Y}{T\,ln(10)} \{ (T/4)\,ln\,(T/4) - T/4 + (T/4) \ln\,(4E / V_Z\,T) \}$$

$$= \frac{V_Y}{ln(10)} \{ ln\,(E/V_Z) - 1 \} \qquad \text{Eq. 9.3.15}$$

In this case, the "waveform signature" is just 1, and since this may be written as *ln*(e), the output becomes

$$= V_Y \; lgt\,(E/eV_Z) \qquad \text{Eq. 9.3.16}$$

Thus, a triangle wave input will effectively cause the intercept to shift up by a factor of *e*, or 8.69 dB.

For a noise input having a Gaussian PDF with an RMS value of E, the effective intercept is most easily calculated by first reducing the formulation to a generalized form. Thus, the average value, μ, of a variable, x, having a unit standard deviation, which has been subjected to a logarithmic transformation, can be expressed as

$$\mu = \frac{\int_0^\infty e^{-x^2/2}\, ln(x)dx}{\int_0^\infty e^{-x^2/2}\, dx} \qquad \text{Eq. 9.3.17}$$

Note that the variable x represents the *instantaneous* value of the input noise voltage variable (so it's actually, x(t), but the time dimension is an unnecessary complication for this calculation). The numerator and denominator are both standard forms[1]:

$$\int_0^\infty e^{-\alpha x^2}\, ln(x)dx = (\gamma + ln\, 4\alpha)\sqrt{\pi/4\alpha}$$

where γ is Euler's constant, and

$$\int_0^\infty e^{-\alpha x^2}\, dx = \sqrt{\pi/4\alpha}$$

Hence

$$\mu = (\gamma + ln\, 2)/4$$

which evaluates to $ln(1/1.887)$.

Therefore, the average value of the logarithmic output in response to a Gaussian input of "unit" RMS value is equivalent to a "DC" input of 1/1.887, that is

$$AVE(V_W) = V_Y\, lgt\,(E_{RMS}/1.887V_Z) \qquad \text{Eq. 9.3.18}$$

1 "Tables of Integrals, Series and Products", I.S. Gradshteyn and I.M. Ryzhik, Academic Press, 1980; Art 3.321.3 (page 307) and Art 4.333 (page 574)

This corresponds to an upward intercept shift of 5.52 dB. It is interesting to note that this is only 0.5 dB different from the calibration for a sinewave input, and it is quite likely to be ascribed to measurement error in the evaluation of the noise performance of practical Log Amps. These results have been carefully verified using the AD640 Log Amp.

9.3.5 THE TRANSLINEAR LOG AMP

Logarithmic converters intended for use at DC or low frequencies generally use a *translinear* technique. The term refers to the remarkably exact logarithmic relationship between the collector current I_C and the base-emitter voltage V_{BE} in a bipolar junction transistor (BJT). This simple fact has profound consequences in the design of analog bipolar circuits. Most importantly, it results in the transconductance being linear with I_C. This interesting but seemingly prosaic property is actually at the heart of the behavior of inumerable circuits, and is important enough to deserve the special term.

Reduced to essentials, this relationship can be written as

$$V_{BE} = V_T \, ln \{ I_C/I_S + 1 \} \qquad \text{Eq. 9.3.19}$$

where I_S is a basic scaling parameter for the BJT, called the saturation current. It is never *accurately* known for design purposes and is a strong function of temperature, roughly doubling every 8 °C. Furthermore, there is a direct dependence of the thermal voltage $V_T = kT/q$ on temperature. So it might first seem that the use of this aspect of BJT behavior in accurate logarithmic conversion circuits is unpromising. As we shall see, the concept can be developed to a considerable degree of refinement.

First, let's convert Eq 9.3.19 to base-10 logarithms to bring it into line with our Log Amp theme:

$$V_{BE} = V_Y \, lgt \{ (I_C + I_S)/ I_S \} \qquad \text{Eq. 9.3.20}$$

where

$$V_Y = V_T \, ln(10) \qquad \text{Eq. 9.3.21}$$

Thus, the logarithmic slope V_Y is proportional to absolute temperature (PTAT). It evaluates to 59.5 mV/decade at T = 300 K. The logarithmic intercept is simply the saturation current, I_S, typically between 10^{-17} and 10^{-15} Amperes at room temperature. Note that the "signal" input I_C is augmented by this tiny current; we later address the consequences of this slight anomaly in the otherwise straightforward Log Amp form of the equation.

It is important to note that V_{BE} bears this valuable relationship to the *collector* current. The finite beta of the transistor has no effect on the accuracy of these equations, although more will be said about this later. Some texts have erroneously ascribed errors in logarithmic converters of this type to the current-dependence of beta, by starting with expressions for V_{BE} that are functions of the *emitter* current I_E. Note that a current-driven *diode-connected* transistor would exhibit anomalies in logarithmic behavior due to this effect.

THE PATTERSON OR TRANSDIODE LOG AMP

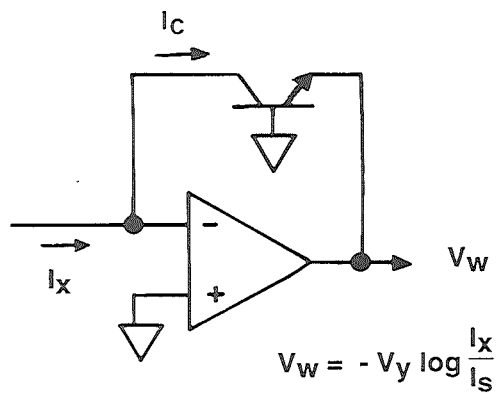

Figure 9.3.5

Figure 9.3.5 shows a typical scheme to force I_C to equal I_X, the signal current. This is sometimes called a "transdiode connection" or "Paterson diode". We show here the usual NPN form, but it is obvious that use of a PNP transistor would simply reverse the required polarity of input current and the resulting polarity of output voltage. In practice, monolithic PNP transistors of sufficient quality are only available in a few complementary bipolar processes.

The op-amp forces the collector current of the transistor to equal the input current I_X while maintaining its collector-base voltage very close to zero. The $V_{CB} = 0$ condition is not essential: for *most* purposes little harm will result if the collector junction is strongly reversed-biased (this effectively increases I_S), or even becomes slightly forward biased. Later, we will show that it is actually advantageous to use a specific value of reverse collector bias ($V_{CB} \approx -100$ mV) in certain applications.

The logarithmic output is taken from the emitter node, and the op-amp allows this to be loaded quite heavily while preserving accuracy. In most cases, I_S will be much less than I_X and, replacing I_C by I_X we can simplify Eq. 9.3.20 to

$$V_W = -V_Y \, lgt \, (I_X / I_S) \qquad \text{Eq. 9.3.22}$$

9.3.5.1 ERRORS AT HIGH TEMPERATURE

In the special case of operation at high temperatures and very low currents, the simplification used in Eq. 9.3.22 is inappropriate, since I_S is now roughly comparable with the input current. Eq. 9.3.20 correctly predicts that V_{BE} should approach zero as I_C approaches zero, for any I_S. However, the departure from a strictly logarithmic response in this region can be corrected by using a particular reverse bias at the collector. To understand this, we need to go back to the

basic Ebers-Moll modeling of collector current. For a transistor having a forward alpha α_F close to unity

$$I_C = I_S\left(exp\frac{V_{BE}}{V_T} - 1\right) - \frac{I_S}{\alpha_R}\left(exp\frac{-V_{CB}}{V_T} - 1\right) \qquad \text{Eq. 9.3.23a}$$

where α_R is the inverse alpha. If we make the further simplifying assumption at this point that α_R is also is close to unity (high inverse beta), then

$$I_C = I_S\left(exp\frac{V_{BE}}{V_T} - exp\frac{-V_{CB}}{V_T}\right) \qquad \text{Eq. 9.3.23b}$$

Now, when $V_{CB} = 0$ this reduces to the expression from which Eq. 9.3.19 follows directly, but when the collector is strongly reverse-biased the second terms vanishes, and Eq. 9.3.22 becomes exact. Even for modest amounts V_{CB} of the second term quickly becomes negligible.

At this point an interesting observation can be made. For the practical case of α_R less than unity, there is a unique value of V_{CB} to achieve exactly logarithmic operation. This is easily shown from Eq.9.3.23a to be

$$V_{CB} = -V_T\, ln(1 - \alpha_R) \qquad \text{Eq. 9.3.24}$$

that is, a small *forward*-bias on the collector. For an α_R of 0.5 the ideal V_{CB} would be $V_T\, ln(2)$, or 24.9mV at T = 150°C; for $\alpha_R = 0.8$ it would be 58.7mV.

For a given monolithic process, α_R is quite consistent, so it would be an easy matter to provide the correct PTAT voltage required by Eq. 9.3.24 to ensure accurate operation right down to, and beyond, the theoretical intercept. This voltage is not particularly critical and may be introduced either at the op-amp non-inverting input node or at the base of the transistor. In the first case, by elevating the voltage at the summing node it might cause errors in the input current I_X if this does not originate from a perfect current-source.

Even the few millivolts of V_{OS} of a MOS-input op-amp could create serious errors due to leakage resistance from the input node to ground. The relatively large 60 mV "inverse-alpha fix" across a leakage resistance of 100 MΩ would cause an error in I_X of 600 pA. Guarding is essential to prevent leakage paths to even more hazardous bias sources, such as the supplies. In the second case, the correction voltage would not affect the summing node potential, but would slightly alter the output voltage.

Remember, these details are only of importance in Log Amps which must operate accurately with picoampere inputs and at high temperatures. We of course assume that the op-amp has extremely small input currents, using a junction FET or MOS input stage.

9.4 LOG-AMP DESIGN

9.4.1 THE PROGRESSIVE COMPRESSION LOG-AMP

Almost without exception, high-frequency log-amps distribute their total dynamic range over many stages, each of which has low gain, and they achieve their function through a process of *progressive compression*. The theory is not especially well developed in the literature, particularly with regard to the all-important matter of scaling, that is, a comprehensive consideration of the fundamentals on which the accuracy of this nonlinear function depend. In developing a theory from first principles, we will be paying close attention to this topic.

We begin with the "target" function

$$V_W = V_Y \log (V_X/V_Z) \qquad \text{Eq. 9.4.1}$$

where V_W is the output voltage, V_X is the input voltage, V_Y will be called the *slope* voltage and V_Z the *intercept* voltage. Note at the outset that we are careful to use variables of the correct dimensions (all voltages, in this case) throughout. Since at this point we're considering *baseband* (non-demodulating) log-amps, V_X and V_W (shown in **bold** throughout this section to differentiate them from constants and internal voltages) are the *instantaneous* values of the input and output. The choice of logarithmic base is arbitrary; to preserve generality, it is not defined in Eq. 9.4.1. A change of base merely results in a change in V_Y. Later, we will use base-10 logarithms, in keeping with the decibel-oriented context.

THE LOGARITHMIC TRANSFER FUNCTION

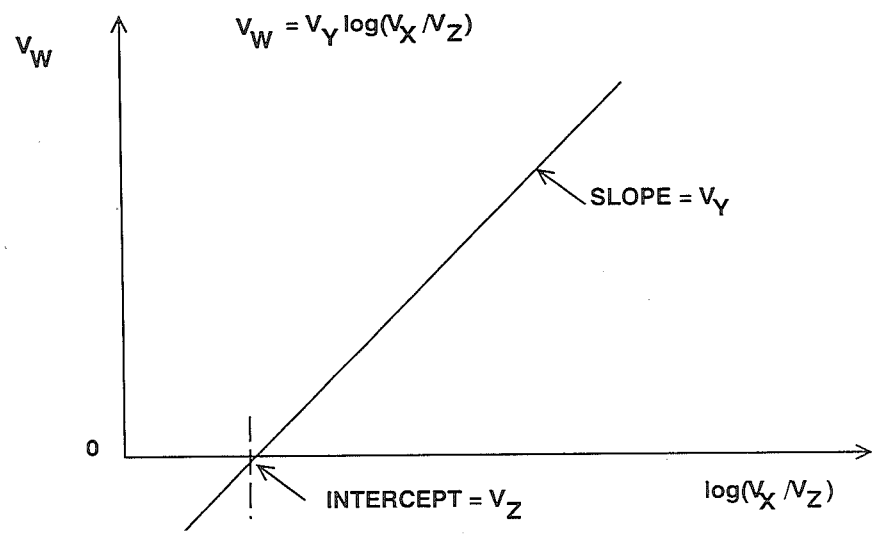

Figure 9.4.1

Figure 9.4.1 shows a plot of this function, Our objective is to find the scaling parameters V_Y and V_Z for specific circuits, of increasing complexity, as a foundation for a full theory of demodulating logarithmic amplifiers.

Imagine an amplifier stage having the DC transfer function shown in Figure 9.4.2. For the time being, we will be concerned only with its response to positive inputs, but the theory is completely applicable to a symmetrical response. Throughout this analysis, we will not be concerned with frequency-dependent aspects of the amplifier.

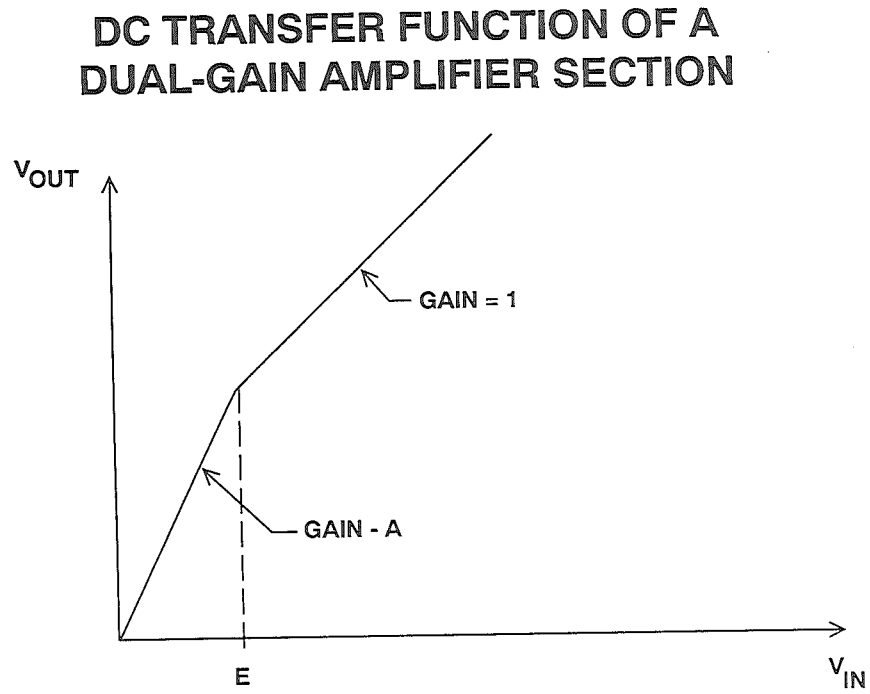

Figure 9.4.2

The gain for small inputs is A, a well-defined quantity moderately greater than one (typically between 2 and 4), and remains so up to an input ("knee") voltage of E, at which point the gain abruptly drops to unity. We will call this a "dual-gain amplifier", and use the symbol A/1 in the figures. Thus

$$V_{OUT} = AV_{IN} \qquad \text{for } V_{IN} \leq E \qquad \text{Eq. 9.4.2a}$$

and

$$V_{OUT} = AE + (V_{IN}-E)$$

$$= (A-1)E + V_{IN} \qquad \text{for } V_{IN} > E \qquad \text{Eq. 9.4.2b}$$

Without any analysis, we can immediately reach some conclusions about the behavior of a log-amp built from a series-connected set of such amplifier sections.

First, because the transfer function just defined is piecewise-linear, it follows that the overall function, although more complicated, can never be anything but a piecewise-linear approximation. Clearly, the more stages of lower gain that are used to cover a given dynamic range, the closer this approximation can be; put another way, we can expect the approximation error to be some increasing function of the gain stage, A. We will find later that practical circuits, having a softened gain transition, or even gain which varies continuously with V_{IN}, can provide arbitrarily close approximations to a true logarithmic response.

Second, we can be certain that the logarithmic slope V_Y and intercept V_Z in the target function must both be *directly proportional* to the knee voltage, E, that is, we can expect them to have the general form

$$V_Y = y\,E$$

and

$$V_Z = z\,E$$

where y and z are some functions of A and (certainly in the case of the intercept) N which control the magnitude of the slope and intercept, respectively. We can predict this simple proportionality with total assurance, because if some polynomial in E were needed, there would have to be other parameters with the dimension of voltage to restore dimensional consistency, that is, we cannot blithely propose something like

$$V_Y = a_1E + a_2E^2 + a_3E^3 \ .....$$

without giving due thought to where the coefficients of the higher-order terms in E derive *their* dimensionality[1].

The immediate challenge, then, is to find the functions y and z for the cascade of N dual-gain amplifier sections shown in Figure 9.4.3. This turns out to be easier that might at first seem; the reader is encouraged to follow this analysis through, step by step, because it provides a firm foundation for understanding all classes of log-amps using piecewise-linear progressive compression methods.

[1] The reader is urged to apply this type of reasoning, and constant vigilance to matters of scaling, in the development or application of any nonlinear analog processing block. It is usually risky (although occasionally unavoidable) to use "constants" in which dimensional quantities are embedded.

A BASEBAND LOG AMP COMPRISING A CASCADE OF DUAL-GAIN AMPLIFIER SECTIONS

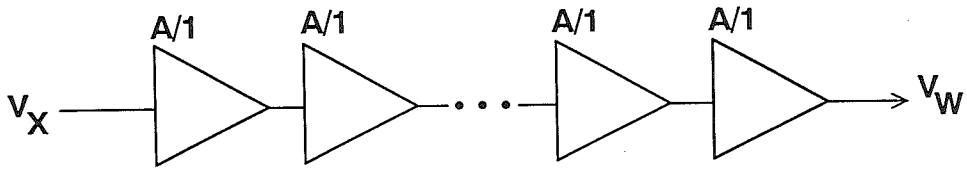

Figure 9.4.3

The overall input is labeled V_X and the output V_W in observance of the nomenclature used in the target function of Eq 9.4.1. For very small inputs, the overall gain is simply A^N. At a critical value of V_X, the input to the last (N-th) stage reaches its knee voltage, E. Since the gain of the preceding N–1 stages is A^{N-1}, this must occur at a voltage

$$V_X = E/A^{N-1}$$

This is sometimes called the "lin-log" transition, because for smaller inputs the cascade is simply a linear amplifier, while for larger inputs it enters a region of approximately logarithmic behavior. Above this point, the overall incremental gain falls to A^{N-1}. As the input is raised further, a second critical point is reached, when the input to the (N–1)-th stage reaches *its* knee. Then

$$V_X = E/A^{N-2}$$

which is simply A times larger than the first critical voltage. We can call this the first "mid-log" transition. Above this point, the incremental gain falls by a further factor of A, to A^{N-2}, and so on.

It will be apparent that the cascade is characterized by a total of N transitions, the last occurring at $V_X = E$. Figure 9.4.4 shows the voltages at all exposed nodes in this system at all the transition points.

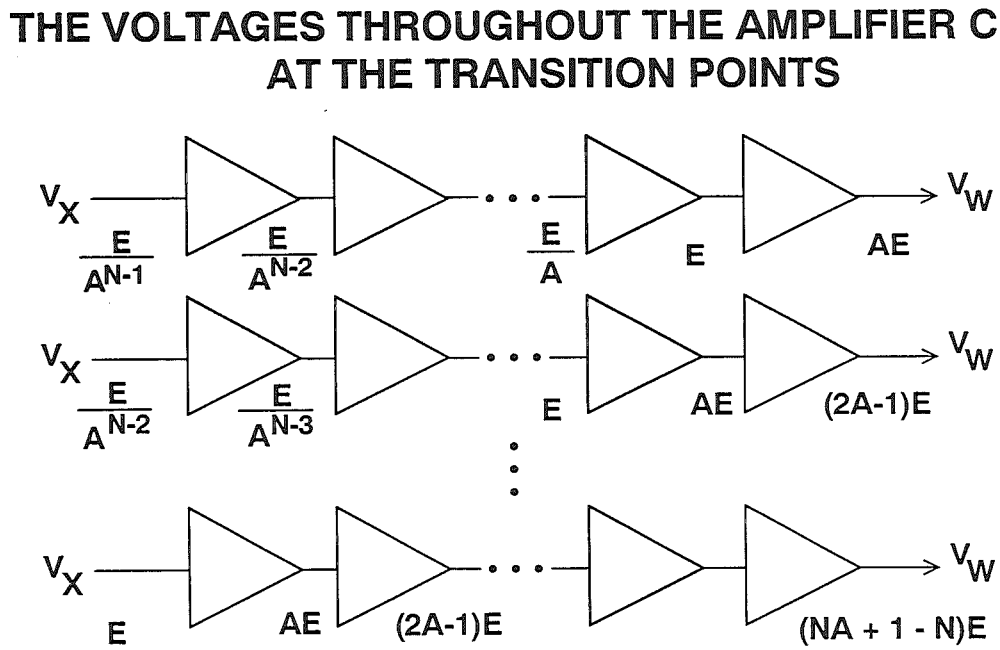

Figure 9.4.4

The key point here is that these transitions are at voltages separated by a *constant ratio*, equal to the gain A of each amplifier section. This already looks promising, since if V_X is represented along a logarithmic axis, these transitions occur at equal linear increments.

The next step is to find the corresponding values of V_W for all intervals above the lin-log transition and up to $V_X = E$. Eq. 9.4.2b can quickly adapted for the first interval:

$$V_W = (A-1)E + V_N \qquad \text{Eq. 9.4.3}$$

where V_N is the input to the N-th stage. Precisely at the lin-log transition, $V_N = E$, and therefore $V_W = AE$. Up to the second transition, V_N is just $V_X A^{N-1}$, so for the interval between the lin-log transition and the first mid-log transition,

$$V_W = (A-1)E + V_X A^{N-1} \qquad \text{Eq. 9.4.4}$$

We can use this starting point to find an expression for V_W for all values of V_X. However, we really don't need to delineate all possible values of V_W, since our aim at this juncture is just to find the effective slope and intercept of the overall piecewise-linear function. This task will be aided by using Figure 9.4.5, which shows the critical points and their coordinates, with an estimate of what the complete function might look like for a four-stage prototype.

THE LOCATION OF THE "LIN-LOG" AND "MID-LOG" TRANSITION POINTS

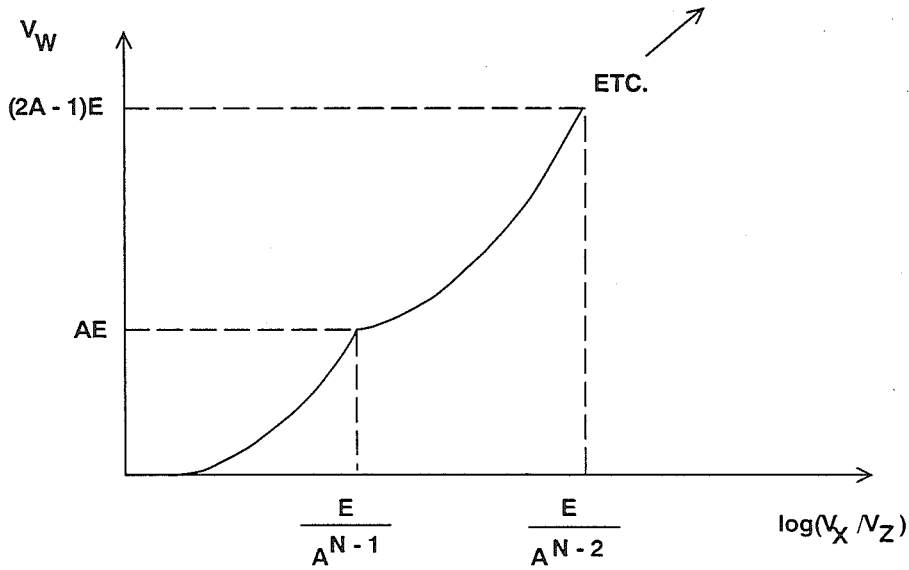

Figure 9.4.5

Right at the first mid-log transition, the output of the (N–1)-th stage is simply AE, so the output of the next stage, which is also the final output, is, from Eq. 9.4.4,

$$V_W = (A-1)E + AE$$

$$= (2A-1)E \qquad \text{Eq. 9.4.5}$$

So the output increased from AE to (2A–1)E, an amount (A–1)E, for a *ratio* change of A in V_W. Continuing this line of reasoning, we can demonstrate that at the next transition $V_W = (3A-2)E$, and so on: ***the change in V_W is always by the fixed amount (A–1)E as V_X increases by each factor of A.***

Now, a "factor of A" can be stated as "some fractional part of a decade"; but that is just *lgt*A, where *lgt* denotes "logarithm to base 10". For example, a ratio of 4 is slightly over six-tenths of a decade, since *lgt*4 = 0.602.

We can therefore state that the slope of the output function, corresponding to a line drawn through all the transition points, is

$$V_Y = \frac{\text{Absolute voltage change in } V_W}{\text{Ratio change in } V_X} = \frac{(A-1)E}{lgtA} \qquad \text{Eq. 9.4.6}$$

As expected, is V_Y proportional to E. What may be a little surprising is that the slope is unaffected by the number of stages, N.

Since we are now using base-10 logarithms V_Y can in this case be read as "Volts per decade", but it will be more generally referred to as the "Slope voltage", because any base may be used in the formal function of Eq. 9.4.1.

To determine the intercept, we need only to insert one point into the target equation and use the known value of slope. We can conveniently choose the lin-log transition, at which point $V_X = E/A^{N-1}$ and $V_W = AE$. Thus

$$AE = \frac{(A-1)E}{lgtA} \; lgt \left\{ \frac{E}{V_Z A^{N-1}} \right\} \qquad \text{Eq. 9.4.7}$$

which solves to

$$V_Z = \frac{E}{A^{N + 1/(A-1)}} \qquad \text{Eq. 9.4.8}$$

N finally makes an appearance in the expression for the intercept! And, as we should expect, for each added stage this intercept just moves to the left (in Figure 9.4.5), to a voltage A times lower. Our original task has therefore been accomplished. There remain only a few loose ends before we are ready to design a practical baseband log-amp along these lines. But before proceeding, let us apply "sanity checks" to the results so far.

Suppose A = 4, N = 8 and E = 1 V. We only have a dim idea at this point that these might be suitable numbers, but they can be roughly rationalized in the following way: a gain of 4 for each section is consistent with high accuracy and wide bandwidth in a simple amplifier cell; using 8 stages and this gain, the useful dynamic range will be of the order of 4^8 which corresponds to 96dB; E = 1 V is just a starting-point.

With these figures, the slope works out to about 5 V per decade and the intercept is about 10 μV. Clearly, in a practical amplifier handling several decades and operating within the constraints of typical supplies, a lower value of E would be required. Figure 9.4.6 shows the simulated output of an 8-stage system. for which E = 392.7 mV and A = 4.145, choices relating to a particular practical design not presented here. The scale is 2 V per decade, a convenient 100 mV/dB; the

intercept is at 2.86 μV. Note that the intercept could readily be shifted to 10 μV by the simple expedient of including a ×3.5 attenuator ahead of the log-amp's input.

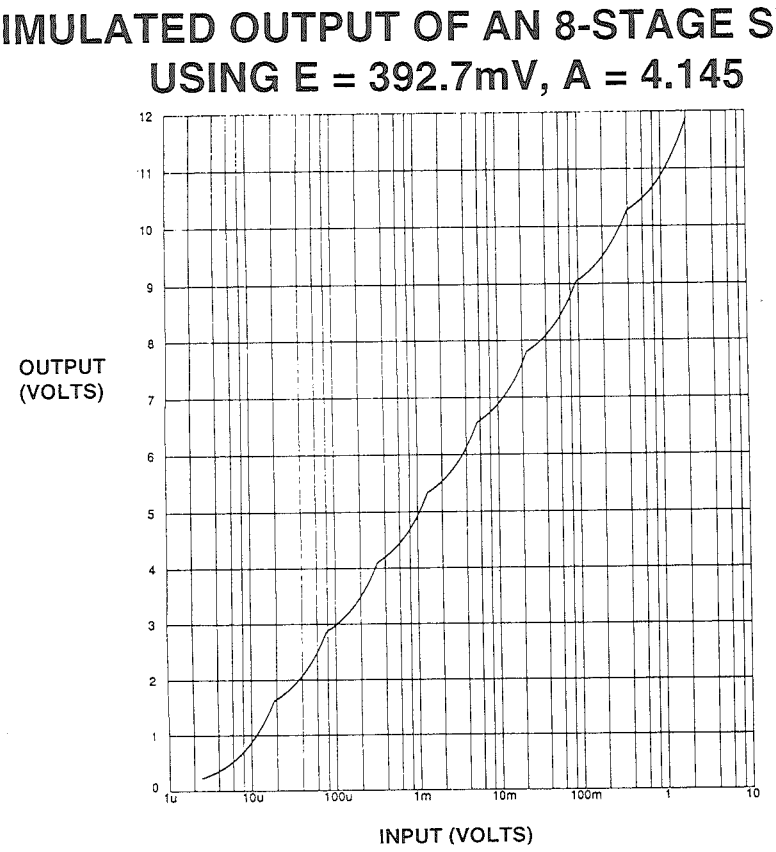

Figure 9.4.6

9.4.2 DYNAMIC RANGE, MAXIMUM OUTPUT AND PEAK ERROR

At inputs much below the lin-log transition at $V_X = E/A^{N-1}$ or much above the top transition, at $V_X = E$,corresponding to a dynamic range of A^{N-1}, the deviation of the piecewise-linear approximation from the ideal logarithmic line rapidly becomes excessive. However, examination of the transfer function in Figure 9.4.6 quickly reveals that it extends to at least a factor of A above and below these outer transition points. Thus, the practical dynamic range is actually rather more than A^{N+1}, depending on the allowable error at the extremities of the range.

Beyond the top transition, the output can readily be shown to be

$$V_W = N(A-1)\,E + V_X \qquad \text{Eq. 9.4.9}$$

Thus, in our example, the output at $V_X = 2$ V is 11.88 V, a value consistent with a traditional IC op-amp context, although not appropriate to RF log-amps. Figure 9.4.7 shows the error

computed by subtracting the ideal output from the actual output and presenting the result in equivalent decibels:

$$Error_{dB} = 20 \{ V_W/V_Y - lgt\,(V_X/V_Z) \} \qquad \text{Eq. 9.4.10}$$

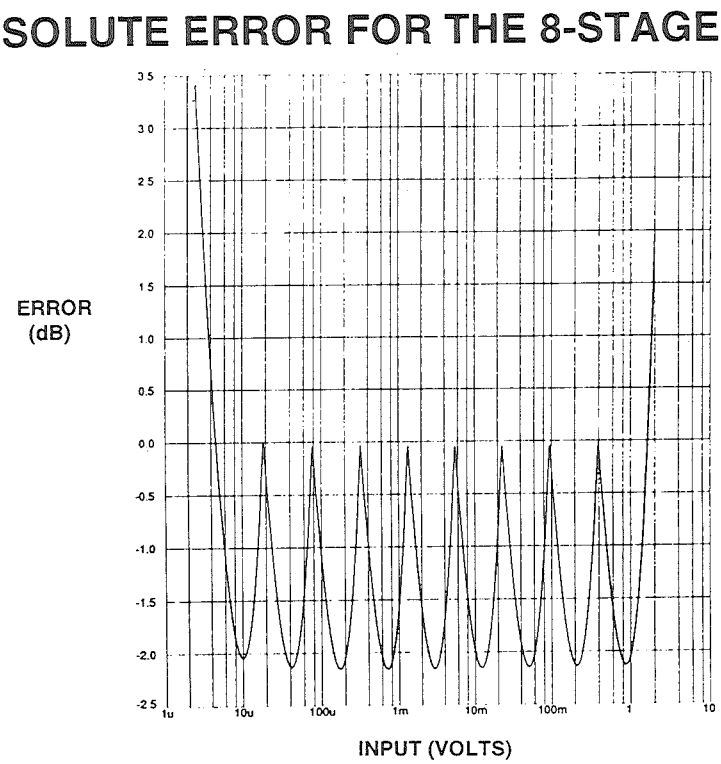

Figure 9.4.7

Rigorous analysis of the ripple is straightforward, but the solution lacks immediate impact. An alternative is presented here which makes only the assumption that the maximum deviation occurs at the mid-point between the transitions, that is, at an input level $\sqrt{A}$ greater than the lower point of any interval, which of course is also a factor $\sqrt{A}$ below the upper point.

The first of these mid-points occurs between the lin-log transition and the first mid-log transition, in other words, at

$$V_X = E/A^{N-1}\sqrt{A} \qquad \text{Eq. 9.4.11}$$

at which point the *actual* output is

$$V_{WA} = E\,(A + \sqrt{A} - 1) \qquad \text{Eq. 9.4.12}$$

The *ideal* output is

$$V_{WI} = V_Y \, lgt(V_X/V_Z)$$

which, for this particular input and using the complete values for V_Y and V_Z from Eqs. 9.4.6 and 9.4.8 respectively, is

$$V_{WI} = \frac{(A-1)E}{lgtA} \, lgt \, \frac{\dfrac{E\sqrt{A}}{A^{N-1}}}{\dfrac{E}{A^{N+1/(A-1)}}} \qquad \text{Eq. 9.4.13}$$

The fact that this simplifies down to

$$V_{WI} = (3A-1)E/2$$

should lead us to suspect that there's probably a simpler way to find this result! The difference between V_{WA} and V_{WI} is the peak output-voltage error:

$$Error_{pk} = (A - 2\sqrt{A} + 1)E/2 \qquad \text{Eq. 9.4.14}$$

Converted to its equivalent decibel error by dividing this by V_Y, we find

$$Error_{pk\,dB} = 10\{(A - 2\sqrt{A} + 1)\, lgtA\}/(A-1) \qquad \text{Eq. 9.4.15}$$

As might be expected, *the error expressed in decibels is dependent only on the stage gain* A. For A = 4.145, the value used to generate the error plot of Figure 9.4.7, this evaluates to 2.11dB, in excellent agreement with that simulation. Other values are 0.52 dB for A = 2, 1 dB for A = 2.65, 1.40 dB for A = $\sqrt{10}$, 1.72 dB for A = 3.6 and 2 dB for A = 4. Using more practical amplifier transfer functions, having continuously-varying gain as a function of their input voltage, the error ripple is much lower in amplitude and roughly sinusoidal in form, rather than parabolic as in this case.

Numerous circuit arrangements are possible to implement a near-ideal dual-gain stage at low frequencies. However, an even simpler topology, eminently suitable for monolithic integration (in a somewhat revised form) can achieve precisely the same function, and, in practice, equal or better accuracy.

9.4.3 LOG-AMPS USING AMPLIFIER/LIMITER STAGES

A somewhat different approach uses an amplifier-limiter stage, for which the gain remains A for small signals, but drops to *zero* for inputs above the knee voltage, E. This can be called an amplifier/limiter stage, and denoted on the figures by the symbol A/0. Figure 9.4.8 shows the transfer function of this stage; in this case, we have chosen to show the symmetry of the response to inputs of either polarity, because we'll be making use of this later. The basic equations are

$$V_{OUT} = AV_{IN} \quad \text{for } -E \le V_{IN} \le E \qquad \text{Eq. 9.4.16a}$$

$$V_{OUT} = AE \quad \text{for } V_{IN} > E \qquad \text{Eq. 9.4.16b}$$

and

$$V_{OUT} = -AE \quad \text{for } V_{IN} < -E \qquad \text{Eq. 9.4.16c}$$

DC TRANSFER FUNCTION OF AN AMPLIFIER/LIMITER SECTION

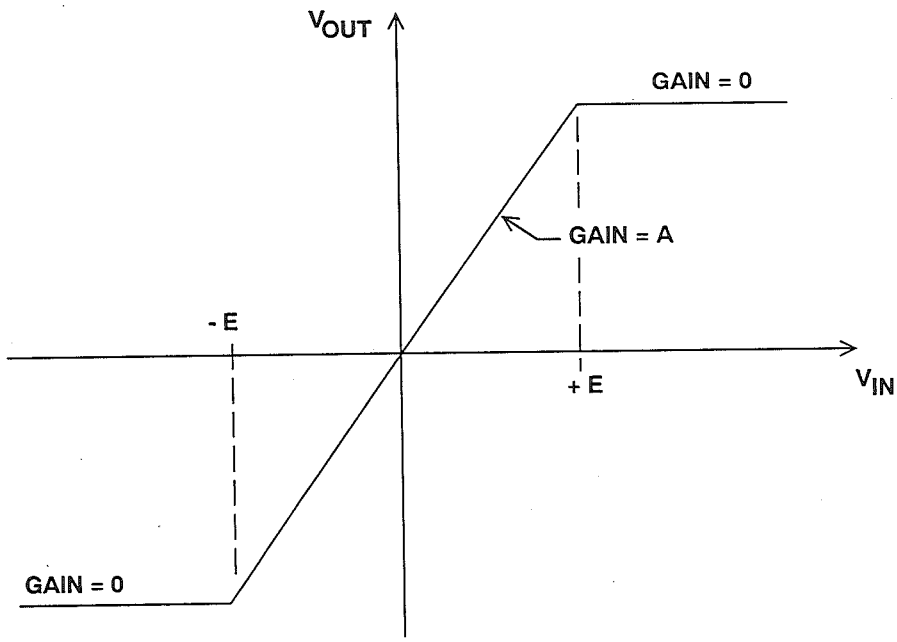

Figure 9.4.8

As before, a logarithmic function will be synthesized using the piecewise-linear behavior of a cascade of N stages, first to realize a baseband log-amp and later in a demodulating log-amp. We will establish the theory for idealized stages having abrupt limiting, then adapt it to more realistic wideband circuit cells, which have "soft" limiting and a knee voltage which is a strong function of temperature, so that special means are required to stabilize the scaling attributes.

Figure 9.4.9 shows the general structure of a baseband log-amp made up of N such A/0 stages. Now, it will immediately be apparent that we can no longer just use the output of the *final* stage, since as soon as this stage goes into limiting, which happens when $V_X = E/A^{N-1}$, the output will simply limit at AE and be unable to respond to further increases in V_X.

Instead, *the outputs of all stages must be summed*, usually, though not necessarily, with equal weighting, to form the logarithmic output V_X. This only slightly complicates the mathematics, and having conquered the analysis of the A/1 cascade, we should not have too much difficulty in tackling this new situation. As before, the approach will be to methodically work toward finding the basic scaling parameters V_Y and V_Z in the transfer function

$$V_W = V_Y \log (V_X/V_Z) \qquad \text{(quoting Eq. 9.4.1)}$$

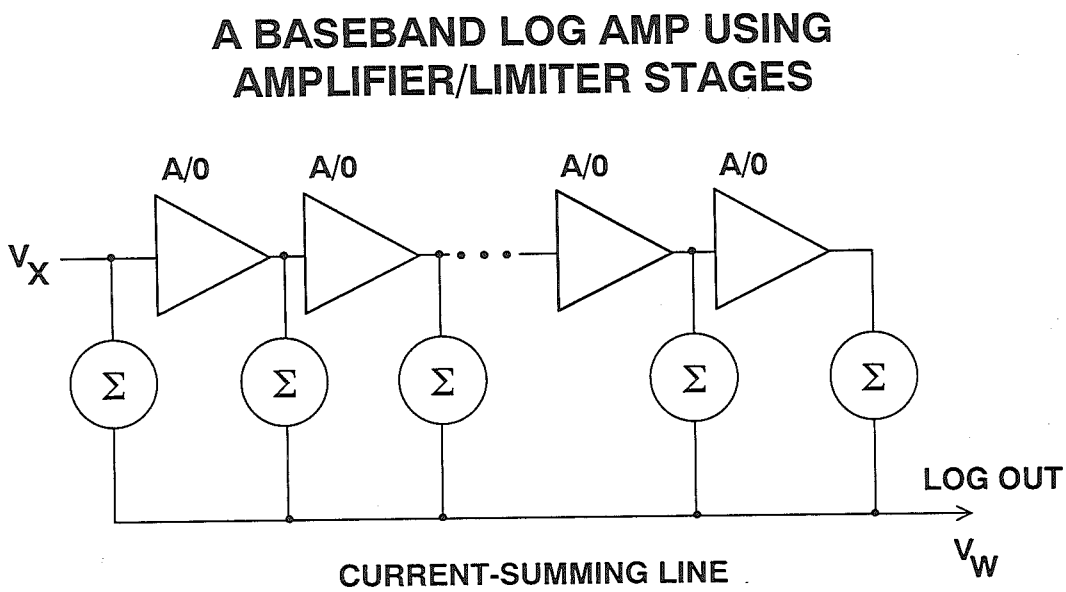

Figure 9.4.9

We are now well-enough informed to know that the slope voltage V_Y and the intercept voltage V_Z must both be simply proportional to E.

For very small values of input, the gain to the output of the k-th stage is simply A^k. At a critical value of V_X, the input to the N-th stage reaches its knee voltage, E. Since the gain of the first N–1 stages is A^{N-1}, this must occur at a voltage

$$V_X = E/A^{N-1}$$

We earlier called this the "lin-log" transition, because for smaller inputs the cascade behaves a linear amplifier, while for larger inputs it becomes pseudo-logarithmic. As the input is raised further, a second critical point is reached, when the input to the (N–1)-th reaches its knee.

This happens when

$$V_X = E/A^{N-2}$$

which is just A times larger than the first critical voltage. This the first "mid-log" transition. Just as for the cascade of A/1 stages, this system is characterized by a total of N transitions, the last occurring at $V_X = E$, and therefore the milestones along the log-input axis are at exactly the same values of V_X. As before, these transitions are at voltages separated by a *constant ratio*, equal to the gain A of each amplifier section.

Now we have to find the corresponding values of the output V_W for all values of input V_X up to, and slightly beyond, E. For small inputs, below the lin-log transition, and for equal weighting of the limiter outputs

$$V_W = A^N V_X + A^{N-1} V_X + \ldots\ldots\ldots\ldots + V_X$$

$$= (A^N + A^{N-1} + \ldots\ldots\ldots\ldots + 1)\, V_X \qquad \text{Eq. 9.4.17}$$

Precisely at the lin-log transition

$$V_W = (A^N + A^{N-1} + \ldots\ldots\ldots\ldots + 1)\, E/A^{N-1}$$

$$= (A + 1 + \ldots\ldots\ldots\ldots + 1/A^{N-1})\, E \qquad \text{Eq. 9.4.18}$$

At the first mid-log transition

$$V_W = (A + A + 1 + \ldots\ldots\ldots + 1/A^{N-2})\, E \qquad \text{Eq. 9.4.19}$$

Between these two inputs, the output has changed by

$$\Delta V_W = (A - 1/A^{N-1}) E$$

while the input increased by a factor A, or *lgt*A decades. Thus, the slope for this first interval, measured on the transition coordinates, is

$$V_{Y1} = \frac{(A - 1/A^{N-1}) E}{lgtA} \qquad \text{Eq. 9.4.20}$$

For typical values of A and N, this is very close to AE/*lgt*A.

At the second mid-log transition

$$V_W = (A + A + A + 1 + \ldots\ldots + 1/A^{N-3}) E \qquad \text{Eq. 9.4.21}$$

So over this interval the slope is

$$V_{Y2} = \frac{(A - 1/A^{N-2}) E}{lgtA} \qquad \text{Eq. 9.4.22}$$

Again, for typical values of A and N, this remains close to AE/*lgt*A. For example, if A = 4 and N = 8, the exact value of V_{Y2} is 6.6422E while the "simplified" value is 6.6435E. It is therefore reasonable to use the expression

$$V_Y = \frac{AE}{lgtA} \qquad \text{Eq. 9.4.23}$$

for the slope of this log-amp over the entire lower portion of its dynamic range. At the top transition V_W = NAE while at the penultimate transition

$$V_W = \{ (N-1) A + 1 \} E \qquad \text{Eq. 9.4.24}$$

so the slope between the two *uppermost* transitions is

$$V_{YN} = \frac{(A - 1) E}{lgtA} \qquad \text{Eq. 9.4.25}$$

which is the same value as for the cascade of A/1 stages, while the next pair from the top have a slope

$$V_{YN-1} = \frac{(A - 1/A)\,E}{lgtA} \qquad \text{Eq. 9.4.26}$$

Thus, we conclude that there is a slight reduction in the slope over the last few transition intervals, that is, at the top end of the dynamic range. As we shall see in just a moment, this artifact can be corrected, and the top-end logarithmic conformance in a high-accuracy design can thereby be improved, by simply using a higher summation weighting on the output from the first stage.

To determine the intercept, we follow the procedure used earlier, and insert one input/output point into the target equation and use the known value of slope. As before, we can use the lin-log transition, at which point $V_X = E/A^{N-1}$ and

$$V_W = (A + 1 + \ldots\ldots + 1/A^{N-1})\,E \qquad \text{(quoting Eq. 9.4.18)}$$

Thus

$$(A + 1 + \ldots\ldots + 1/A^{N-1})\,E = \frac{AE}{lgtA}\, lgt\, \{\frac{E}{V_Z A^{N-1}}\} \qquad \text{Eq. 9.4.27}$$

Multiplying both sides by (A–1)/A and reducing

$$A + 1/A^N = \frac{A-1}{lgtA}\, lgt\, \{\frac{E}{V_Z A^{N-1}}\} \qquad \text{Eq. 9.4.28}$$

This equation is almost identical with Eq. 9.4.7 and for practical purposes has the same solution

$$V_Z = \frac{E}{A^N + 1/(A-1)} \qquad \text{(Eq. 9.4.8)}$$

The simulated results for an 8-stage system, using ideal A/0 cells, are shown in Figures 9.4.10. The theoretical slope and intercept are 1.661 V and 2.4 μV respectively.

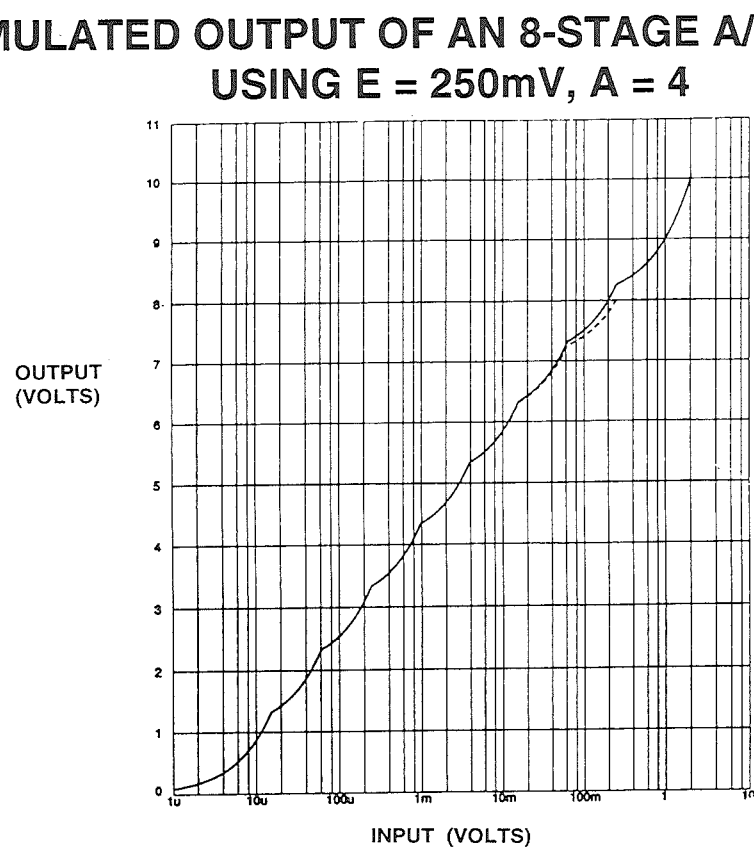

Figure 9.4.10

The ripple calculation for this system follows the same approach as used above and yields essentially identical results, that is

$$\text{Error}_{\text{pk dB}} = 10 \{ (A - 2\sqrt{A} + 1) \, lgt A \} / (A-1) \qquad \text{(quoting Eq. 9.4.15)}$$

For the stage gain of A = 4 used in the above examples, this evaluates to 2 dB.

9.4.3.1 A Nice Trick

Now, supposing that we alter the summation weighting of *just the input term*, from 1 to A/(A–1). Then, at the lin-log transition

$$\begin{aligned} V_W &= \{ (A^N + A^{N-1} + \ldots\ldots + A/(A-1) \} \, E/A^{N-1} \\ &= \{ \quad A \quad + 1 \quad + \ldots\ldots + 1/(A-1)A^{N-2} \} \, E \end{aligned} \qquad \text{Eq. 9.4.29}$$

which collapses to

$$V_W = \{ A^2/(A-1) \} \, E \qquad \text{Eq. 9.4.30}$$

At the first mid-log transition

$$V_W = \{ A + A + 1 + \ldots + A/(A-1)A^{N-2} \} E \qquad \text{Eq. 9.4.31}$$

which reduces to $V_W = \{ (2A^2-A)/(A-1) \} E$ Eq. 9.4.32

Between these two inputs, the output now changes by *exactly*

$$\Delta V_W = AE$$

Thus, the slope for this first interval is now *exactly*

$$V_{Y1} = \frac{AE}{lgtA} \qquad \text{Eq. 9.4.33}$$

By continuing this process it will be found that the difference in V_W between each transition is *now always AE*. In other words, by this simple measure, we have eliminated the annoying variation in slope at the top end of the dynamic range.

9.4.4 SUMMATION VIA G/0 STAGES

Next we need to consider any effects on the mathematics which may arise when the summation is performed by transconductance (*gm*) cells which exhibit similar "amplifier/limiter" behavior as the gain stages.

The use of *gm* stages is appealing, because current-mode signals can be summed by simply connecting the outputs of all stages together; conversion back to voltage form is easily accomplished using a simple resistive load or a transresistance stage. Further, they provide unilateral transmission to this output, minimizing the likelihood of unwanted reverse coupling to sensitive early nodes in the signal path. More importantly, they provide the means to *separate the slope calibration from the parameters which control the behavior of the main amplifier*. This last benefit is central to the scaling of monolithic log-amps using differential bipolar pairs as the gain cells, since their knee voltage is a strong function of temperature (in fact, as shown in Section 9.4.6, it's proportional to absolute temperature, or PTAT) and, as we've learned, it is this voltage that controls the slope in all the structures considered up to this point.

For a *gm* stage, the parameter corresponding to the dimensionless gain A is now the small-signal transconductance G: a voltage input V_K (the signal at any node K) generates a current output, GV_K. In the most general case, the knee voltage at which this *gm* abruptly drops to zero could be different from the corresponding voltage for the A/0 amplifier stage, but we will not pursue that general analysis here because (a) we anticipate that the practical circuit form which will be used for the G/0 stages has exactly the same (PTAT) knee voltage, E, as the A/0 stages and (b) the clarity of the mathematics and the intuitive appreciation of the system behavior are both needlessly impaired by retaining this redundant generality. The maximum output from a G/0

stage (that is, when $V_K \geq E$) is GE, analogous to AE for the gain stage. However, the dimensional change inherent in the *gm* stage means that this peak output is simply a current, which will here be called I_Y (the "Y" referring to the logarithmic slope in Eq. 9.4.1, since it is obvious that it will be this current which controls the slope). Therefore, $I_Y = GE$.

Figure 9.4.11 shows the new scheme. The summed currents from the G/0 stages are converted back to voltage by the resistor R_Y, to which the logarithmic slope is also proportional. It's safe to assume that the basic operation of this system will be similar to that we've encountered already, but we will nevertheless use a step-by-step procedure to put the scaling of this revised form on a firm foundation.

As before, we begin by considering the circumstances at the lin-log transition. The input to the last *gm* stage (numbered N+1) is the output from the N-th amplifier stage, so this first transition now occurs at a system input V_X which is A times lower than in either of the two earlier log-amp structures.

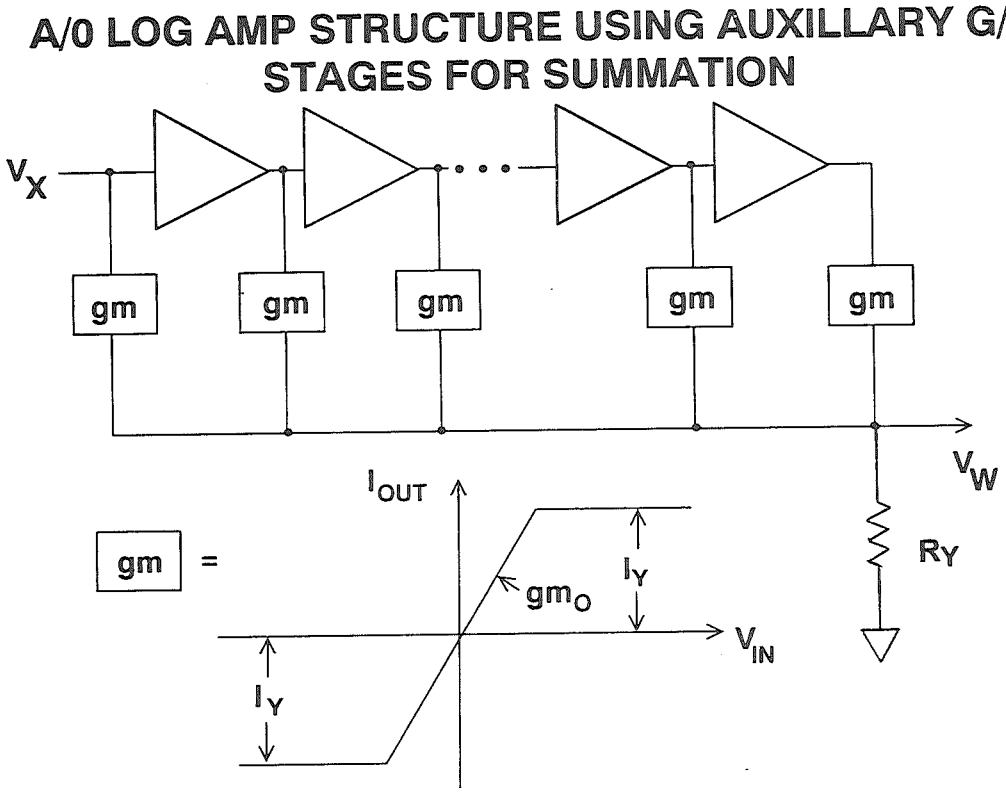

Figure 9.4.11

Thus, at the lin-log transition

$$V_X = E/A^N \qquad \text{Eq. 9.4.34}$$

Summing the outputs of the G/0 stages, starting at the last stage (whose output is the largest) and progressing back to the input stage the output is

$$V_W = R_Y \{ GE + GE/A + \ldots\ldots + GE/A^N \} \qquad \text{Eq. 9.4.35}$$

As previously noted, the product GE is the peak current output I_Y of the G/0 stage, so the repeated products $R_Y GE$ can be contracted to a simple constant scaling voltage $V_S = I_Y R_Y$. Note that this is not yet the slope voltage V_Y of the target equation 9.4.1. Hence, at the lin-log transition

$$V_W = V_S \{ 1 + 1/A + \ldots\ldots + 1/A^N \} \qquad \text{Eq. 9.4.36}$$

The next condition of interest is the first mid-log transition. This occurs when the input to the N-th A/0 stage reaches its knee voltage, E, which is also the voltage at which the N-th G/0 stage reaches this condition. The system input voltage at which this occurs is

$$V_X = E/A^{N-1} \qquad \text{Eq. 9.4.37}$$

and the output at this point is

$$V_W = R_Y \{ GE + GE + GE/A + \ldots\ldots + GE/A^{N-1} \}$$

$$= V_S \{ 1 + 1 + 1/A + \ldots\ldots + 1/A^{N-1} \} \qquad \text{Eq. 9.4.38}$$

By subtracting the voltage at the lin-log transition (Eq. 9.4.36) from this voltage, we find that the output has changed by

$$\Delta V_W = V_S (1 - 1/A^N) \qquad \text{Eq. 9.4.39}$$

For the interval between this transition and the next mid-log point, similar reasoning shows that

$$\Delta V_W = V_S (1 - 1/A^{N-1}) \qquad \text{Eq. 9.4.40}$$

We've been here before. The slope is going to end up being dependent on just which interval we consider, unless we use "The Trick" to fix things up. In fact, we will carry out the algebra more slowly here, like a benign magician, to show how the trick is done.

Let's go back to Eq. 9.4.36, but apply a weighting A/(A–1) to the *gm* of the first stage (last term). Since the knee voltage has not be altered, the peak output current of that stage is also increased by the same factor. Hence:

$$V_W = V_S \{ \quad 1 \quad + \quad 1/A \quad + \quad \ldots\ldots \quad + \quad 1/A^{N-1} \quad + \quad A/(A-1)A^N \quad \}$$

$$= V_S \{ \quad 1 \quad + \quad 1/A \quad + \quad \ldots\ldots \quad + \quad 1/A^{N-1} \quad + \quad 1/(A-1)A^{N-1} \} \qquad \text{Eq. 9.4.41}$$

where we have spaced out the terms and also included the penultimate one, in anticipation of the nest step. As before, we now multiply all the terms by (A–1), and bring this factor outside the brackets, to get a series of the form

$$V_W = V_S \{ (A-1) + (A-1)/A + \quad \ldots\ldots\ldots \quad + \quad (A-1)/A^{N-1} + 1/A^{N-1} \}/(A-1)$$

$$= V_S \{ A - 1 + 1 - 1/A + 1/A + \ldots - 1/A^{N-2} + 1/A^{N-2} - 1/A^{N-1} + 1/A^{N-1} \}/(A-1)$$

The reduced-size terms show how *all* the internal products generate cancelling pairs, leaving just

$$V_W = V_S A/(A-1) \qquad \text{Eq. 9.4.42}$$

as the output at the lin-log transition.

Now let's carry out the expansion for the first mid-log transition, with the A/(A–1) weighting of the first *gm* stage included:

$$V_W = V_S \{ \quad 1 \quad + \quad 1 \quad + \quad 1/A + \ldots\ldots \quad + \quad 1/A^{N-2} \quad + A/(A-1)A^{N-1} \}$$

$$= V_S \{ \quad 1 \quad + \quad 1 \quad + \quad 1/A + \ldots\ldots \quad + \quad 1/A^{N-2} \quad + \quad 1/(A-1)A^{N-2} \}$$

$$= V_S \{ A-1 \quad + \quad A-1 \quad + \quad (A-1)/A + \ldots\ldots \quad + (A-1)\ 1/A^{N-2} \quad + \quad 1/A^{N-2} \}/(A-1)$$

After generating the inner products, this collapses to just

$$V_W = V_S (2A-1)/(A-1) \qquad \text{Eq. 9.4.43}$$

for the output at the first mid-log transition. The change in V_W between the mid-log and lin-log transitions is thus

$$\Delta V_W = V_S (2A-1)/(A-1) - V_S A/(A-1)$$

$$= V_S \qquad \text{Eq. 9.4.44}$$

At the next mid-log transition, the same process yields

$$V_W = V_S\,(3A-2)/(A-1) \qquad \text{Eq. 9.4.45}$$

and the change in V_W is thus

$$\Delta V_W = V_S\,(3A-2)/(A-1) - V_S\,(2A-1)/(A-1)$$

$$= V_S$$

Continuing on this way, it is apparent that, with the modified weighting on just the first G/0 stage, the change in V_W between *any* adjacent pair of transitions is always exactly V_S .

The logarithmic slope voltage V_Y can now be calculated. As before, between any two transitions the input changes by a ratio of A, which can be expressed as *lgt*A. (see Section 9.4.1)

Thus

$$V_Y = \frac{V_S}{lgt A} \qquad \text{Eq. 9.4.46}$$

A valuable consequence of the use of the G/0 stages, therefore, is that the slope voltage can be controlled independently of the knee voltage, E, through the bias currents I_Y and the load resistor R_Y.

The result expressed in Eq. 9.4.46 could perhaps have been reached by the following intuitive argument: The inputs to the G/0 stages are separated by amplifiers having a gain A; the outputs of these stages starts at zero and limits at I_Y, so the voltage output V_W increments by $V_S = I_Y R_Y$ for a ratio increase of A at the system input V_X. But, if it's that simple, why does the first stage have to have a higher *gm*?

The explanation is to be found by examining the individual outputs of the *gm* stages as shown in Figure 9.4.12. Note that for the lower-signal region the output at each transition point includes contribution from all of the "higher" detector stages. It can easily be shown that these secondary terms have relative magnitudes which form a series $1/A + 1/A^2 + 1/A^3$ .... which sums to 1/(A–1). Thus, when added to the "main" term, of unit magnitude, we find the complete output at these "low-end" transitions is 1 + 1/(A–1), which can be written A/(A–1). On the other hand, the top transition does not have the benefit of these additional terms, so *all* of the output must come from just the one detector, which must thus have a weighting A/(A–1).

CURRENT STEPS FROM EACH OF THE G/0 STAGES WITH THE A/(A-1) FIX

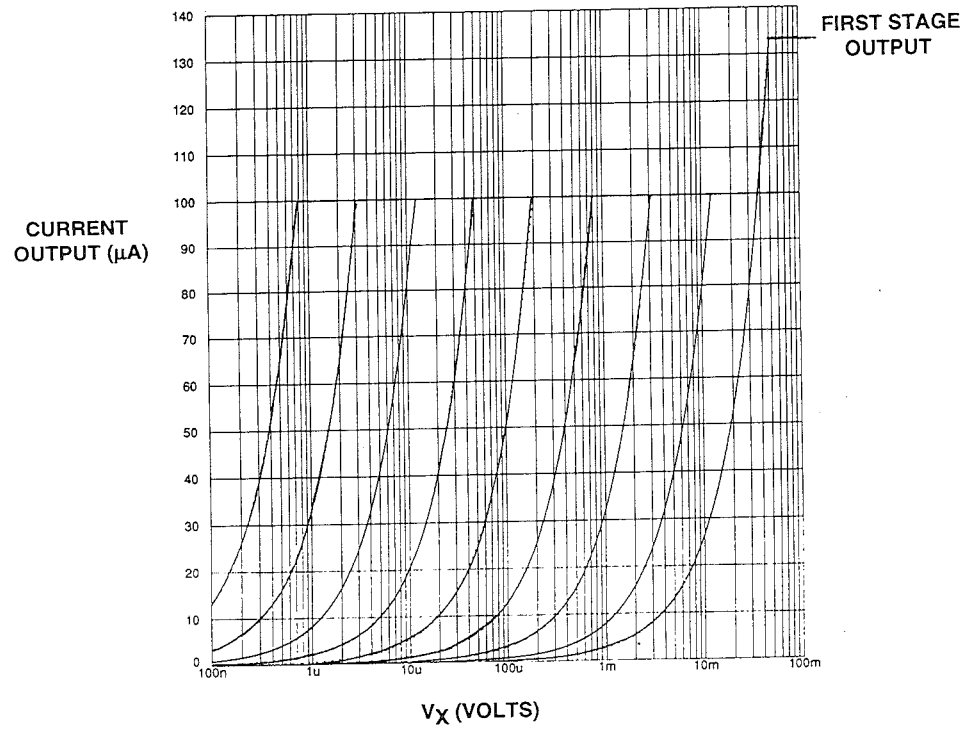

Figure 9.4.12

The intercept V_Z is determined as in all previous cases, that is, by inserting a known V_X, V_W pair into the general equation, in which all but V_Z are known. We will once again use the lin-log transition point. Combining Eqs. 9.4.1, 9.4.34, 9.4.42 and 9.4.46 we have

$$\frac{AV_S}{A-1} = \frac{V_S}{lgtA}\, lgt \frac{E/A^N}{V_Z} \qquad \text{Eq. 9.4.47}$$

which yields

$$V_Z = \frac{E}{A^N + A/(A-1)} \qquad \text{Eq. 9.4.48}$$

Compare Eq. 9.4.48 with Eq. 9.4.8.

Thus, the intercept voltage V_Z is traceable to the knee of the A/0 and G/0 stages, while the slope voltage V_Y depends on a decoupled variable, I_Y.

9.4.5 CONVERSION TO DIFFERENTIAL FORM

It is quite feasible to build log-amps using the single-sided prototypes we have been considering up to this point. In fact, some manufacturers have for years been doing that, although it is immediately apparent from a casual glance at their schematics that very little thought has been put into the matter of scaling calibration or temperature stability of the basic cells. All single-sided structures are very prone to HF problems caused by signals on the supply lines (that is, they have poor power-supply rejection).

Suffice it to say that fully-differential topologies have several advantages, one of which is a high degree of immunity to power-supply sensitivity. All signals, including the summation signals from the G/0 stages, have completely-defined current-circulation paths, keeping unwanted signals away from "common" and "supply" lines. At the very high gains and bandwidths typical of multistage log-amps, only a very small amount of feedback from a down-stream stage to the input can easily cause oscillation. The problem, of course, becomes severe in a monolithic implementation, which is one reason why there are practically no multistage monolithic amplifiers available. For example, a 90 dB amplifier chain, with an overall bandwidth of 100MHz has a gain-bandwidth product of about 3200 GHz! Fastidious management of all signal routing is imperative, even when differential technique are employed throughout.

Figure 9.4.13 shows the same log-amp system discussed in the last section, but in fully differential form. It will be apparent that, with appropriate care in the specification of variables, that the mathematics is unaffected by this modification of structure.

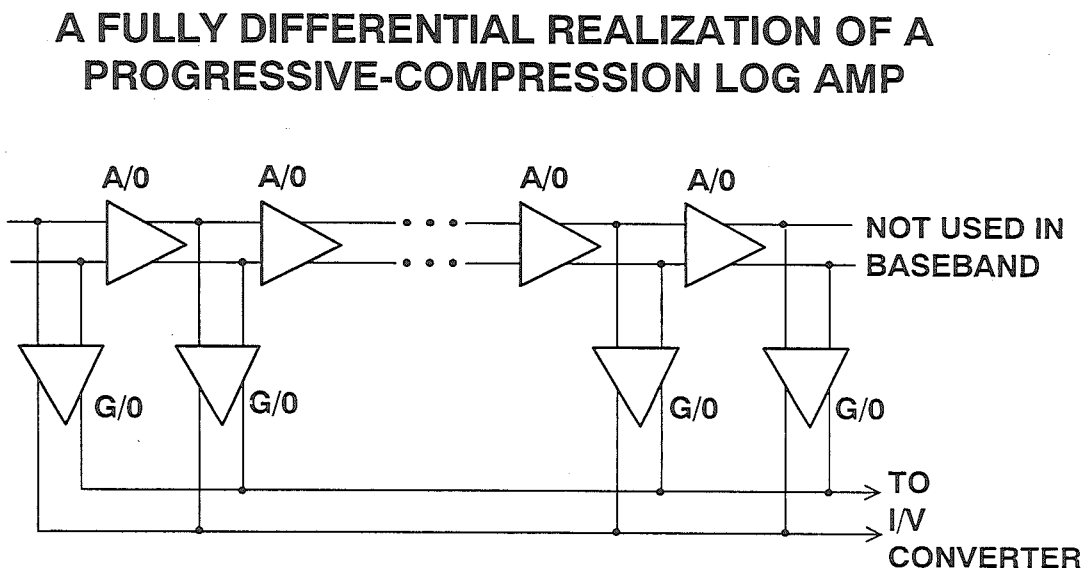

Figure 9.4.13

9.4.6 THE AD640 LOG AMP

In the past, it has been necessary to construct high performance, high frequency successive detection log amps using a number of individual limiting amplifiers. These are typically assembled in complex and costly hybrids. Recent advances in IC processes have allowed this complete function to be integrated into a single chip.

The AD640 log amp contains five limiting stages (10dB per stage) and five full-wave detectors in a single IC package, and its logarithmic performance extends from dc to 145MHz. Furthermore, its amplifier and full-wave detector stages are balanced so that, with reasonable well-considered layout, instability from feedback via supply rails is unlikely. A block diagram of the AD640 is shown in Figure 9.4.14.

BLOCK DIAGRAM OF THE AD640 LOG AMP

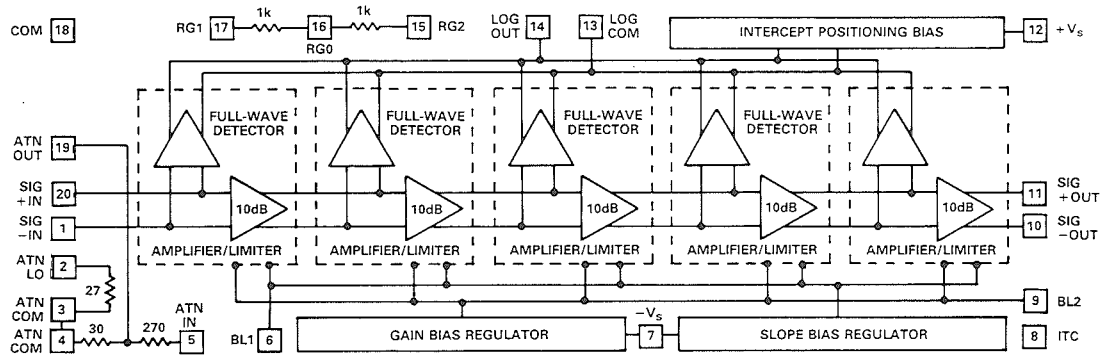

Figure 9.4.14

Unlike all previous integrated circuit log amps, the AD640 is laser trimmed to a high absolute accuracy of both slope and intercept, and is fully temperature compensated. Key features of the AD640 are summarized in Figure 9.4.15.

AD640 LOG AMP FEATURES

- 45dB Dynamic Range - Two AD640s Cascadable to 95dB
- Bandwidth dc to 145MHz - 120MHz when Cascaded
- Laser-Trimmed Slope of 1mA/decade - Temperature Stable
- Less than 1dB Log Non-Linearity
- Balanced Circuitry for Stability
- Minimal External Component Requirement

Figure 9.4.15

Each of the five stages in the AD640 has a gain of 10dB and a full-wave detected output. The transfer function of the device is shown in Figure 9.4.16 along with the error curve. Note the excellent log linearity over an input range of 1 to 100mV (40dB). Although well suited to rf applications, the AD640 is dc-coupled throughout. This allows it to be used in LF and VLF systems, including audio measurements, sonar, and other instrumentation applications requiring operation to low frequencies or even dc.

DC LOGARITHMIC TRANSFER FUNCTION AND ERROR CURVE FOR SINGLE AD640

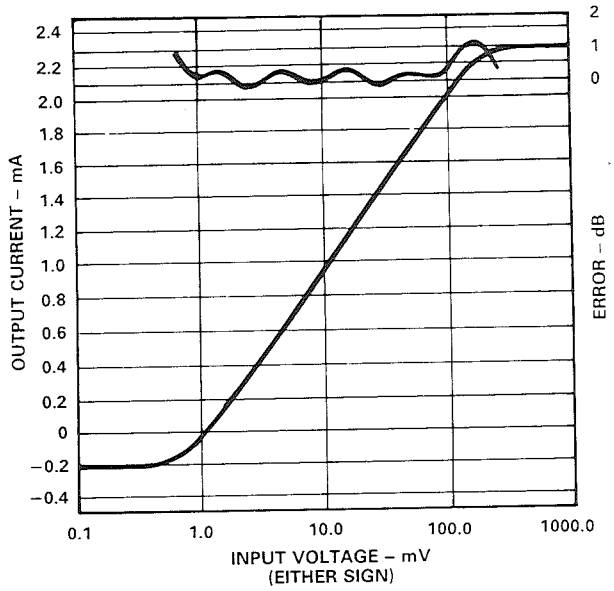

Figure 9.4.16

When two AD640s are cascaded, the second will be delivering an output from the noise of the first. If the full potential dynamic range is to be realized, the bandwidth must be limited because of noise. This may be done with high-pass, low-pass, or band-pass filters, depending on the required response, but, the voltage gain of these filters in their passband must be unity, or there will be a kink in the log response. Figure 9.4.17 shows a 70dB log amp for broadband operation from 50 to 150MHz. The 100MHz passband limits the possible dynamic range, but the performance is still exceptional. Figure 9.4.18 shows a 95dB 10Hz to 100kHz log amp using two cascaded AD640s.

70dB LOG AMP FOR 50-150MHz USING TWO AD640s

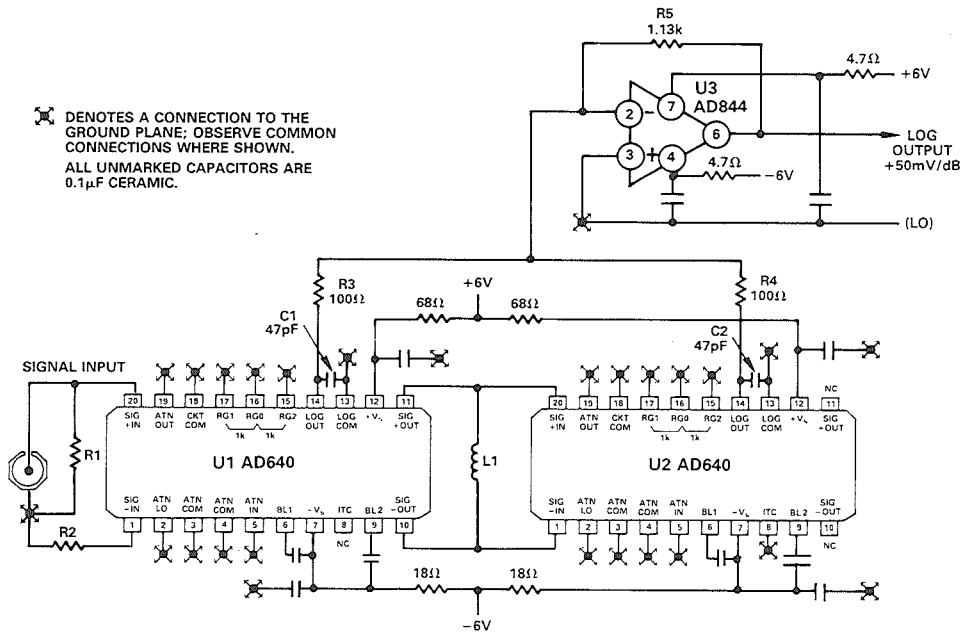

Figure 9.4.17

95dB LOW FREQUENCY LOG AMP (10Hz - 100KHz) USING TWO AD640s

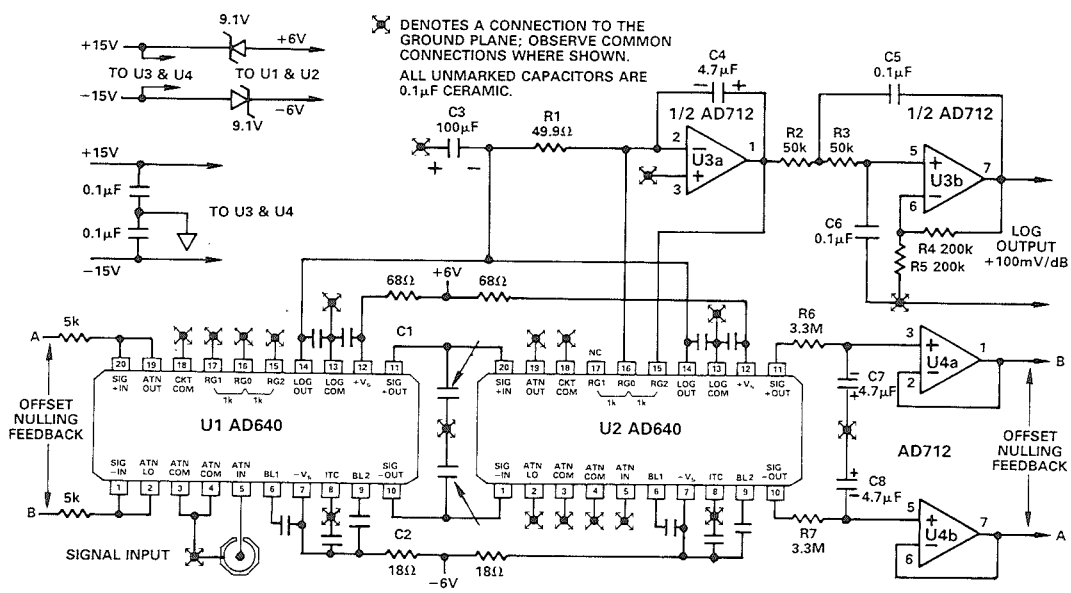

Figure 9.4.18

9.5 SOME ASPECTS OF LOG-AMPS BASED ON BIPOLAR DIFFERENTIAL STAGES

9.5.1 THE DIFFERENTIAL PAIR AS AN AMPLIFIER/LIMITER

The classical BJT differential-pair shown in Figure 9.5.1 can be used to implement both the A/0 (amplifier/limiter) and G/0 (limited-output *gm*) cells discussed in Section 9.4.

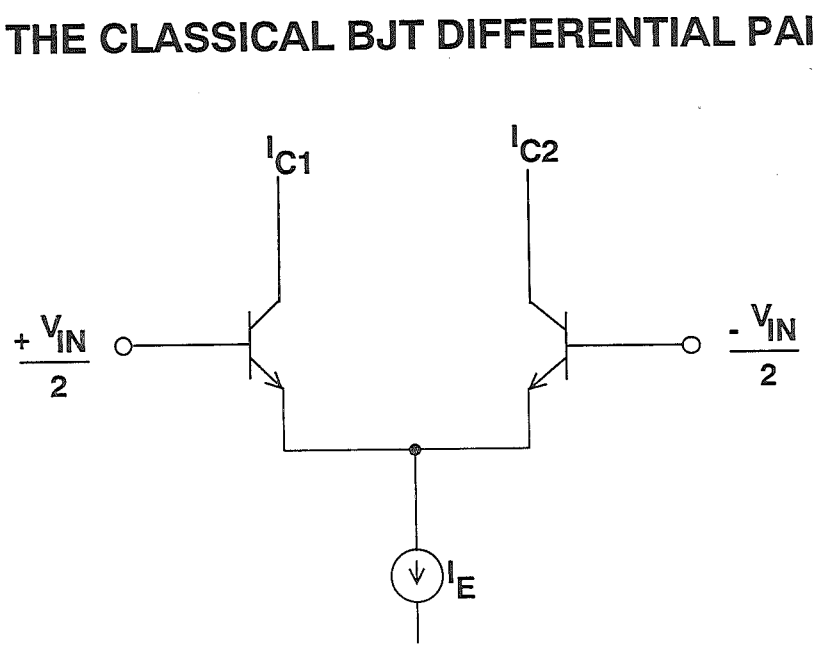

Figure 9.5.1

The transfer function for ideal transistors, shown in Figure 9.5.2, is the well-known hyperbolic tangent:

$$I_{OUT} = I_{C1} - I_{C2} = I_E \tanh (V_{IN}/2V_T) \qquad \text{Eq. 9.5.1}$$

DC TRANSFER FUNCTION OF CLASSICAL BJT PAIR

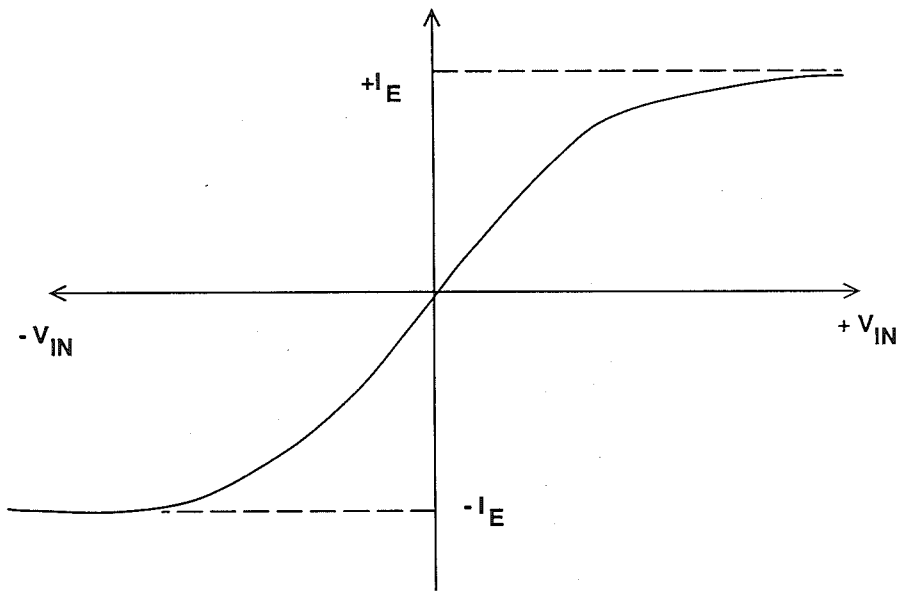

Figure 9.5.2

It follows that

$$gm = \frac{dI_{OUT}}{dV_{IN}} = \frac{I_E}{2V_T} sech^2(V_{IN} / 2V_T) \qquad \text{Eq. 9.5.2}$$

The *gm* therefore has a value of $gmo = I_E/2V_T$ for $V_{IN} = 0$ and falls asymptotically to zero for large inputs. A differential amplifier/limiter can be realized by simply the addition of load resistors, as shown in Figure 9.5.3.

AN A/0 AMPLIFIER BASED ON THE BIPOLAR DIFFERENTIAL PAIR

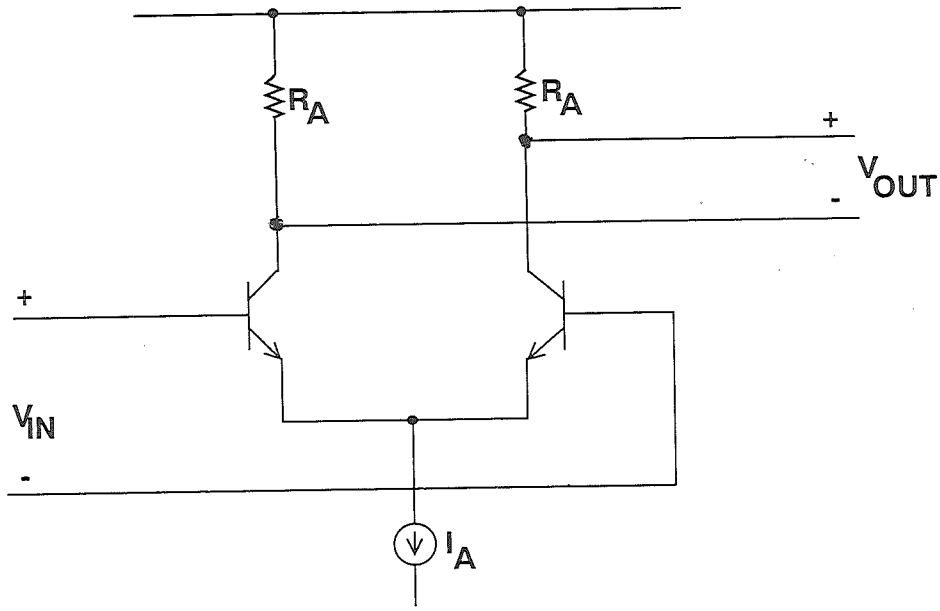

Figure 9.5.3

The small-signal gain A of the amplifier cell is simply

$$A = gmo\, R_A = I_A R_A / 2V_T \qquad \text{Eq. 9.5.3}$$

from which it is immediately apparent that the tail current I_A must be PTAT (proportional to absolute temperature) to cancel the PTAT form of V_T (= kT/q) if the gain, and thus, the system dynamic range, is to be stable with temperature. Unlike the highly-abstracted stages discussed in Section 9.4, this stage does not have a clearly-defined knee voltage at which the gain exhibits an abrupt transition. In fact, the *gm* diminishes continuously with increasing $|V_{IN}|$, as implied by Eq. 9.5.2.

Nonetheless, the theory which the abstractions of Section 9.4 made possible turns out to be remarkably robust, and we can find appropriate values for all of the parameters used up to this point to correctly predict the behavior of log-amps built with these more practical A/0 and G/0 stages.

Thus, for both the amplifier/limiter cell and the limited-output *gm* cell the *effective* knee voltage is just that voltage which, at a fixed *gm* = *gmo*, would take the output to its limiting value. This makes

$$E = 2V_T \qquad \text{Eq. 9.5.4}$$

that is, about 52 mV at 27 °C. This is shown in Figure 9.5.4.

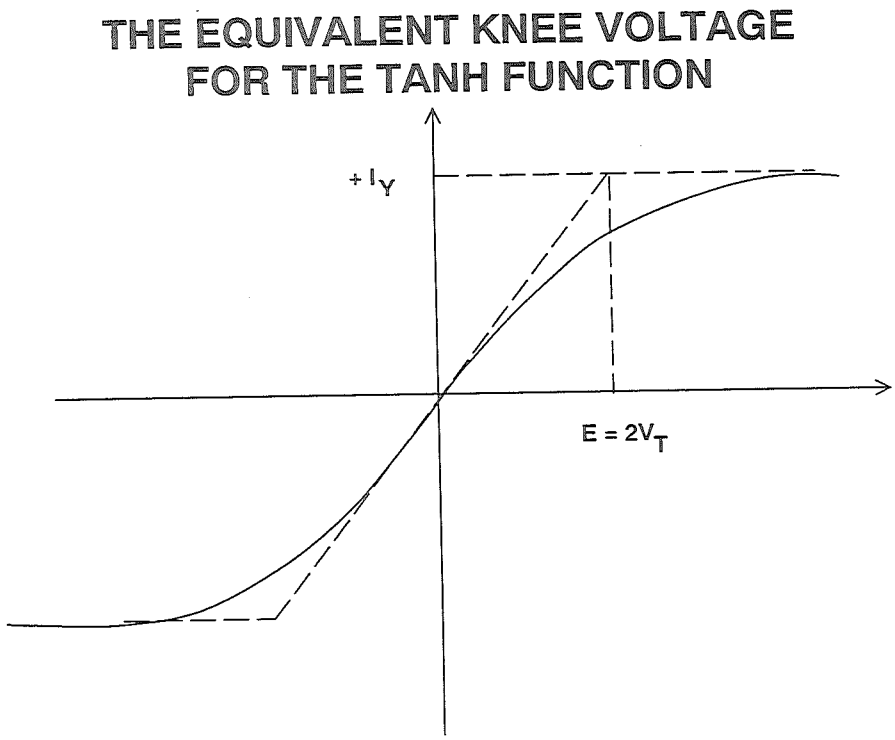

Figure 9.5.4

Now, recalling the lessons taught in Section 9.4, the scaling voltages V_Y and V_Z of a basic logarithmic amplifier are both proportional to this voltage. However, using the later system based on A/0 gain stages (with knee voltage = E) and G/0 summing stages (with peak current = I_Y), the slope voltage V_Y can be rendered arbitrarily accurate and temperature-stable, leaving just the intercept V_Z highly temperature-dependent. It's important to understand that this problem isn't helped by making the tail current of the gain stage (that is, I_E) proportional to absolute temperature: that measure only stabilizes the *small-signal gain* over temperature. The end result is that log-amps based on bipolar differential pairs unavoidably require temperature-compensation of the intercept voltage, V_Z.

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ANALOG DEVICES

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APPLICATION NOTE

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Using the AD834 in DC to 500 MHz Applications: RMS-to-DC Conversion, Voltage-Controlled Amplifiers, and Video Switches

by Mark Elbert and Barrie Gilbert

INTRODUCTION

The AD834 is the fastest four quadrant multiplier available, having a useful bandwidth of 800 MHz, compared to the 60 MHz bandwidth of the AD539 two-quadrant multiplier, the 10 MHz bandwidth of the AD734 four-quadrant multiplier, or the 1 MHz bandwidth of the industry-standard AD534 four-quadrant multiplier. Its monolithic construction and high speed makes the AD834 a candidate for such HF applications as balanced modulation-demodulation, power measurement, gain control, and video switching, at frequencies that were previously beyond the scope of analog multipliers.

The AD834 does not sacrifice accuracy to achieve its speed. In common with all of the Analog Devices multipliers, laser trimming is used during manufacture to null input and output offsets and to establish precise scaling. In typical applications the total static error can be held to less than ±0.5%.

It is available in 8-pin plastic DIP, SOIC, and ceramic packages for the commercial, industrial, and military temperature ranges and operates from ±5 V supplies.

The main challenge in using the AD834 arises from its current-mode output stage. In order to maintain the highest possible bandwidth, the AD834's outputs are in the form of a pair of differential currents from open collectors. This is an inconvenience when a more conventional ground-referenced voltage output is needed. Thus, this application note discusses methods for the accurate conversion of these currents to a single-sided ground-referenced voltage.

These applications include a wideband mean-square detector, an rms-to-dc converter, two wideband voltage-controlled amplifiers, a high-speed video switch, and transformer-coupled output circuits. These applications provide the user with a complete and proven solution, in many cases including recommended sources for critical components.

OVERVIEW OF THE AD834

The AD834, shown in block schematic form in Figure 1, is the outcome of Analog Devices' continuing dedication to high-accuracy analog signal processing. In particular,

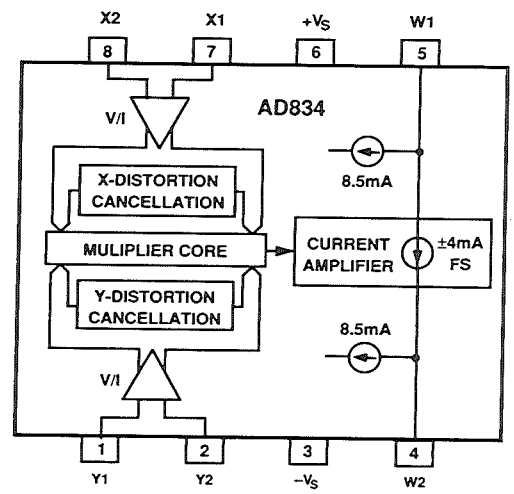

Figure 1. AD834 Block Diagram

it incorporates the experience gained in twenty years of manufacturing analog multipliers. The part is constructed on a 3 GHz epitaxial bipolar transistor process using laser-trimmed thin-film resistors. Attention to many subtle details has resulted in unusually low distortion and noise. Figure 2 shows a more detailed, but still simplified, circuit schematic.

The X- and Y-inputs are applied to high-speed voltage-to-current (V/I) converters, having a transresistance of 285 Ω and a small-signal input resistance of about 25 kΩ. The full-scale input voltage is ±1 V for both inputs. The input bias currents are typically 45 μA. Therefore, the dc resistance seen by both inputs of a differential pair must be equal to minimize offset voltages, just as for an op amp. Resistors at the inputs also minimize the risk of

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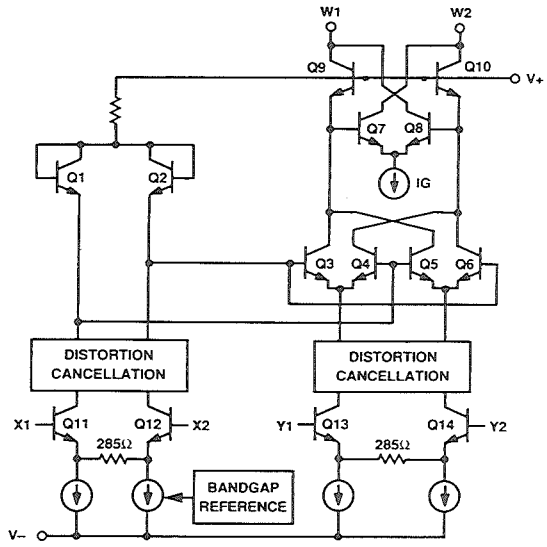


Figure 2. Simplified AD834 Schematic

high frequency oscillations. The V/I converters have a common-mode range of ±1.2 V, using the recommended supply voltages. Within that range, the differential inputs exhibit a common-mode rejection of 70 dB, conservatively specified for f < 100 kHz. Even-order distortion in the V/I converters is inherently low, while distortion cancellation circuitry is included to reduce odd order nonlinearity to typically ±0.05%.

The *multiplier core* is a well-known translinear circuit. The translinear principle [Ref. 1] exploits the precise logarithmic relationship between the base-emitter voltage (V_{BE}) and collector current (I_C) of a bipolar transistor. The input and output signals of translinear circuits are always in current form. Voltage swings at the internal nodes are very small, so that parasitic junction capacitances do not have to be charged and discharged, a common cause for bandwidth reduction and slew-rate limiting. Thus, translinear multiplier cells are inherently fast; they are also readily implemented in monolithic form. However, they can introduce distortion if not carefully designed.

This distortion is due primarily to emitter area mismatches and ohmic resistances in the core transistors (Ref. 2). Using the traditional convention in naming the channels, as shown in Figure 2, the X channel is susceptible to these effects, while the Y signal-path is essentially linear (the four output devices, Q3 through Q6; behaving in many respects like common-base stages, or cascodes). Therefore, the signal requiring the lowest possible distortion should always be handled by the Y channel. For example, in a balanced modulator application, the carrier (local oscillator voltage) should be applied to the X input and the baseband signal to the Y input.

The output from the core is in the form of a pair of differential currents. Now, the scaling of these currents is customarily controlled by adjustment of the bias currents in the V/I converter used on the X-input, which also determines the currents in the diode-connected transistors, Q1 and Q2.

In classical voltage-output multipliers, the range of adjustment needed to absorb the inevitable resistor mismatches is small, and this method of trimming the scaling factor is acceptable. In the AD834, however, the transfer function involves the two input voltages V_X and V_Y, the scaling voltage (generated in the band-gap reference circuit, and trimmed to an accurate value which is assumed here to be 1 V) and the output current, I_W:

$$I_W = \frac{V_X V_Y}{1V} \cdot \frac{I}{R} \qquad (1)$$

In this expression, the value of a resistance, R, determines the calibration of the output current. As fabricated, thin-film resistors have an initial uncertainty which can be as large as ±20%, and the customary methods of trimming the scale factor would result in other compromises (for example, erosion of the available signal range in the X-input V/I converter).

Therefore, the AD834 uses a "Gilbert gain-cell" [Reference 3] after the core to provide the needed adjustment of the effective value of R, which, in fact, is achieved by varying the current gain of this cell through trimming the current I_G. R, after the I_G trim, has an effective value of 250 Ω, resulting in a full-scale output current of ±4 mA when both inputs are at their full-scale value of ±1 V. The typical current-gain is 1.6, and because this type of amplifier is very fast and buffers the core outputs, the overall bandwidth of the multiplier is actually enhanced over that which would be obtained using the core outputs directly.

The bias currents from the core, and the gain-setting current I_G, result in a fairly large standing current—typically 8.5 mA—which flows into the outputs W1 and W2 (Pins 4 and 5). Only the *differential* output is precisely specified to be ±4 mA.

The output currents can be converted back to voltages in a variety of ways. In the simplest case, load resistors connected to the positive supply might be used, but these do not convert the (two) differential outputs to a single-sided voltage.

For the AD834 to operate properly, the output Pins (4 and 5) must be pulled above V+ to avoid saturation of Q7–Q10. To avoid using a separate supply to do this, several of the circuits included here use a voltage-dropping resistor in series with the positive supply Pin (6) of the AD834; this is a higher value than necessary for decoupling purposes.

This dropping resistor lowers the voltage at Pin 6 to provide an extra margin of bias for the output transistors. For example, in the mean-square circuit in Figure 3, 11 mA of quiescent current across the 169 Ω dropping resistor creates 1.86 V of headroom. The decoupling re-

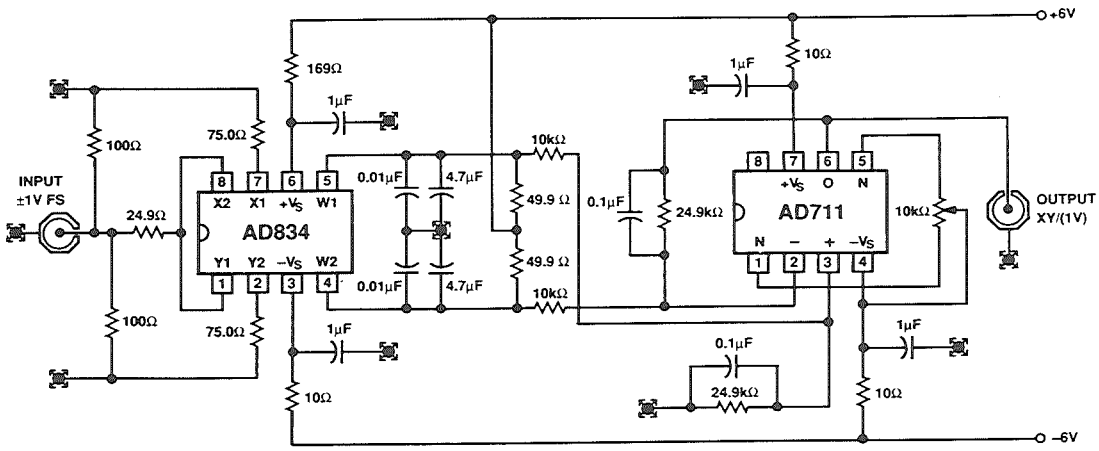


Figure 3. A DC to 500 MHz Mean Square Circuit

sistor in series with the negative supply to Pin 3 is only 10 Ω, since it is included just to decouple the supplies.

Much of this application note, however, is concerned with *more effective ways* of loading the outputs. For example, because they are fully calibrated, the outputs of two or more AD834's can be accurately summed by simply connecting them in parallel, as is done in the rms application discussed later in this application note.

MEAN-SQUARED DETECTOR

We will begin with a discussion of a mean square detector (Figure 3), whose output is a dc voltage proportional to the input power. This circuit is useful in that it requires only a calibrated signal generator and a dc voltmeter to demonstrate the very high speed of the AD834.

The input signal is applied to the X- and Y-inputs connected in parallel. The *instantaneous* output current is thus proportional to the square of the input voltage. The square of a sinusoidal input voltage of amplitude A is an offset cosine at twice the frequency:

$$A(\sin\omega t)^2 = A^2(1 - \cos 2\omega t)/2 \qquad (2)$$

If the input to the AD834 has this sinusoidal form, then the instantaneous output current (using Equation 1) is simply

$$I_W = 2A^2(1 - \cos 2\omega t)\ mA \qquad (3)$$

the average value of which is just 2 mA for the maximum 1 V amplitude sinusoid.

The full-scale differential voltage which would be measured across Pins 4 and 5 of the AD834 is, therefore, 2 mA × (50 Ω + 50 Ω), or 200 mV. This average is extracted by the low-pass filter formed by the 4.7 μF 22 μF (AVX part #SR505E475MMAA and #SR505a223JAA) capacitors in conjunction with the 50 Ω collector load resistors, having a −3 dB frequency of about 650 Hz.

Two capacitors are used in parallel since the 4.7 μF capacitor uses the compact but lossy Z5U dielectric material while the 22 μF capacitor uses a high Q NPO dielectric which ensures good filtering at the highest frequencies. Note that the 4.7 μF capacitors have a −20% to +80% tolerance, so their −3 dB frequency is not accurate, nor does it usually need to be. Further filtering is performed by the capacitors in shunt with the feedback resistors of the AD711 operational amplifier, configured to have a −3 dB frequency of 65 Hz.

Due to finite averaging of the circuit, there will be some ripple for low frequency inputs. For the circuit shown, a 1 kHz input will produce the mean-square plus a −42 dB 2 kHz ripple; for 100 kHz input, the ripple will be only −80 dB. Since the output is band limited, we can use a generic low speed op amp with ample common-mode range, obviating the need for level shifting. The differential gain of the amplifier can be chosen to provide a convenient scale factor.

The full-scale gain of the circuit in Figure 3 is calculated as follows. The average output current is ±2 mA for 1 V (peak) sinusoidal input, which creates ±100 mV across each 50 Ω output load resistor or 200 mV differential. The amplifier is configured for a differential gain of 2.5 (feedback resistance over source resistance), yielding a circuit gain of 0.5 V dc output for 1 V rms input.

The bandwidth of this circuit is limited by package capacitance and inductance. In the 8-pin cerdip, the multiplier's response normally starts to rise at 500 MHz due to package resonance and peaks at 800 MHz before rolling off. A 24.9 Ω resistor at the input dampens the resonance yielding an essentially flat response out to 800 MHz. (The package inductance will be different for a surface mount AD834.) Figure 4 shows the results over frequency for three different power levels using the test configuration shown in Figure 5.

Neglecting the 24.9 Ω in series with the high impedance inputs, the input resistance to the mean square circuit in Figure 3 is 50 Ω. Since the full-scale input range is ±1 V, the maximum measurable power with a 50 Ω input load is 10 mW (20 dBm), assuming a sinusoidal input.

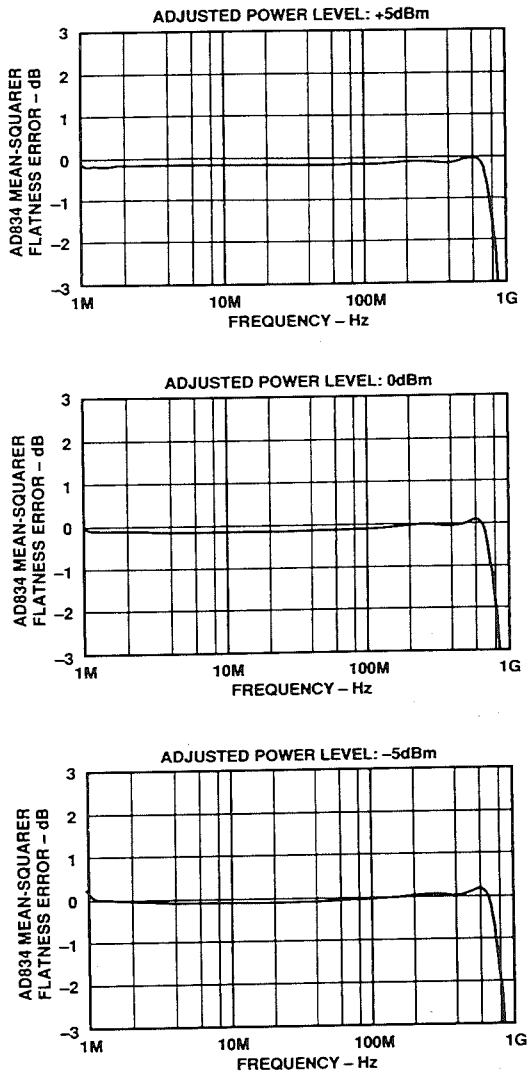


Figure 4. Frequency Response of Mean Square Circuit for Input Power Levels of −5 dBm, 0 dBm, and +5 dBm

For greater input ranges, a voltage divider with a series resistance of 50 Ω at the input will scale down the voltage seen by the AD834 while maintaining a proper termination resistance. For example, if the input signal is applied to a 45 Ω resistor in series with a 5 Ω resistor to ground, then taking the AD834's input from the middle node of the voltage divider provides 20 dB attenuation of the input signal, while maintaining a termination resistance of 50 Ω (45 Ω + 5 Ω).

Detection of low power signals is limited by dc offsets and the common-mode rejection of the op amp. For example, a −20 dBm signal, corresponding to 22.4 mV rms across 50 Ω, would result in a 4.5% error in the presence of only 1 mV of offset in the op amp. A 10% error can occur if the AD834's X channel offset is just 2 mV.

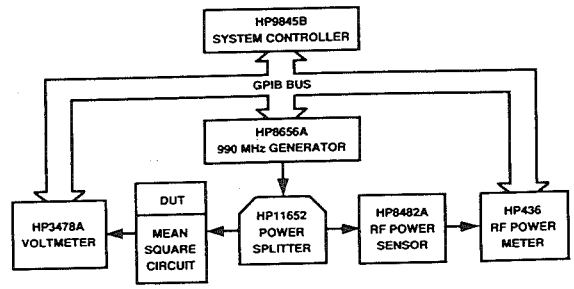


Figure 5. Test Configuration

RMS-TO-DC CONVERTER

The root mean square (rms) circuit (Figure 6) is little more than the mean square detector circuit described above followed by a square root circuit. The frequency response is determined by the front end squarer and output filter. From the mean-square discussion, the squarer functions well past 500 MHz, while the lower −3 dB frequency response is 340 Hz (100 Ω and 4.7 μF). Note that a resistor divider network at the input determines the full-scale input voltage to be ±2 V peak.

The square root function is performed by a squaring AD834 in the feedback loop of an AD711 operational amplifier. The 2N3904 transistor functions as a buffer. The resistive divider network (two 100 Ω) between the buffered output and the X and Y channel inputs of the AD834 used in the square root section determines the output scaling to be ±2 V full scale.

The outputs of the two AD834s are current-differenced. Accurate output differencing and summing is possible owing to the precision of the laser trimmed AD834 output signal current scaling. The AD711 forces the difference between the two AD834 signal current to zero. Any error in the nulling generates a voltage across the two 100 Ω pull-up resistors.

After additional filtering and level shifting by the 15 kΩ, 85 kΩ, and 0.1 μF network, the residual error is amplified by the full AD711 open loop gain. The amplified error signal forces the AD834 in the feedback loop to match its output to the mean-squaring AD834's output. The error is nulled when the rms circuit's output is equal to the square-root of the circuit's input mean-squared, hence the rms function.

The accuracy of the circuit at small signal levels is limited by inevitable offset voltages. While a nominal 0 V input with a 1 mV error to a mean-square function generates a 1 μV output error, the same input error generates a 31.6 mV output error through a square root circuit.

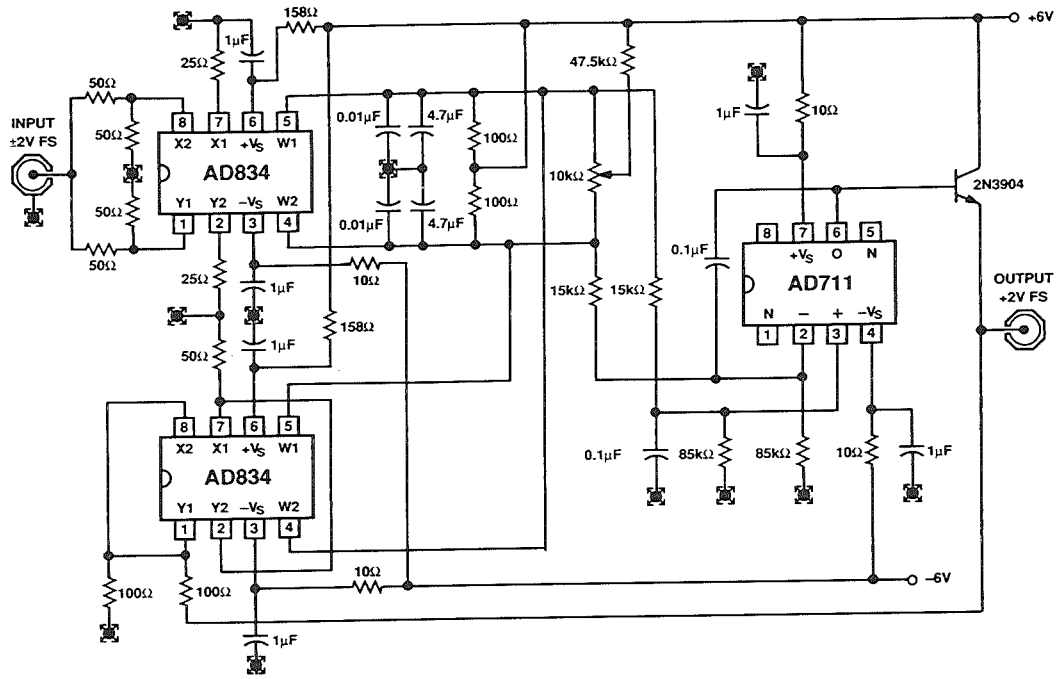


Figure 6. DC to 500 MHz RMS-to-DC Converter

DC COUPLED VCA APPLICATIONS

Where the dc response of the AD834 cannot be discarded, some form of level shifting, either passive or active must be employed, since high speed op amps often have inadequate common-mode range. The following applications show the use of active and passive level shifting circuits in the implementation of wideband voltage-controlled amplifiers.

A DC TO 60 MHz VOLTAGE-CONTROLLED AMPLIFIER USING PASSIVE LEVEL SHIFTING

Figure 7 shows the schematic of a circuit employing a passive network as a level shifter. The op amp chosen here is the AD5539.

The AD5539 is built on the same process as the AD834 and provides a 2 GHz gain-bandwidth product at high closed-loop gain. Unlike most op amps, the AD5539

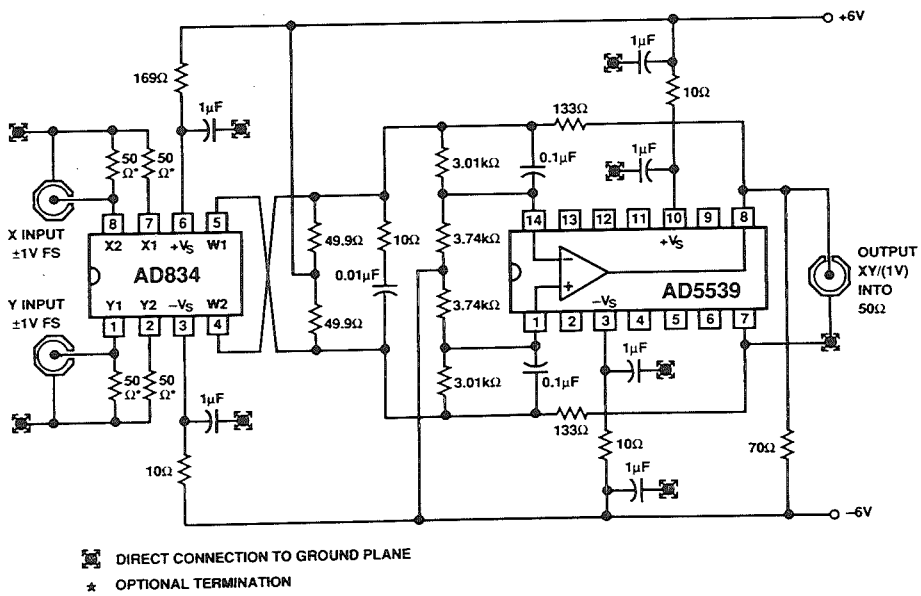


Figure 7. DC to 60 MHz Voltage-Controlled Amplifier Using Passive Level Shifting

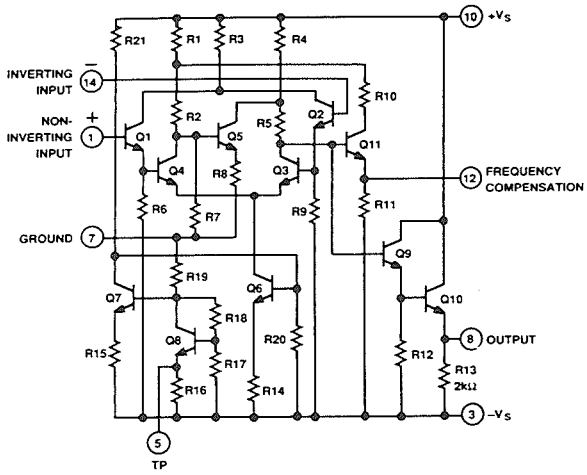


Figure 8. AD5539 Operational Amplifier Simplified Schematic

features a ground pin and an all-NPN output stage which operates in "Class A" to achieve the part's high speed (see Figure 8). Closer examination shows that there is a limited amount of "headroom" between the output node and the inputs, and between these voltages and ground. This, its high speed, and other unusual attributes of the AD5539 require special care in its use.

First, consider the consequences of its Class A output stage. In most op amps, the output can both "pull up" and "pull down" on the load, but the NPN emitter-follower output stage can only pull up. The AD5539 has an internal pull-down resistor (R11) of 2 kΩ, which can only supply two or three milliamps. A general-purpose high-speed multiplier must be able to swing to at least ±1 V while driving the minimum likely load resistance of 50 Ω. At this output level, the load current will be ±20 mA, which must therefore be supplied by an external pull-down resistor. In fact, the pull-down current must be considerably more than this, and requires careful consideration.

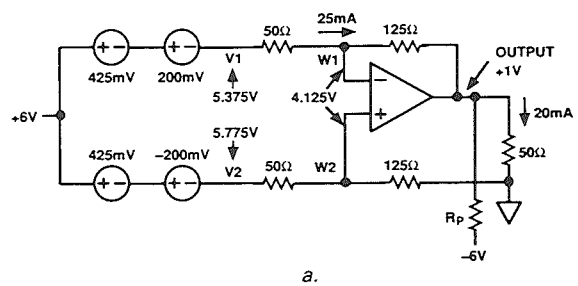
Figure 9 shows how the calculation is done. The 425 mV voltage sources are just "I_BR_C," that is, the standing current of 8.5 mA at the AD834 multiplied by the load resistor R_C, which we have here set to 50 Ω. The 200 mV sources in Figure 9 (a) are the "I_WR_C" generators when the full-scale output current is +4 mA. From here, we calculate V1 – 5.375 V and V2 – 5.775 V.

Next, we calculate the voltage at W2. Because the input current to an ideal op amp is zero, there is no loading at W2 and the voltage is simply V2 multiplied by the attenuation ratio 125/(125 + 50), or 4.125 V. Because the input voltage to an ideal op amp is zero, W1 is at the same voltage, so we can now calculate the current in the upper 50 Ω resistor as (5.375–4.125)/50 mA or 25 mA. Again, there is essentially no current at the input of the op amp, so the 25 mA all flows in the feedback resistor of 125 Ω , resulting in a voltage drop across it of 3.125 V. Finally, we calculate the output as the voltage at W1 (4.125 V) minus this drop; that is, the output is at +1 V.

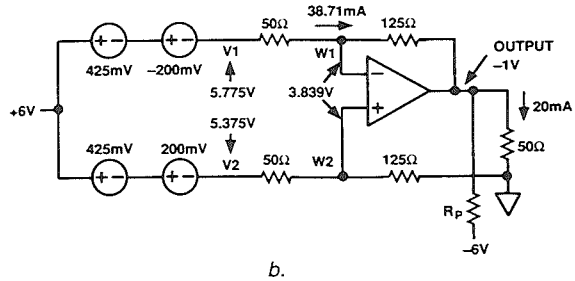
Notice a somewhat surprising result at this point: although a current of 20 mA flows into the load, a larger current, 25 mA, flows in the feedback resistor! This unusual state of affairs is due to the very low value of the feedback resistor needed to reduce the scaling factor to the desired value, and the relatively large voltage needed at the output of the AD834 to ensure proper biasing of its outputs W1 and W2. Thus, even though the load needs to be sourced 20 mA, we still need to provide at least 5 mA in the pull-down resistor R_P to bias the output emitter-follower in the AD5539. The situation gets more severe when the output current of the AD834 is reversed, because we now need to sink 20 mA in the 50 Ω load and the voltage across the feedback resistor is now even higher.

This situation is shown in Figure 9(b). The calculation is exactly as before, and we discover that the current in the feedback resistor is now 39.7 mA. So R_P needs to provide the load current of 20 mA and an additional 40 mA or so in the feedback path, while the voltage across it is 5 V. This would require R_P = 83 Ω. In practice, it should be slightly lower to prevent slew rate limiting the fall time. Also, the feedback resistor will be raised from 125 Ω to 133 Ω to make up for the finite gain of the AD5539 under these heavily-loaded conditions. If we take the parallel sum of the 50 Ω load, the 70 Ω pull-down and about 150 Ω effective feedback resistance, the actual load on the amplifier is only 24 Ω!

The AD5539 is stable for uncompensated gains of greater than 5, and the AD5539 in this circuit is operating at a gain of just over 3. The 0.01 μF and 10 Ω network compensates by throwing away enough open loop gain to be stable when driving a 50 Ω load. For higher impedance loads, the 10 Ω compensation resistor may need to be reduced.



a.



b.

Figure 9. Equivalent Circuits for Calculating the Value of the Pull-Down Resistor

A level-shifting network is included between the nodes W1 and W2, whose average voltage is about +4 V, to the input of the AD5539 which must be close to ground. With the values shown, the op amp inputs are set slightly below ground (about −460 mV). This network halves the low frequency open-loop gain, which has some effect on the dc accuracy in the presence of offset voltages at the input to the AD5539. If output offset is important, a 500 Ω potentiometer should be inserted in series with the 3.74 kΩ resistors and its slider taken to −6 V. It is then adjusted for zero output with both X and Y inputs set to zero.

Note also that the "inner" Pins X1 and Y2 on the AD834 are grounded to minimize HF feedthrough; the resulting phase-reversal at the X input is corrected by swapping W1 and W2.

Figure 10 shows the pulse response with the input pulse applied to the X input and the Y input set to +1 V, indicating a rise time of 6 ns.

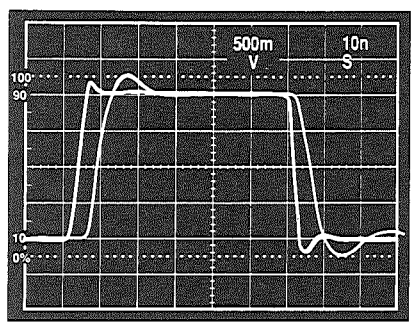


Figure 10. Pulse Response of the DC to 60 MHz Voltage-Controlled Amplifier

Figure 11 shows a set of frequency responses taken on an HP8753B network analyzer for Y inputs of +1 V, 316 mV, +100 mV, and 0 V. In the case of 0 V, the Y input is adjusted to null the input offsets. Note that the high frequency feedthrough is less than −65 dB of full scale (f < 3 MHz).

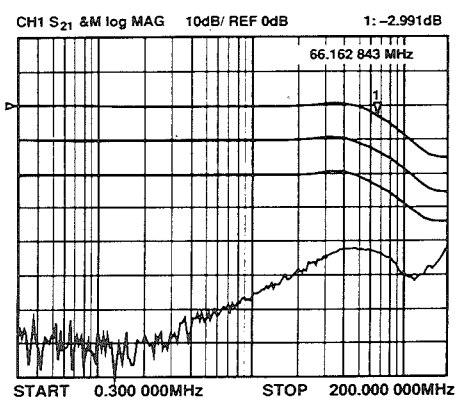


Figure 11. Frequency Response of the DC to 60 MHz Voltage-Controlled Amplifier

A DC TO 480 MHz VOLTAGE-CONTROLLED AMPLIFIER USING ACTIVE LEVEL SHIFTING

Figure 12 (a) shows an active level shifter, using a PNP transistor as a common base stage or cascode. Here, the AD834 is modeled by three ideal current sources, two for the 8.5 mA bias currents and one for the ±4 mA differential signal current. The transistors' bases are tied to +5 V, setting the emitter potential stays at 5.7 V resulting in a voltage of 3.3 V across the resistors R1 and R2 in the absence of signal. Figure 12 (b) shows an equivalent circuit.

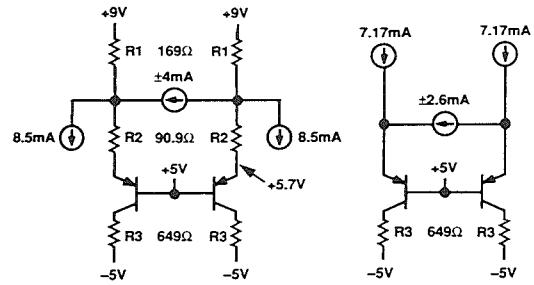


Figure 12. An AD834 Output Stage Using Active Level Shifting

The equivalent dc bias current of 7.17 mA is found by solving for the current flowing into the emitter when the signal current generator is zero. In the ac domain, the signal current generator sees R1 and R2 both tied to low impedance nodes. By inspection, the original signal current has been scaled by:

$$\pm 2.6mA = \pm 4\ mA \times \frac{R1}{R1 + R2} \qquad (4)$$

Since AD834's outputs have very high output impedances, the equivalent series resistance can be ignored. The entire 7.17 mA flowing into the cascode's emitter flows out the cascode's collector, assuming a good α, and across R3. The voltage across R3 is:

$$4.65\ V = 7.17\ mA \times 649\ \Omega \qquad (5)$$

The operational amplifier's inputs are 350 mV below ground and are within the common-mode range of a wideband amplifier.

The bandwidth of a transistor configured as a cascode is the unity gain frequency (f_T) of the transistor, provided that the user does not create any spurious poles. Choosing an R1 and R2 such that their parallel sum is too large for the transistor's parasitic emitter-base capacitance or an R3 too large for the transistor's parasitic collector-base capacitance will create unwanted poles that lower the frequency response of the circuit.

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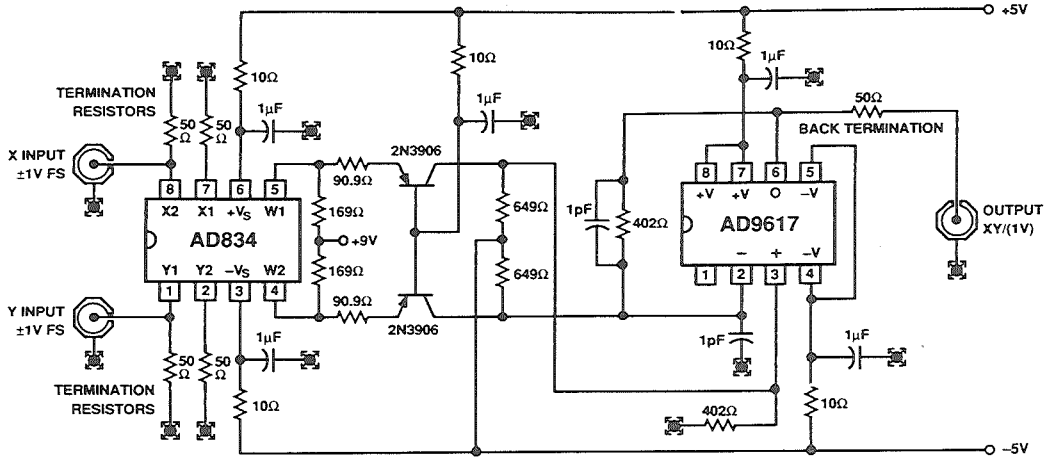

Figure 13. A DC to 480 MHz Voltage-Controlled Amplifier Using Active Level Shifting

Another potential pitfall when using the active PNP level shifter is oscillations at the cascode's emitter. The input impedance of a bipolar junction transistor's emitter is inductive at frequencies approaching its gain-bandwidth product (f_T), while the AD834's output is capacitive. Due to the high bandwidth of the system, these impedances can lead to oscillation.

To prevent such oscillations, the emitter in Figure 12 has been isolated from the AD834's output by R2. This prevents oscillations while providing signal attenuation (gain control) as related in Equation 4. The 2N3906s provide wideband level shifting without resonance or oscillation. Care must be taken when using alternative transistors.

The signal current at the cascodes' collectors is now fed to a wideband amplifier in a differential current to voltage converter configuration as shown in Figure 13. This configuration is similar to an op amp driven current-to-voltage converter which typically follows a current output multiplying digital-to-analog converter.

The AD9617 makes an excellent choice to drive the current to voltage converter. The AD9617 is a second-generation transimpedance amplifier (also known as a current feedback or TZ amplifier) with a fully complementary output stage (unlike the AD5539), and optimized for use with a 400 Ω feedback resistor.

The AD9617 inputs are tied directly to the collectors of the cascodes. The op amp creates a virtual short between the input nodes, forcing all the signal current to flow in the feedback paths. The differential transresistance of the convertor is 400 Ω. The desired scaling can be attained by means of the R1 and R2 attenuation network described above. The full-scale gain of the circuit (X = Y = 1 V) at the AD9617's output is calculated as:

$$2 \times 2.6\,mA \times 400\,\Omega = 2.08\,V \qquad (6)$$

or 1.04 V after the reverse termination resistor. The actual circuit shows a full-scale gain closer to unity.

Figure 14 shows the full-scale step response (−1 V to +1 V) applied to the X input and the Y input set to +1 V demonstrating the circuit's capabilities with a rise time of under 2 ns while exhibiting some overshoot, but no ringing. Note that the output slews at over 500 V/μs.

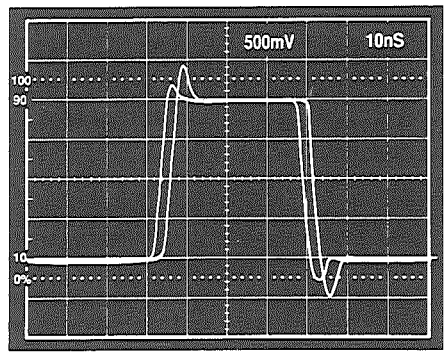

Figure 14. Step Response of the Wideband VCA

Figure 15 shows a set of frequency responses taken on the HP8753B network analyzer for Y inputs of +1 V, 316 mV, +100 mV, and 0 V. The Y input is actually adjusted to null the input offsets. Note that the circuit has a small-signal bandwidth of 500 MHz (at an input power level of 0 dBm). This bandwidth is possible with the two 1 pF capacitors at the inverting node. The high frequency feedthrough is less than −80 dB of full-scale (f < 2 MHz).

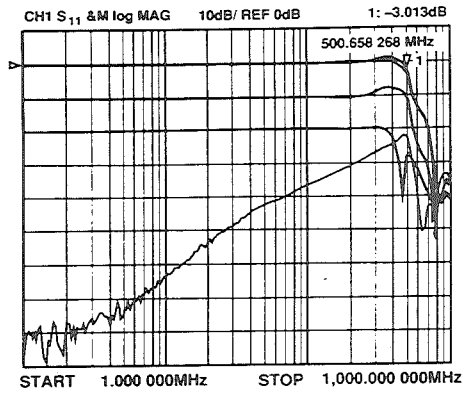

Figure 15. Frequency Response of the Wideband VCA

THE AD834 AS A VIDEO SWITCH

With 0 V or +1 V applied to the X channel as gate control and the video signal to the Y channel, the AD834 becomes a high-speed video switch. Figure 16 illustrates this idea with a high speed current switching circuit centered around an ECL switch. The current flows through either Q1 or Q2, depending on the input voltage. Current switching ensures fast and clean switching to determined levels (+1 V and ground), and allows the user to over- or under-drive the gate input.

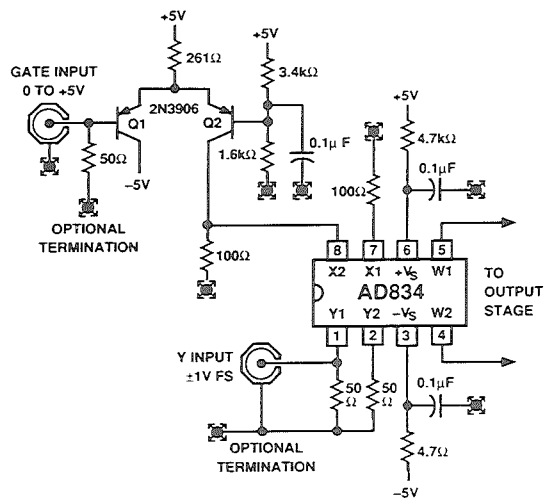

Figure 16. The AD834 as a High-Speed Video Switch

The AD834 switches on as the gate input rises from +1 V through +2 V at the gate circuit input. Below 1 V, Q1 absorbs almost all of the current from the 216 Ω resistor; the 2N3906 transistor is turned off. In this state, the 100 Ω resistor from the X2 input to ground accurately shuts the Y channel off, with Y channel feedthrough to the output measured at −50 dB. With the base of Q2 held at 1.6 V, the transistor's emitter potential is 2.35 V. A steady 10.2 mA (minus base current) from the 261 Ω resistor generates +1 V across the 100 Ω resistor at the X2 input independent of the exact high level of the gate input.

Figure 17 shows a scope photograph of a 1.5 ns rise-time pulse gating a 200 MHz signal. The resulting envelope rise time is 2.7 ns; it has a fall time of 3.0 ns. Although the switched signal may be much slower, the output stage from the AD834 should have a bandwidth greater than 100 MHz in order to maintain an envelope rise time of 3.5 ns.

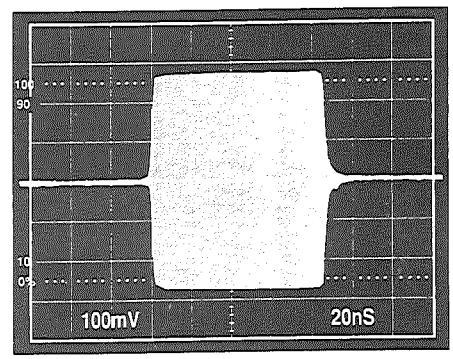

Figure 17. Rise Time of the Video Switch

AC OUTPUT-COUPLING METHODS

In many applications, the dc component at the output can be discarded. In such cases, a wideband buffer can easily ac couple to the AD834 output. The circuits below show the use of simple transformers and baluns for passive, ac coupled output circuits.

TRANSFORMER-COUPLED OUTPUT

Figure 18 shows the use of a center-tapped output transformer, which provides the necessary dc load condition at the outputs W1 and W2, and is designed to match into the desired load impedance by appropriate choice of turns ratio. The specific choice of the transformer design will depend entirely on the application. Transformers may also be used at the inputs. Center-tapped transformers can reduce high frequency distortion and lower HF feedthrough by driving the inputs with balanced signals. Suitable center-tapped transformers include the Coilcraft WB2010PC, which the manufacturer specifies for 0.04 MHz to 250 MHz operation.

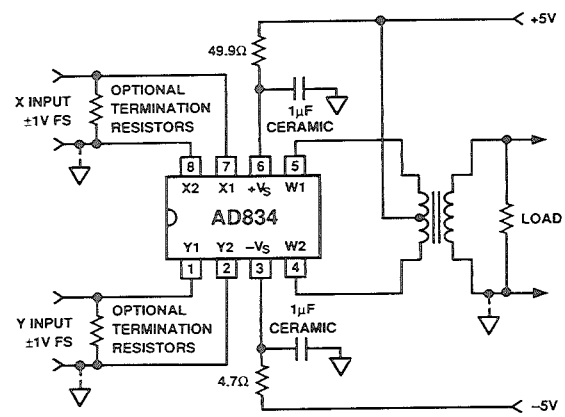

Figure 18. The AD834 with Transformer-Coupled Output

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BALUN-COUPLED OUTPUT

Figure 19 shows a circuit which uses blocking capacitors to eliminate the dc offset, and a balun, a particularly effective type of transformer, to convert the differential (or balanced) signal to a single-sided (or unbalanced) output. A balun consists of a short length of transmission line wound on to a toroidal ferrite core, which converts the 'bal'anced output to an 'un'-balanced one (hence the use of the term).

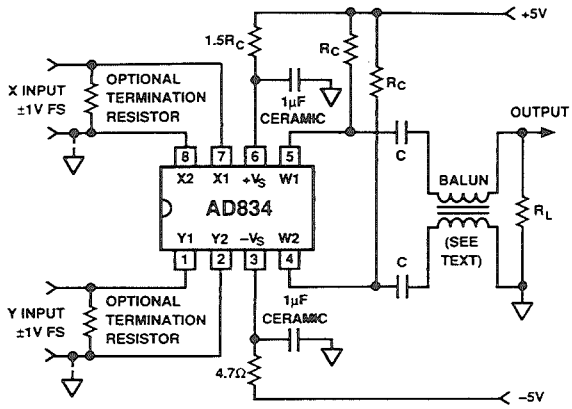

Figure 19. The AD834 with Balun-Coupled Output

Although the symbol used is identical to that for a transformer, the mode of operation is quite different. In the first place, the load should now be equal to the characteristic impedance of the line, although this will usually not be critical for short line lengths. The collector load resistors R_C may also be chosen to reverse-terminate the line, but again this will only be necessary when an electrically long line is used. In most cases, R_C will be made as large as the dc conditions allow, to minimize power loss to the load. The line may be a miniature coaxial cable or a twisted pair.

It is important to note that the upper bandwidth limit of the balun is determined only by the quality of the transmission line; hence, it will usually exceed that of the multiplier. This is unlike a conventional transformer, where the signal is conveyed as a flux in a magnetic core, and is limited by core losses and leakage inductance. The lower limit on bandwidth is determined by the series inductance of the line, taken as a whole, and the load resistance (if the blocking capacitors C are sufficiently large). In practice, a balun can provide excellent differential-to-single-sided conversion over much wider bandwidths than a transformer.

IMPLEMENTATION

Building these circuits requires good high frequency techniques. The circuit schematics suggest suitable layout. **Ground plane is essential for all of the circuits described in this applications brief.** It should cover as much of the component side of the PCB as possible, but not directly underneath the IC or encircling any individual pins. Sockets add to the pin capacitance and inductance, and should be avoided. If sockets are necessary, use individual pin sockets such as AMP p/n 6-330808-3. They contribute far less stray reactance than the molded socket assemblies. Each power trace should be decoupled at the IC with a 0.1 µF low inductance ceramic capacitor, in addition to the main decoupling capacitor. All lead lengths should be kept as short as possible. For lead lengths longer than an inch, stripline techniques should be used.

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[Ref. 2] Gilbert, Barrie, "A Precise Four-Quadrant Multiplier with Subnanosecond Response," *Journal of Solid-State Circuits*, Vol. SC-3, No. 4, pp. 365-373.

[Ref. 3] Gilbert, Barrie, "A New Wideband Amplifier Technique," *Journal of Solid-State Circuits*, Vol. SC-3, No. 4, pp. 353-365.

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Video VCAs and Keyers Using the AD834 and AD811

by Eberhard Brunner, Bob Clarke, and Barrie Gilbert

INTRODUCTION

Voltage-controlled amplifiers (VCAs) built from analog multipliers take one of two forms. In the first, the multiplier acts as a voltage-controlled attenuator ahead of a fixed-gain amplifier. This type of VCA is used in applications where only a moderate maximum gain, but a fairly high maximum loss, are needed. In the second, the variable attenuation is placed in the feedback path around an op amp, which, in fact, implements an analog divider, more suitable for applications requiring high gains.

This application note describes practical circuits in which the wide bandwidth of the Analog Devices AD834 Four-Quadrant Multiplier and the AD811 Current-Feedback Op Amp are exploited to provide a video-quality VCA with a maximum gain of 12 dB (×4) or 20 dB (×10), based on the first of the above methods. A slightly modified form of this VCA, using two multipliers whose outputs are summed, provides the first of two video keyer designs; a second design uses global negative feedback around the multipliers to achieve improved accuracy and some simplification.

A VIDEO-QUALITY VCA

The VCA is shown in Figure 1. The AD834 multiplies the signal input by the control voltage. Its outputs are in the form of differential currents from a pair of open collectors, ensuring that the full bandwidth of the multiplier (which exceeds 500 MHz) is available for certain applications. In this case, more moderate bandwidth is obtained using current-to-voltage conversion, provided by the AD811 op amp, to realize a practical amplifier with a single-sided ground-referenced output. Using feedback resistors R8 and R9 of 511 Ω the overall gain ranges from −70 dB for V_G ~0 to +12 dB (a numerical gain of four) when V_G = +1 V.

The −3 dB bandwidth is 90 MHz (Figure 2) and is essentially independent of gain. The response can be maintained flat to within ±0.1 dB from dc to 40 MHz at full gain (Figure 3) with the addition of an optional capacitor of about 0.3 pF across the feedback resistor R8. The circuit produces a full-scale output of ±4 V for a ±1 V input, and can drive a reverse-terminated load of 50 Ω or 75 Ω to ±2 V. Figure 4 shows the typical pulse response.

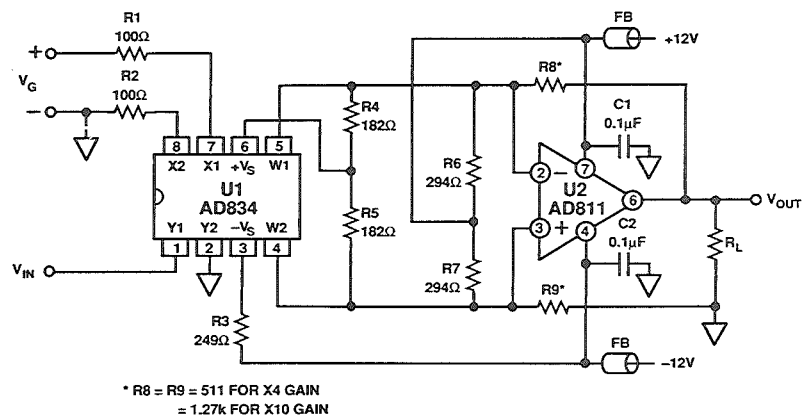

Figure 1. Complete VCA Provides Up to 20 dB of Gain (G = BW = 25 MHz) and a Bandwidth of Over 90 MHz (G = 12 dB)

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The gain can be increased to 20 dB (×10) by raising R8 and R9 to 1.27 kΩ, with a reduction of the −3 dB bandwidth to about 25 MHz (also shown in Figure 2) and a maximum output voltage of ±9 V using the ±12 V supplies. It is not necessary to alter R6 and R7 for the high gain version of the amplifier, although an optimized design would raise these slightly to restore the common-mode voltage at the input of the AD811 to +5 V.

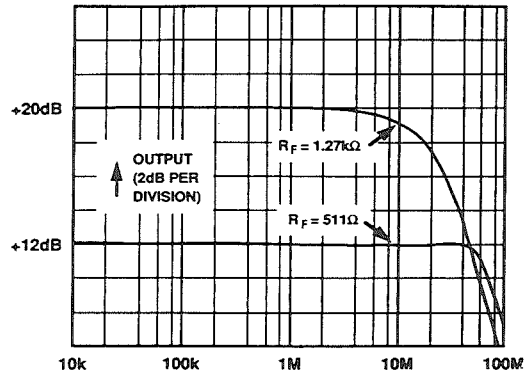

Figure 2. Small-Signal Response of the VCA Shows a −3 dB Bandwidth of 90 MHz for the 12 dB Version and 25 MHz for the 20 dB Version

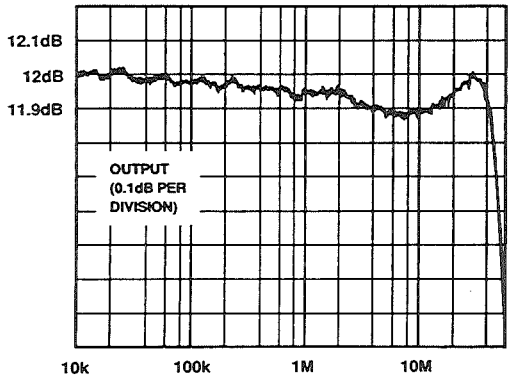

Figure 3. AC Response Can Be Held Flat to Within ±0.1 dB from DC to 40 MHz by Addition of a 0.1 pF Capacitor Across R8

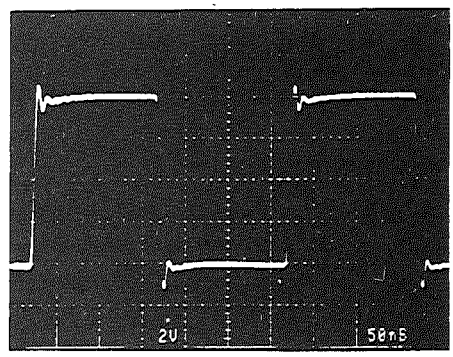

Figure 4. Full-Output Pulse Response for the 12 dB Amplifier

The gain-control input may be a positive or negative ground-referenced voltage, or fully differential, depending on the user's choice of connections at Pins 7 and 8. As shown, a positive value of V_G results in an overall noninverting response. Reversing the sign of V_G simply causes the sign of the overall response to invert. In fact, although we have called this a voltage-controlled amplifier, it can just as well be used as a general-purpose four-quadrant multiplier with good load-driving capabilities and fully symmetrical responses from X- and Y-inputs.

We have used the Y-input of the multiplier for the signal, since this port is slightly more linear than the X-input, and have shown X2 and Y2 grounded. These inputs each draw about 45 μA of bias current, so the grounded (unused) inputs should be terminated preferably in the same resistance as the source, in each case, to minimize offset voltages. The resistance of the signal source may in some cases be essentially zero (as in the case of a transformer-coupled input, or certain signal generators); note that a doubly terminated cable line of impedance Z_O will present a dc resistance of $Z_O/2$ at the input. Resistors R1 and R2 have been included in Figure 1 to minimize the likelihood of small aberrations arising in the signal path in those cases where V_G is derived from a source having poor HF characteristics; they may be omitted in the four-quadrant multiplier application.

High-frequency circuits such as those described herein are sensitive to component layout, stray capacitance, and lead lengths. Use a ground plane and make short, direct connections to ground. Bypass the power-supply connections—inductance in the power-supply leads can form resonant circuits that produce response peaking or even sustained oscillations.

Circuit Analysis

To understand the operation of the VCA, we need first to consider the scaling properties of the AD834, which is actually an accurate nonlinear (two-input) voltage-controlled current source. Figure 5 shows a simplified schematic of the whole VCA.

The exact transfer function for the AD834 would show that the differential voltage inputs at X1, X2 and Y1, Y2 are first multiplied together, divided by the scaling voltage of 1 V (determined by the on-chip bandgap reference) and the resulting voltage is then divided by an accurate 250 Ω resistor to generate the output current. A simplified form of this transfer function is

$$I_W = (X_1 - X_2)(Y_1 - Y_2) \times 4mA \quad (1)$$

where I_W is the differential current output from W1 to W2 and it is understood that the inputs X_1, X_2, Y_1, and Y_2 are expressed in volts. Thus, when both differential inputs are 1 V, I_W is 4 mA; this current is laser-calibrated to close tolerance, which simplifies the use of the AD834 in many applications. Note carefully the direction of this current in determining the correct polarity of the output connections.

It is easy to show that the output of the AD811 is

$$V_{OUT} = 2 \times I_W \times R_F \quad (2)$$

where R_F is the feedback resistor. For R_F = 500 Ω (499 Ω is the nearest standard resistor value), the overall transfer function of the VCA becomes

$$V_{OUT} = 4(X_1 - X_2)(Y_1 - Y_2) \quad (3)$$

which reduces to $V_{OUT} = 4 V_G V_{IN}$ using the labeling conventions shown in Figure 1. As noted, the phase of the output reverses when V_G is negative. A slightly higher value of R_F is used to compensate for the finite gain of the AD811.

Both the AD811 and the AD834 can operate individually from power-supply voltages of ±5 V. However, to ensure proper operation of the AD811's input stage, the common-mode voltage at W1 and W2 must be within the common-mode range of these inputs. There are several ways to do this. We can use separate supplies of ±5 V for the AD834 and ≥ ±9 V for the AD811. Here, we have chosen to show how the VCA can be biased from one dual supply of nominally ±12 V. Figure 5 also helps to understand the dc biasing design.

We begin by deciding to place the AD834's outputs at about +5 V (a little higher than they operate in the other published applications of this product). Under dc conditions, the high open-loop gain of the op amp forces W1 and W2 to assume the same potential. We calculate the values of R_A to introduce the required 7 V drop, by considering the components of the total current in each of these resistors for the zero-signal condition.

First, when V_{OUT} = 0, the current in resistors R_F must be 10 mA (5 V/ 500 Ω). Second, the standing current into W1 and W2, due to the AD834's internal biasing, is 8.5 mA per side. Third, in this application we provide the positive supply voltage for the AD834 (at Pin 6) via resistors R_B which each carry one-half of the total supply current of 11 mA. Thus, the total current in resistors R_A is 24 mA (10 + 8.5 + 5.5 mA) and a value of 294 Ω is chosen (the closest standard value to 7 V/24 mA) for these resistors. Finally, we choose R_B to set the voltage at Pin 6 to +4 V, which is high enough to ensure accurate operation of the AD834 over the full signal and temperature ranges; the nearest standard resistor value is 182 Ω (1 V/ 5.5 mA).

The presence of these resistors (whose parallel sum is 112 Ω on each side) at the input of the op amp causes it to operate at a "noise gain" of 4.45 (499 Ω/112 Ω), but this neither has any significant effect on the dc scaling of the system, nor does it lower the closed-loop bandwidth (as would be the case for a conventional voltage-feedback op amp).

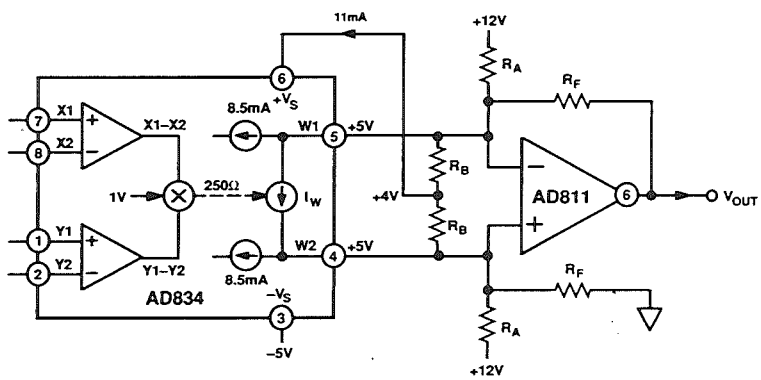

Figure 5. Simplified Schematic of the VCA for Analysis Purposes

A VIDEO KEYER BASED ON THE VCA

Using two AD834s and adding a 1 V dc source, a special form of a two-input VCA called a video keyer (Figure 6) can be assembled. Keying is the term used in reference to blending two or more video sources under the control of a further signal or signals to create such special effects as dissolves and overlays. The circuit described here is a two-input keyer, with video inputs V_A and V_B, and a control input V_G. The output at the load is given by

$$V_{OUT} = GV_A + (1 - G)V_B \quad (4)$$

where G is a dimensionless variable (actually, just the gain of the "A" signal path) that ranges from 0 when $V_G = 0$, to 1 when $V_G = +1$ V. Thus, V_{OUT} varies continuously between V_A and V_B as G varies from 0 to 1.

The operation is straightforward. Consider first the signal path through U1, which handles video input V_A. Its gain is clearly zero when $V_G = 0$ and the scaling we have chosen ensures that it is unity when $V_G = +1$ V; this takes care of the first term in Equation 4. On the other hand, the V_G input to U2 is taken to the *inverting* input X2 while X1 is biased at an accurate +1 V. Thus, when $V_G = 0$, the response to video input V_B is already at its full-scale value of unity, whereas when $V_G = +1$ V, the differential input $X_1 - X_2$ is zero. This generates the second term in Equation 4.

To generate the 1 V dc needed for the "1–G" term, an AD589 reference supplies 1.225 V ±25 mV to a voltage divider consisting of resistors R2 through R4. Potentiometer R3 should be adjusted to provide exactly +1 V at the X1 input.

In this case, we have shown an alternative arrangement using dual supplies of ±5 V for the AD834 and ±12 V for the AD811. Also, the overall gain in this case is arranged to be unity *at the load*, when it is driven from a reverse-terminated 75 Ω line. This means that the "dual VCA" has to operate at a maximum gain of ×2, rather than ×4 as in Figure 1. However, this cannot be achieved by lowering the feedback resistor, since below a critical value (not much less that 500 Ω) the AD811 will become unstable. This is because the dominant pole in the closed-loop ac response of a current-feedback amplifier is controlled by this feedback resistor. It would be possible to operate at a gain of ×4 and then attenuate the signal at the output. Instead, we have chosen to attenuate the signals by 6 dB at the input to the AD811; this is the function of R8 through R11.

The −3dB bandwidth is about 85 MHz and the gain is flat within ±0.1 dB to 30 MHz (Figure 7). Output noise and signal isolation with either channel fully off and the other fully on is about −60 dB to 20 MHz. The feedthrough at 100 MHz is limited primarily by board layout.

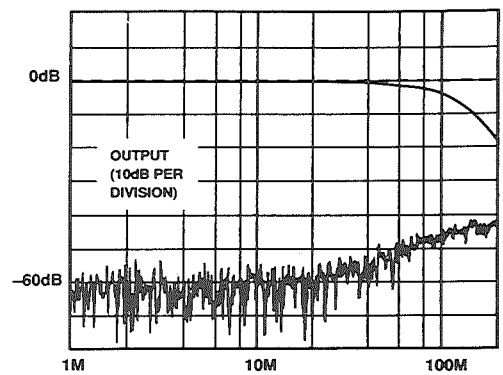

Figure 7. AC Response of the Video Keyer, at V_G = Zero and +1 V; Feedthrough Is About −60 dB

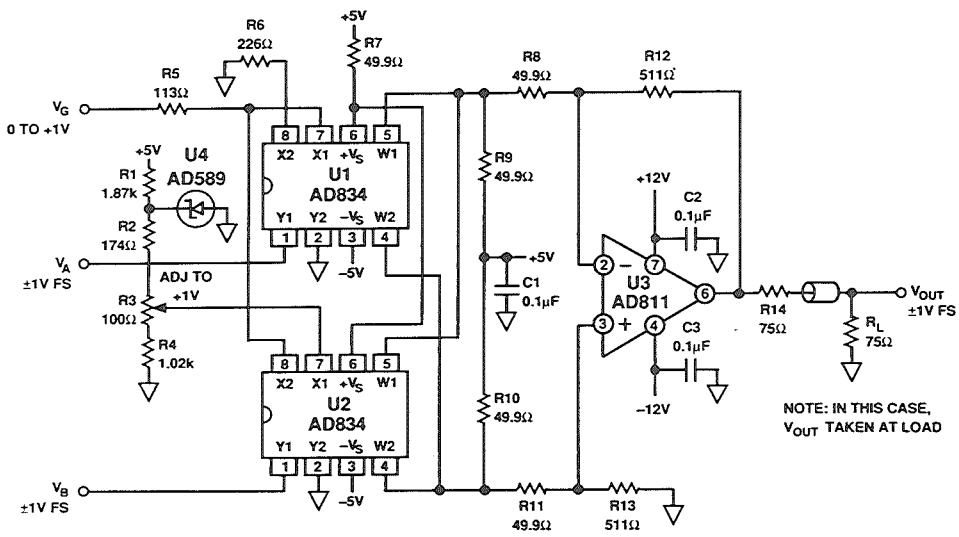

Figure 6. A Two-Input Video Keyer Based on the VCA

A FEEDBACK KEYER

The gain accuracy of the "VCA-based" keyer is dependent on the feedback resistor, R_F. Also, any nonlinearity in the multipliers will show up as a differential gain error. Using an alternative technique, in which the feedback is routed back to unused signal inputs on the AD834s, we can eliminate the feedback resistor and achieve higher accuracy. In the design shown here, we have also used a level-shifting network between the AD834 and the AD811 that eliminates the need for separate power supplies for the two ICs. (In fact, this technique can also be used in the VCAs.)

The basic idea is shown in Figure 8. Note first that V_{OUT} is returned to the inverting inputs Y2 of the multipliers and that their outputs are added. The sum is forced to zero by the assumed high open-loop gain of the op amp. Multiplier M1 produces an output $G(V_A–V_{OUT})$, while M2 produces an output $(1–G)(V_B–V_{OUT})$, where G is $V_G/(1\ V)$ and ranges from 0 to 1. Therefore, the complete system is described by the limiting condition

$$G(V_A–V_{OUT}) + (1–G)(V_B–V_{OUT}) \rightarrow 0 \qquad (5)$$

which requires that

$$V_{OUT} = GV_A + (1–G)V_B \qquad (6)$$

exactly as required for a two-input keyer. The summation of the differential current-mode outputs of the two AD834s is simply achieved by connecting together their respective W1 and W2 nodes. The resulting signal—essentially the loop error represented by the left-hand side of Equation 5—is forced to zero by the high gain of an AD811 op amp.

Figure 9 provides a practical embodiment of these ideas. The gain-control details to provide G and (1–G) terms

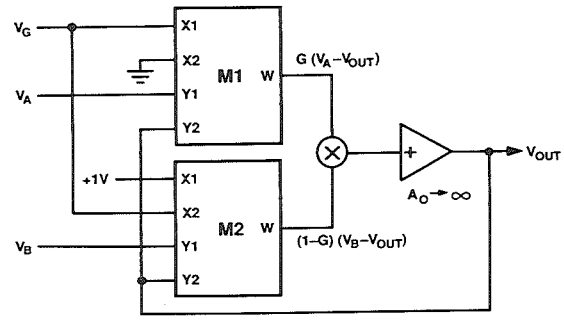

Figure 8. Elements of a Feedback Keyer

are identical to those used previously. The bias currents required at the output of the multipliers are provided by R8 and R9. A dc-level-shifting network comprising R10/R12 and R11/R13 ensures that the input nodes of the AD811 are positioned within an acceptable common-mode range for this IC. At high frequencies, C1 and C2 bypass R10 and R11, respectively.

R14 is included to lower the HF loop gain, and is needed because the voltage-to-current conversion in the AD834s, via the Y2 inputs, results in an effective value of the feedback resistance of 250 Ω (see Figure 5); this is only half the minimum value of 500 Ω required for HF stability of the AD811. (Note that this resistance is unaffected by G: when G = 1, all the feedback is via U1, while when G = 0 it is all via U2.) Resistor R14 reduces the fractional amount of output current from the multipliers into the current-summing inverting input of the AD811, by sharing it with R8. This resistor can be used to adjust the bandwidth and damping factor to best suit the application.

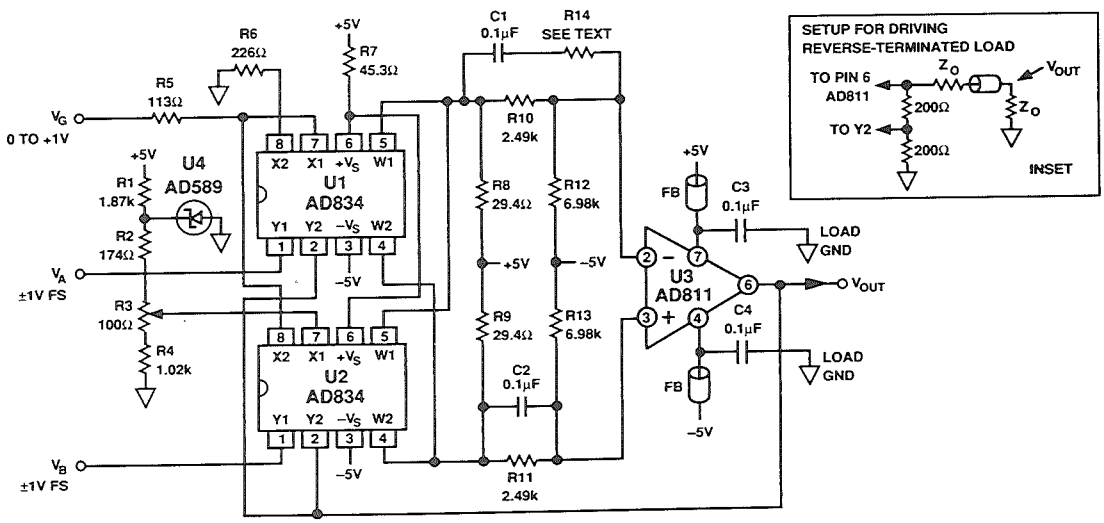

Figure 9. A Practical Embodiment of a Feedback Keyer. The Inset Shows the Feedback Configuration (Gain of ×2) for Driving a Reverse-Terminated Load.

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Figure 10 shows the small-signal ac response of this system of the "A" channel at unity gain and zero gain; as is inevitably the case, there is a small amount of feedthrough at the highest frequencies. Two representative values of R14 are shown; using 402 Ω, the pulse response is considerably overdamped, resulting in a −3 dB bandwidth of 15 MHz, while a value of 107 Ω provides a maximally flat response with a −3 dB bandwidth of 70 MHz.

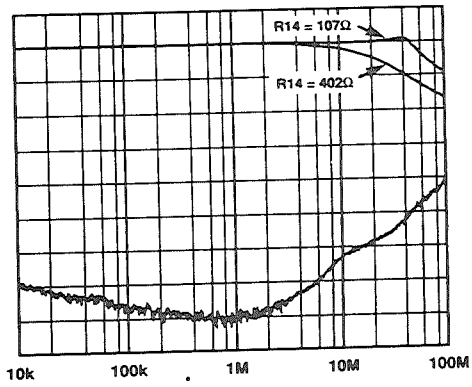
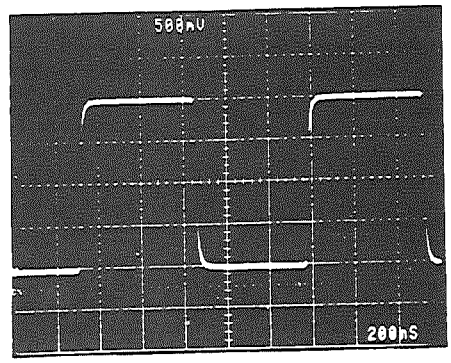
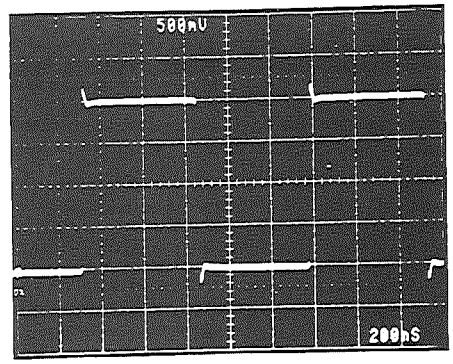


Figure 10. AC Response of the Feedback Keyer. For V_G = +1 V, the −3 dB Bandwidth Is 15 MHz Using R14 = 402 Ω and 70 MHz with R14 = 107 Ω. For These Measurements, R_L = 50 Ω

Figure 11 shows the pulse response at unity gain: in (a) R14 = 402 Ω, while in (b) R14 = 107 Ω. The frequency and pulse responses of the "B" channel, and of the gain-control input are the same, being limited by the output amplifier rather than the AD834s. Likewise, the differential gain and phase behavior will be determined primarily by the AD811; the data sheet should be consulted for more information. The feedthrough at 1 MHz is about −80 dB and −64 dB at 10 MHz and, as before, is eventually limited by board layout. All of these results used a 50 Ω load at the output.



a.



b.

Figure 11. Pulse Response of the Feedback Keyer. In (a), R14 = 402 Ω While in (b), R14 = 107 Ω. For These Measurements, R_L = 50 Ω

Unlike Figure 6's circuit, this keyer provides unity-gain operation. In applications where a reverse-terminated line (50+50 Ω or 75+75 Ω) is to be driven, the gain can be doubled by the inclusion of a resistive divider between V_{OUT} and the Y2 pins; equal resistors of 200 Ω can be used (see the inset in Figure 9). This halving of the feedback voltage also lowers the bandwidth, which can now be restored by reducing, or even eliminating, R14. Figures 12 and 13 show the modified circuit's performance when driving a 50 Ω reverse-terminated line.

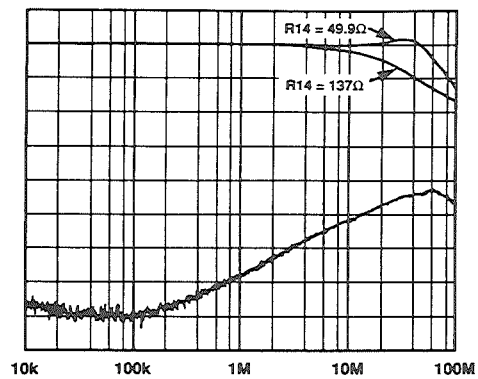
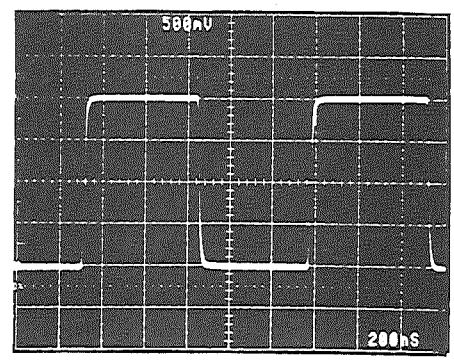
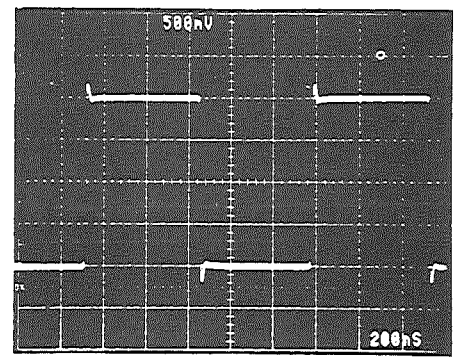


Figure 12. AC Response of the Feedback Keyer, Now Configured for a Gain of ×2. For V_G = + 1 V, the −3 dB Bandwidth Is 15 MHz Using R14 = 137 Ω and 70 MHz with R14 = 49.9 Ω. For These Measurements, R_L = 50 Ω



a.



b.

Figure 13. Pulse Response of the Feedback Keyer Now Configured for a Gain of ×2. In (a), R14 = 137 Ω While in (b), R14 = 49.9 Ω. For These Measurements, R_L = 50 Ω

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