SECTION VIII
VIDEO AND OTHER HIGH SPEED OP AMP APPLICATIONS

- Introduction to Broadcast Video
- Video Applications:
  Video Cable Driving, A Composite Video Sync Tip DC Restorer, A Video Sync Stripper Circuit, A High Performance Video ADC Differential Input Buffer
- Applying Ultra High Speed Op Amps:
  A Low Distortion Drive Circuit for Precision Wide Dynamic Range ADCs, Ultra High Speed Buffers, High Speed Differential Line Drivers and Receivers, A High Speed Three Op Amp Instrumentation Amplifier

SECTION VIII

VIDEO AND OTHER HIGH SPEED OP AMP APPLICATIONS

WALT KESTER, WALT JUNG, DAVE WHITNEY, CHRIS HYDE

INTRODUCTION TO BROADCAST VIDEO

WALT KESTER

Before discussing a few professional video applications, we will review some basics regarding the video signal. The standard video format is the specification of how the video signal looks from an electrical point of view. Light strikes the surface of an image sensing device within the camera and produces a voltage level corresponding to the amount of light hitting a particular spatial region of the surface. This information is then placed into the standard format and sequenced out of the camera. Along with the actual light and color information, synchronization pulses are added to allow the receiving device - a television monitor, for instance - to identify where the sequence is in the frame data.

A standard video format image is read out on a line-by-line basis from left to right, top to bottom. A technique called *interlacing* refers to the reading of all even numbered lines, top to bottom, followed by all odd lines as shown in Figure 8.1.

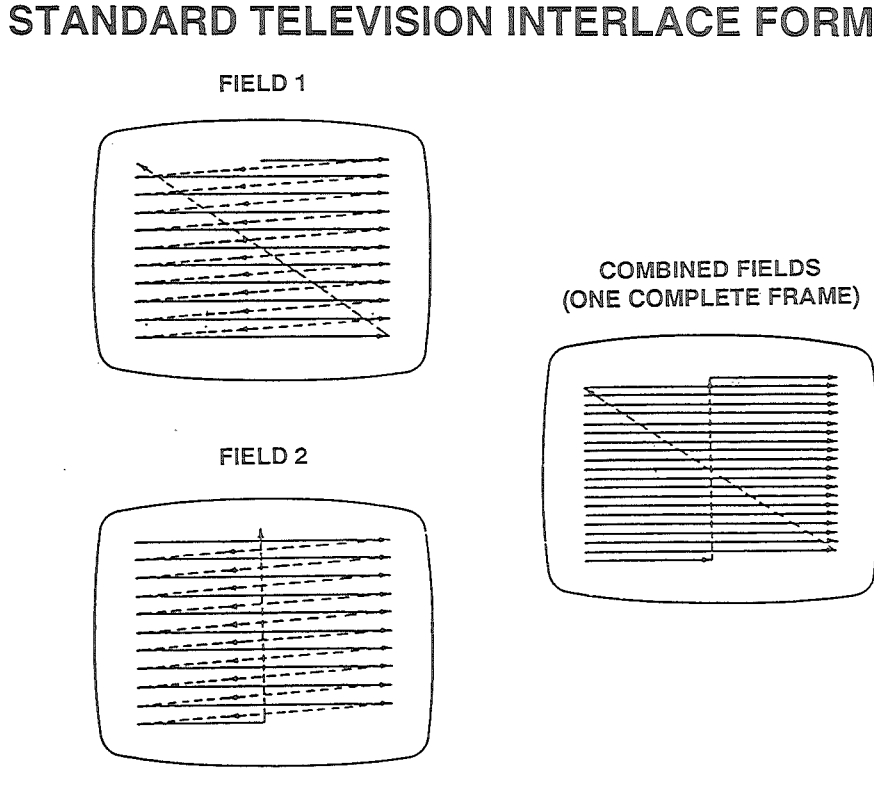


Figure 8.1

The television picture *frame* is thus divided into even and odd *fields*. Interlacing is used to produce an apparent update of the entire frame in half the time that a full update actually occurs. This results in a television image with less apparent flicker. Typical broadcast television frame update rates are 30 and 25 Hz, depending upon the line frequency.

The original black and white, or *monochrome*, television specification is the EIA RS-170 specification which prescribes all timing and voltage level requirements for standard commercial broadcast video signals. The standard specification for color signals, NTSC, modifies RS-170 to work with color signals by adding color information to the signal which otherwise contains only brightness information.

A video signal comprises a series of analog television lines. Each line is separated from the next by a synchronization pulse called the *horizontal sync*. The fields of the picture are separated by a longer synchronization pulse called the *vertical sync*. In the case of a monitor receiving the signal, its electron beam scans the face of the display tube with the brightness of the beam controlled by the amplitude of the video signal. Whenever a horizontal sync pulse is detected, the beam is reset to the left side of the screen and moved down to the next line position. A vertical sync pulse, indicated by a horizontal sync pulse of longer duration, resets the beam to the top left point of the screen to a line centered between the first two lines of the previous scan. This allows the current field to be displayed between the previous one. A single line for the NTSC color video signal is shown in Figure 8.2, and the field timing diagram in Figure 8.3.

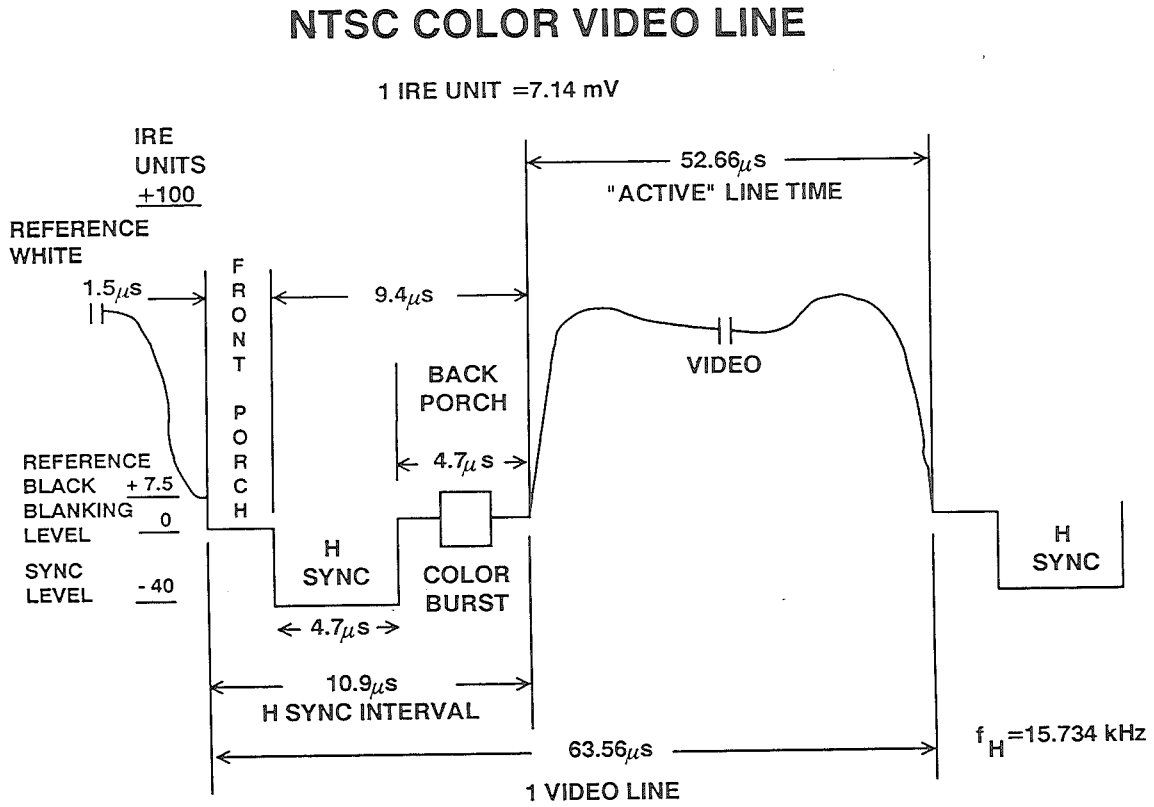


Figure 8.2

NTSC FIELD TIMING DIAGRAM

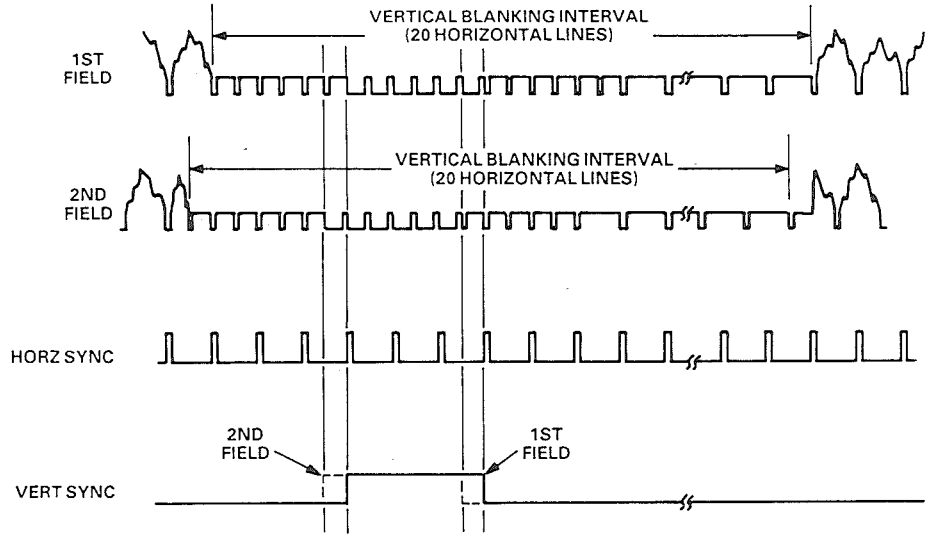


Figure 8.3

A simplified block diagram of the NTSC color processing system is shown in Figure 8.4. The three color signals (RGB: red, green, and blue) from the color camera are combined in a *matrix* unit to produce what is called the *luminance* signal (Y) and two color difference signals (I and Q). These *components* are further combined to produce what is called the *composite* color signal.

In the NTSC system (used in the U.S. and Japan), the color subcarrier frequency is 3.58MHz. The PAL system (used in the U.K. and Germany) and SECAM system (used in France), use a 4.43MHz color subcarrier. Comparisons between the NTSC system and the PAL system are given in Figure 8.5

GENERATING THE COMPOSITE NTSC COLOR SIGNAL

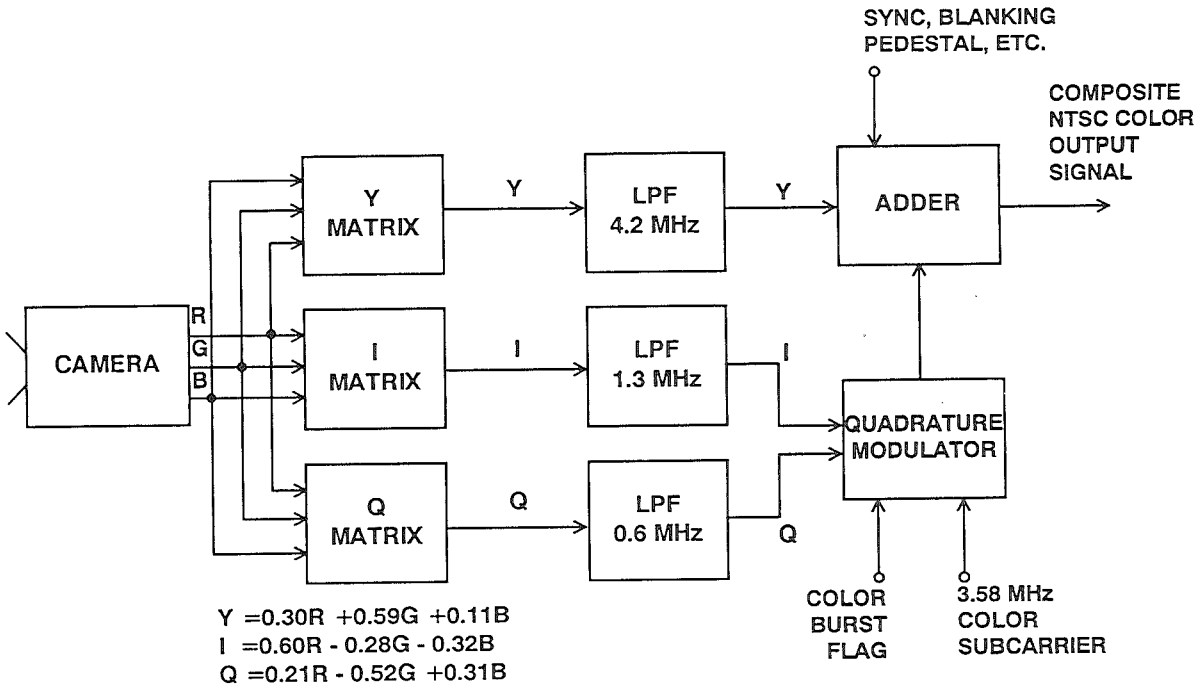


Figure 8.4

NTSC AND PAL SIGNAL CHARACTERISTICS

	NTSC	PAL
Horizontal Lines	525	625
Color Subcarrier Frequency	3.58MHz	4.43MHz
Frame Frequency	30Hz	25Hz
Field Frequency	60Hz	50Hz
Horizontal Sync Frequency	15.734kHz	15.625kHz

Figure 8.5

The color (or *chrominance*) information in the composite video signal is contained in the amplitude and phase of the subcarrier. The intensity of the color is determined by the amplitude of the subcarrier signal, and the color is determined by the phase of the subcarrier signal with respect to the color burst.

The chrominance signal modulates the luminance signal which determines the relative blackness or whiteness of the color. Therefore, in order to preserve color fidelity, it is important that the amplitude and phase of a constant-amplitude and phase color subcarrier remain constant across the entire range from black to white. Any variation of the *amplitude* of the color subcarrier from black to white levels is called *differential gain* (expressed in %), and any variation in phase with respect to the color subcarrier is called *differential phase* (expressed in degrees). Although several percent differential gain and several degrees differential phase is acceptable for home viewing purposes, individual components in the signal path (such as amplifiers, switches, etc.) must meet much tighter specifications. This is because the signal must pass through many circuits from the camera to the home. Individual professional video systems therefore have stringent requirements for differential gain and phase, usually limiting changes to less than 0.1% and 0.1°. These system specifications mandate even more stringent standards for individual components, with the differential gain and differential phase requirements for op amps approaching 0.01% and 0.01°.

Figure 8.6 shows a high resolution setup that uses a HP3314A arbitrary waveform generator and a HP8753A network analyzer to measure differential gain and phase to better than 0.01% and 0.01° accuracy. The arbitrary waveform generator generates a staircase that simulates the luminance (picture level) portion of the video waveform. The network analyzer supplies the color subcarrier waveform, in this case a 4.43MHz color subcarrier. The network analyzer also measures the differences in the color subcarrier's phase and gain by comparing the output of the DUT and the reference signal returned by the HP11850 signal splitter. Note that the 4.43MHz color subcarrier and the staircase signal are summed at the input to the op amp. This summing action superimposes the color subcarrier on the staircase, thus generating the standard video test waveform. The differential phase and gain is defined as the maximum difference in the phase or gain between any of the steps in the staircase waveform. Actual measurements taken on an op amp are shown in Figure 8.7.

The op amp under test is shown connected as a gain-of-two amplifier driving a 75Ω reverse-terminated line. The 75Ω series termination resistor both absorbs reflections from the line and isolates the op amp from the capacitive load presented by the line. The 75Ω termination resistor and the 75Ω load form a voltage divider, so the net gain from the input to the DUT circuit to the load is unity.

PRECISION MEASUREMENT OF DIFFERENTIAL GAIN AND PHASE

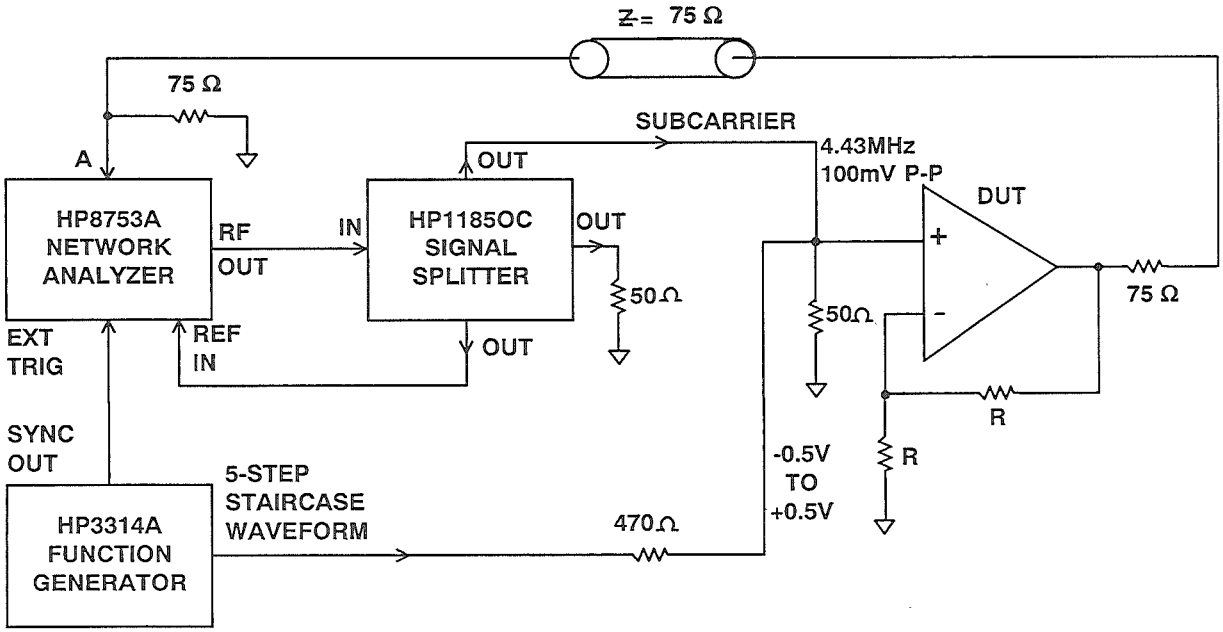


Figure 8.6

DIFFERENTIAL GAIN AND PHASE MEASURED WITH PRECISION TEST SET

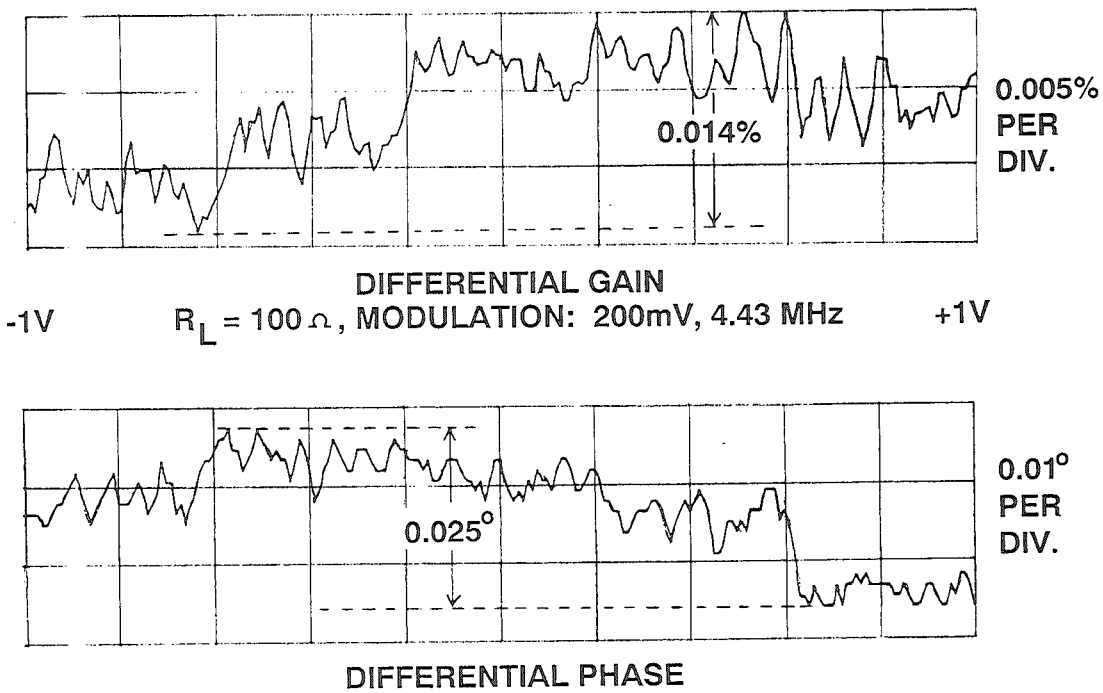


Figure 8.7

VIDEO CABLE DRIVING

WALT JUNG, DAVE WHITNEY

The recently introduced Analog Devices AD811 is the most up- to-date as well as the highest performer in a growing line of transimpedance amplifiers. Like such forerunners as the AD844, the AD846, the OP-160/OP-260, and the AD9617/AD9618, the AD811 is aimed primarily at high speed AC applications. While the part's mainstay uses are intended to be broadcast, studio and HDTV video signal processing, it should also find diverse other applications.

Amplifier categories such as those requiring wide band, large signal, low distortion operation are candidates. Some examples are signal generators and other lab instruments, radar IF and ultrasound amplifiers, medical instrumentation, gamma detectors, ADC & DAC input/ output buffers, and other demanding applications.

Built on AD's advanced high speed complementary bipolar (CB) process, the AD811 achieves new highs for performance vis-a- vis many industry predecessors. Highlights include a bandwidth of over 100 MHz and a SR of 2500 V/μs, combined with an output current capability of more than 100mA with very low distortion. In addition the AD811 settles quickly and cleanly; for a 2V step the time is 25ns to 0.1% , while for a 10V step it settles in just 65ns to 0.01%. The AD811 comes in two temperature grades with similar electrical specs. The AD811A is for -40 to +85°C operation, while the AD811S is for -55 to +125°C use. It is supplied a variety of packages, these include 8 pin plastic and cerdip, 16 and 20 pin SOIC, and 20 pin LCC formats. Key specifications for the AD811 are summarized in Figure 8.8.

8

AD811 HIGH PERFORMANCE VIDEO OP AMP KEY SPECIFICATIONS

- 120MHz Bandwidth (3db, G = +2)
- 35MHz Bandwidth (0.1dB, G = +2)
- Video Specs: 0.01% Differential Gain, 0.01° Differential Phase
- Low Distortion: THD = -74dB @ 10MHz
- ±100mA Output Current
- 0.5mV Input Offset, 5μV/°C Drift

Figure 8.8

Most importantly however, the device is specified for premium levels of performance in demanding video applications. The AD811's differential gain and phase is rated as 0.01% and 0.01° respectively (G=2 @ 3.58 MHz, R_L=150Ω). Further, it is also specified for a tight gain accuracy of 0.1dB at 35MHz... a performance parameter important for HDTV systems. In general the above features have optimum accessibility to the designer, since the AD811 is rated for operation from supplies of ±5V to ±15V. While there is some performance degradation with the lower supplies, the part is video characterized for various gains for these supply ranges. As a result, the user knows just what the tradeoffs will be (more on this below).

The basic circuit of the AD811 (not shown) is like many other similar transimpedance ICs. Nonetheless, the performance distinctions setting it apart come from attention to various design details within. With device trimming at the input stage, low offset voltage and bias current result. These are a Vos of 0.5mV and a bias current of 2μA; both low figures for this type of amplifier. In AC terms, an input stage slew enhancement circuit comes into play for large and fast non-inverting signals, allowing closer signal tracking and lower distortion. This removes a problem common in many other transimpedance amps when they operate as followers.

Transimpedance amplifiers as a rule aren't noted for high gain accuracy, for either DC or AC. Open loop gain in a transimpedance amplifier is maximum when the loaded transimpedance (R_t) is high, and the inverting node input resistance (R_{IN}) is low. In the AD811, the typical figures for these parameters are 1.5MΩ (unloaded) and 14Ω, respectively. The open loop gain is equal to R_t/R_{IN}, or 107,000. Even when loaded in 200Ω, the transimpedance only drops to 750,000Ω. The AD811's R_{IN} is 14Ω, and in general, the lower this parameter the better, as low R_{IN} values allow the amplifier to maintain more bandwidth as closed loop gain is raised.. a hallmark trait of the transimpedance topology.

A parallel array of high speed, large geometry complementary transistors is used in the output circuit of the AD811, with current limiting set at ±150mA. With the high gain linearity so provided by the effective output transistors, this allows loads of 100Ω to be driven to ±10V levels with low distortion. In addition, a special drive configuration optimizes gain flatness for various loads, and this stage's low open loop output resistance of 11Ω also contributes to load immunity. In addition to the NTSC video specs already cited, the 10MHz distortion of the AD811 is also low, at -74dBc, and the third order intercept is 43dBm. Harmonic distortion performance of the AD811 is shown in Figure 8.9.

For video designers, a more relevant aspect of the AD811 is that it is fully specified for typical "bread and butter" video uses, that is the circuit environment needed for a direct performance assessment. Figure 8.10 illustrates this point, showing a standard application of a gain-of-2 video buffer or line driver. This circuit replicates a standard NTSC video signal V_{IN}, with the input line terminated in 75Ω. The AD811 stage operates at a gain of 2, driving a pair of 75Ω output lines through 75Ω back terminations. V_{OUT1} and V_{OUT2} are thus individually isolated/buffered unity gain versions of V_{IN}. With the overall terminated gain of unity, this circuit serves well as a low distortion buffer, or a video distribution amp.

AD811 HARMONIC DISTORTION PERFORMANCE
G = +2, R_{load} = 100Ω, V_{out} = 2V p-p

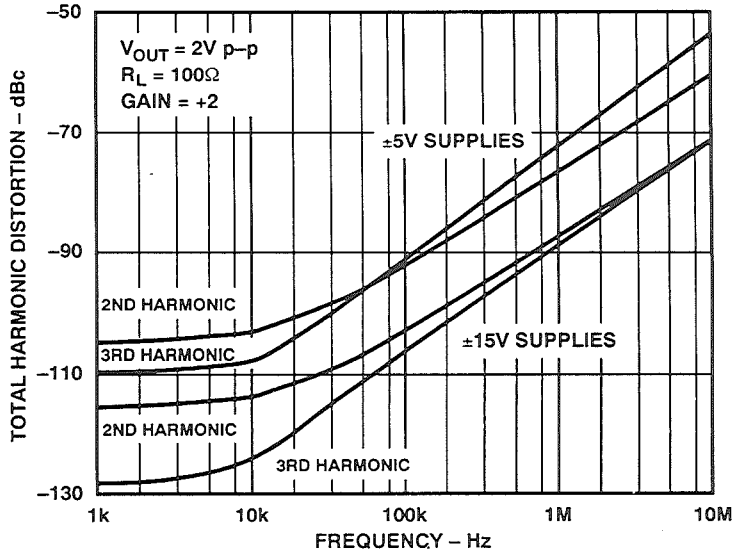


Figure 8.9

AD811 VIDEO LINE DRIVER

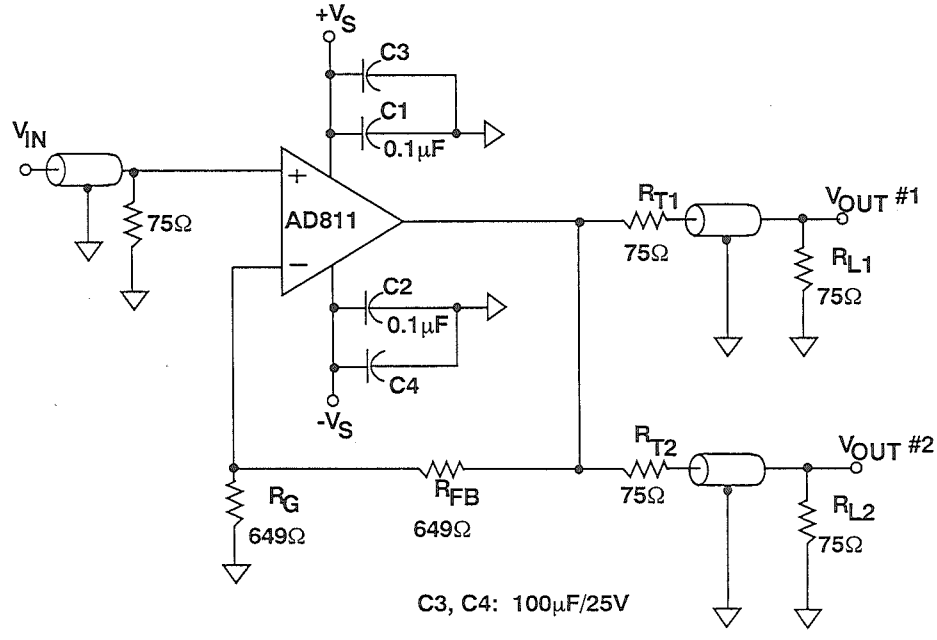


Figure 8.10

Exactly as shown and operated from ±15V supplies, the circuit has a -3dB bandwidth of 120 MHz, and differential gain/phase of 0.01%/0.01° with one line driven (R_L = 150Ω). Driving two lines, the gain errors are essentially the same, while the phase errors rise to about 0.04°. The gain flatness (ripple free) of this circuit is within 0.1dB to 35MHz with ±15V supplies. As expected, lower supplies do degrade performance some, but differential phase is still less than 0.18° with ±5V power. The -3dB point falls to 80MHz, and 0.1dB gain flatness is maintained to 25MHz (see Figure 8.11). Note however in Figure 8.12 that essentially full differential phase is achieved for supplies above ±10V, thereby allowing ±12V supply (frequently used in professional video systems) operation with minimal degradation in video specifications.

Figure 8.13 summarizes performance for this basic circuit for a variety of other gain options (up to ±10), for both power supplies. The resistor values chosen are standard 1% values for various gains, making different setups straightforward. Note that for best accuracy and stability, the use of metal film resistor types are recommended.

Construction of this and other AD811 circuits should be in accordance with high speed rules. A solid, heavy copper ground plane should be used, and circuit layout should be compact with low capacitance, especially at the inverting input pin. In fact, the ground plane area immediately surrounding the inverting input pin should be etched away to insure minimum stray capacitance at this critical node. In addition, the power supplies should be well bypassed. As a minimum, local low inductance/low ESR RF bypass caps

AD811 VIDEO LINE DRIVER FREQUENCY AND PULSE RESPONSE

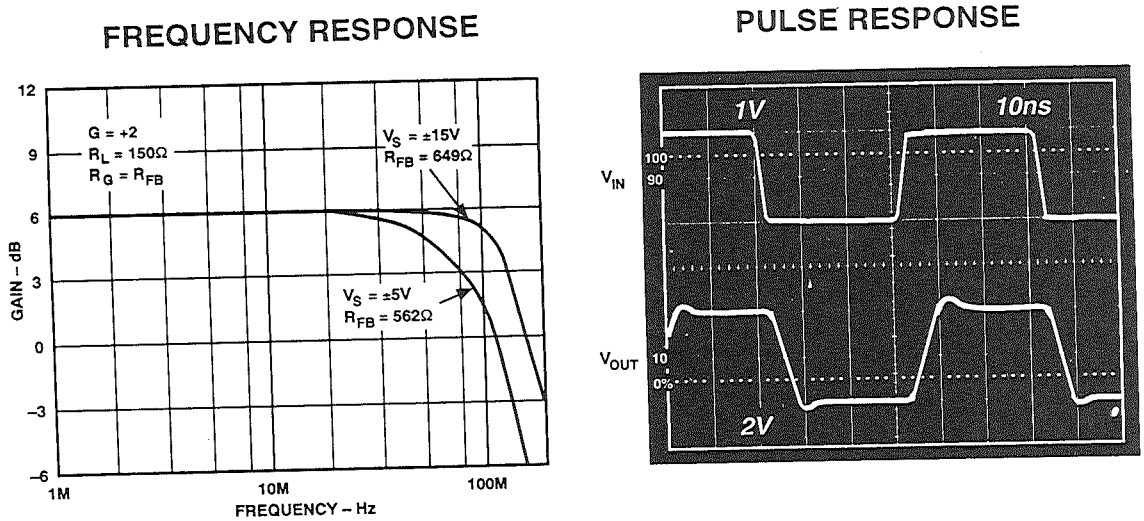


Figure 8.11

AD811 VIDEO LINE DRIVER DIFFERENTIAL GAIN AND PHASE PERFORMANCE

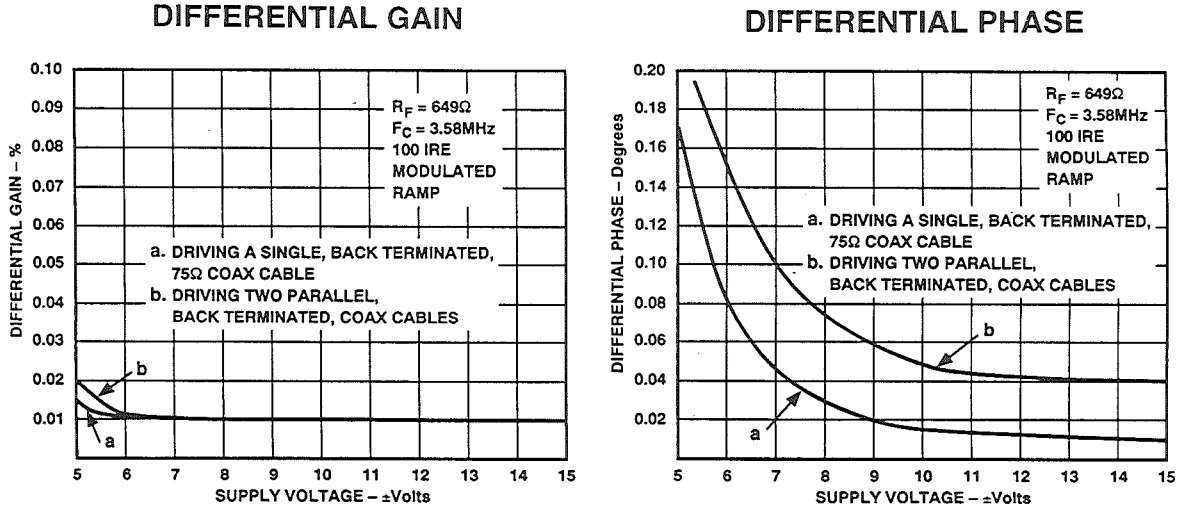


Figure 8.12

AD811 RECOMMENDED RESISTOR VALUES AND RESULTING BANDWIDTHS

V_S = ±15V Closed-Loop Gain	R_{fb} (Ω)	R_g (Ω)	-3dB BW (MHz)
+1	750		140
+2	649	649	120
+10	511	56.2	100
-1	590	590	115
-10	511	51.1	95
V_S = ±5V Closed-Loop Gain	R_{fb} (Ω)	R_g (Ω)	-3dB BW (MHz)
+1	619		80
+2	562	562	80
+10	442	48.7	65
-1	562	562	75
-10	442	44.2	65

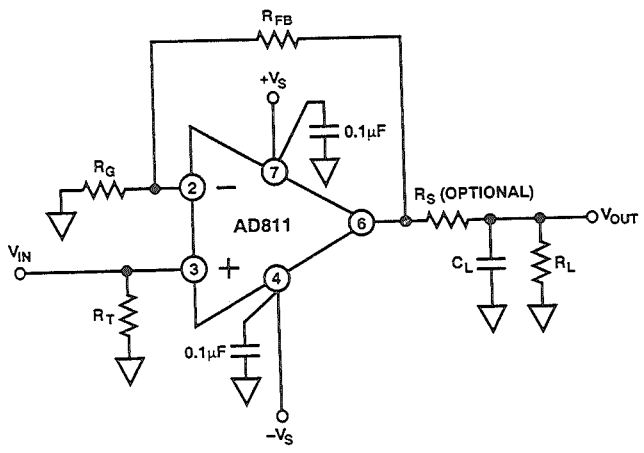
Figure 8.13

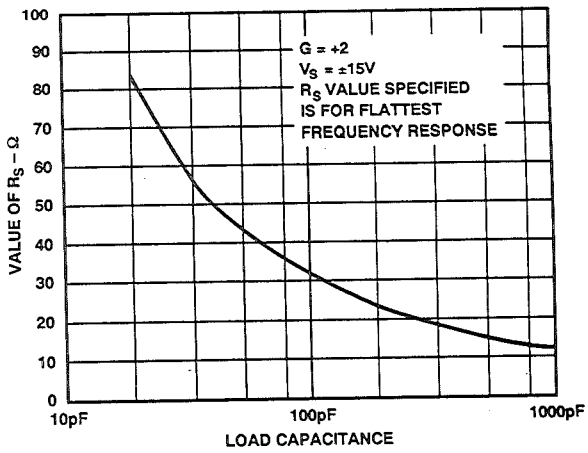
should used right at the device supply pins, shown as C1/C2. These are 0.1μF surface mount chips (or other low inductance type). When driving high peak current loads, these high frequency bypasses should be augmented by local, short lead/large value low ESR electrolytics such as C3/C4, in the range of 47-100μF. These capacitors will carry the transient currents, and can be either tantalum, or aluminum types rated for high frequency (i.e., switching supply types).

The feedback and gain resistor values shown in Figure 8.13 will result in very flat closed-loop responses in applications where the load capacitance is below 10pF. Capacitances greater than this will result in increased gain peaking and overshoot, although not necessarily in a sustained oscillation. The recommended way to stabilize the AD811 for load capacitances greater than 10pF is to add a small resistor in series with the output of the amplifier to isolate it from the capacitive load. The recommended resistor values for various values of capacitive loads are shown in Figure 8.14

Power management can be important with the AD811, as it can dissipate fairly large power levels, even for relatively light loading. The quiescent current drain is about 15mA, which is relatively independent of voltage. As a result, it will consume 150mW at ±5V, and just over 3 times this at ±15V. To minimize power, video applications with low output swings can use supplies of ±10-12V, which yields the best performance with the least power. For applications requiring ±15V supplies, the lower thermal resistance cerdip and LCC packages should be considered. Alternately, a small heatsink on the plastic DIP package will be helpful, such as the Aavid #5801.

DRIVING CAPACITIVE LOADS GREATER THAN 10pF WITH THE AD811





NOTE: R_L = 10kΩ

Figure 8.14

A COMPOSITE VIDEO SYNC TIP DC RESTORER

WALT JUNG, DAVE WHITNEY

A common video signal processing requirement is DC restoration, or clamping. When used with a composite NTSC video signal, sync tip clamping is commonly used. This fixes the most negative excursion of the signal to a fixed DC level, which is usually ground. With a constant input signal level, note that this operation also fixes the remainder of the signal with respect to ground. The circuit of Figure 8.15 is an example of a sync tip clamper, using 2 ICs and a pair of discrete transistors. With a standard NTSC composite video signal at the input, the circuit DC restores the signal to a ground reference, and makes the DC restored and buffered version available at the output, source terminated by 75Ω.

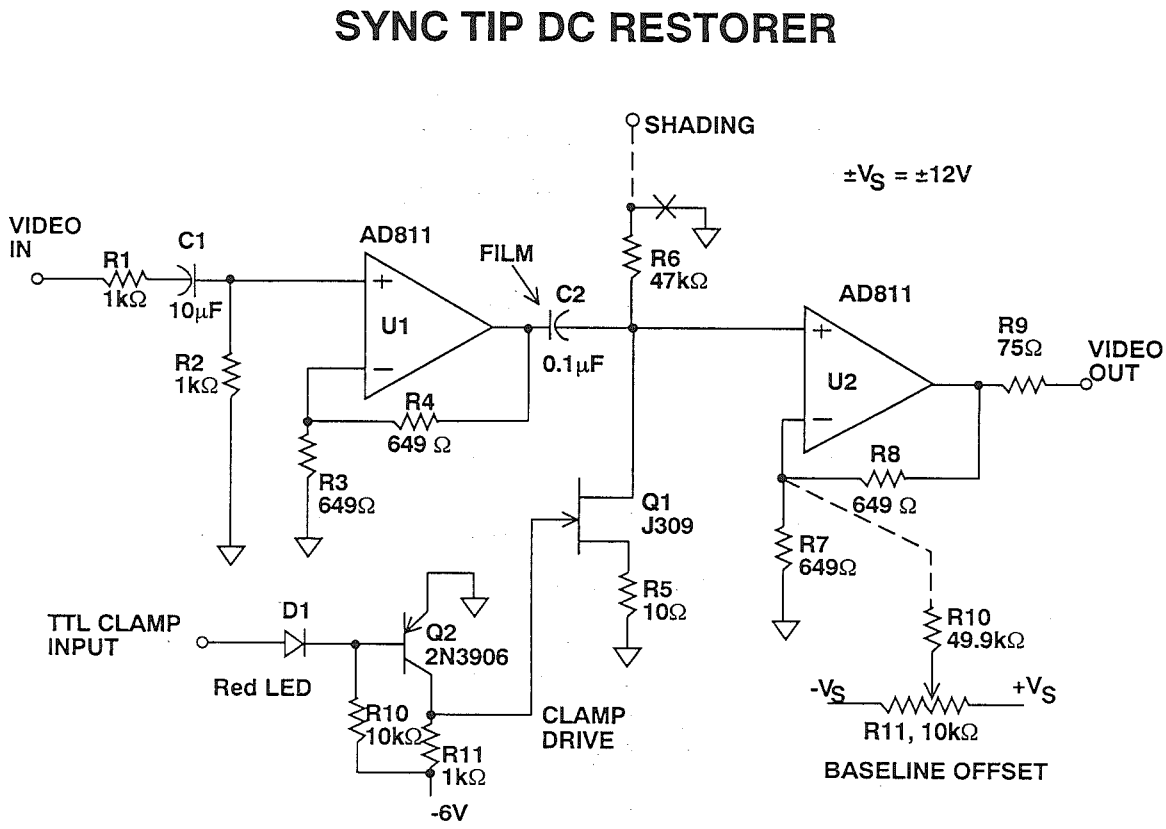


Figure 8.15

In operation, the U1 stage functions as an input line isolator and buffer. The signal at the input is divided by a factor of 2 by R_1 and R_2, and is AC coupled into U1. U1 is an AD811 configured as a wideband times 2 amplifier, by virtue of the R_4-R_3 ratio. With the values shown for R_4-R_3 and the use of ±10V (or more) DC supplies, the 0.1dB bandwidth of stages U1 (and U2) will be more than 30MHz.

The output of U1 drives Q1, a shunt JFET switch through a film coupling cap, C_2. The N channel JFET is a low capacitance, high transconductance unit, chosen for 50Ω or less of on-resistance. The low capacitance allows it to be easily driven from U1, minimizing potential distortion to the signal. The low on-resistance of Q1 and high output current of the AD811 driver stage allows very fast charging of capacitor C_2 between sync tips, at a rate that will be limited to $I_{max(U1)}/C_2$ V/s. With a ±100mA output from the AD811 and a 0.1μF value for C_2, this allows maximum charging rates on the order of ±1 V/μs, applicable during the interval when switch Q1 is on (the clamp sample period). If this period is for example a 0.1μs time, then the circuit can correct ±100mV of baseline change for each clamp sample.

Since the overall video signal is on the order of 1Vp-p and corrections tend to be longer term, these design limits are conservative in practice. For example, for an interfering 60 Hz hum of 1 volt peak, the clamp circuit will see a maximum rate of change or slew rate of

$$SR = f \cdot 2\pi \cdot Vpeak .$$

For 60Hz and 1V, the rate of change is 376.80V/s. In an NTSC 63.5μs line interval, the maximum change of this hum signal is 376.80·63.5e-6 = 0.024V, which is correctable.

The clamp sample period drive signal is derived elsewhere, and is presented to this circuit as a TTL signal at D1-Q2. This signal, , is an active low TTL logic signal, and is timed to occur during the video waveform negative sync tips. The low state signal drives both Q2 and Q1 on, effectively connecting C_2 to ground through Q1-R_5, and so provides the DC reference path to ground described above.

During the remaining time period of a video line time, the switch Q1 is off due to the -6V bias from R_{11}. The bias current of U2 is the main DC load on the C_2-R_6 voltage node during this time, which will tend to ramp ±, slowly charging C_2 with the bias current of U2. Since this current could be as high as 5μA, the baseline ramp error in 50μs time could be (5e-6/0.10e-6)*50e-6 volts, or 2.5mV. However, this is not likely to be a problem, as the typical AD811 bias current is lower, and the video signal is appreciably larger in amplitude.

On the other hand, if an intentional ramp up or down waveform is desired, R_6 can optionally be returned to a variable DC voltage to achieve this effect (by breaking the ground at "X"). This will produce a horizontal shading (a black-to-white or white-to-black background).

Another option possible with the circuit is to introduce a variable DC baseline to the clamped signal, for example to provide a specific bias point for a following stage. The optional bias network consisting of resistor R_{10} and R_{11} can provide this function. The variable DC voltage from R_{11} injects a current through R_{10} which is added in voltage form at the output of U2, effectively allowing signal baseline offset of ±150mV about the DC clamping potential (which otherwise is ground). Note that if this feature is used, the value of R_7 may require some adjustment for exact gain, and that DC voltages ±Vs should be clean.

The output stage U2 is a second wideband AD811, configured as a 75Ω line driver in this case. U2 presents the DC restored video signal to the output, with a level equal to the original input signal.

A VIDEO SYNC STRIPPER CIRCUIT

WALT JUNG, DAVE WHITNEY

Another common video signal processing requirement is the function of sync stripping. In a sync stripper, horizontal and vertical timing information is removed from the composite NTSC video signal and converted to logic levels for further processing. The circuit of Figure 8.16 is a self-contained sync stripper, using 1 IC and a pair of discrete transistors. It is driven from an NTSC composite video signal and delivers TTL compatible positive going sync at the output.

In this circuit the U1 stage performs three functions. First, components L_1-C_2 act as a low pass filter, removing the 3.58MHz chrominance components. U1, an AD811, also is an isolator with gain as well as a buffer to drive the following stage, which is a low input impedance sync tip clamp. The input signal is divided by a nominal factor of 2 by R_1 and R_2-R_3, and AC coupled to the input of U1. U1 is configured as a wideband times 6 amplifier, by the R_5-R_4 ratio. This yields an overall luminance signal gain of three times, from the input to C_3. With the gain values shown and ±5V (or more) DC supplies for U1, the stage can handle normal video signals without clipping at the output.

U1's output drives Q1, a PNP shunt clamp in an unusual configuration. In steady-state DC terms, Q1 is held in saturation by the bias current from R_7, where the emitter is close to ground. Since the AC signal driving Q1 through C_3 is a composite video signal with the sync tips the most negative limit, on a

SYNC STRIPPER GENERATES COMPOSITE SYNC

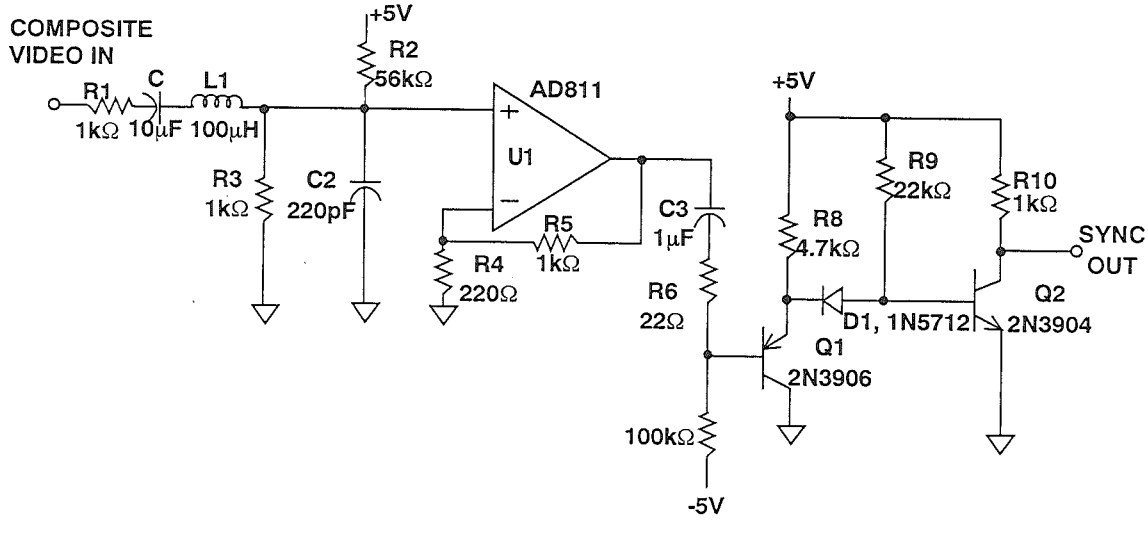


Figure 8.16

dynamic basis Q1 acts as a DC restorer. The negative going video waveform sync tips drive Q1 into hard saturation, and the more positive parts of the waveform bring it out of saturation, where it acts as a linear emitter follower. This action produces a DC restored composite video signal at the emitter of Q1, with the sync tips referred to ground.

The output of Q1 is coupled to the base of NPN switch Q2, through Schottky diode D1. The combination of this diode's forward drop and the V_{BE} of Q2 produce a switching threshold at the base of Q2 which, with consideration of the signal levels, causes Q2 to switch on/off cleanly at about the sync tip 50% amplitude point.

The output from Q2 consists of clean, noise-free sync timing information, positive going during sync tips. This signal is TTL compatible, by virtue of the +5V supply to Q2 as shown. Practical hints in getting the most from this circuit involve some attention to good decoupling of the U1 stage. The high instantaneous currents during the sync tips can generate power supply and/or ground noise. Local bypassing of U1 with large capacitors to the logic supply ground will help to control this, as will a compact layout and the use of a ground plane.

A HIGH PERFORMANCE VIDEO ADC DIFFERENTIAL INPUT BUFFER

WALT JUNG, DAVE WHITNEY

Closely related to video applications are analog-digital- converter (ADC) input buffers. This class of circuit is in some regards even more demanding in performance. The distortion levels are desirably in the -60 to -70dB range for signals around 1V full scale, and up to 10MHz or more in frequency. In addition, high speed ADCs are often difficult to drive in terms of non-linear input capacitance, differential mode operation, and quite importantly, they often use supplies of 5V. All of these factors place demands upon the buffer amplifier used in driving the converter.

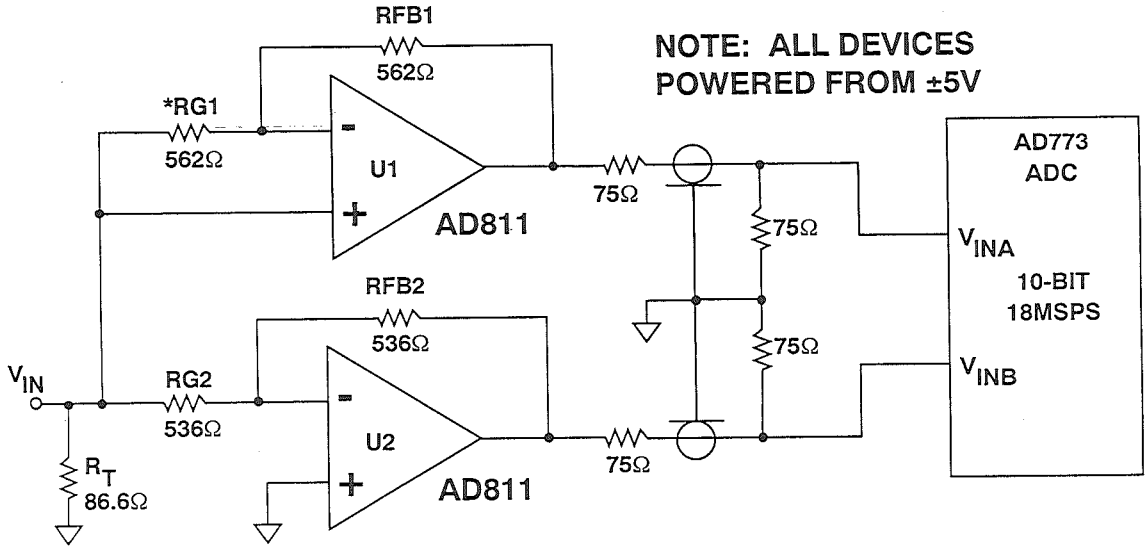
The circuit of Figure 8.17 is useful for driving high speed 10 bit ADCs. Operating from ±5V supplies, it was developed specifically as an interface to the differential input AD773, a 10-bit resolution 18 MSPS pipelined architecture ADC. With minor variation, it can be used with many other converters, both single-ended and differential mode. Since it can operate directly from ±5V, it eliminates the possibility of destructive ADC overdrive with higher supply voltage buffers.

The AD773 ADC operates best when driven differentially between inputs V_{INA} and V_{INB}, with full scale signals of ±500mV. The dual AD811 driver translates a ±500mV single ended signal across R_{Tin} to dual ±250mV signals at V_{INA} and V_{INB}.

In many differentially driven applications, the two output signals should maintain gain and phase flatness for high performance. This is desirable to above the highest frequency of interest, in addition to low signal distortion. In this driver, the AD811s used for U1 and U2 operate as gain/phase matched buffers with precise gains of ±1. While the inverter U2 is conventional, the follower U1 has a distinction which greatly impacts overall performance.

Normally, a transimpedance amplifier such as the AD811 used as a unity gain follower would use just a single resistor for feedback (R_{FB1}). Here however, a dummy input resistor R_{G1} is added, providing a noise gain for U1 like that of U2. With matched devices for U1-U2 and carefully selected resistance values this allows similar gain/phase characteristics, important for the accurate conversion of video and other high resolution signals.

OPTIMIZED AD811 DIFFERENTIAL ADC BUFFER



*RG1 MAKES NOISE GAIN OF U1=NOISE GAIN OF U2

Figure 8.17

This gain/phase matching is quite effective, with results of 0.05dB and 0.5° between the two output signals at 20MHz, loaded as shown. These figures are 5-10 times better than they would be with the use of a conventional follower (i.e., without R_{G1}). Bandwidth of this driver is 80MHz at the -3dB point, and the 0.1dB bandwidth is 25MHz. Second harmonic distortion results at 8MHz with the AD773 using the buffer showed an improvement of about 15dB over more simple drive schemes.

While this example has illustrated driving an AD773 directly, it is worth noting that the line driving capability of the AD811 will allow this driver to be located remote from an ADC, if necessary.

8

APPLYING ULTRA-HIGH SPEED OP AMPS

WALT KESTER, CHRIS HYDE

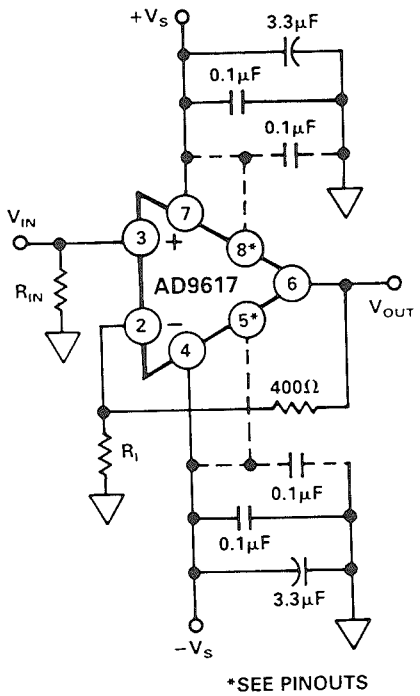
New high speed complementary bipolar processes with matching PNP and NPN transistors having F_ts of approximately 3GHz coupled with proprietary circuit designs have resulted in the development of an entire new class of ultra high speed op amps having bandwidths in excess of 150MHz. These op amps typically operate on ±5V supplies and deliver up to ±3V into video loads. Extremely low distortion and fast settling times are some of the other attractive characteristics. An example of such an amplifier is the AD9617 whose key specifications are given in Figure 8.18

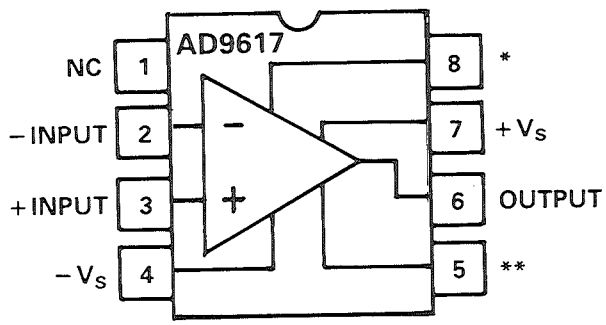
AD9617 CURRENT FEEDBACK AMPLIFIER KEY SPECIFICATIONS

- Usable Closed Loop Gain Range: ±1 to ±40
- Low Distortion: -67dBc @ 20MHz
- Small Signal BW: 190MHz (A_V = +3)
- Settling Time: 10ns to 0.1%, 14ns to 0.02%
- ±5V Power Supplies

Figure 8.18

PROPER LAYOUT AND DECOUPLING IS CRITICAL TO AD9617 OP AMP PERFORMANCE





NOTE: FOR BEST SETTLING TIME AND DISTORTION PERFORMANCE, USE OPTIONAL SUPPLY CONNECTIONS. PERFORMANCE INDICATED IN SPECIFICATIONS IS BASED ON SUPPLY CONNECTIONS TO THESE PINS.

Figure 8.19

AD9617 FREQUENCY RESPONSE AND SETTLING TIME PERFORMANCE

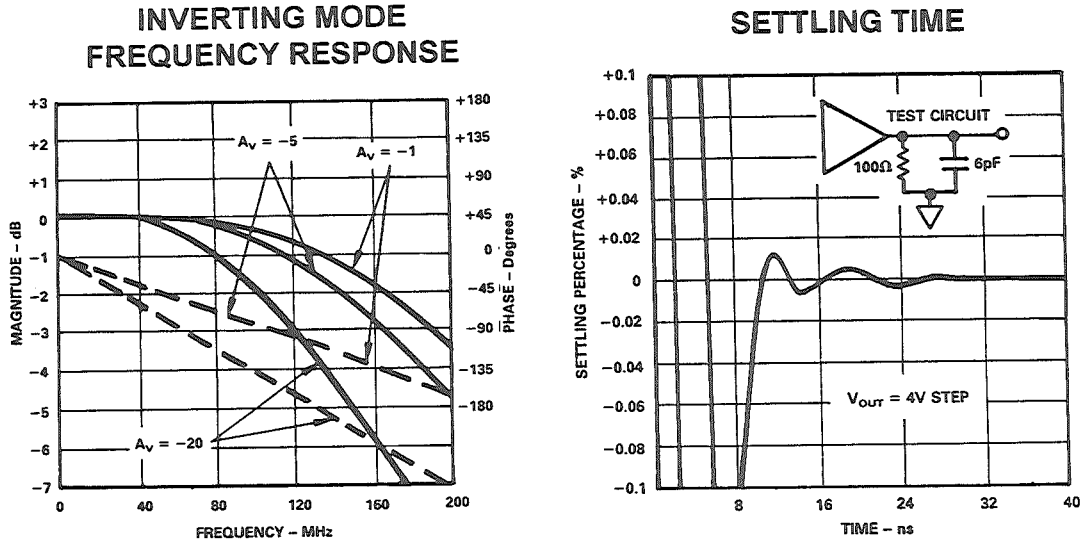


Figure 8.20

In order to achieve performance levels of this type, extreme attention must be given to every detail of PCB layout. Each power supply trace should be decoupled close to the package with a low inductance 0.1μF low inductance ceramic capacitor and at least a 3.3μF tantalum capacitor as shown in Figure 8.19. Gain setting resistors should be chosen for low values of parasitic capacitance and inductance, i.e., microwave, or carbon film resistors. Stripline techniques should be used for lead lengths in excess of one inch. Sockets should be avoided because of their stray capacitance and inductance. If sockets are necessary, individual pin sockets such as AMP p/n 6-330808-3 should be used. Molded socket assemblies are unacceptable! On a proper layout with good decoupling techniques described above, the AD9617 frequency response and settling time characteristics shown in Figure 8.20 will be achieved. Harmonic distortion performance is shown in Figure 8.21 for both 100Ω and 500Ω loads. Note that even when heavily loaded in 100Ω, the harmonic distortion at 100MHz is better than -40dB.

Stray capacitance on the inverting input greater than 5pF will cause gain peaking and increases in settling time. Output load capacitance greater than 20pF will also cause settling time to increase unless the proper value of series isolation resistance is added. The effects on settling time due to input and unisolated output capacitance are shown graphically in Figure 8.22. The proper value of series isolation resistor for various values of load capacitance is shown in Figure 8.23.

AD9617 HARMONIC DISTORTION PERFORMANCE

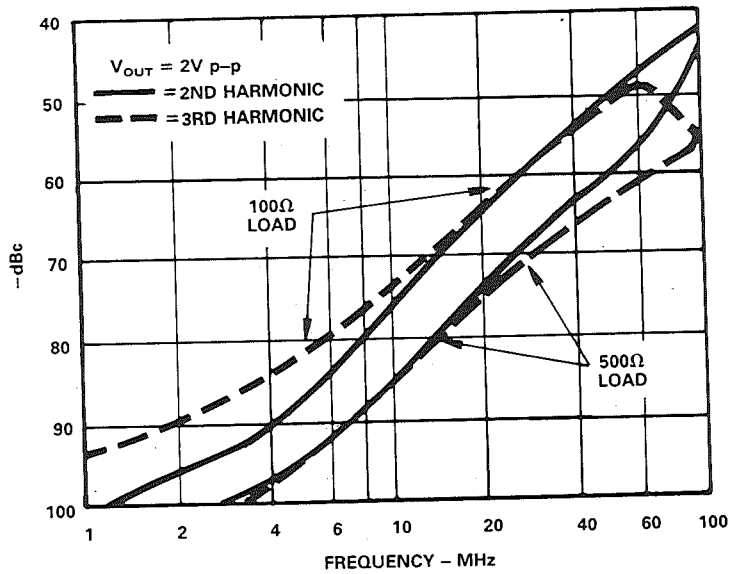


Figure 8.21

EFFECTS OF INPUT AND OUTPUT LOAD CAPACITANCE ON AD9617 SETTLING TIME

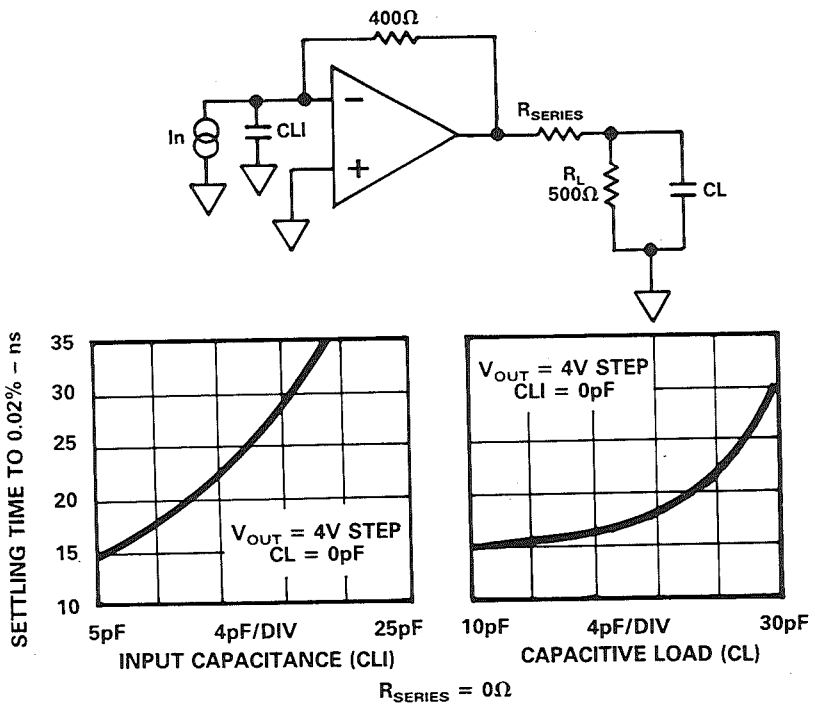


Figure 8.22

SERIES RESISTOR ISOLATES AD9617 OUTPUT FROM CAPACITIVE LOADS GREATER THAN 20pF

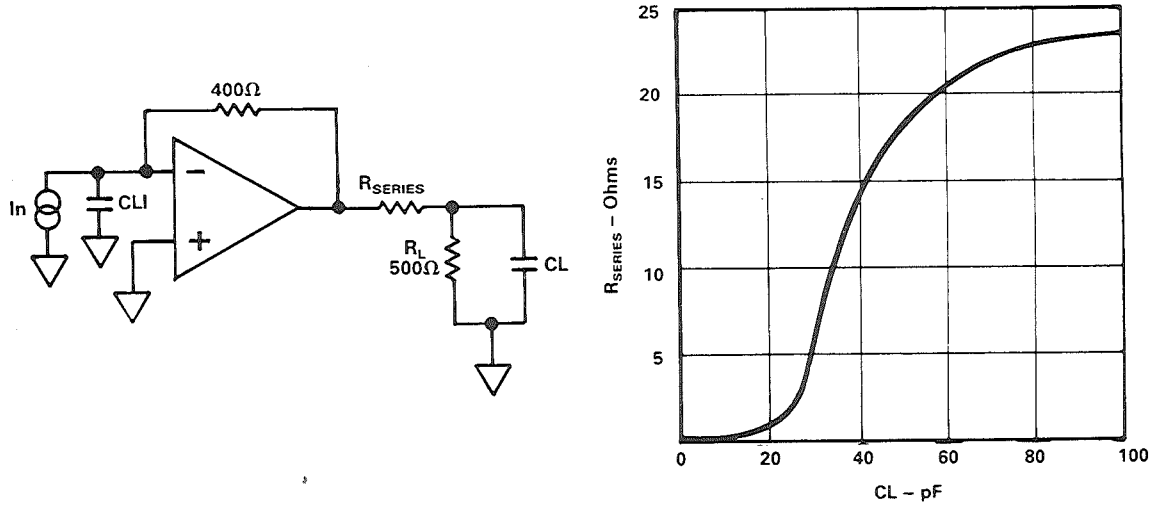


Figure 8.23

A LOW DISTORTION DRIVE CIRCUIT FOR PRECISION WIDE DYNAMIC RANGE ADCS

8

When gain is required ahead of precision wide dynamic range ADCs such as the AD9014, the circuit shown in Figure 8.24 is recommended in order to give ultra-low distortion levels. This configuration works well for analog input frequencies through 10MHz without introducing spurs that degrade the ADC's dynamic range. At 2.3MHz and 2V p-p output, all spurs generated in the drive circuit are less than -100dBc. The signal path is through U3 and U4, which are set up in a series inverting configuration to cancel even-order harmonics that are generated as the loop gain diminishes with frequency. U1 and U2 reduce the drive current of U3 and U4, respectively. Since U1 and U2 are set up in gains twice that of U3 and U4, the net effect is that the output stages of U3 and U4 are unloaded. This minimizes the odd-order harmonics generated in the output stages of U3 and U4. The gain of the overall block is +402Ω/R, and the input impedance is R/2.5. The output of the amplifier circuit is set up to drive either 2V p-p into 75Ω or 4V p-p into 150Ω by properly selecting R_p.

LOW DISTORTION DRIVE CIRCUIT (>100dBc) FOR AD9014 USING AD9617 OP AMPS

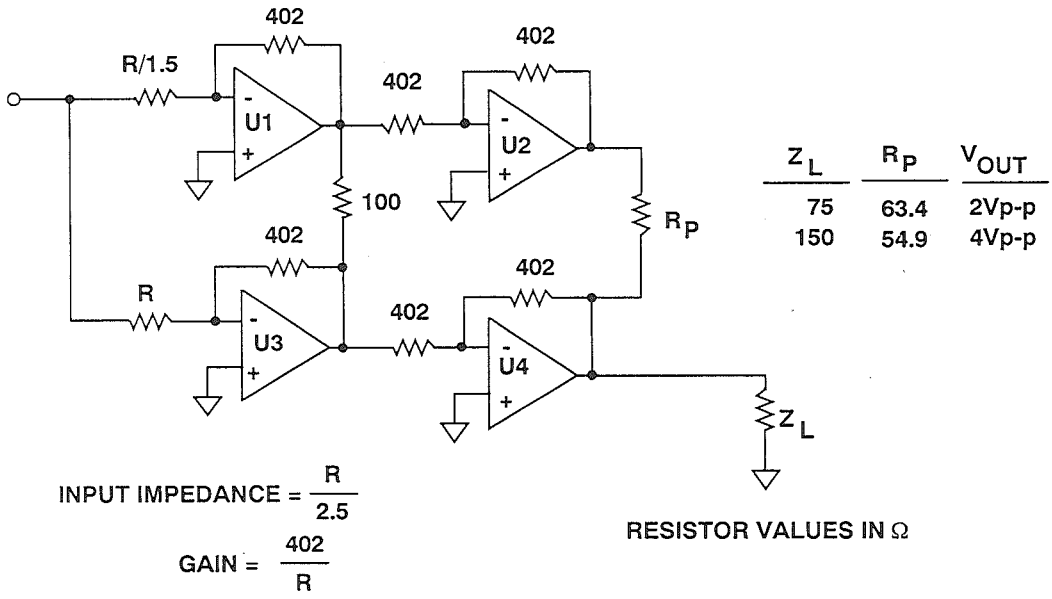
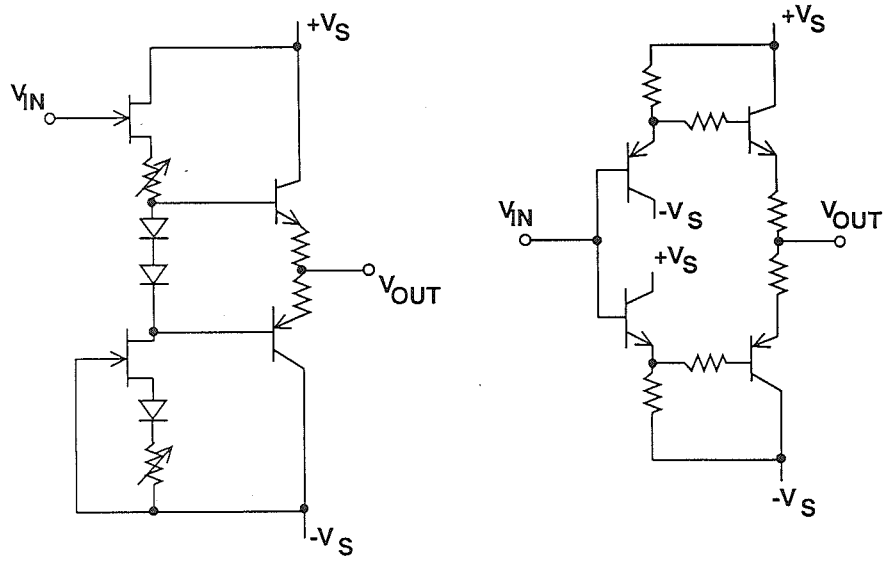


Figure 8.24

ULTRA HIGH SPEED BUFFERS

Buffer stages are basic to analog circuits, and are used to preserve signal accuracy and/or drive difficult loads. The previous section has discussed both video and ultra-high speed op amps which may be used as high performance signal buffers. In the early 1970's, before high speed IC op amps were available, the term *high speed buffer* usually referred to discrete *open loop* source and/or emitter follower circuits such as the two shown in Figure 8.25. The FET input circuit shown on the left was first implemented in hybrid form by National Semiconductor, Inc., and resulted in the industry-standard LH-0033 buffer. For circuits requiring higher speed without a FET input, the bipolar circuit on the right in Figure 8.25 was implemented by Analog Devices in a hybrid, the HOS-100. Although bandwidths in excess of 100MHz were achieved at fairly respectable levels of harmonic distortion, these hybrids were costly, high-power, and suffered from non-linearities (dc and ac) when loaded with impedances much less than 500Ω. An early IC implementation of these functions was the Precision Monolithic's, Inc. (now the PMI division of Analog Devices) BUF-03 shown in Figure 8.25. This open-loop IC buffer achieved a bandwidth of about 50MHz.

EARLY OPEN-LOOP, 100MHz BANDWIDTH HYBRID BUFFERS



LH-0033 HOS-100

Figure 8.25

EARLY IC OPEN-LOOP, 50MHz BUFFER, THE BUF-03

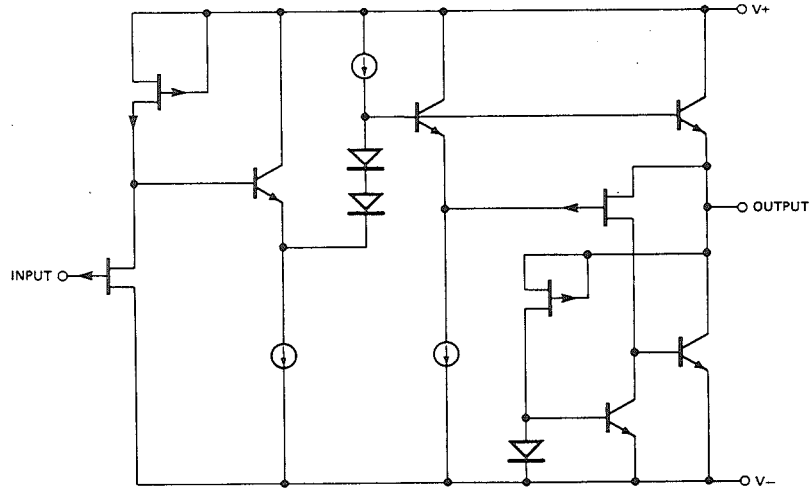


Figure 8.26

One of the problems with open loop buffers is that although high bandwidths may be achieved, these devices cannot take advantage of the "curative" effects of negative feedback. Distortion and DC performance suffers considerably when open loop buffers are loaded with typical video impedance levels of 50, 75, or 100Ω.

As IC processes evolved and high speed general-purpose op amps became available, it became possible to build relatively high speed buffers using these op amps as building blocks. Usually, however, the general-purpose op amps are compensated to operate over a relatively wide range of gains and feedback conditions. Therefore, bandwidth suffers somewhat at low gains, especially in the unity-gain non-inverting mode because of the additional external compensation usually required.

High speed complementary bipolar (CB) processes with matching PNP and NPN transistors have led to an entire new generation of op amps based on both traditional voltage feedback (VFB) and current feedback CFB) topologies. These amplifiers take advantage of negative feedback and innovative circuit design to provide excellent distortion performance under a variety of load and gain conditions. Many are optimized to operate under specific gain conditions to achieve optimum performance. For instance, AD9620 is a 600MHz voltage feedback op amp which is optimized for maximum performance as a unity-gain follower. The impressive specifications are summarized in Figure 8.27.

As in the case of other high speed devices, this level of performance can be achieved only if careful attention is given to layout and decoupling as shown in Figure 8.28. In the case of the AD9620, settling time and ac performance will be optimized with surface mount 0.1μF

AD9620 ULTRALOW DISTORTION 600MHz BUFFER KEY SPECIFICATIONS

- **Gain Accuracy: 0.994V/V**
- **Wide Bandwidth: 600MHz**
- **Slew Rate: 2200V/μs**
- **Ultralow Distortion: -73dBc @ 20MHz, -91dBc @ 2.3MHz**
- **Fast Settling Time: 8ns to 0.02%**
- **±40mA Output Current**
- **Low Noise: 2nV/$\sqrt{Hz}$**

Figure 8.27

PROPER LAYOUT AND DECOUPLING IS CRITICAL TO AD9620 BUFFER PERFORMANCE

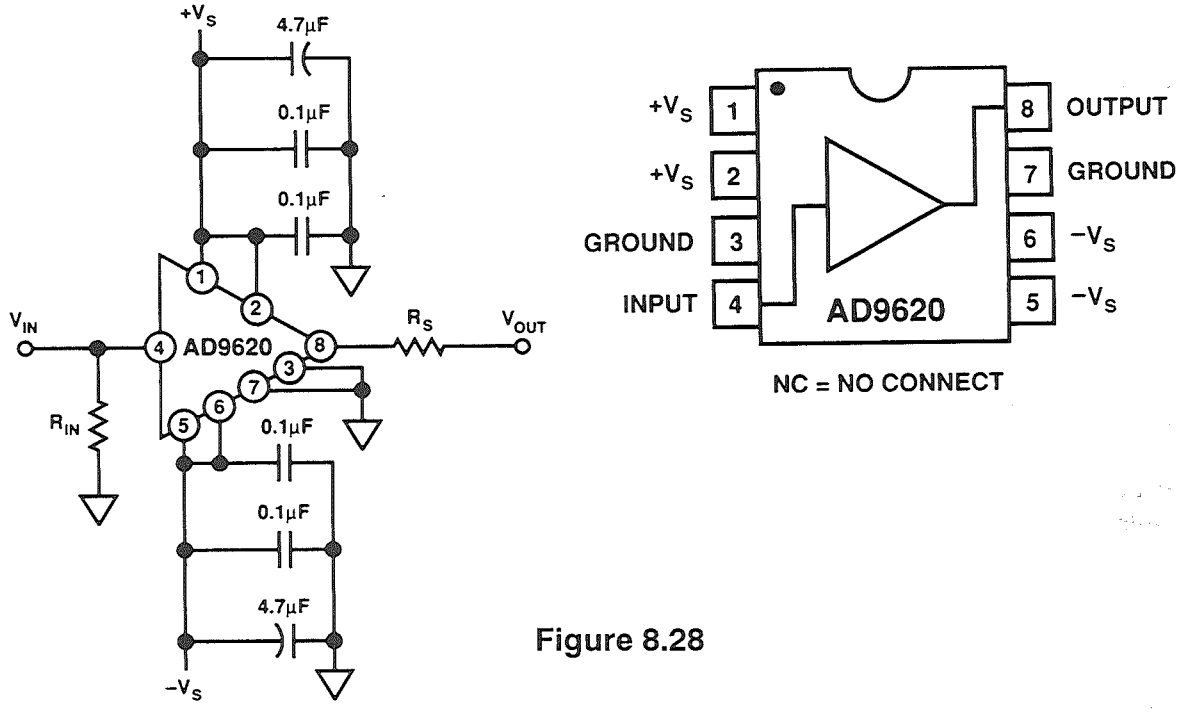


Figure 8.28

decoupling capacitors located within 50mils of their corresponding device pins, with the opposite side of the capacitor soldered directly to the ground plane. If surface mount capacitors cannot be used, radial lead ceramic capacitors with lead lengths less than 30mils are recommended. Low frequency power supply decoupling is also necessary and can be accomplished with 4.7µF tantalum capacitors mounted within 0.5 inch of the voltage supply pins. The interaction of the series inductance of the tantalum capacitor with the 0.1µF decoupling capacitor and the supply leads may cause high frequency oscillations at the output. These can be eliminated with a ferrite bead mounted between the tantalum and ceramic capacitors.

Connections to the AD9620 should be as short as possible. If either the source circuit or the driven circuit is further than 1 inch from the buffer, the PCB line impedances should be matched to the buffer input and output resistors. Basic microstrip techniques should be observed. The input and output termination resistors should both be connected as close to the AD9620 as possible.

The AD9620 should be soldered directly to the PCB with minimum vertical clearance. Molded sockets should not be used due to high pin reactances which will cause gain peaking and possibly induce oscillation. If sockets must be used for test or prototyping purposes, individual pin sockets such as the AMP-6-330808 series are recommended.

If the proper high speed techniques described above are observer, bandwidth and settling time performance shown in Figure 8.29 will be achieved.

AD9620 BUFFER FREQUENCY RESPONSE AND SETTLING TIME

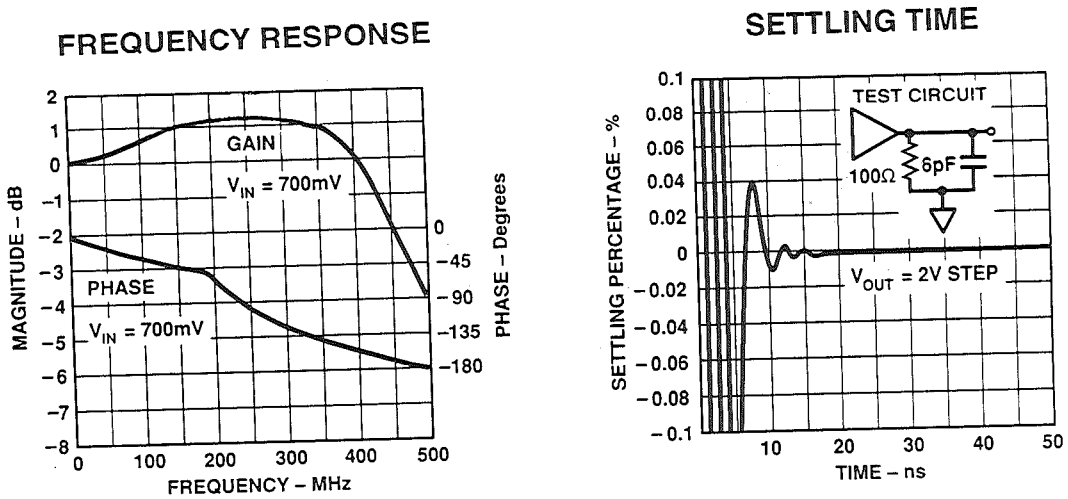


Figure 8.29

AD9620 BUFFER DC ENDPOINT LINEARITY ERROR FOR 100Ω AND 200Ω LOADS INDICATES OPEN-LOOP GAIN STABILITY OVER SIGNAL RANGE

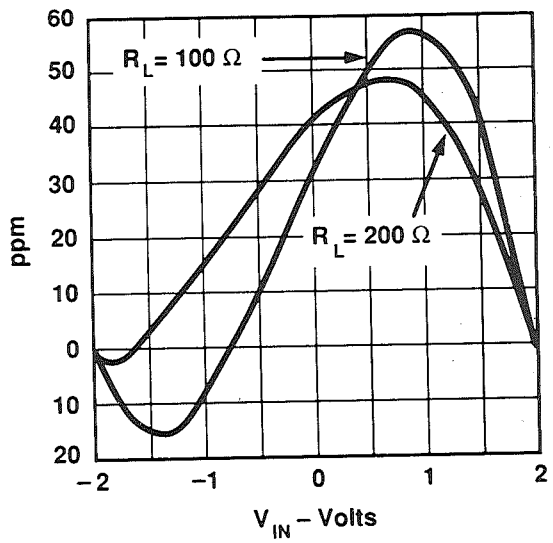


Figure 8.30

AD9620 BUFFER HARMONIC DISTORTION PERFORMANCE

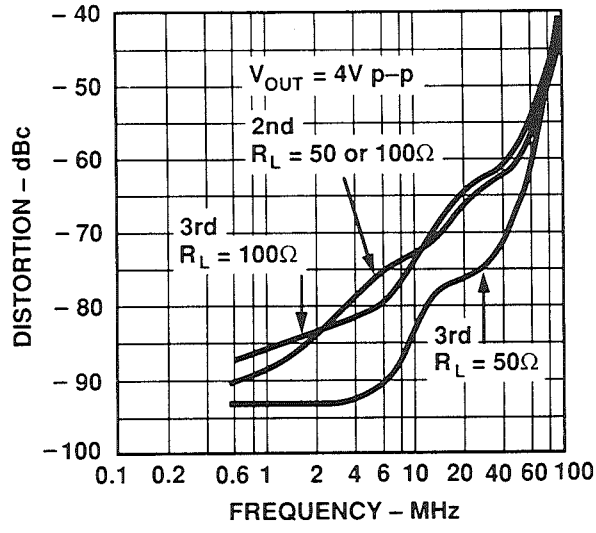
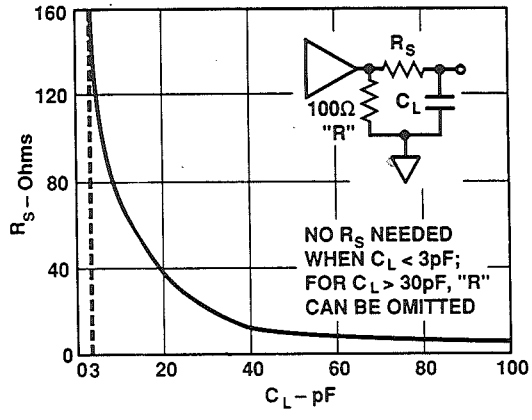


Figure 8.31

ISOLATION RESISTOR STABILIZES AD9620 WHEN DRIVING CAPACITIVE LOADS GREATER THAN 3pF

8

ISOLATION RESISTOR SELECTION



FREQUENCY RESPONSE

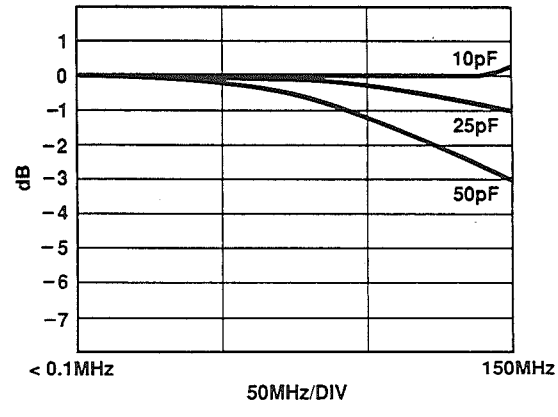


Figure 8.32

Although the open loop dc gain of the AD9620 is only about 2000, the proprietary voltage feedback circuit design of the AD9620 (Patents Pending) insures that this value is relatively constant under a variety of load and frequency conditions. DC endpoint linearity for a 100Ω load is better than 60ppm (85dB) as shown in Figure 8.30.

Because of the proprietary circuit design of the AD9620 buffer, excellent harmonic distortion is maintained up to 100MHz, where the distortion is still better than -40dBc as shown in Figure 8.31

Excessive gain peaking may occur when using the AD9620 to directly drive loads with more than 3pF of capacitance. To prevent this, a small value of resistance should be placed in series with the buffer output. Figure 8.32 shows the recommended value of resistance as a function of capacitive load as well as the resulting frequency response. Note that with a load of 50pF, the overall bandwidth is 150MHz.

The DC characteristics of the AD9620 shown in Figure 8.33 illustrate that the proper combination of process technology and circuit design allows respectable dc performance to be maintained along with the impressive ac characteristics.

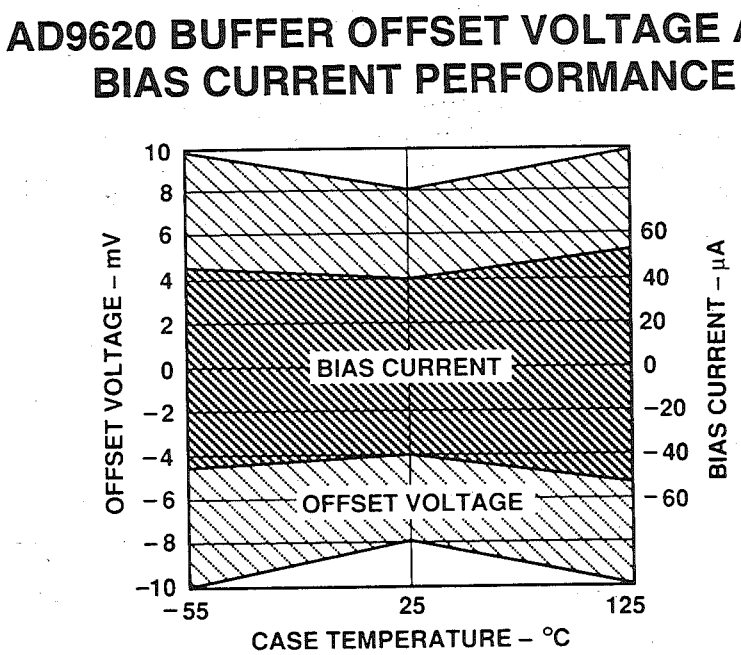


Figure 8.33

HIGH SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

WALT KESTER, CHRIS HYDE

A problem which has plagued the high speed circuit designers for years is that of transmitting video signals across noisy interfaces. This problem has been largely solved at low frequencies with high CMRR instrumentation amplifiers. At audio frequencies, products such as the SSM-2142 balanced line driver and SSM-2141/ SSM2143 line receiver offer outstanding CMRRs and the ability to transmit low-level signals in the presence of large amounts of noise.

The problem at video frequencies is twofold. First, video signals are generally single-ended and therefore don't adapt easily to balanced transmission line techniques. In addition, shielded twin-conductor coaxial cable with good bandwidth is usually somewhat bulky and expensive. Second, designing high bandwidth, low distortion differential video amplifiers with high CMRRs at high frequencies is an extremely difficult task.

Even with the above problems, there are differential techniques available now which offer distinct advantages over single-ended methods. Some of these techniques make use of discrete components, while others utilize the latest in state-of-the-art video differential amplifiers.

Three solutions to the problem of differential transmission and reception are shown in Figure 8.34. The first represents the ideal case, where a balanced differential line driver drives a balanced twin-conductor coaxial cable which in turn drives a differential line receiver. This circuit, however, is difficult to implement fully at video frequencies for the reasons previously discussed.

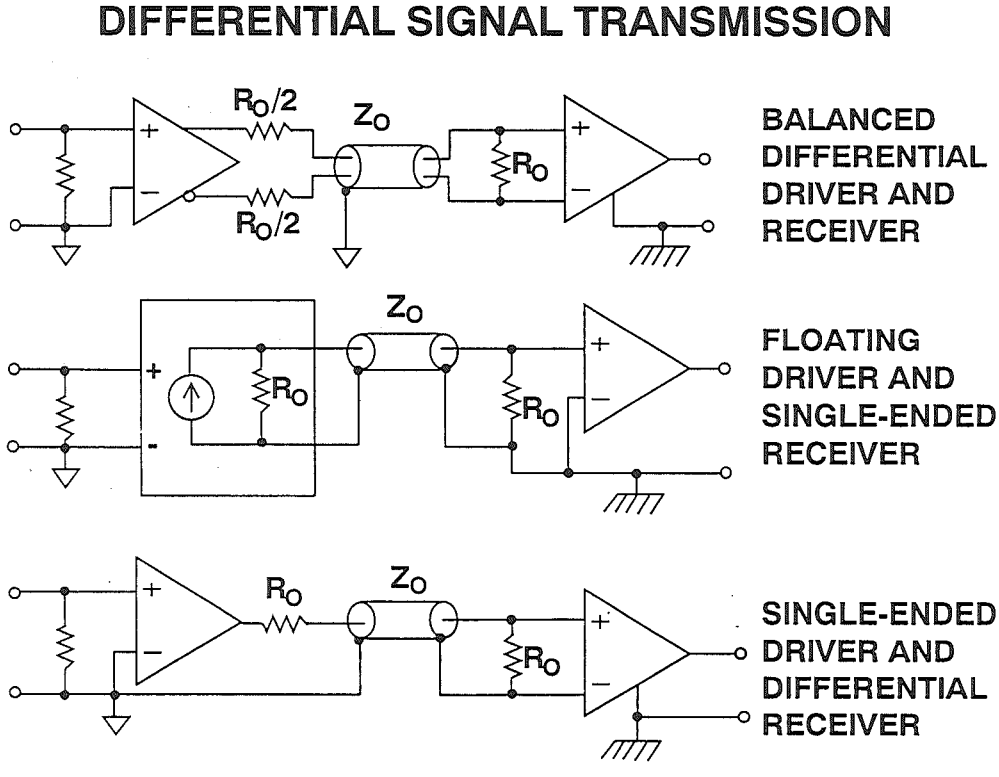


Figure 8.34

The second approach shown in Figure 8.34 uses a floating line driver (represented by the floating current source) to drive a single-conductor coaxial cable which is terminated at the receiving end in its characteristic impedance. Both the shield and the center conductor of the cable are driven by the floating line driver, and the cable is terminated at the receiving end. In this manner, noise between the two ground systems is isolated from the receiver output by the CMRR of the floating line driver.

The third approach makes use of a single-ended driver which drives a source-terminated coaxial cable. The shield of the coaxial cable is grounded at the transmitting end. At the receiving end, the coaxial cable is terminated in its characteristic impedance, but the shield is left floating. The common mode ground noise is rejected by the CMRR of the differential line receiver.

Figure 8.35 shows an implementation of the balanced driver and receiver approach using AD9617 op amps. Although bandwidths in excess of 100MHz can be achieved with this circuit, the CMRR at 5MHz is limited to between 35 and 40dB, even with the CMRR trims.

The second approach shown in Figure 8.34 using the floating line driver may be implemented using two Howland current sources (Reference 3, pp. 209-214, and Reference 4.). The single-ended Howland current source is shown in Figure 8.36 along with the equations which govern the resistor ratios. Two such circuits are connected as shown in Figure 8.37, one acting as a current source, and the other as a sink. This circuit provides about 800Ω of isolation between the two grounds, and yields better than 60dB harmonic distortion performance at 20MHz.

VIDEO DIFFERENTIAL LINE DRIVER AND RECEIVER USING AD9617 OP AMPS

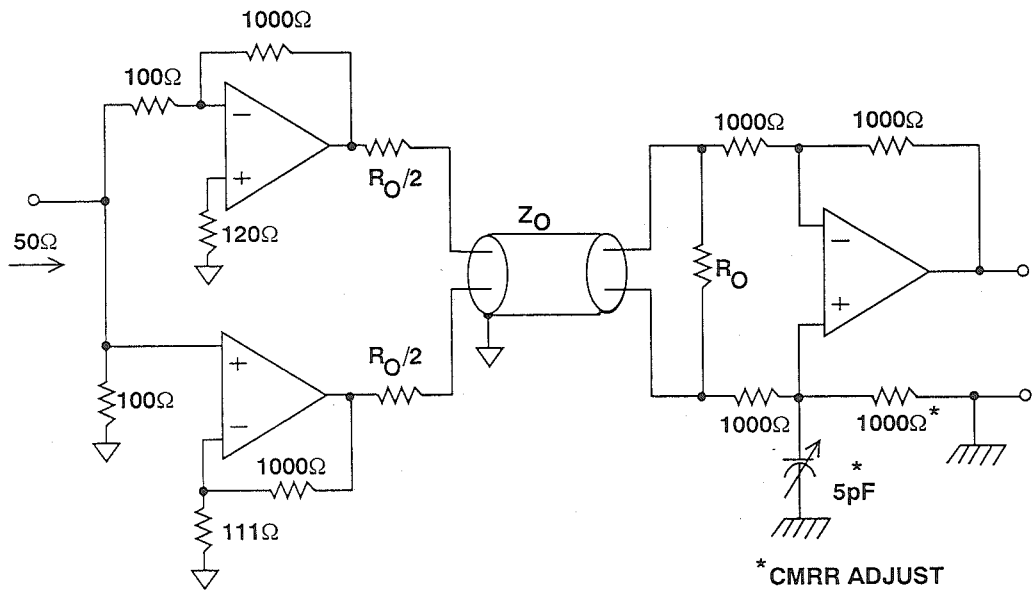
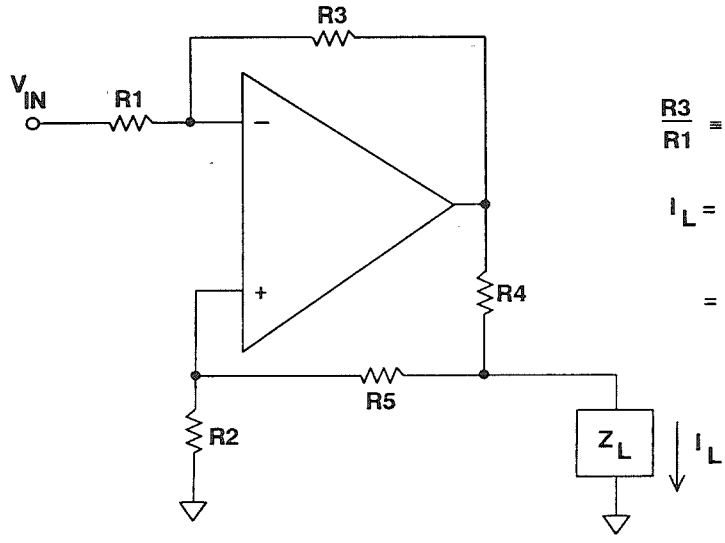


Figure 8.35

HOWLAND CURRENT SOURCE



$$\frac{R3}{R1} = \frac{R4 + R5}{R2}$$

$$I_L = \frac{-V_{IN}\,R3}{R1 \cdot R4}$$

$$= \frac{-V_{IN}\,(R4 + R5)}{R2 \cdot R4}$$

Figure 8.36

FLOATING LINE DRIVER

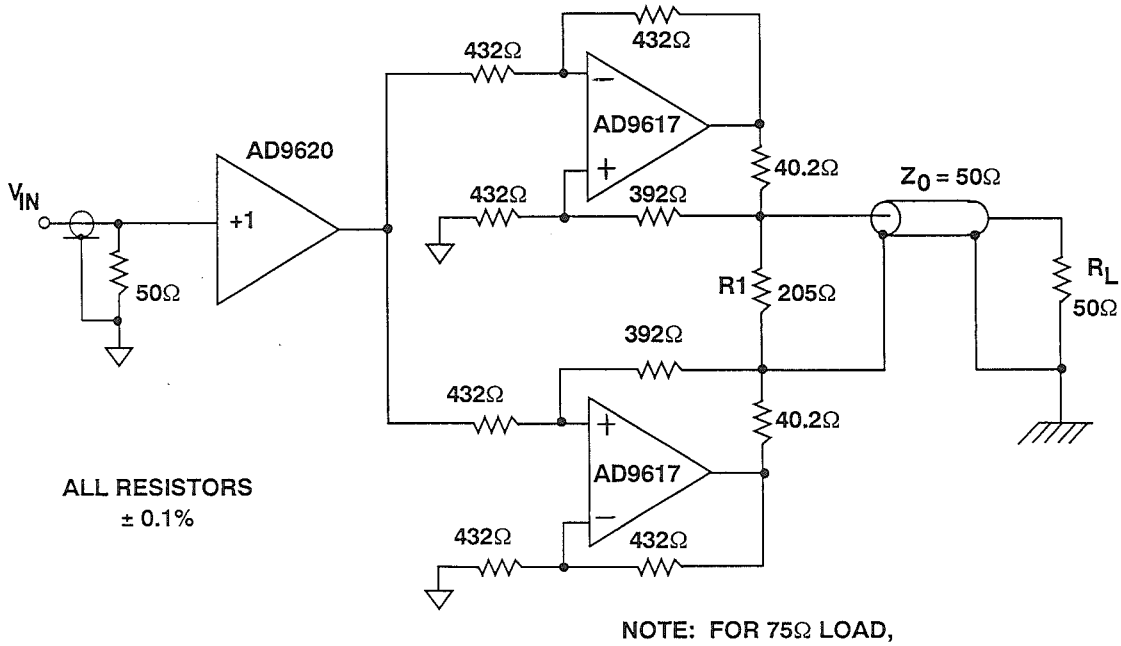


Figure 8.37

Implementation of the third approach shown in Figure 8.34 is based on a state-of-the-art video difference amplifier, the AD830. A functional block diagram of the device is shown in Figure 8.38, and key specifications are given in Figure 8.39

CMRR and bandwidth performance for the device are shown in Figure 8.40, and harmonic distortion and differential gain and phase in Figure 8.41.

AD830 50MHz VIDEO DIFFERENCE AMPLIFIER FUNCTIONAL DIAGRAM

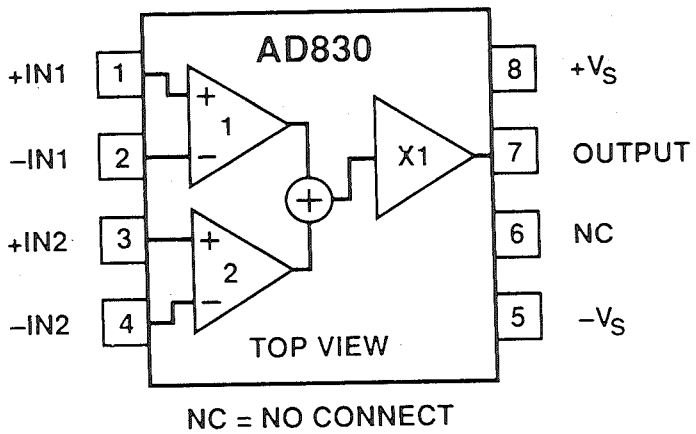


Figure 8.38

The AD830 may be configured in several ways, all of which yield the same excellent video performance. Figure 8.42 shows the basic configuration for a differential line receiver. The signal from system "A" is received differentially relative to A's ground, and that voltage is exactly reproduced relative to the ground in system B. Any common mode noise is rejected by the AD830 as shown in the previous curves in Figure 8.40.

The AD830 may also be configured for gains greater than 1 and provide instrumentation amplifier style amplification as shown in Figure 8.43. The input signal is connected differentially to the internal V-to-I converter #1. The gain is set via the feedback resistors R2 and R1 in the same manner as a non-inverting op amp circuit. The polarity of the gain is established by the relative connections at input pins 1 and 2. Inverting gain is set by reversing the shown connections to the input. As in a conventional voltage feedback op amp, the bandwidth decreases with increasing gain.

AD830 VIDEO DIFFERENCE AMPLIFIER KEY SPECIFICATIONS

- Common Mode Voltage Range: ±11.5V
- Differential Voltage Range: ±2V
- CMRR: 60dB @ 4.43MHz, 50dB @ 10MHz
- Bandwidth: 50Mhz
- Distortion: -60dBc @ 4.43Mhz
- Differential Gain: 0.1%, Differential Phase: 0.1°

Figure 8.39

AD830 CMRR AND FREQUENCY RESPONSE FOR ±5V AND ±15V SUPPLIES

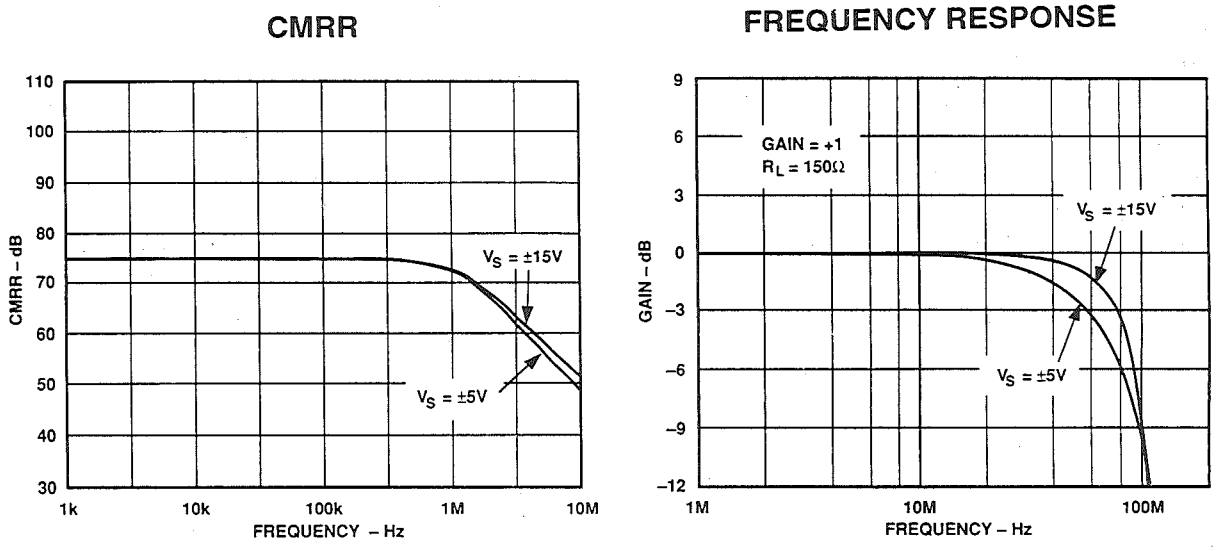


Figure 8.40

AD830 DIFFERENTIAL GAIN, PHASE, AND HARMONIC DISTORTION PERFORMANCE

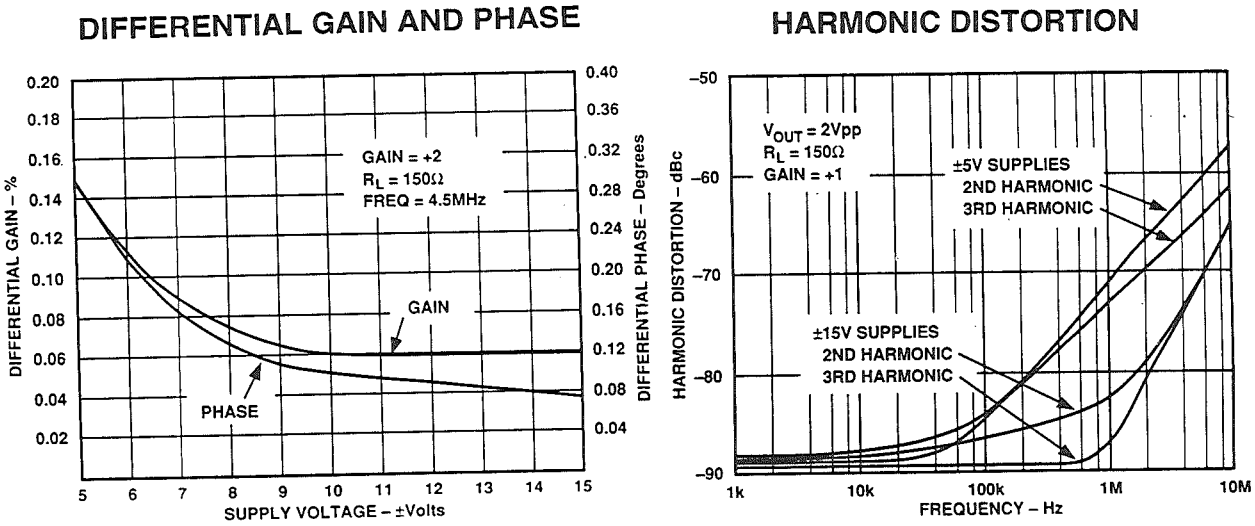


Figure 8.41

DIFFERENTIAL LINE RECEIVER USING THE AD830

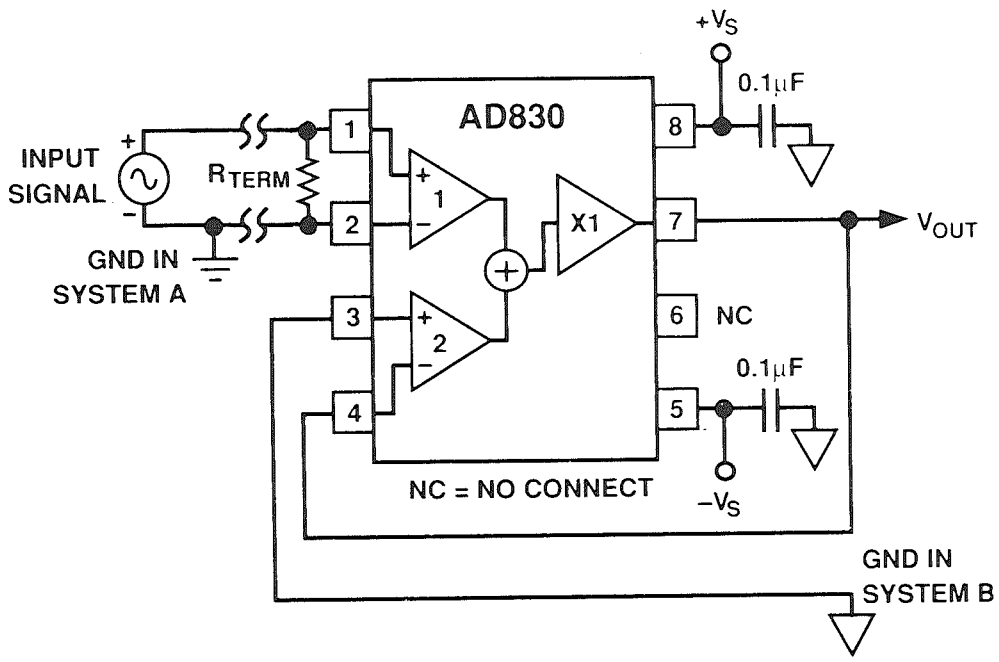
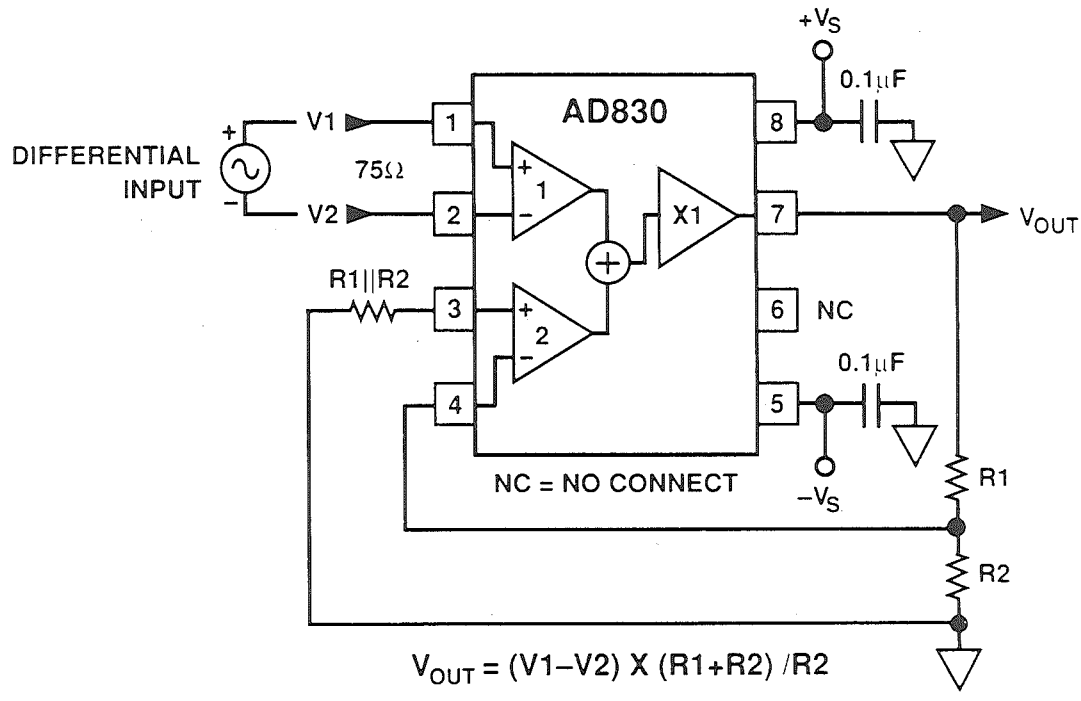


Figure 8.42

GAIN-OF-N INSTRUMENTATION AMPLIFIER USING THE AD830



$V_{OUT} = (V1–V2) \times (R1+R2) / R2$

$GAIN = (R1+R2) / R2$

Figure 8.43

The AD830 is ideally suited for the video cable receiver circuit shown in Figure 8.44. Here the cable shield is terminated at the driving end. The input signal to the AD830 is taken differentially from the conductor to shield and then amplified relative to the PCB ground. The 499Ω resistors set the gain at 2, with the 249Ω resistor included in series with the input to ground to cancel input bias current induced offsets. The 75Ω resistor connected in series with the output serves as the standard back termination impedance. Therefore, the net gain to the load resistor is unity.

VIDEO CABLE RECEIVER/DRIVER USING THE AD830

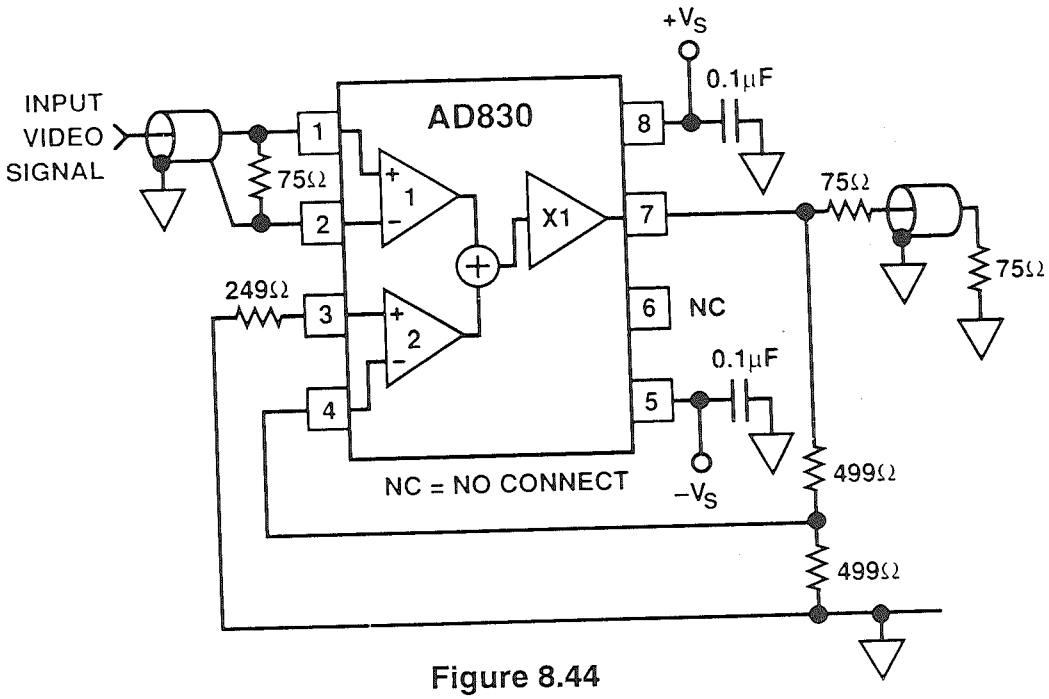
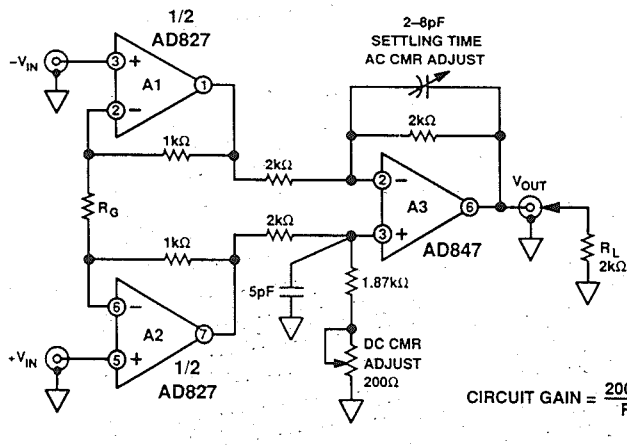


Figure 8.44

A HIGH SPEED THREE OP AMP INSTRUMENTATION AMPLIFIER

The circuit shown in Figure 8.45 lends itself well to CCD imaging and other video speed applications. It uses two high speed CB process op amps: Amplifier A3, the output amplifier, is an AD847. The input amplifier (A1 and A2) is an AD827, which is a dual version of the AD847. This circuit has the optional flexibility of both dc and ac trims for common-mode rejection, plus the ability to adjust for minimum settling time. Performance data is also given on Figure 8.45.

A HIGH SPEED, THREE OP AMP INSTRUMENTATION AMPLIFIER



INPUT FREQUENCY	CMRR
100Hz	88.3dB
1kHz	87.4dB
10kHz	86.2dB
100kHz	67.4dB
1MHz	47.1dB
10MHz	26.4dB

BANDWIDTH, SETTLING TIME AND TOTAL HARMONIC DISTORTION VS. GAIN

GAIN	R_G	C_{ADJ} (pF)	SMALL SIGNAL BANDWIDTH	SETTLING TIME TO 0.1%	THD + NOISE BELOW INPUT LEVEL @ 10kHz
1	OPEN	2–8	16.1MHz	200ns	82dB
2	2kΩ	2–8	14.7MHz	200ns	82dB
10	226Ω	2–8	4.5MHz	370ns	81dB
100	200Ω	2–8	660kHz	2.5µs	71dB

Figure 8.45

8

REFERENCES

1. W. A. Kester, *PCM Signal Codecs for Video Applications*, **SMPTE Journal**, No. 88, November 1979, pp. 770-778.

2. *IEEE Standard for Performance Measurements of A/D and D/A Converters for PCM Television Circuits*, **IEEE Standard 746-1984**.

3. Thomas M. Frederiksen, **Intuitive Operational Amplifiers**, McGraw Hill, 1988.

4. Tim Henry, *Analysis and Design of the Op Amp Current Source*, Application Note AN-587, Motorola, Inc., 1973.

5. **High Speed Design Seminar Notes**, 1990, Analog Devices.