SECTION VII
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SECTION VII

DRIVING ADCs

WALT KESTER

INTRODUCTION

Selecting the appropriate drive amplifier for an ADC involves many tradeoffs. In order to make these tradeoffs, overall system requirements must be understood as well as how they relate to the ADC and the drive circuitry. In most real-time DSP signal processing applications (see Figure 7.1), the dynamic performance of the ADC is critical. Therefore ADCs with integral sample-and-hold functions (usually called *sampling* ADCs) are often selected. Such specifications as signal-to-noise ratio, effective number of bits, full-power bandwidth, harmonic distortion, total harmonic distortion, and spurious free dynamic range are often used as selection criteria for the ADC. It then becomes important that the op amp driving the ADC not introduce errors which will degrade the ADC performance.

The antialiasing filter must usually be considered in conjunction with the drive amplifier. This is necessary in order to calculate noise performance correctly. The filter may be passive or active, depending on the signal frequencies of interest. It must be designed based on the signal characteristics and the dynamic range required. Further discussions regarding active and passive filters will be found in Section 6.

There are many signal processing applications where both ac performance and dc precision are important. In these applications, there are even more tradeoffs to make.

In some applications the signal to be digitized is dc or changing very slowly relative to the conversion time, and a sampling ADC is not required. Even

AMPLIFIERS AS PART OF
REALTIME SIGNAL PROCESSING SYSTEMS

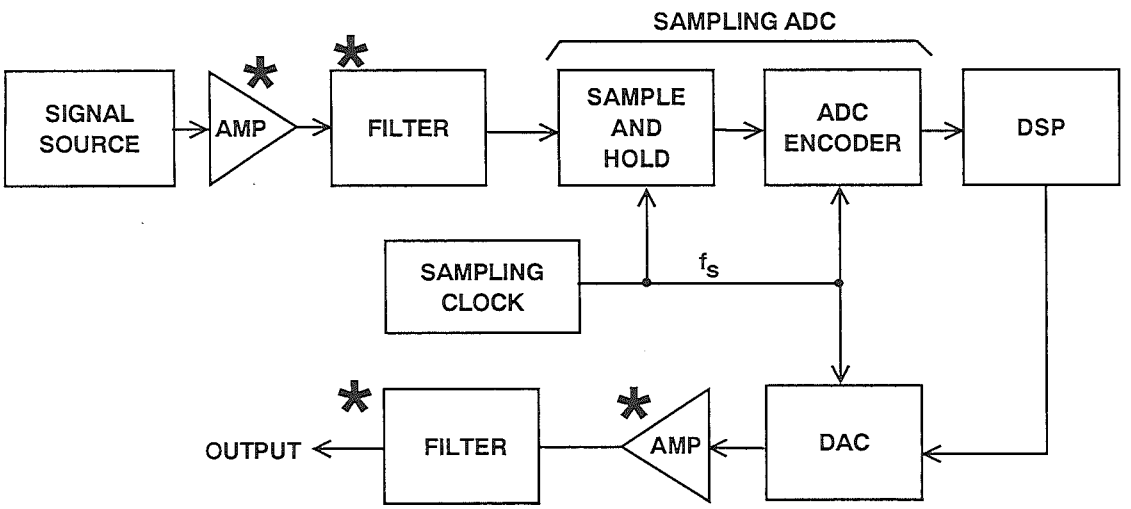


Figure 7.1 #1

these dc applications may place certain requirements on the op amp's ac performance because of the design of the ADC input circuits.

Finally, there are applications where the sample-and-hold function is performed ahead of the ADC, such as in a CCD imaging system or a multiplexed simultaneous-sampling data acquisition system as shown in Figure 7.2. In these systems, the settling time of the amplifier driving the ADC is critical to digitizing the signal accurately.

Before intelligent decisions can be made regarding the drive amplifier, it is necessary to have an understanding of the overall system performance requirements. Key to system performance is the ADC which will be discussed in the next few sections.

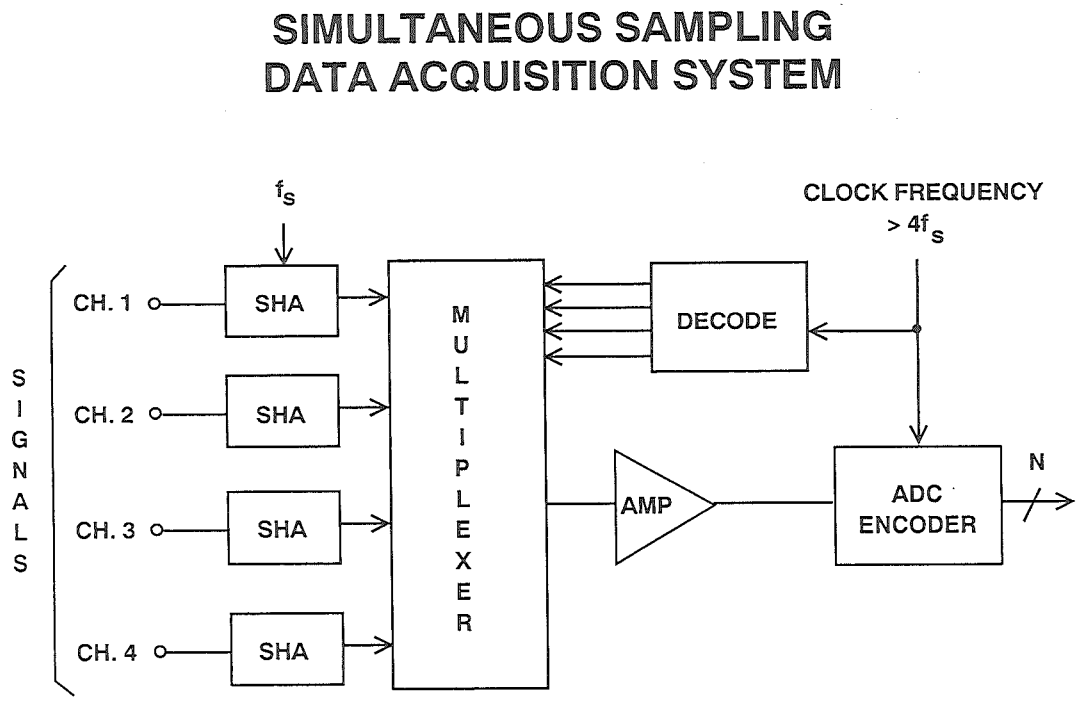


Figure 7.2

ADC PERFORMANCE SPECIFICATIONS

At this point we should distinguish between *sampling* ADCs (ADCs with an internal sample-and-hold function) and ADCs designed to operate on signals which remain constant during the encoding interval. We shall refer to the latter classification as ADC *encoders*.

Successive approximation ADCs, such as the industry-standard 12 bit AD574, require that the analog input signal be held constant during the entire conversion cycle. Otherwise, large errors in the conversion process will result. Encoders such as the AD574 are therefore specified in terms of traditional dc parameters such as those listed in Figure 7.3.

External sample-and-hold amplifiers (SHAs) are often used ahead of this type of encoder when processing ac signals. However, the overall ac performance of the SHA/encoder combination is difficult to determine from the individual specifications of the two devices. Often the correct interface timing for optimum ac performance must be determined experimentally. Another popular ADC encoder

architecture is called digitally-corrected-subranging (DCS). The conversion is made in multiple steps of several bits each, therefore, a SHA is also required for accurate sampling of ac signals using converters with this architecture.

Recent innovations in circuit design and IC process technology allow the SHA function to be included on the same chip with the ADC encoder. This type of ADC is usually referred to as a *sampling* ADC. These converters are completely specified in terms of dc and ac parameters, making their application much easier. In addition, users no longer have to concern themselves with optimizing the SHA/encoder interface.

There are many factors which go into the selection of an ADC for a system application. Most are based upon the particular characteristics of the signal to be processed. Signal bandwidth usually determines the minimum sampling rate required of the ADC. Nyquist's Criterion states that the signal must be sampled at a rate equal to at least twice the maximum signal frequency in order to avoid aliasing. As we will see later, higher sampling rates are usually chosen in order to ease the requirements placed on the antialiasing filter.

TRADITIONAL DC SPECIFICATIONS FOR NON-SAMPLING ADC ENCODERS

- Offset, Offset Temperature Coefficient
- Gain, Gain Temperature Coefficient
- Integral Non-Linearity
- Differential Non-Linearity
- Conversion Time

Figure 7.3

ADCs FOR DSP APPLICATIONS

- Most are *Sampling* ADCs Containing on-chip SHA as Opposed to *Encoders*, which have no SHA
- Interface Between SHA and ADC Handled on-chip
- Complete DC and AC Specifications Usually Provided

Figure 7.4

SHANNON'S INFORMATION THEOREM AND NYQUIST'S CRITERION

- Shannon: An Analog Signal with a *BANDWIDTH* of f_a Must be Sampled at a Rate $f_S > 2f_a$ in Order to Avoid the Loss of Information
- Nyquist: If $f_S < 2f_a$, then a Phenomena Called *ALIASING* will Occur

Figure 7.5

In addition to establishing the minimum sampling rate, f_S, the resolution of the ADC must be determined. Figure 7 shows the weight of the least significant bit (relative to a 10 Volt peak-to-peak analog input range) for ADCs of various resolutions. Also shown is the theoretical rms quantization noise for an ideal N-bit ADC with no dc or ac errors. The theoretical value of the quantization noise within the Nyquist bandwidth, $f_S/2$, is , where q is the weight of the least significant bit (LSB). The resulting theoretical signal-to-noise ratio (SNR) for a perfect N bit ADC is given by SNR = 6.02N + 1.76dB. This value is also given in Figure 7.6.

BIT SIZES, THEORETICAL QUANTIZATION NOISE, AND SNR FOR 10V FULLSCALE CONVERTERS

Resolution (Bits)	1 LSB = q	%FS	ppm FS	RMS Quantization Noise, $q/\sqrt{12}$	Theoretical SNR (dB)
4	625mV	6.25	62500	180mV	25.8
6	156mV	1.56	15625	45mV	37.9
8	30mV	0.39	3906	11.2mV	50.0
10	9.76mV	0.098	977	3.46mV	62.0
12	2.44mV	0.024	244	704µV	74.0
14	610µV	0.0061	61	176µV	86.0
16	153µV	0.0015	15	44µV	98.1
18	38µV	0.0004	4	11µV	110.1
20	9.5µV	0.0001	1	2.7µV	122.2
22	2.4µV	0.000024	0.24	0.7µV	134.2
24	0.6µV	0.000006	0.06	0.2µV	146.2

Figure 7.6

SIGNAL-TO-NOISE RATIO (SNR) AND EFFECTIVE BITS (ENOB)

In testing ADCs, the SNR is usually calculated using DSP techniques while applying a pure sinewave signal to the input of the ADC. A typical test system is shown in Figure 7.7.

The Fast Fourier Transform (FFT) processes a finite number of time samples and converts them into a frequency spectrum such as the one shown in Figure 7.8 for the AD676 16 bit 100kSPS sampling ADC. The frequency spectrum is then used to calculate the SNR as well as harmonics of the fundamental input signal, a technique very similar to that of an analog spectrum analyzer.

The rms value of the signal is first computed. Then the rms value of all other frequency components over the Nyquist bandwidth (this includes not only noise but also distortion products) is computed. The ratio of these two quantities, expressed in dB is the SNR. Various error sources in the ADC cause the measured SNR to be less than the theoretical value, 6.02N + 1.76dB. These errors are due to integral and differential nonlinearities, missing codes, and internal ADC noise sources. In addition, the errors are a function of input slewrate and therefore increase as the input frequency gets higher. In calculating the rms value of the noise, it is customary to include harmonics of the fundamental signal. This is sometimes referred to as the

ADC DYNAMIC TESTING

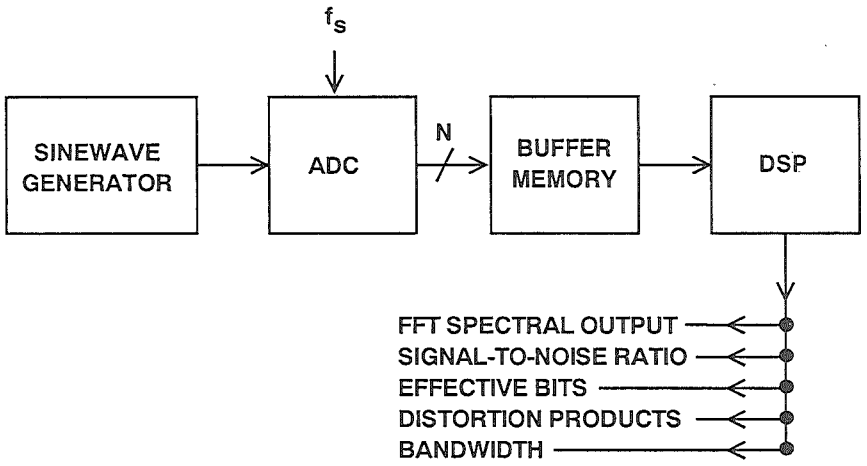


Figure 7.7

AD676 16-BIT, 100kSPS ADC FFT OUTPUT

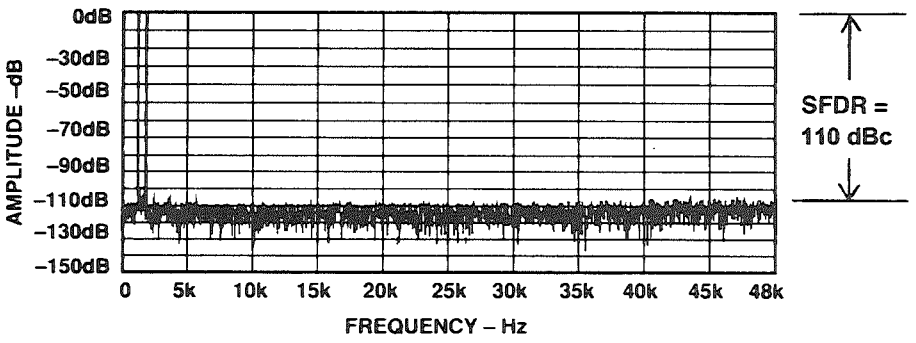


Figure 7.8

signal-to-noise-plus-distortion, S/(N+D), but is usually called simply SNR. A typical plot of S/(N+D) for the AD676 sampling ADC (16 bits, 100kSPS) is shown in Figure 7.9.

This leads to the definition of another important ADC dynamic specification, the *effective-number-of-bits*, or ENOBs. The effective bits are calculated by first measuring the SNR of an ADC with a fullscale sinewave input signal. The measured SNR (SNR_{actual})is substituted into the equation for SNR, and the equation is solved for N as shown in Figure 7.10. In the case of the AD676, a 16 bit ADC, an SNR of 88dB corresponds to approximately 14 effective bits. This means that the same dynamic performance will be achieved if the imperfect 16 bit ADC is replaced by a perfect 14 bit ADC.

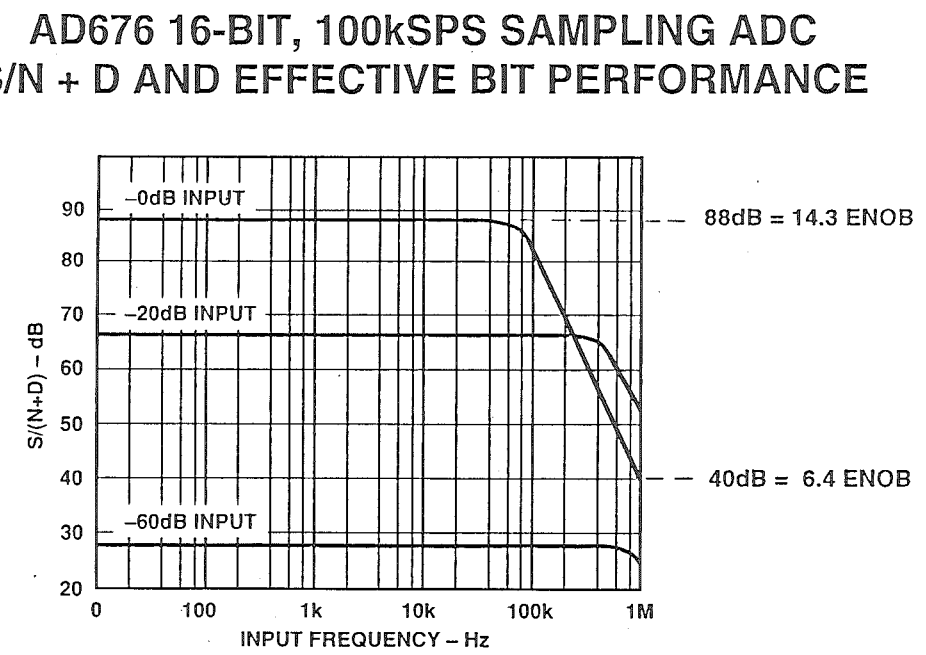


Figure 7.9

QUANTIZATION THEORY BASICS

- RMS Quantization Noise in Nyquist Bandwidth, $f_S/2$:
  $q/\sqrt{12}$, q = LSB Weight
- Fullscale Sinewave RMS Signal to RMS Noise Ratio in Nyquist Bandwidth:

$$SNR = 6.02N + 1.76dB$$

- Effective Number of Bits (ENOB):

$$ENOB = \frac{SNR_{ACTUAL} - 1.76dB}{6.02} = \frac{88\text{-}1.76}{6.02} = 14.3 \text{ (AD676)}$$

Figure 7.10

PEAK SPURIOUS, PEAK HARMONIC CONTENT, AND SPURIOUS FREE DYNAMIC RANGE (SFDR)

The peak spurious or peak harmonic component is the largest spectral component excluding the input signal and dc. This value is expressed in dB relative to the rms value of a fullscale input signal as shown in the previous Figure 7.8. The peak spurious specification is also occasionally referred to as spurious free dynamic range (SFDR). SFDR is usually measured over a wide range of input frequencies and at various amplitudes.

It is important to note that the harmonic distortion or SFDR of an ADC is not limited by its theoretical SNR value. The SFDR of a 12 bit ADC may exceed 85dB, while the theoretical SNR is only 74dB. On the other hand, the S/N+D of the ADC may be limited by poor harmonic distortion performance, since the harmonic components are included with the quantization noise when computing the rms noise level.

TOTAL HARMONIC DISTORTION (THD)

Total harmonic distortion (THD) is the ratio of the rms sum of the harmonic components to the rms value of a input signal and is expressed in a percentage or in dB. For input signals or harmonics that are above the Nyquist frequency, the aliased components are used in making the calculation. THD is usually measured at several input signal frequencies and amplitudes.

FULL-POWER BANDWIDTH

The full-power bandwidth (FPBW) of an ADC is that input frequency at which the amplitude of the reconstructed FFT *fundamental* is reduced by 3dB for a fullscale input. Full-power bandwidth must be examined in conjunction with SNR, ENOB, and THD in order to determine the dynamic performance of the ADC at the FPBW frequency. For example, the FBBW of the AD676 ADC is 1MHz, but at 1MHz, the SNR is only 40dB, or 6.4 effective bits.

The FPBW specification is important when selecting the ADC drive amplifier. The output noise spectral density of the amplifier must be integrated over the entire small-signal bandwidth of the ADC if there is no filter between the amplifier and the ADC. The small signal ADC bandwidth is approximately equal to the FPBW if there is no slew rate limiting. In cases where the FPBW is significantly less than the small signal bandwidth, the small signal bandwidth should be used in noise calculations.

ADC FULL-POWER BANDWIDTH

- The Frequency at Which the Amplitude of the *Fundamental* Component in the FFT Output is Down 3dB
- FPBW Usually > f_S (Except for ΣΔ ADCs)
- Must Examine ENOB and THD at FPBW Frequency
- Example: AD676 FPBW = 1MHz, But Only 6.4 ENOB @ 1MHz
- Use FPBW or Small Signal BW (if Greater Than FPBW) for Noise Calculations

Figure 7.11

EFFECTS OF ADC DRIVE AMPLIFIER ON SYSTEM PERFORMANCE

Because the ADC drive amplifier is in the signal path to the ADC, its error sources (both dc and ac) must be considered in calculating the total error budget. Ideally, the ac and dc performance of the amplifier should be such that there is no degradation of the ADC performance. It is rarely possible to achieve this, however; and therefore, the effects of each amplifier error source on system performance should be evaluated individually.

Evaluating and selecting op amps based on the dc requirements of the system is a relatively straightforward matter. For many applications it is common for the amplifier to be selected first on the basis of ac performance (bandwidth, THD, noise, etc.). If the ac perfor-

mance is satisfactory for the application, then the dc specifications are examined in light of system requirements.

The primary functions of the ADC drive amplifier are to provide signal buffering, gain (if required), and level shifting (if required) as shown in Figure 7.12.

The amplifier output drive capability must match the ADC input requirements. ADCs usually present both a resistive and a reactive load to the amplifier. The amplifier must be stable under the required gain and load conditions. The input circuits of the ADC may inject high frequency current spikes into the op amp output. This places a requirement on the op amp settling time and ac output impedance which will be discussed shortly.

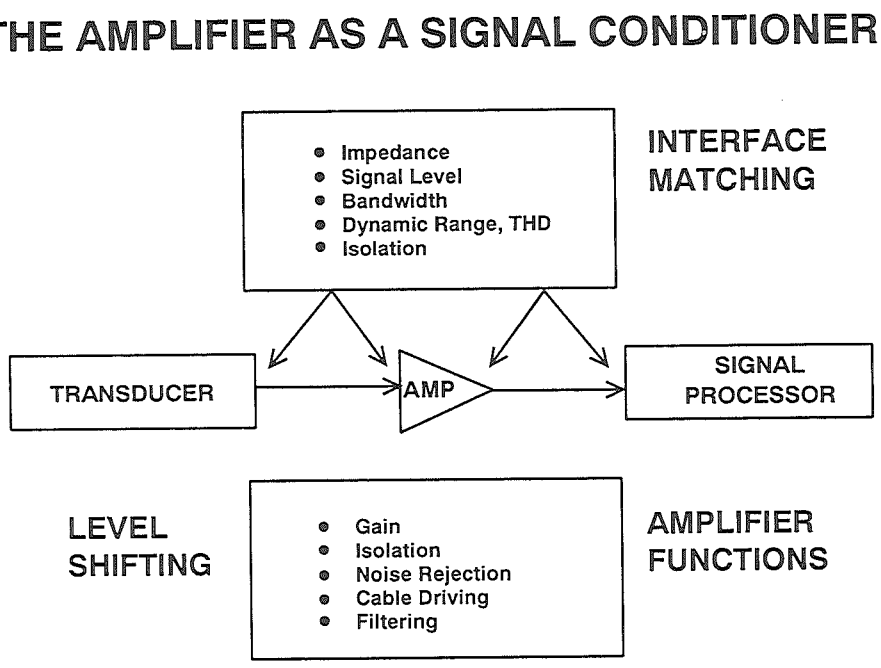


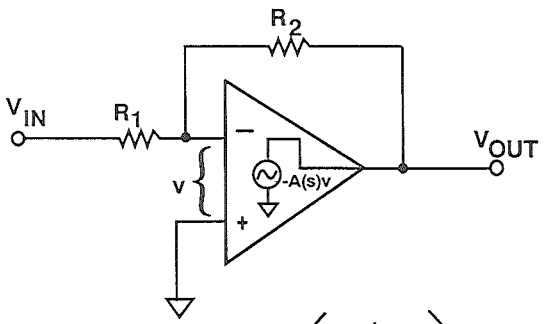
Figure 7.12

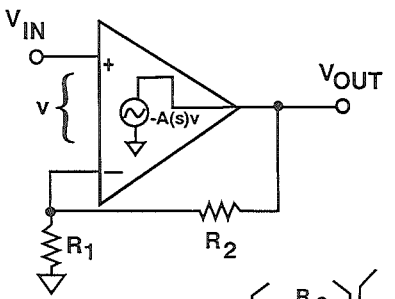
VOLTAGE FEEDBACK AMPLIFIERS

The equivalent circuit for a voltage feedback amplifier is given in Figure 7.13. The input voltage is multiplied by the open loop gain A(s) to yield the output voltage. The feedback attenuation factor is β. The equations relating the input and output voltage for the inverting and the non-inverting mode are also given in Figure 7.13.

The term $A(s)\beta$ is referred to as the *loop gain*. It is the value of the loop gain at any frequency which will determine the overall accuracy of the op amp. The so-called *curative* effects of feedback at any frequency are determined by the available amount of loop gain at that frequency. Loop gain affects gain accuracy and stability, linearity, distortion, input, and output impedance. (For further discussions see Reference 3, pp. 26-29). The corresponding Bode plot for a single pole rolloff with fixed compensation is shown in Figure 7.14. Notice that the product of the closed loop gain, $1/\beta$, and the closed loop bandwidth, A_{cl}, is constant over a wide range of frequencies. The frequency f_u is referred to as the unity gain bandwidth frequency.

VOLTAGE FEEDBACK OP AMP EQUIVALENT CIRCUITS





$$\text{INVERTING SIGNAL GAIN} = -\left(\frac{R_2}{R_1}\right)\left(\frac{1}{1+\frac{1}{A(s)\beta}}\right)$$

$$\text{NON-INVERTING SIGNAL GAIN} = \left(1+\frac{R_2}{R_1}\right)\left(\frac{1}{1+\frac{1}{A(s)\beta}}\right)$$

A(s) = OPEN LOOP VOLTAGE GAIN

β = FEEDBACK FACTOR = $\dfrac{R_1}{R_1+R_2}$

$\dfrac{1}{\beta}$ = NOISE GAIN = $1+\dfrac{R_2}{R_1}$

LOOP GAIN = $A(s)\beta$

Figure 7.13

LOG-LOG BODE PLOT FOR VOLTAGE FEEDBACK OP AMP

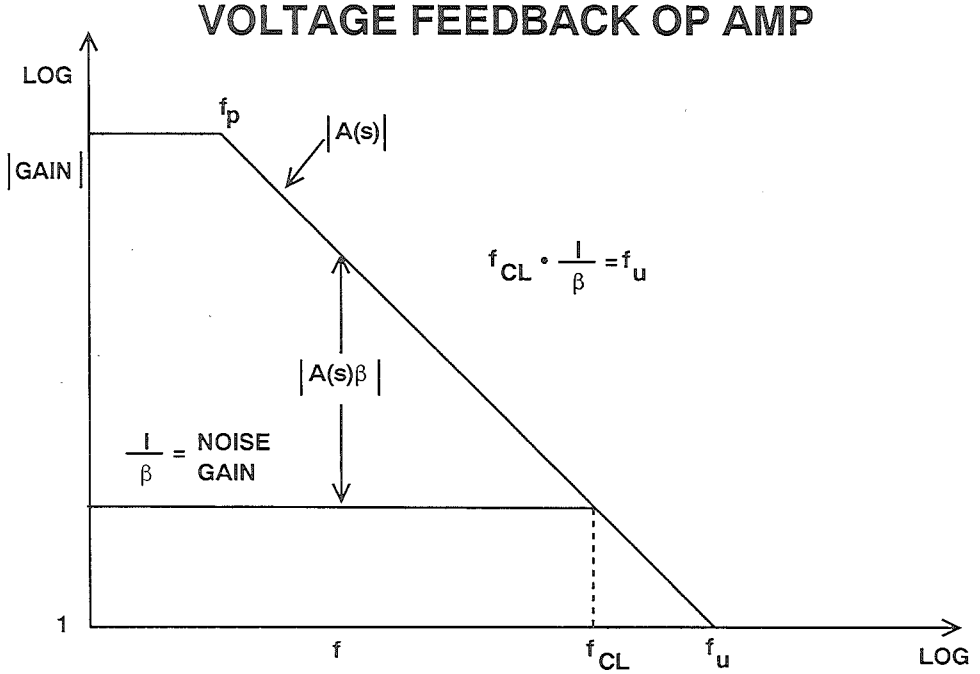


Figure 7.14

DC GAIN ACCURACY OF VOLTAGE FEEDBACK AMPLIFIERS

The dc open loop gain of the op amp must be sufficient to provide the necessary closed loop accuracy for the application. The dc gain error (assuming no gain errors in the feedback components) ε_{dc} is approximately equal to $1/|A_0\beta|$, where $A_0\beta$ is the loop gain at dc. For example, if 16 bit accuracy (0.0015%) is required for a unity gain inverter (Noise Gain = $1/\beta = 2$), then the dc open loop gain must be at least 131,072, or 102dB. The corresponding values of open loop gain required for 14 and 12 bit gain accuracy are 32,678 (90dB) and 8,192 (78dB) respectively. Note that for larger values of closed loop gain, correspondingly larger values of open loop gain are required to maintain the same amount of gain accuracy. The dc open loop gain specification of the amplifier should always be checked under the dc load conditions the ADC presents to the op amp output. In most op amps, the dc open loop gain decreases with heavier loading (decreasing load resistance).

Shift in the open loop gain over temperature will cause a corresponding shift in the closed loop gain. Variations by a factor of two are not uncommon in voltage feedback amplifiers. The percentage change in closed loop gain, ΔA_{cl}, for a percentage change in open loop gain, ΔA, is approximately equal to $\Delta A/|A_0\beta|$, where A_0 is the nominal dc open loop gain at room temperature. If this shift is too large, the designer can increase the feedback factor, β, select an op amp with better dc open loop gain stability, or select an op amp with a higher nominal dc open loop gain.

CALCULATING OP AMP OPEN LOOP GAIN REQUIRED FOR SPECIFIED DC GAIN ACCURACY

- $\varepsilon_{dc} \approx 1 / |A_O\beta|$
- Example: Unity-Gain Inverter ($\beta = 0.5$)
  16 Bit Gain Accuracy ($\varepsilon_{dc} = 0.000015$)

  $\therefore A_O = 131,072$, or 102dB

Figure 7.15

CALCULATING CHANGE IN CLOSED LOOP GAIN FOR CHANGE IN OPEN LOOP GAIN

- $\Delta A_{Cl} \approx \Delta A / |A_O\beta|$
- ΔA = Percentage Change in dc Open Loop Gain
- A_O = Nominal dc Open Loop Gain
- β = Feedback Factor
- ΔA_{Cl} = Percentage Change in Closed Loop Gain

Figure 7.16

VOLTAGE FEEDBACK OP AMP (G = -1, β = 0.5) DC LOOP GAIN, CLOSED LOOP BANDWIDTH, GAIN ACCURACY, AND GAIN STABILITY

Model Number	Closed Loop Bandwidth (MHZ)	Typical DC Loop Gain	Absolute Gain Accuracy (Bits)	Gain Stability Over Temperature (Bits)
AD829	50	25000	14.7	16.7
AD847	25	2000	10	12
AD841	20	20000	14.3	16.3
AD843	16	12000	13.6	15.6
AD845	8	125000	17	19
AD744	6.5	200000	17.7	19.7
OP-27	4	500000	19	21
AD711	1.5	100000	16.7	18.7

Note: $\pm$ 25% DC Loop Gain Variation Over Temperature Assumed

Figure 7.17

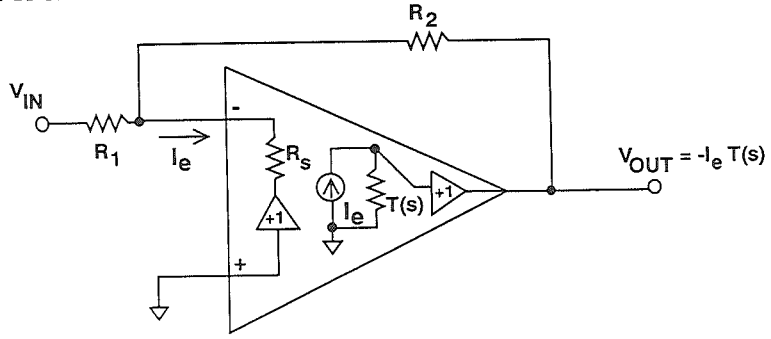
The dc loop gain, absolute gain accuracy (in bits), and closed loop bandwidth for a number of popular voltage feedback amplifiers are given in Figure 7.17 for the unity gain inverting mode.

It is also important that op amp open-loop gain be stable with output signal level. Changes in open-loop gain with signal level produce closed-loop non-linearity. Amplifiers which have lower initial open loop gains are obviously more sensitive to this effect.

CURRENT FEEDBACK AMPLIFIERS

The equivalent circuit for a current feedback amplifier is shown in Figure 7.18. The signal at the non-inverting input is applied to the inverting input through a unity-gain buffer with an output impedance R_S (usually between 10 and 100Ω). The current entering the inverting input is multiplied by the *transimpedance open loop gain*, T(s), to yield the output voltage. The feedback attenuation factor the current feedback amplifier is different than for the voltage feedback amplifier because of the low inverting input impedance, R_S). Solving the feedback equation yields the transfer function shown in Figure 7.18 The expression for the current feedback amplifier loop gain is different from that for a voltage feedback amplifier, however, it can be used in exactly the same manner in determining the amplifier closed loop accuracy at any frequency.

CURRENT FEEDBACK OP AMP EQUIVALENT CIRCUIT



$$\text{INVERTING SIGNAL GAIN} = -\left(\frac{R_2}{R_1}\right)\left(\frac{1}{1+\frac{1}{LG}}\right) \qquad \text{NON-INVERTING SIGNAL GAIN} = \left(1+\frac{R_2}{R_1}\right)\left(\frac{1}{1+\frac{1}{LG}}\right)$$

T(s) = OPEN LOOP TRANSIMPEDANCE GAIN

$$\beta_{cf} = \text{FEEDBACK FACTOR} = \frac{R_S \| R_1}{R_S \| R_1 + R_2}$$

$$A_{cf}(s) = \text{OPEN LOOP VOLTAGE GAIN} = \frac{T(s)}{R_S}$$

$$\text{LOOP GAIN} = LG = A_{cf}(s)\,\beta_{cf} = \frac{T(s)\{R_S \| R_1\}}{R_S\{R_S \| R_1 + R_2\}}$$

Figure 7.18

DC GAIN ACCURACY OF CURRENT FEEDBACK AMPLIFIERS

Further examination of the equivalent circuit of the current feedback amplifier reveal that the small error current, I_e, flows into the low impedance (R_S) inverting input of the amplifier and is multiplied by the open loop transimpedance gain, T_O (expressed in ohms), to give the output voltage. The feedback attenuation factor for the current feedback amplifier is given by $\beta_{cf} = R_S \| R_1/\{R_S \| R_1 + R_2\}$. The open loop dc voltage gain is given by $A_{cfo} = T_O/R_S$. Notice that if $R_S \rightarrow \infty$, the expression for β_{cf} reduces to $R_1/\{R_1 + R_2\}$ which is the same as for a voltage feedback amplifier. The expression for loop gain shown in Figure 7.18 can be used in exactly the same manner as with a voltage feedback amplifier in determining the gain accuracy and the gain drift.

The dc loop gain, absolute gain accuracy (in bits), and closed loop bandwidth for a number of popular current feedback amplifiers are given in Figure 7.19 for the unity gain inverting mode. The use of the recommended feedback resistor for optimum performance is assumed.

Although the loop gain of the AD9617 is only 2000, the circuit was designed to be extremely stable with signal level as shown in Figure 7.20, where the maximum deviation in dc closed loop gain across the 4V span is only 0.0009% (equivalent to 17 bits linearity).

7

CURRENT FEEDBACK OP AMP (G = -1) DC LOOP GAIN, CLOSED LOOP BANDWIDTH, GAIN ACCURACY, AND GAIN STABILITY

Model Number	Closed Loop Bandwidth (MHZ)	Typical DC Loop Gain	Absolute Gain Accuracy (Bits)	Gain Stability Over Temperature (Bits)
AD9617	190	2000	11	13
AD846	80	182000	17	19
OP-260	55	2600	11.4	13.4
AD844	20	2700	11.4	13.4

Note: ± 25% DC Loop Gain Variation Over Temperature Assumed

Figure 7.19

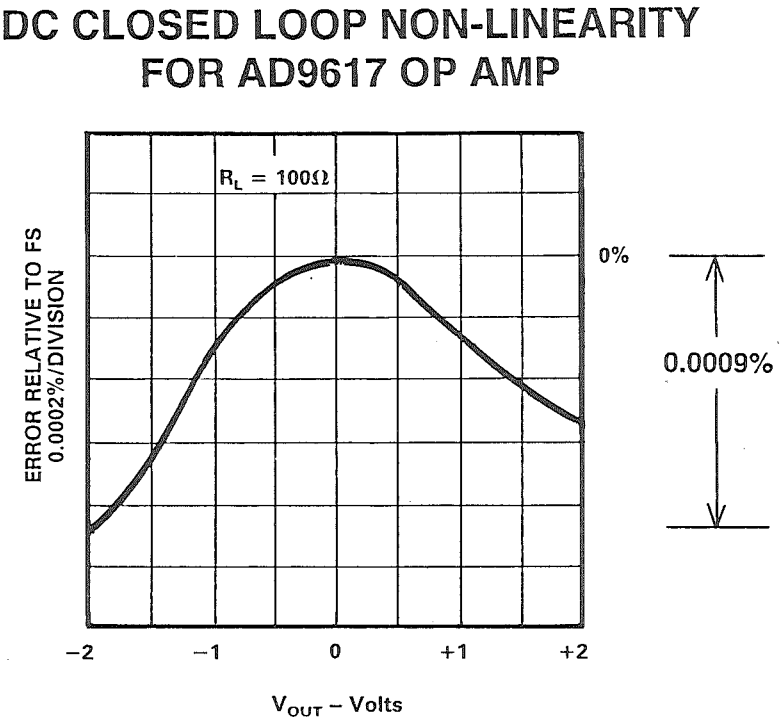


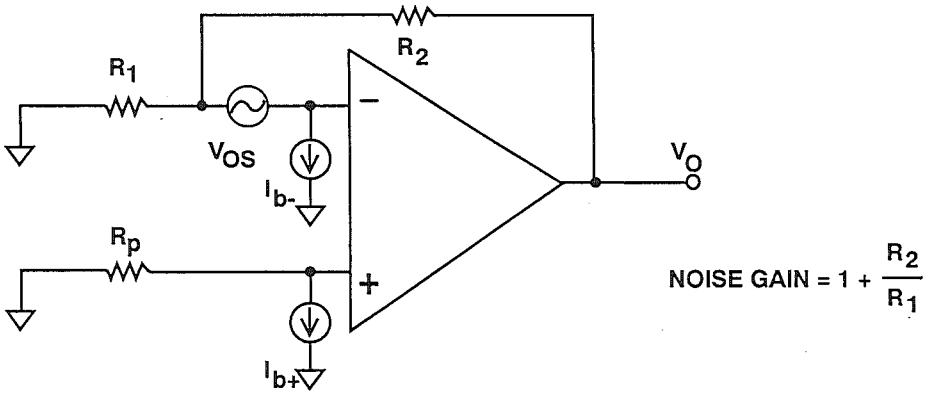
Figure 7.20

CALCULATING TOTAL OUTPUT VOLTAGE OFFSET AND DRIFT OF AN OP AMP

Calculating the dc error components which make up the output voltage offset and drift can be facilitated with the equations shown in Figure 7.21. These equations are applicable for either voltage feedback amplifiers or current feedback amplifiers. However, the inputs of a voltage feedback amplifier are symmetrical; therefore, the input bias currents are approximately equal. Due to the non-symmetrical input structure of the current feedback amplifier, however, the bias currents are usually different, and therefore, appropriate values as given in the data sheet must be used in the equation for I_{b+} and I_{b-}.

The total amplifier output offset voltage and offset voltage drift may then be summed with the dc errors of the ADC to obtain the total dc error. The equations assume that the op amp has infinite open loop gain, and that there is no error created by tolerances or drift in the components comprising the feedback network. In practice, it is common to provide small adjustments for gain and offset to eliminate the need for extremely tight resistor tolerances. Nevertheless, metal film resistors should be used in order to provide good ratio tracking and stability over time and temperature.

OP AMP OUTPUT OFFSET VOLTAGE MODEL



$$V_O = \pm V_{OS}\left[1 + \frac{R_2}{R_1}\right] \pm I_{b+}R_p\left[1 + \frac{R_2}{R_1}\right] \pm I_{b-}R_2$$

Figure 7.21

LARGE OFFSET SHIFTS REQUIRE GAIN REDUCTION TO PREVENT ADC CLIPPING

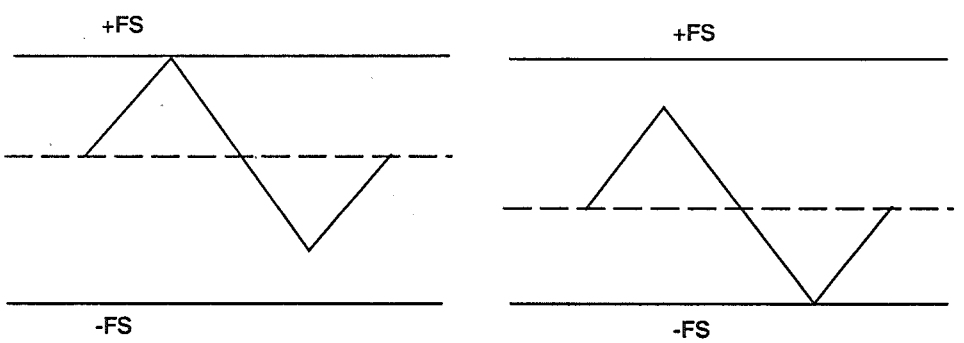


Figure 7.22

EFFECTS OF DC DRIFT ON SYSTEM DYNAMIC RANGE

DC drift in the op amp and the ADC limit the system dynamic range as shown in Figure 7.22. Ideally, the effective gain of the system should be set such that the maximum expected peak-to-peak input signal exactly fills the input range of the ADC. This setting will give the highest dc resolution, but the ADC may clip the fullscale signal if there is sufficient offset and/or gain drift. In order to prevent clipping, therefore, the signal gain is reduced slightly to provide sufficient headroom. Large drifts require more headroom, and thereby further reduce the effective dynamic range of the system.

VOLTAGE FEEDBACK OP AMP BANDWIDTH SPECIFICATIONS

The gain-bandwidth product of an op amp is simply the product of the closed loop gain and the corresponding bandwidth at a specified frequency. For a voltage feedback amplifier which has a single-pole frequency response, this product is constant over a wide range of frequencies (see Figure 7.23). If the op amp is stable at unity gain, the frequency at which the open loop response crosses unity gain is called the unity gain bandwidth frequency. The gain-bandwidth specification may thus be used to calculate the closed-loop bandwidth for various values of closed-loop gain.

A key point often confused in selecting voltage feedback op amps based on bandwidth is that the closed loop gain, A_{cl}, refers to the *noise gain*, $1/\beta$, and not the signal gain (see Figure 7.24). For instance, in the non-inverting mode, the dc signal gain ($1+R_2/R_1$) is equal to the dc noise gain. In the inverting mode, however, the noise gain remains $1+R_2/R_1$, but the signal gain is now $-R_2/R_1$. For example, if an op amp has a gain-bandwidth product of 10MHz, the closed loop bandwidth for a non-inverting unity gain configuration is 10MHz, while that of a unity-gain inverter is only 5MHz.

Another important point is that some op amps are optimized to operate at high gains, and are not stable under low- or unity-gain conditions. With these op amps, the gain-bandwidth product is meaningful only over the region of stable closed loop gains. This type of amplifier can, however, be used at low inverting signal gains by the addition of a shunt resistor to ground as shown in Figure 7.25. The extra resistor is chosen such that the noise gain is greater than the minimum value required for stability. The penalty is increased sensitivity to input offset voltage and input noise voltage as well as lower signal bandwidth.

LOG-LOG BODE PLOT FOR VOLTAGE FEEDBACK OP AMP

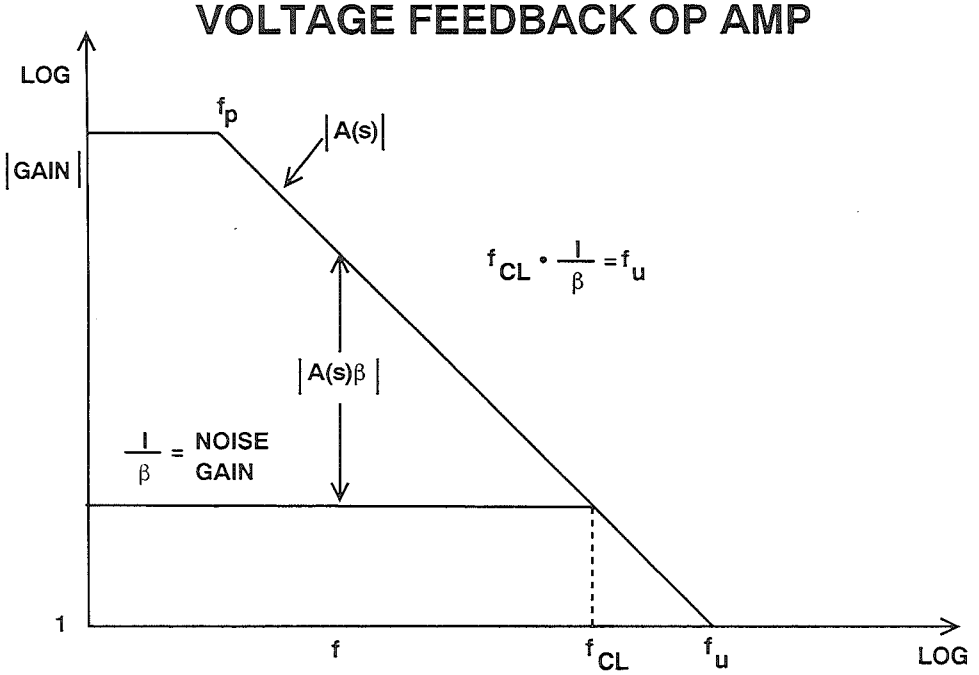
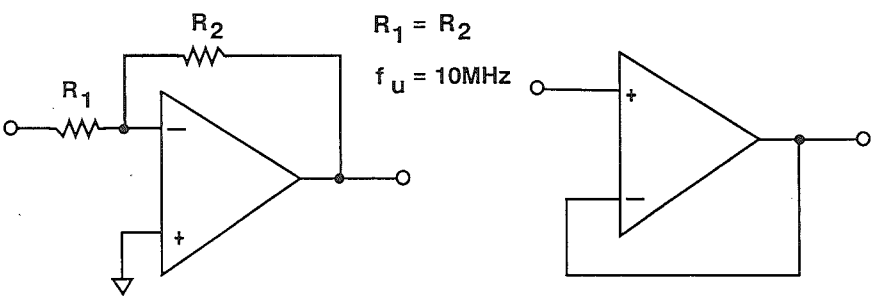


Figure 7.23

7

RELATIONSHIP BETWEEN NOISE GAIN, SIGNAL GAIN, AND BANDWIDTH FOR OP AMP WITH UNITY GAIN BW OF 10MHz



NOISE GAIN = $\frac{1}{\beta} = 1 + \frac{R_2}{R_1} = 2$

SIGNAL BW = 5MHz

SIGNAL GAIN = -1

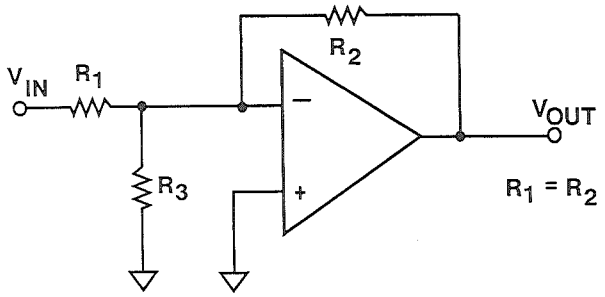
NOISE GAIN = 1

SIGNAL BW = 10MHz

SIGNAL GAIN = +1

Figure 7.24

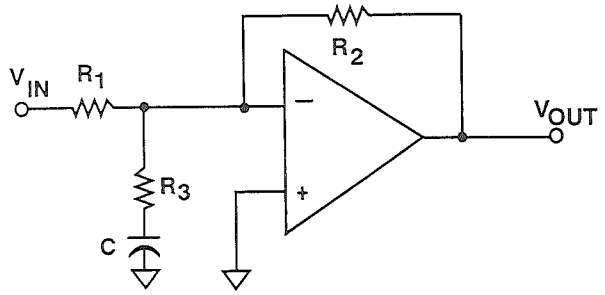
OPERATING NON-UNITY GAIN STABLE OP AMPS AT UNITY GAIN IN THE INVERTING MODE



$$\text{SIGNAL GAIN} = -\frac{R_2}{R_1} = -1$$

$$\text{NOISE GAIN} = 1 + \frac{R_2}{R_1 \| R_3}$$

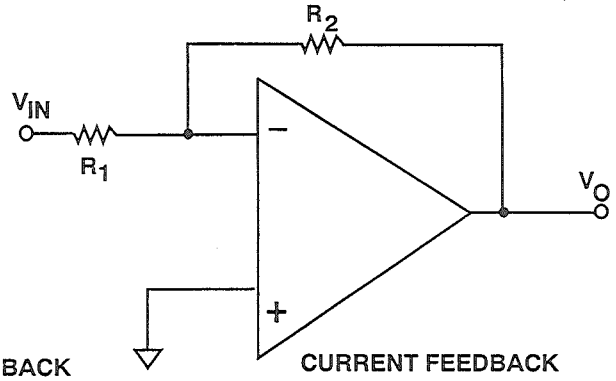
CHOOSE R_3 FOR MINIMUM STABLE NOISE GAIN



LARGE C GIVES HIGH AC NOISE GAIN, BUT DC NOISE GAIN REMAINS LOW

Figure 7.25

VOLTAGE FEEDBACK AND CURRENT FEEDBACK INVERTER CLOSED LOOP GAIN EQUATIONS



VOLTAGE FEEDBACK

$$\frac{V_O}{V_{IN}} = \frac{-R_2/R_1}{1 + \frac{1}{A(s)}\left[1 + \frac{R_2}{R_1}\right]}$$

CURRENT FEEDBACK

$$\frac{V_O}{V_{IN}} = \frac{-R_2/R_1}{1 + \frac{R_2}{T(s)}\left[1 + \frac{R_S}{R_1} + \frac{R_S}{R_2}\right]}$$

ASSUME $R_S << R_1$ AND R_2 NOTE: R_2 FIXED

$$\frac{V_O}{V_{IN}} \approx \frac{-R_2/R_1}{1 + \frac{R_2}{T(s)}}$$

Figure 7.26

CURRENT FEEDBACK OP AMP BANDWIDTH SPECIFICATIONS

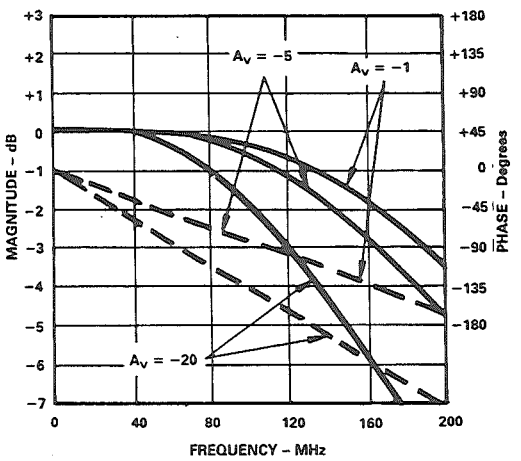
The inverting mode transfer functions for the voltage feedback amplifier and the current feedback amplifier are compared in Figure 7.26. Notice that for the voltage feedback amplifier, the frequency-dependent term, 1/A(s), is multiplied by the noise gain, $(1 + R_2/R_1)$. This implies that the closed loop bandwidth is approximately inversely proportional to the noise gain, hence, the product of the noise gain and the closed loop bandwidth is constant.

In the current feedback amplifier, however, if $R_S << R_1$ and R_2, the closed loop bandwidth is independent of the gain, R_2/R_1, and depends only upon the feedback resistor R_2. Furthermore, most current feedback amplifiers are optimized for best performance for a fixed value of R_2. This implies that the closed loop bandwidth of a current feedback amplifier will remain fairly constant regardless of closed loop gain, provided the gain is changed by varying only R_1.

Current feedback (or transimpedance) op amps therefore have bandwidths which are relatively independent of closed loop gains (assuming a the feedback resistor value remains constant). Therefore, it is inappropriate to refer to the gain-bandwidth product of this type of amplifier. For instance, the signal bandwidth of the AD9617 with a 400Ω feedback resistor is approximately 190MHz for a closed loop signal gain of -1, and approximately 165MHz for a closed loop-signal gain of -5 (see Figure 7.27). In the first case, the so-called gain-bandwidth product would be 190MHz (1 x 190MHz), while in the second case it would be 825MHz (5 x 165MHz). In addition, current feedback amplifiers are usually optimized for a fixed value of feedback resistor. Increasing the feedback resistor lowers the bandwidth proportionally, while decreasing the value may lead to instability. The closed loop signal bandwidth for current feedback amplifiers should therefore be determined from curves on the data sheet.

7

GAIN AND PHASE RESPONSE FOR AD9617 CURRENT FEEDBACK OP AMP



GAIN	BW	PRODUCT
-1	190MHz	190MHz
-5	165MHz	825MHz

Figure 7.27

CALCULATING GAIN ERRORS FOR OP AMPS AS A FUNCTION OF FREQUENCY

Gain error for various input frequencies can be approximated by the useful formula $f_{max} = f_c\sqrt{2\varepsilon}$, where f_c is the op amp (single-pole response assumed) closed loop signal bandwidth, and ε is the amplitude error at frequency f_{max} (Reference 1, p.101). For example, in order for a signal be remain flat within 0.1dB ($\varepsilon = 0.01$) up to a frequency of 50kHz, a minimum closed loop signal bandwidth of 353kHz is required. If an amplitude flatness of 0.1dB is required up to a frequency of 30MHz, a closed loop signal bandwidth of 212MHz is needed.

CALCULATING GAIN ERRORS OVER FREQUENCY

- $f_{max} = f_{cl}\sqrt{2\varepsilon}$
- f_{max} = Maximum Input Frequency for Gain Error < ε
- f_{cl} = Single-Pole Closed-Loop Bandwidth
- Example: For ε = 0.1dB @ f_{max} = 30MHz,

  f_{cl} = 212MHz

Figure 7.28

OP AMP DISTORTION SPECIFICATIONS

In selecting a drive amplifier for an ADC, it is most important that the harmonic distortion performance of the amplifier exceed that of the ADC, so that the op amp does not limit the system SFDR. Distortion specifications must be examined in addition to bandwidth specifications in making the right selection. Ideally, the amplifier harmonic distortion should be measured under the amplitude and loading conditions presented by the ADC.

Most amplifiers suitable for ADC drivers will have harmonic distortion versus frequency plots on the data sheet. A typical plot for the AD845 amplifier (GBW = 16MHz) is shown in Figure 7.29. Output amplitude is 3V rms (8.5V peak-to-peak), and loading is 500Ω. Notice that the harmonic distortion product of the AD845 are greater than 100dB below fullscale for signals up to 100kHz.

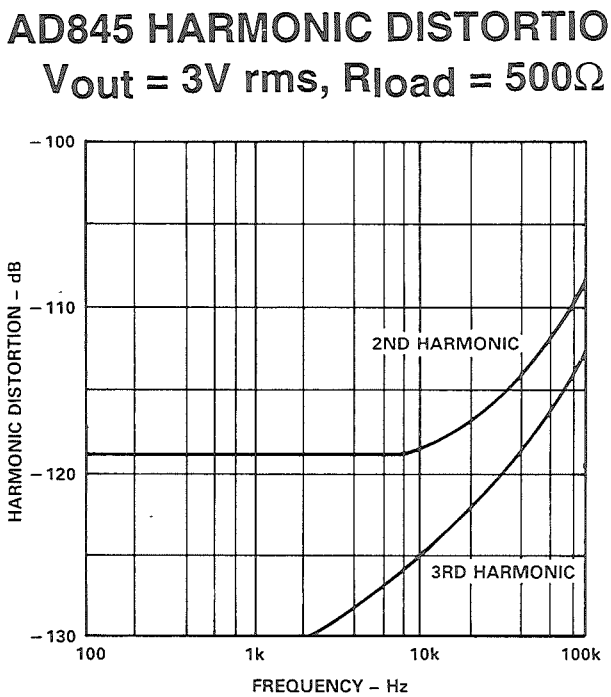


Figure 7.29

7

OP AMP SETTLING TIME SPECIFICATIONS

Settling time is especially important in applications such as pulse-height analysis where the amplitude of pulses must be measured accurately. Other applications requiring fast settling time are in multiplexer output buffering and CCD Imaging. Measuring settling time directly with a standard oscilloscope is difficult because the scope is severely overdriven. Therefore, settling time measurements in the inverting mode usually utilize a circuit such as that shown in Figure 7.30 for measuring the settling time of the AD845 (see Figure 7.31). The error signal generated at the false summing junction is much less likely to overdrive the scope.

Special digital sampling oscilloscopes such as the Data Precision mainframe with the 640 digitizing plug-in can be used to measure settling time directly as shown in Figure 7.32 for the AD9617 current feedback amplifier.

SETTLING TIME TEST SETUP FOR AD845

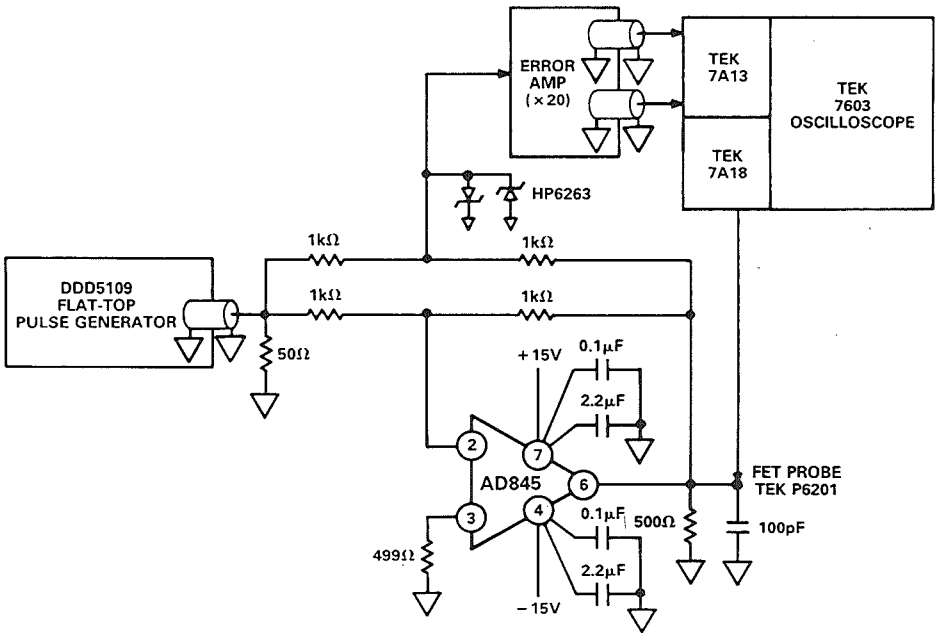


Figure 7.30

AD845 OP AMP SETTLING TIME

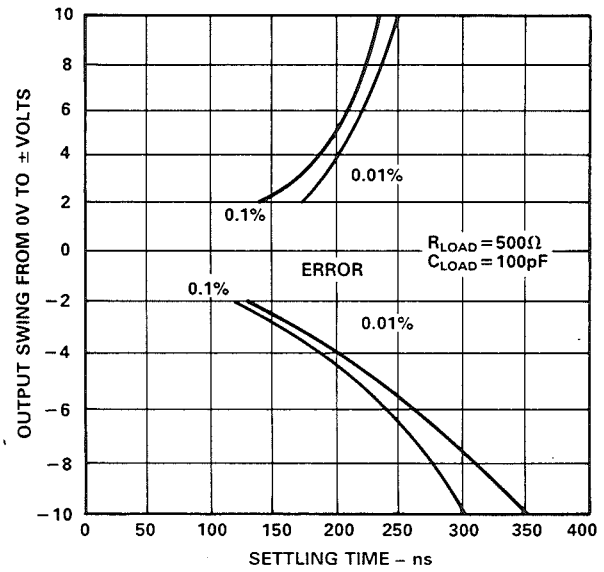


Figure 7.31

AD9617 SETTLING TIME MEASURED WITH DATA PRECISION 640 DIGITIZING PLUG-IN

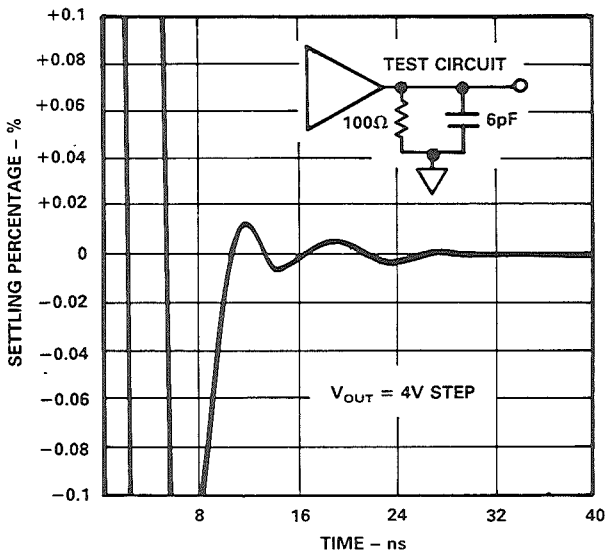


Figure 7.32

7

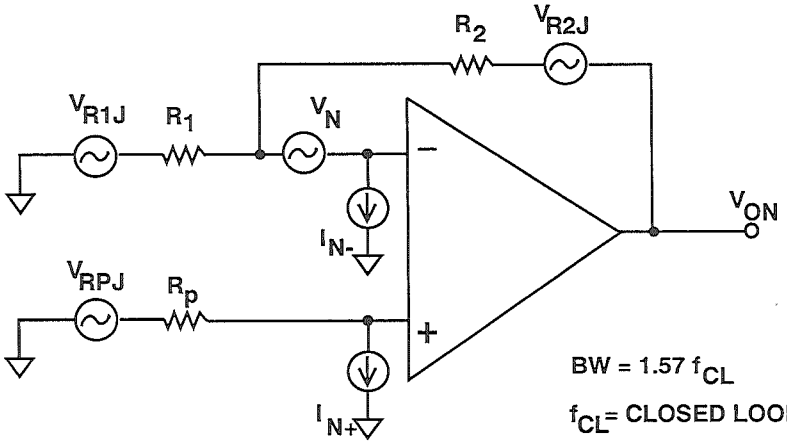
OP AMP NOISE SPECIFICATIONS

Op amp noise performance is usually specified in terms of input voltage noise spectral density and input current noise spectral density. The other source of noise in the op amp circuit is the thermal noise, or Johnson noise, generated by the external resistors. A general model showing all the noise sources is shown in Figure 7.33 along with the equations which reflect these noise components to the op amp output.

Although voltage and current noise spectral densities are not constant across the frequency band, specifically in the 1/f region (see Figure 7.34 for the AD OP-27), reasonable estimates of output noise can be made be made by assuming a nominal value across the entire frequency band of integration (the spectral density values at 1kHz are often used, for example). This assumption is especially true in most ADC applications, where the bandwidth of integration extends over several decades of frequency.

The bandwidth for integration depends on the feedback network and the noise component of interest. In the case of the voltage feedback op amp circuit shown in Figure 7.35, the signal bandwidth is limited by the addition of C_2. The input voltage noise, V_n, the Johnson noise contributed by the resistor R_p, and the non-inverting input current noise, I_{n+}, are multiplied by the circuit ac noise gain $(1 + C_1/C_2)$ and integrated over the entire closed loop noise bandwidth, f_{cl}. However, the output noise generated by resistors R_1 and R_2, and the inverting input current noise, I_{n-}, is integrated only over the signal bandwidth f_2 which is equal to $1/2\pi R_2 C_2$.

OP AMP NOISE MODEL



$$V_{ON} = \sqrt{BW}\sqrt{I_{N-}^2 R_2^2 + I_{N+}^2 R_p^2 \left[1+\frac{R_2}{R_1}\right]^2 + V_N^2 \left[1+\frac{R_2}{R_1}\right]^2 + 4kTR_2 + 4kTR_1\left[\frac{R_2}{R_1}\right]^2 + 4kTR_p\left[1+\frac{R_2}{R_1}\right]^2}$$

Figure 7.33

INPUT NOISE SPECTRAL DENSITIES FOR ADOP-27 BIPOLAR 8MHz OP AMP

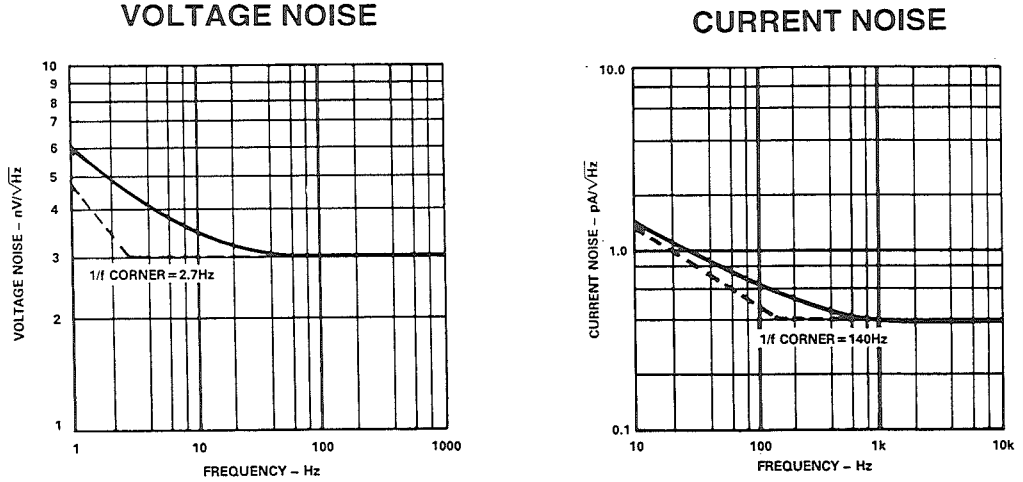
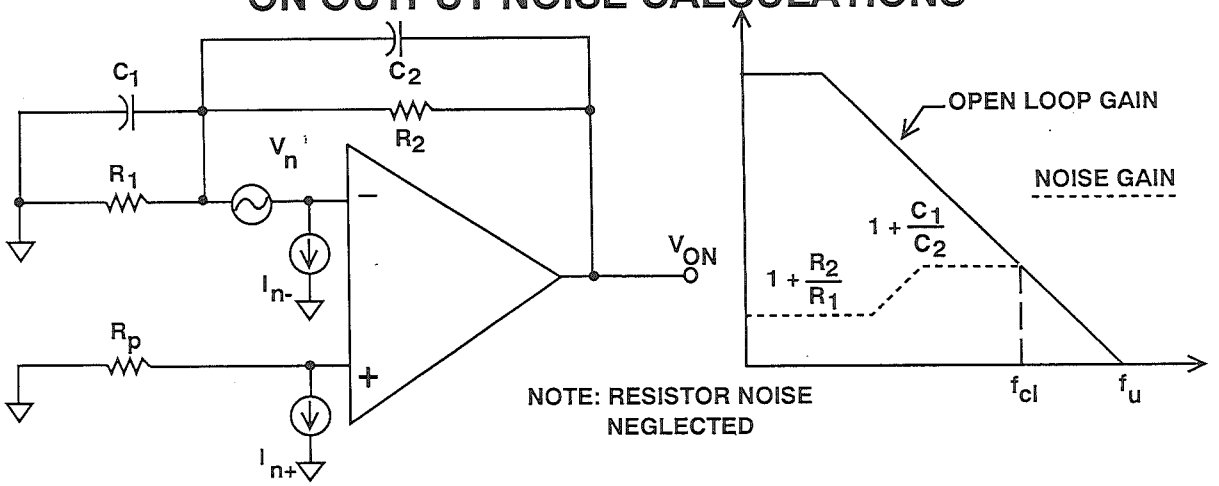


Figure 7.34

EFFECTS OF NOISE GAIN ON OUTPUT NOISE CALCULATIONS



$$V_{ON} \approx \sqrt{V_n^2 \left[1 + \frac{C_1}{C_2}\right]^2 (1.57\, f_{cl}) + I_{n-}^2 R_2^2 (1.57 f_2) + I_{n+}^2 R_p^2 \left[1 + \frac{C_1}{C_2}\right]^2 (1.57 f_{cl})}$$

Where f_u = Op Amp Unity Gain Bandwidth Frequency

$$f_{cl} = \text{Closed Loop Bandwidth} = \frac{f_u}{1 + \frac{C_1}{C_2}}, \quad f_2 = \text{Signal Bandwidth} = \frac{1}{2\pi R_2 C_2}$$

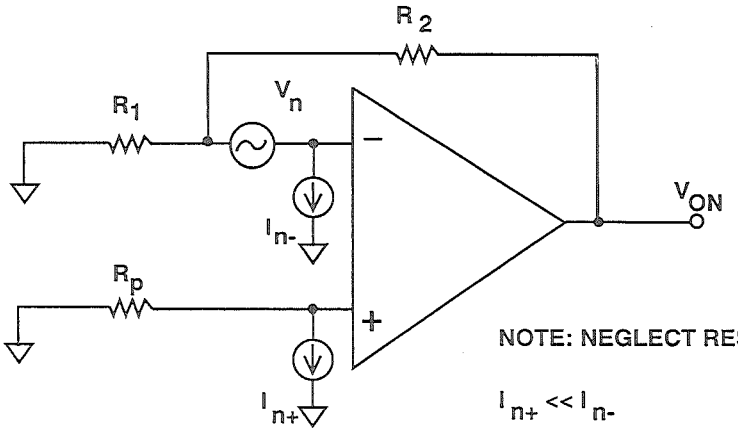
Figure 7.35

The Bode plots of the output noise spectral densities for this circuit are shown in Figure 7.35. The factor of 1.57 in the equations is necessary to convert the single-pole corner frequency to the equivalent noise bandwidth. The total output voltage noise is then obtained by combining each output contributor on an rms basis. Notice that the Johnson resistor noise has been neglected in the equations. This is a valid assumption when working with impedances of less than approximately 10kΩ.

The inverting and non-inverting input current noise for voltage feedback amplifiers is usually equal due to their symmetrical input structure. With current feedback amplifiers, however, the terms are usually different, with the inverting input current noise being the most significant of the two.

With wide bandwidth current feedback amplifiers, the capacitor C_2 is not used, and the bandwidth of integration for all the noise components is the closed loop signal bandwidth. The approximate equations for the calculation of the output noise of a current feedback amplifier are given in Figure 7.36.

CURRENT FEEDBACK OP AMP OUTPUT NOISE APPROXIMATIONS



$$V_{ON} = \sqrt{1.57\, f_{cl}} \sqrt{V_n^2 \left[1 + \frac{R_2}{R_1}\right]^2 + I_{n-}^2 R_2^2}$$

f_{cl} = Op Amp Closed Loop Bandwidth

Figure 7.36

INPUT BANDWIDTH OF ADCs

ADC	Resolution	Maximum Sampling Rate	Input Bandwidth
AD9006	6	500MSPS	550MHz
AD9028/9038	8	300MSPS	250MHz
AD9060	10	75MSPS	175MHz
AD1674	12	100kSPS	1MHz
AD7886	12	750kSPS	20MHz
AD1671	12	1MSPS	2MHz
AD9005A	12	10MSPS	40MHz
AD9032	12	25MSPS	150MHz
AD7871	14	83kSPS	3MHz
AD679	14	100kSPS	1MHz
AD9014	14	10MSPS	60MHz
AD676	16	100kSPS	1MHz
AD7874	16	166kSPS	3MHz
AD1382	16	500kSPS	2.2MHz

Figure 7.37

EFFECTS OF ADC INPUT BANDWIDTH ON AMPLIFIER OUTPUT NOISE

Most of todays sampling ADCs have input bandwidths which far exceed the Nyquist bandwidth, $f_S/2$. This is illustrated in Figure 7.37 for a number of popular sampling ADCs. For a first order approximation, assume that the input bandwidth of the ADC is a single pole filter. This filter may therefore limit the bandwidth of integration for the op amp total output noise voltage.

SPECIFYING THE ANTIALIASING FILTER

Properly specifying the antialiasing filter requires a knowledge of the signal's spectral characteristics as well as the system dynamic range requirements. Consider the case of a signal which has a maximum fullscale frequency content of f_a = 35kHz sampled at a rate of f_S=100kSPS. Assume the signal has the spectrum shown in Figure 7.38 and is attenuated by 30dB at 65kHz (f_S- f_a). Observe that the system dynamic range is limited to 30dB at 35kHz because of the aliased components.

7

ANTIALIASING FILTER EFFECTS ON DYNAMIC RANGE

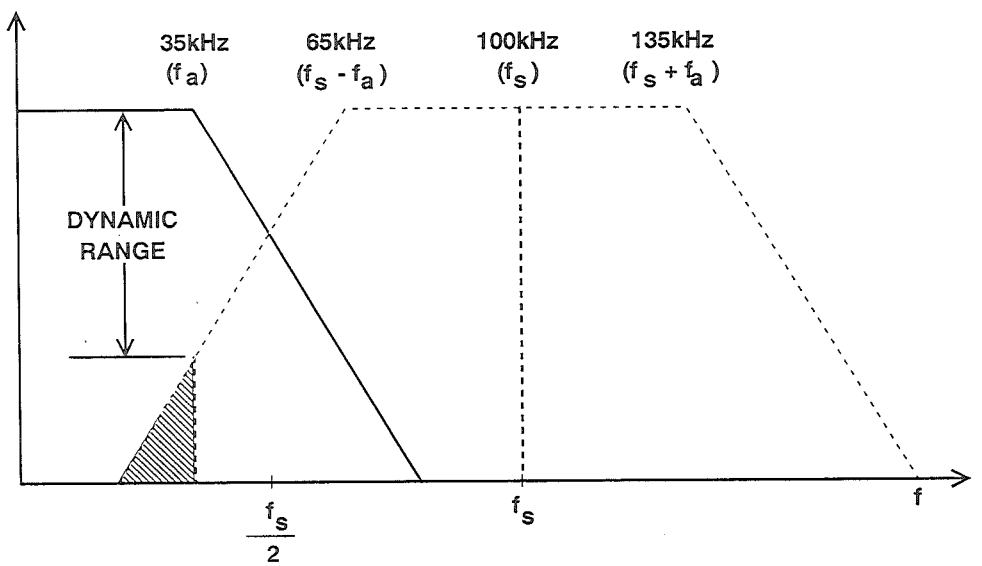


Figure 7.38

If additional dynamic range is required, an antialiasing filter must be provided to provide more attenuation at 65kHz). If a dynamic range of 74dB (12 bits) at 35kHz is desired, then the antialiasing filter attenuation must go from 0dB at 35kHz to 44dB at 65kHz. This is an attenuation of 44dB in approximately one octave, therefore, a 7 pole filter is required. (Each filter pole provides approximately 6dB attenuation per octave).

One must also consider that broadband noise may be present with the signal which can also alias within the bandwidth of interest. This is especially true with wideband op amps which provide low distortion levels.

POSITIONING THE ANTIALIASING FILTER FOR OPTIMUM SYSTEM NOISE PERFORMANCE

For lower frequency antialiasing filters (up to about 200kHz), active filters offer an attractive alternative to traditional passive filters (See Section 6 for further discussions of active filter design). The output of an active filter is usually taken from the final stage op amp in the filter. This final stage should be capable of driving the ADC at the appropriate level and at an acceptable noise and distortion level. Remember that the output noise spectral density of the final stage driving the ADC must be integrated over the entire front-end ADC bandwidth. In most cases, the ADC bandwidth is considerably more than that of the maximum signal of interest.

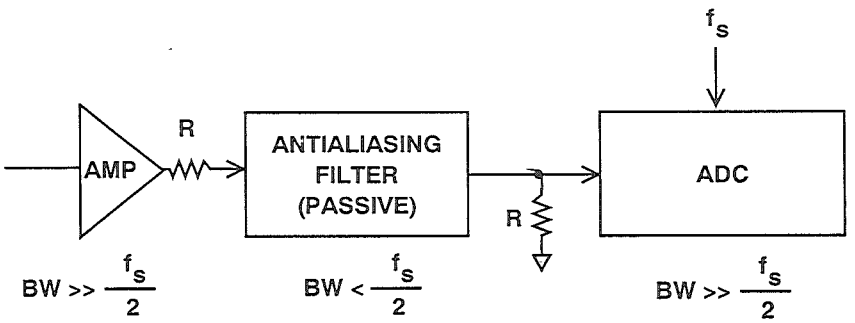
Higher frequency passive filters are usually designed to have impedances between 50 and 100Ω. The input characteristics of the ADC must be fully understood in order to correctly place these filters. If the input of the ADC is a fairly high impedance with low capacitance (relative to the filter impedance), it is better to place the antialiasing filter directly ahead of the ADC as shown in Figure 7.39. This configuration is advantageous because the output noise of the drive amplifier is now bandlimited by the filter.

DRIVING NON-SAMPLING SAR ADCS (AD574-SERIES)

There are many applications which do not require the ADC to digitize dynamic signals. In the past, these needs have been well-served with successive approximation (SAR) ADCs such as the industry-standard AD574 and improved, faster versions such as the AD674B (15μs conversion time) and the AD774B (8μs conversion time). A functional block diagram of the AD774B is shown in Figure 7.40 and key specifications are given in Figure 7.41.

A simplified block diagram of the SAR ADC and the drive amp is shown in Figure 7.42. During the conversion cycle, the internal 12 bit current output DAC is sequenced by the SAR from the most-significant-bit (MSB) to least-significant-bit (LSB) to provide an output current which accurately balances the input signal current through the input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current. If the sum is less, the bit is left on. If more, the bit is turned off. After testing all the bits, the SAR contains a 12 bit binary code which accurately represents the input signal to within ± 1/2 LSB. The ADC input current is thereby modulated by the

ANTIALIASING FILTER REDUCES OP AMP OUTPUT NOISE WHEN DRIVING ADCs WITH LARGE BANDWIDTHS



OP AMP OUTPUT NOISE INTEGRATED OVER FILTER BW, NOT ADC BW

Figure 7.39

7

AD674B/AD774B SAR ADC ENCODER BLOCK DIAGRAM

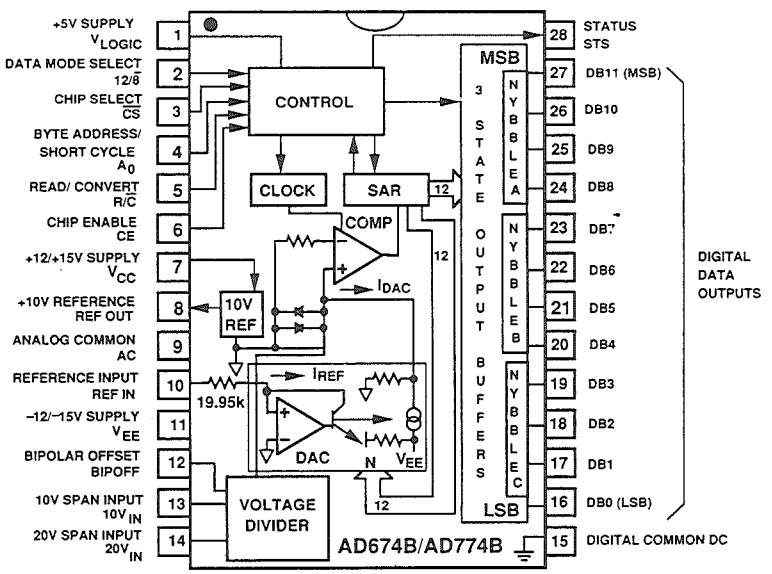


Figure 7.40

AD674B/AD774B KEY SPECIFICATIONS

- Industry-Standard AD574 Pinouts
- 12 Bit Resolution
- 15μs (AD674B) and 8μs (AD774B) Conversion Time
- 375mW Power Dissipation (±15 Volt Supplies)

Figure 7.41

SAR ADC ENCODER INPUT TRANSIENT LOAD CURRENTS

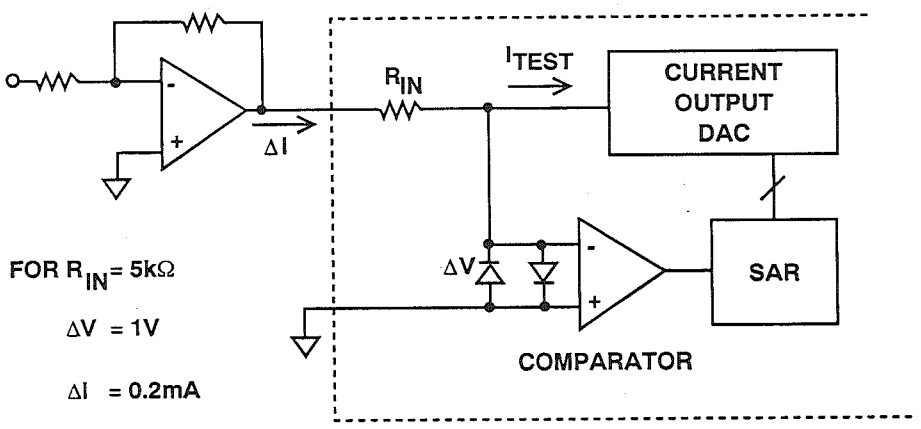


Figure 7.42

DAC test current at a frequency which is equal to the internal clock rate. Each time the internal DAC is switched, transient voltages of a few hundred millivolts may occur across the clamping diodes. For example, a 1V transient across the 5kΩ input resistance produces a transient load current of 0.2mA which must be supplied by the drive op amp.

The 12 bit AD774B has a total conversion time of 8μs. The internal SAR clock frequency is approximately 1.5MHz corresponding to a period of 670ns. Therefore, the output of the drive amp must settle to better than12 bit accuracy (± 1/2 LSB = ±1.2mV for a 10V input range) in less than 670ns after the application of the transient load current. The following discussion will aid in estimating the settling time of op amps to these transient load currents.

The closed loop output impedance of op amps increases with frequency (as shown in Figure 7.43 for the AD845) and may be as great as several hundred ohms at high frequencies due to the equivalent output inductance of the complementary emitter follower output stage. The transient load current will develop a transient voltage across this impedance at the op amp output. This small-signal voltage perturbation will exponentially decay with a time constant equal to $1/2\pi f_{cl}$ (f_{cl} = closed loop bandwidth) if the op amp exhibits single pole response (see Figure 7.44). The simple exponential decay formula can be used to determine the settling to any desired accuracy.

7

AD845 CLOSED LOOP OUTPUT IMPEDANCE

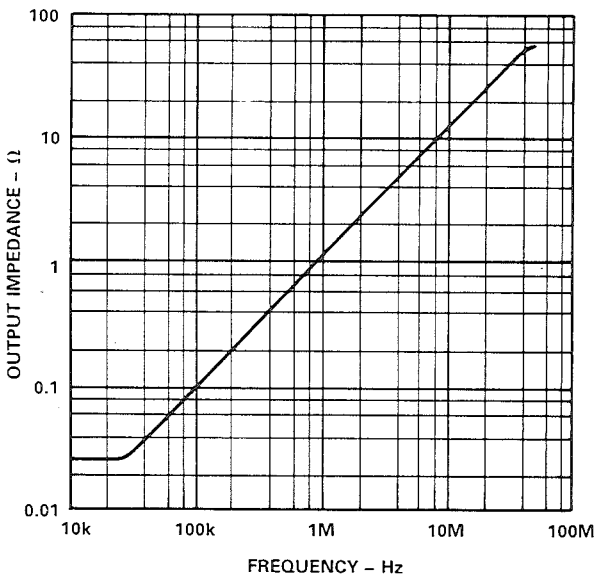


Figure 7.43

SMALL SIGNAL MODEL ALLOWS YOU TO ESTIMATE OP AMP SETTLING TIME DUE TO TRANSIENT LOAD CURRENT

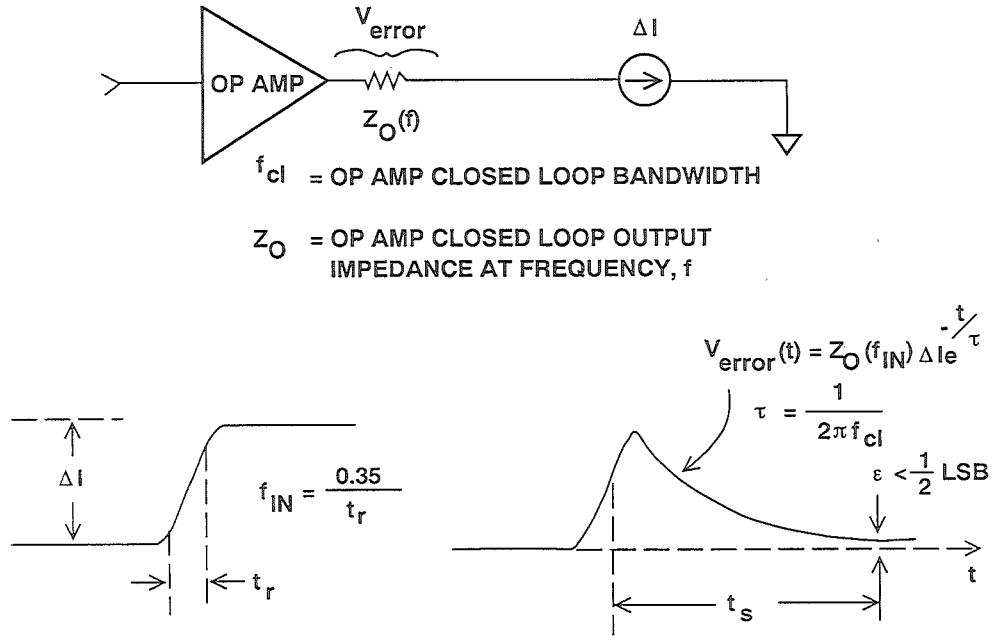


Figure 7.44

AD845 SETTLING TIME

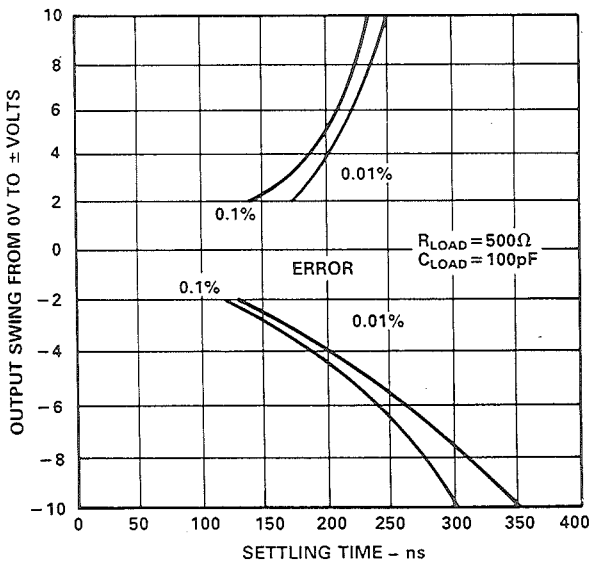


Figure 7.45

A more conservative approach is to examine the actual small signal settling time of the op amp with respect to the internal SAR clock period. Settling times for various output pulse amplitudes to various accuracies for the AD845 is shown in Figure 7.45. Curves such as these may be used to evaluate the amplifier response to transient load currents, and are particularly useful if the transient load currents are large.

The AD845 is a precision CBFET op amp which has a bandwidth of 16MHz, a small signal settling time of less than 200ns to 0.01%, and an open loop gain of 250,000. It is therefore ideally suited to driving precision ADCs with resolutions up to 16 bits. Key specifications for the AD845 are shown in Figure 7.46.

A much less attractive alternative to selecting the proper precision fast-settling op amp is to heavily bypass the ADC input heavily as shown in Figure 7.47. The capacitor must be large enough that the transient current causes its voltage to change by less than 1/2 LSB (1.2mV for a 12 bit ADC with a 10V input range) during the 670ns clock period. For the example shown, a 0.22μF capacitor or greater is required. This implies that the driving op amp must be stable for large capacitive loads. Bandwidth is also severely limited by the large capacitor. Selecting a drive amp with sufficient settling time to the transient load current is usually the preferred solution.

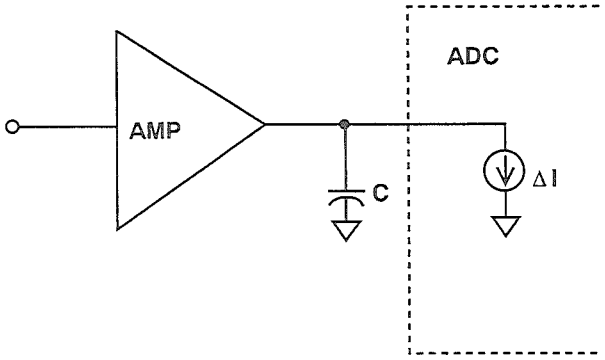
There are many cases where a sufficiently accurate model of the SAR ADC input circuit can be derived from data sheet information as in the above example. This simple model may then be used with the op amp Spice macromodel in to evaluate the effects of the ADC transient load currents on the input signal.

AD845 CBFET KEY SPECIFICATIONS

- 0.25mV Max Input Offset Voltage
- 5μV/°C Max Offset Voltage Drift
- 0.5nA Input Bias Current
- 350ns Settling Time to 0.01%
- 16MHz Unity-Gain Bandwidth
- 25nV/$\sqrt{Hz}$, 2pA/$\sqrt{Hz}$ Noise at 1kHz

Figure 7.46

BYPASSING ADC INPUT TO ABSORB TRANSIENT LOAD CURRENTS



$$C > \frac{\Delta I \cdot \Delta T}{\Delta V}$$

FOR AD774B SAR ADC:

ΔI = 0.2mA

ΔT = 670 ns

ΔV = 0.6mV (1/4 LSB)

THEN C > 0.22μF

Figure 7.47

DRIVING NON-SAMPLING SUBRANGING ADCS (AD671)

Another popular ADC architecture is called *subranging*. Digital correction is often used to correct for errors made in some of individual conversions required to achieve the total required conversion accuracy. A block diagram of the AD671 subranging 12 bit 500ns ADC is shown in Figure 7.48 and key specifications are given in Figure 7.49.

The analog to digital conversion in the AD671 takes place in four independent steps or flashes. The analog input signal is subranged to an intermediate residue voltage for the final 12 bit result by utilizing multiple flashes with subtraction DACs. Overlap bits correct errors made in the first three steps.

A simplified diagram of the input circuit of the AD671 is shown in Figure 7.50. The signal source driving the ADC must be capable of maintaining the input voltage constant under dynamically-changing load conditions. When the AD671 starts its conversion cycle, the subtraction DAC will sink up to 5mA from the source driving the analog input. The source must respond to this current step by settling the input voltage back to a fraction of an LSB before the final 12 bit decision is made. Unlike SAR ADCs, where the input voltage must settle to a fraction of an LSB before each successive bit decision is made, the AD671 requires the analog input voltage to settle to within 12 bits before the third flash conversion, approximately 200ns. Op amps such as the AD841, AD843, AD845, or the AD847 are suitable for this application.

Figure 7.51 shows a four-channel high-speed data acquisition system utilizing the AD684 quad sample-and-hold (1μs acquisition time to 12 bits), the ADG201HS CMOS Multiplexer (50ns switching time), an AD841 buffer amplifier (110ns settling to 0.01%), an AD588 Reference, and the AD671 ADC (200ns conversion time). The AD684 is config-

AD671 12-BIT, 500ns SUBRANGING ADC ENCODER BLOCK DIAGRAM

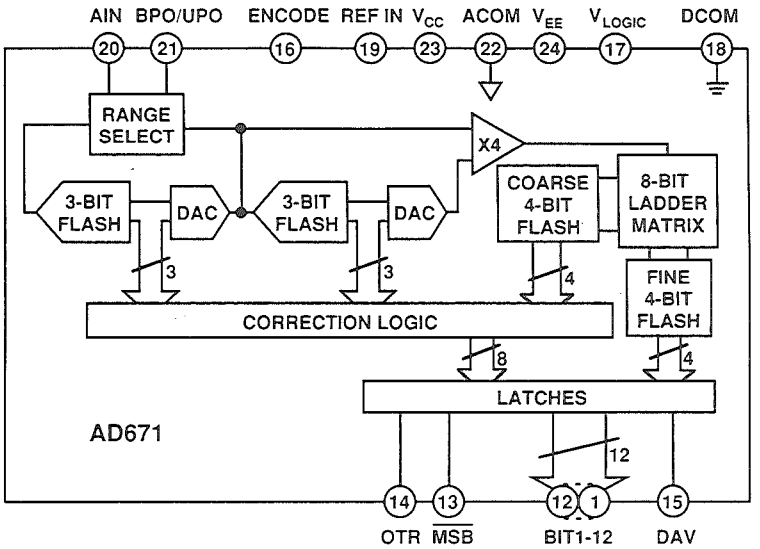


Figure 7.48

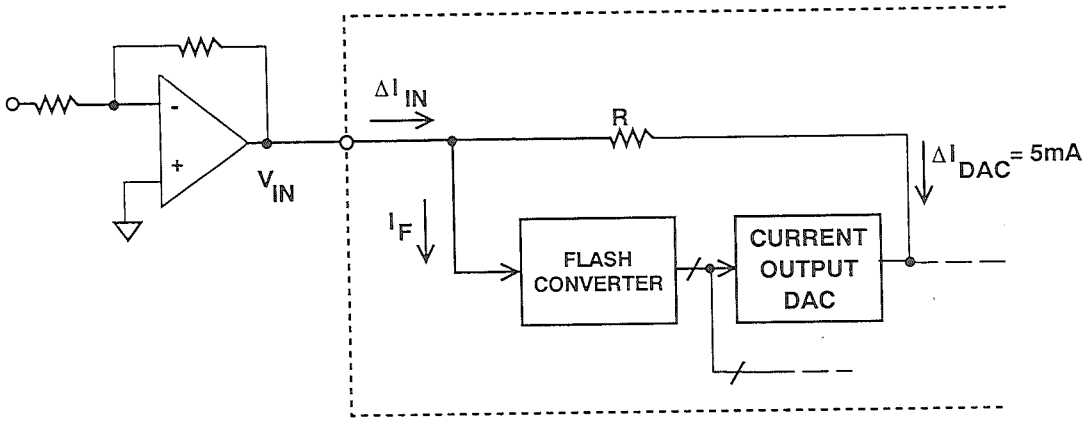
7

AD671 ADC KEY SPECIFICATIONS

- 12 Bit Resolution
- 500ns Conversion Time
- Digitally Corrected Subranging Architecture
- Low Power: 475mW
- 24-Pin Skinny DIP Package

Figure 7.49

AD671 EQUIVALENT INPUT CIRCUIT



- ΔI OCCURS AT START OF CONVERSION
- V_{IN} MUST SETTLE TO WITHIN ½ LSB 200ns AFTER START OF CONVERSION

Figure 7.50

500kSPS DATA ACQUISITION SYSTEM

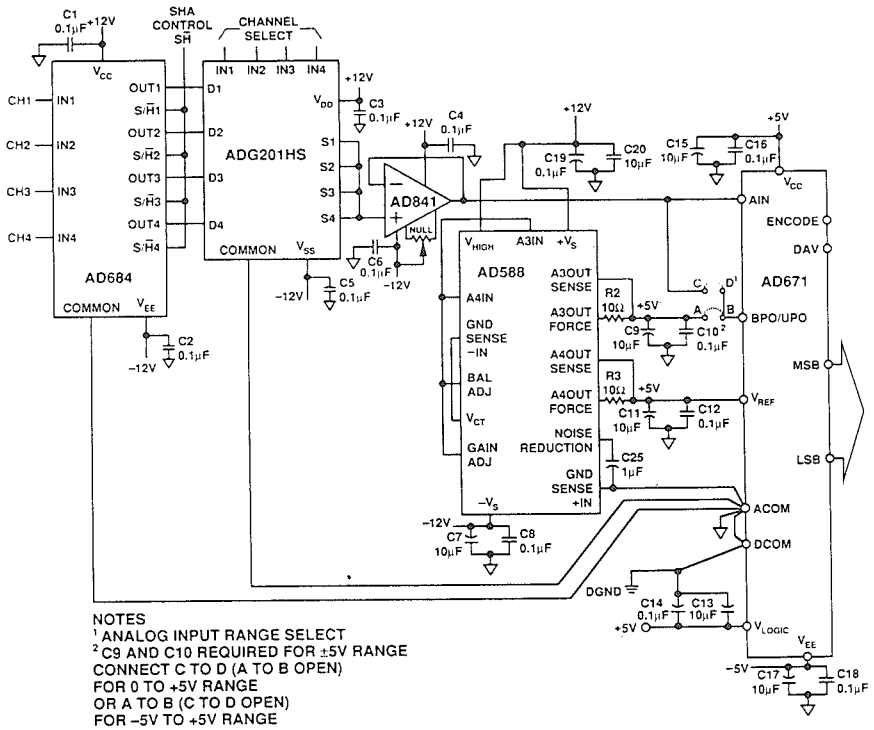


Figure 7.51

ured to sample four analog inputs simultaneously. Each held analog input voltage is then selected by the multiplexer and buffered by the AD841. The multiplexer can be switched between channels every 250ns, therefore the four analog inputs may be simultaneously sampled in a period of approximately 1μs. The minimum total sampling interval is therefore the sum of the SHA acquisition time (1μs) and the total conversion time for the four channels (1μs), or approximately 2μs. This corresponds to a simultaneous input sampling rate of approximately 500kHz.

DRIVING 12-BIT SAMPLING ADCs (AD1674, AD1671)

Before selecting the drive amplifier for a sampling ADC, the characteristics of the particular ADC under consideration must be examined. There are many different possible input architectures. Some produce more transient load current than others. AC performance specifications may differ considerably. For these reasons, it is somewhat difficult to generalize the amplifier selection process. There is, however, an underlying principle that the amplifier should not degrade either the DC or the AC specifications of the sampling ADC significantly.

The AD1674 is a complete 12 bit 100kSPS sampling ADC with user-transparent on-board SHA, reference, and clock. The device is pin-compatible with the industry standard AD574A and AD674A and is fully specified for ac parameters. It is ideal for use in both signal processing as well as traditional dc measurement applications. A block diagram of the AD1674 is shown in Figure 7.53, and key specifications are summarized in Figure 7.54.

7

SELECTING DRIVE AMP BASED ON SAMPLING ADC CHARACTERISTICS

- Analog Input Internal Buffering, Isolation, and Impedance
- Transient Load Currents Injected Into Analog Input
- AC Specifications: S/(N+D), Harmonic Distortion, THD
- Noise Within ADC Bandwidth
- DC Specifications

Figure 7.52

AD1674 12-BIT, 100kSPS SAMPLING ADC BLOCK DIAGRAM

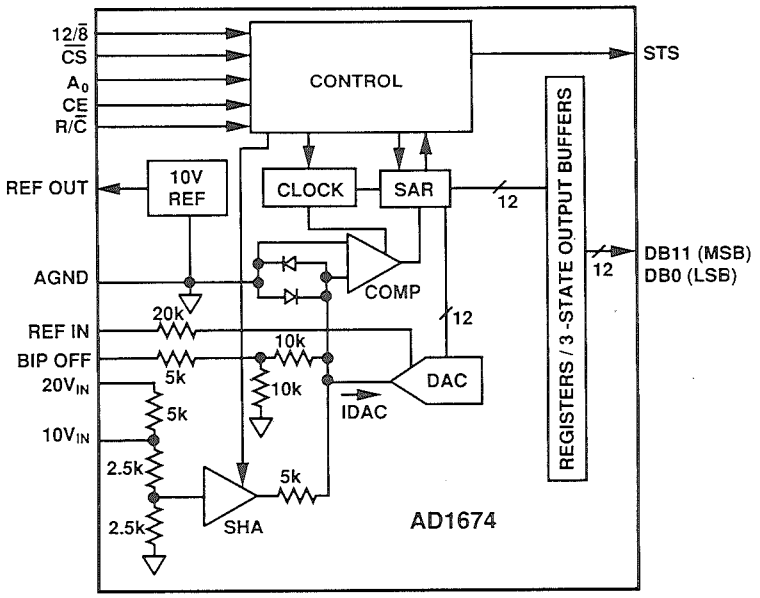


Figure 7.53

AD1674 SAMPLING ADC KEY SPECIFICATIONS

- 12 Bits, 100kSPS Sampling ADC
- Full Power Bandwidth: 1MHz
- 70dB S/(N+D), 90dB THD
- Industry-Standard AD574A Pinouts
- AC and DC Specified and Tested

Figure 7.54

AD1674 12-BIT, 100kSPS SAMPLING ADC DYNAMIC PERFORMANCE

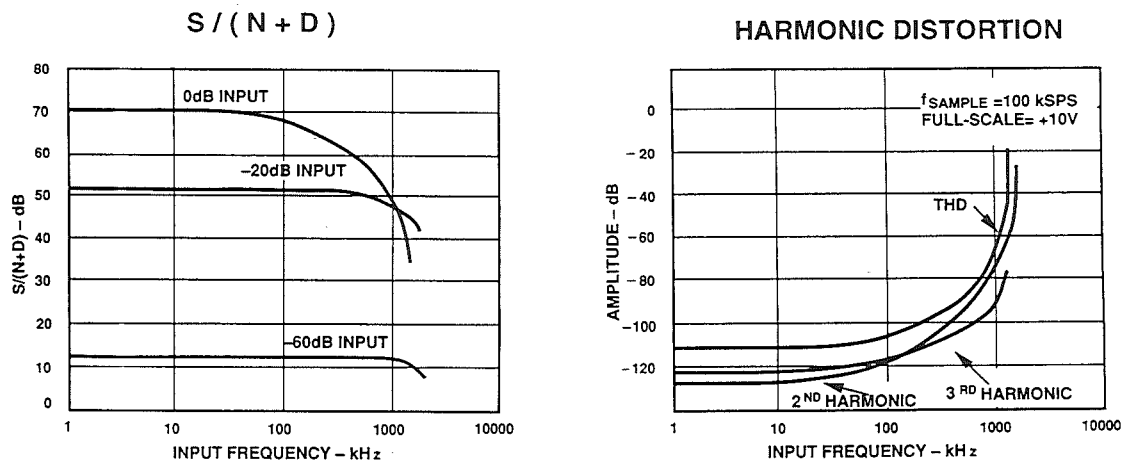


Figure 7.55

7

In selecting the appropriate drive amplifier for a sampling ADC such as the AD1674, it is important that the amplifier does not degrade either the AC or the DC specifications of the ADC significantly. Signal-to-Noise plus Distortion, S/(N+D), and harmonic distortion for the AD1674 are shown in Figure 7.55.

These curves can be used as a minimum criterion in establishing the AC performance of the drive op amp. Figure 7.56 shows the harmonic distortion of the AD845 amplifier which is a good choice (but certainly not the only choice!) for driving the AD1674. A simplified block diagram of the internal sample-and-hold circuit is shown in Figure 7.57. This circuit is typical of most SHAs used in sampling ADCs. Because of the high input impedance of the AD1674 internal SHA (5kΩ for 10V range, and 10kΩ for 20V range), SHA switching transients are well-buffered from the drive amplifier.

The AD1671 is a 12 bit 1.25MSPS sampling ADC which is basically an AD671 with an on-board SHA. The device is completely specified in terms of both AC and DC parameters. The AD1671 is fabricated on Analog Devices' ABCMOS process and uses high speed, low noise bipolar circuitry in the linear sections and low power CMOS for the logic sections. Laser trimmed thin film resistors are used to provide accuracy and temperature stability. A functional block diagram of the AD1671 is shown in Figure 7.58, and key specifications are summarized in Figure 7.59.

Because of its high impedance buffered input, the AD1671 presents only a minimal transient current load to the drive amplifier. The AD845 performance is compatible with the S/(N+D) and THD of the AD1671.

AD845 OP AMP HARMONIC DISTORTION
Vout = 3V rms, Rload = 500Ω

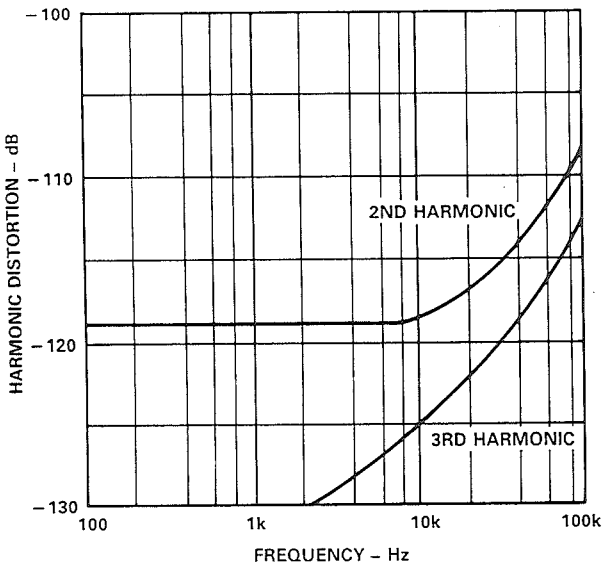


Figure 7.56

AD1674 SAMPLING ADC INPUT CIRCUIT

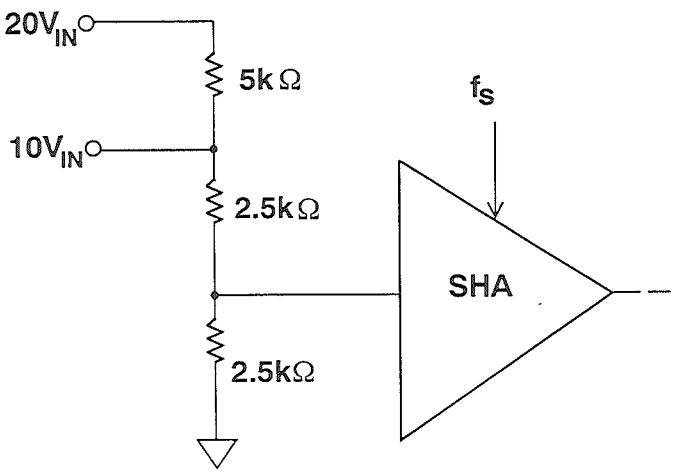


Figure 7.57

AD1671 12-BIT, 1 MSPS DIGITALLY CORRECTED SUBRANGING ADC

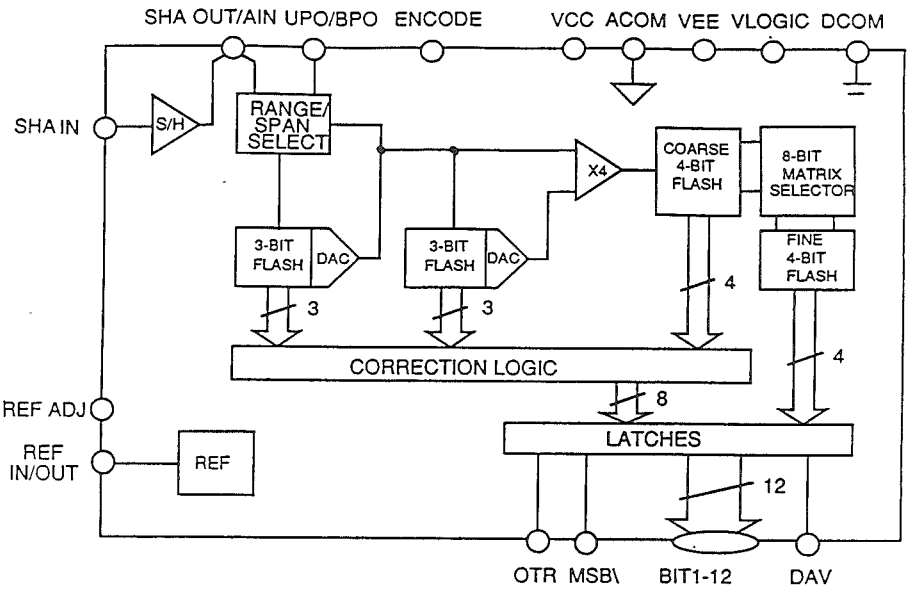


Figure 7.58

7

AD1671 SAMPLING ADC KEY SPECIFICATIONS

- 12 Bits, 1.25MSPS
- On-Chip SHA and Voltage Reference
- Full-Power Bandwidth: 2MHz
- 70dB S/(N+D), 80dB THD
- Input Impedance: 10kΩ||10pF, or 10MΩ||10pF
- Low Power Dissipation: 570mW

Figure 7.59

DRIVING A WIDE DYNAMIC RANGE 14 BIT, 10MSPS SAMPLING ADC (AD9014)

The AD9014 is a high performance 14 bit, 10MSPS ADC designed to provide extremely wide dynamic range for spectrum analysis and imaging applications. A simplified block diagram is shown in Figure 7.60, and key specifications are given in Figure 7.61. The AD9014 is a two-step subranging ADC with digital error correction. Its major system building blocks include a single to differential amplifier; SHA; 8 bit main range flash ADC; 16-bit linear, 8 bit DAC; clamped monolithic summation amplifier; 8 bit residue flash ADC; and digital adder logic. The AD9014 consists of two custom hybrids mounted on a small multilayer PCB.

The wide dynamic range of the AD9014 is shown in Figure 7.62, where the largest harmonic component versus input frequency is plotted. Selection of a compatible op amp to drive the AD9014 is critical to maintain this performance level. The AD9617 is a current feedback amplifier which satisfies this need, and its harmonic distortion is plotted in Figure 7.63. Key specifications are given in Figure 7.64.

AD9014 14-BIT, 10MSPS SAMPLING ADC BLOCK DIAGRAM

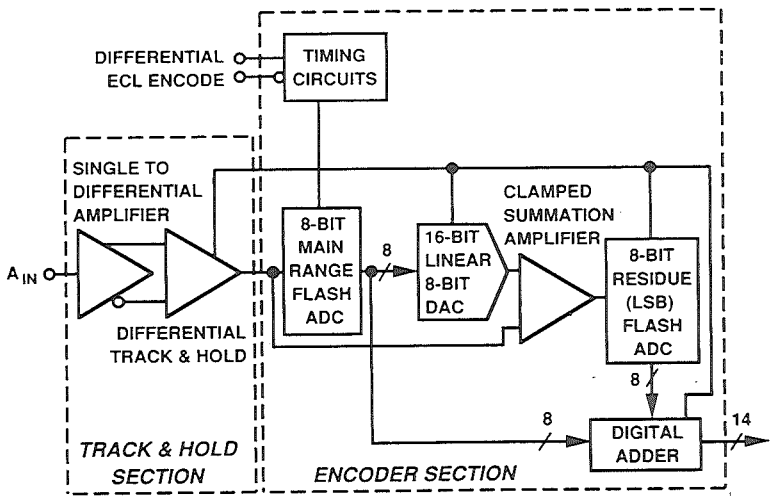


Figure 7.60

AD9014 SAMPLING ADC KEY SPECIFICATIONS

- 14 Bits, 10MSPS Sampling ADC
- 60MHz Full Power Bandwidth
- 92dB Spurious Free Dynamic Range @ 2.3MHz Input, 88dB @ 4.3MHz Input, 72dB @ 10MHz Input
- SNR: 75dB
- 2V p-p Input Range
- Input Impedance: 75Ω||7pF

Figure 7.61

AD9014 HARMONIC DISTORTION

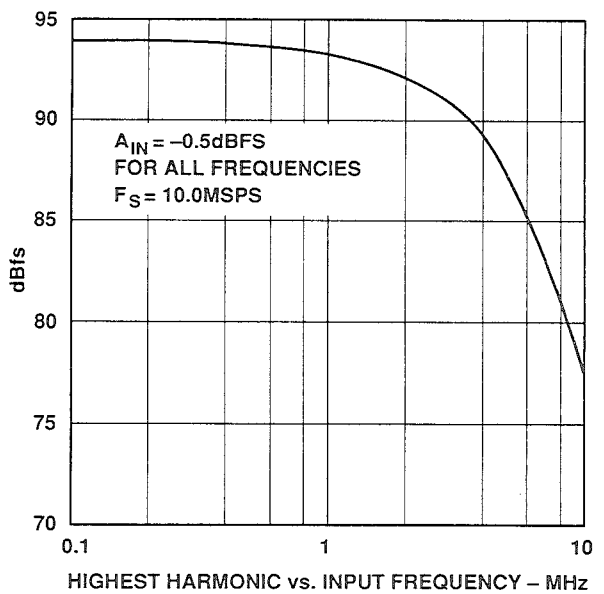


Figure 7.62

AD9617 CURRENT FEEDBACK OP AMP HARMONIC DISTORTION PERFORMANCE

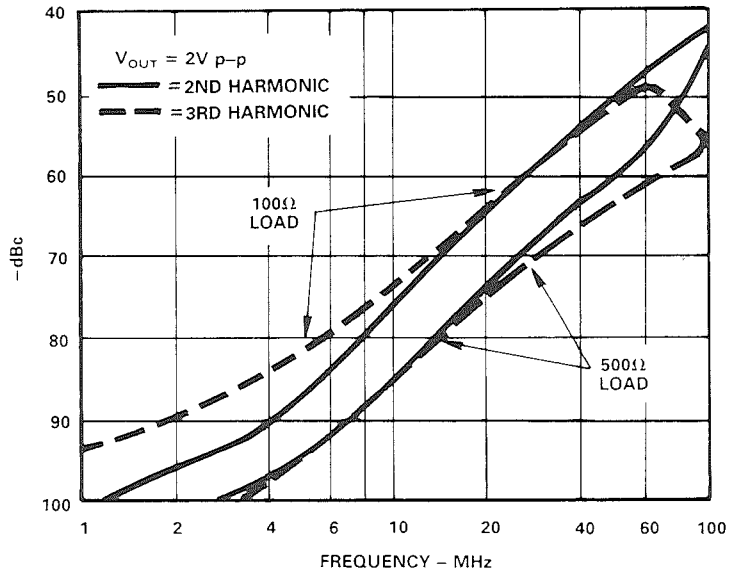


Figure 7.63

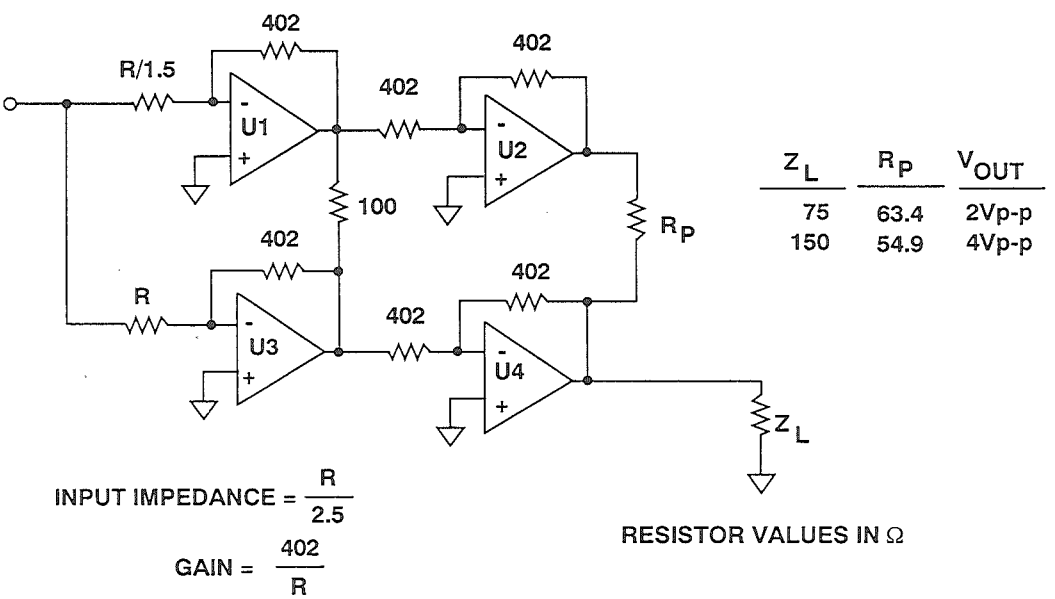
AD9617 CURRENT FEEDBACK AMPLIFIER KEY SPECIFICATIONS

- Usable Closed Loop Gain Range: ±1 to ±40
- Low Distortion: -67dBc @ 20MHz
- Small Signal BW: 190MHz (A_V = +3)
- Settling Time: 10ns to 0.1%, 14ns to 0.02%
- ±5V Power Supplies

Figure 7.64

When gain is required ahead of the AD9014, the circuit shown in Figure 7.65 is recommended in order to give ultra-low distortion levels. This configuration works well for analog input frequencies through 10MHz without introducing spurs that degrade the ADC's dynamic range. At 2.3MHz and 2V p-p output, all spurs generated in the drive circuit are less than -100dBc. The signal path is through U3 and U4, which are set up in a series inverting configuration to cancel even-order harmonics that are generated as the loop gain diminishes with frequency. U1 and U2 reduce the drive current of U3 and U4, respectively. Since U1 and U2 are set up in gains twice that of U3 and U4, the net effect is that the output stages of U3 and U4 are unloaded. This minimizes the odd-order harmonics generated in the output stages of U3 and U4. The gain of the overall block is +402Ω/R, and the input impedance is R/2.5. The output of the amplifier circuit is set up to drive either 2V p-p into 75Ω or 4V p-p into 150Ω by properly selecting R_p.

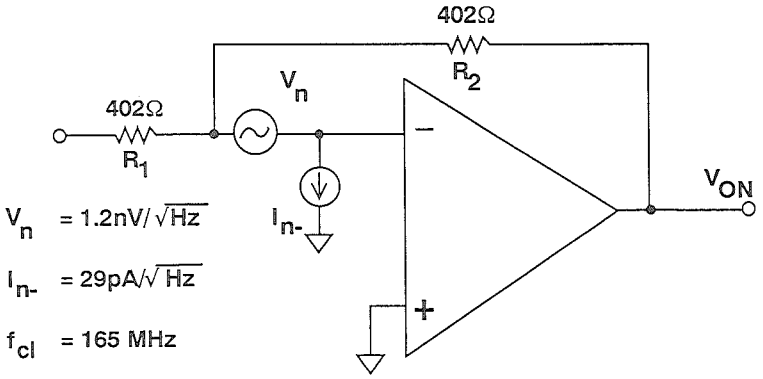
LOW DISTORTION DRIVE CIRCUIT (>100dBc) FOR AD9014 USING AD9617 OP AMPS



Z_L	R_P	V_{OUT}
75	63.4	2Vp-p
150	54.9	4Vp-p

Figure 7.65

AD9617 OUTPUT NOISE SPECTRAL DENSITY



$V_n = 1.2nV/\sqrt{Hz}$

$I_{n-} = 29pA/\sqrt{Hz}$

$f_{cl} = 165\ MHz$

$$V_{ON} = \sqrt{BW}\sqrt{V_n^2\left[1+\frac{R_2}{R_1}\right]^2 I_{n-}^2 R_2^2}$$

$$V_{ON} = \sqrt{BW}\sqrt{(1.2\times10^{-9})^2(2)^2 + (29\times10^{-12})^2(402)^2}$$

$$V_{ON} = \sqrt{BW}\sqrt{5.76\times10^{-18} + 136\times10^{-18}}$$

$$V_{ON} = \sqrt{BW}\ (11.9nV/\sqrt{Hz})$$

Figure 7.66

REDUCING DRIVER NOISE USING ANTIALIASING FILTER

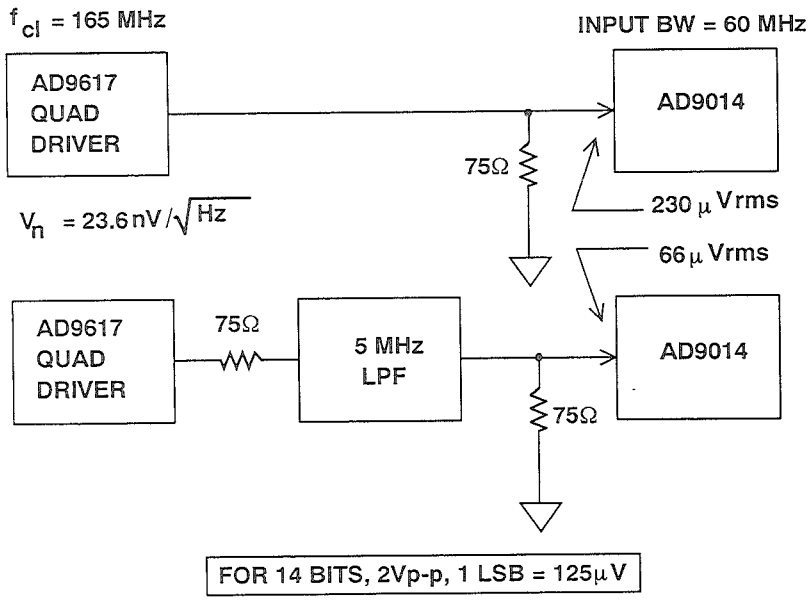


Figure 7.67

The output voltage noise spectral density calculations for a single AD9617 op amp are shown in Figure 7.66. Notice that the inverting input current noise dominates. The equivalent noise bandwidth for integration is the input bandwidth of the AD9014 (60MHz) multiplied by 1.57, or approximately 100MHz. The output voltage noise of the AD9617 integrated over this bandwidth is 119μV rms. The SNR of the AD9617 for a 2V p-p output is therefore 75.5dB, compared to the SNR of the AD9014 of 75dB. The approximate output rms noise of the four op amp drive circuit shown in Figure 7.67 is 230μV rms over the 100MHz equivalent noise bandwidth. This reduces the total SNR to approximately 69dB.

The noise contribution of the op amp drive circuit can be significantly reduced by placing a 75Ω antialiasing filter between the quad driver and the AD9014 as shown in the lower half of Figure 7.67. The gain of the driver circuit must be increased by a factor of two to account for the total attenuation of the filter series and load terminations. If the antialiasing filter is single-pole, and the cutoff frequency is 5MHz, then the output noise of the AD9617 quad driver circuit is reduced by an amount equal to $\sqrt{60/5}$, or 3.46. The rms output noise of the filter is now only 66μV, corresponding to an SNR of 80.6dB. This example dramatically illustrates the noise reduction advantages of placing the antialiasing filter as close to the ADC as possible.

DRIVING HIGH SPEED FLASH CONVERTERS

Driving high speed flash converters presents another set of unique challenges. Most flash converters are designed on bipolar digital processes which makes the addition of low-distortion on-chip buffers difficult. In addition, most flash converters have a fairly large input capacitances which may also be signal-dependent (non linear). The input capacitance is primarily due to the large number of comparators.

A block diagram of the AD9028/AD9038 8-bit, 300MSPS flash converter is shown in Figure 7.69. Notice that the analog input is applied to each of 256 comparators. In reality, the input stage of each comparator is a differential pair. The analog input is applied to one base, and the reference ladder voltage to the other base. The input circuit of the flash converter can be modelled as shown in Figure 7.70. The signal-dependent capacitance is modelled as a reverse-biased diode. The total input capacitance as a function of signal level is also shown in Figure 7.70.

Wideband, low-distortion current feedback amplifiers such as the AD9617 are ideal for driving this type of flash converter. However, a series resistor of approximately 50Ω is required to isolate the amplifier from the flash input capacitance in order to prevent peaking and to maintain stability. Because of the series resistor and the signal-dependent capacitance, harmonic distortion will result as shown in Figure 7.71. The series isolation resistor should therefore be as low as possible in order to maintain op amp stability. Large resistor values will increase the distortion and limit the input bandwidth. Applications information provided on both the amplifier and the flash converter data sheet should be of assistance in selecting the proper resistor value.

DRIVING FLASH CONVERTERS

- Process Limitations Prevent On-Chip Buffering
- Large Input Capacitance May Be Signal-Dependent
- Wideband, Low Distortion Amplifiers May Be Unstable With Large Capacitive Loads
- Sampling Clock Noise Coupling to Input

Figure 7.68

AD9028/AD9038 8-BIT, 300MSPS FLASH CONVERTER BLOCK DIAGRAM

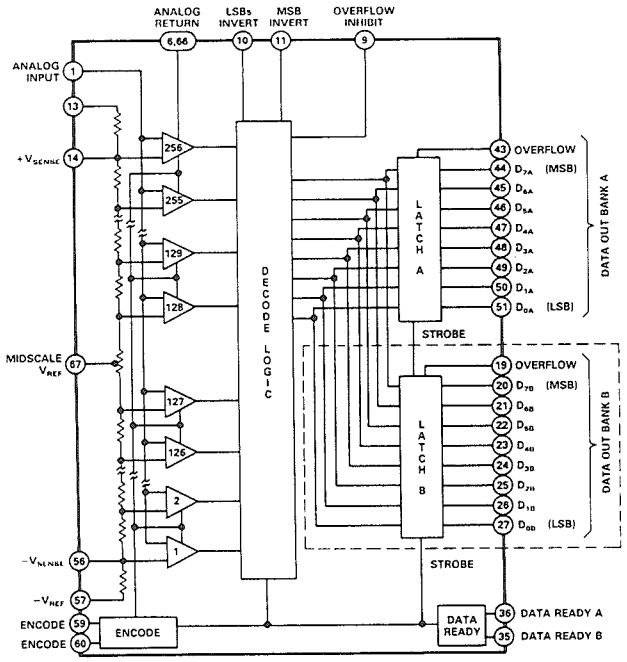


Figure 7.69

AD9028/AD9038 EQUIVALENT INPUT CIRCUIT AND SIGNAL-DEPENDENT CAPACITANCE

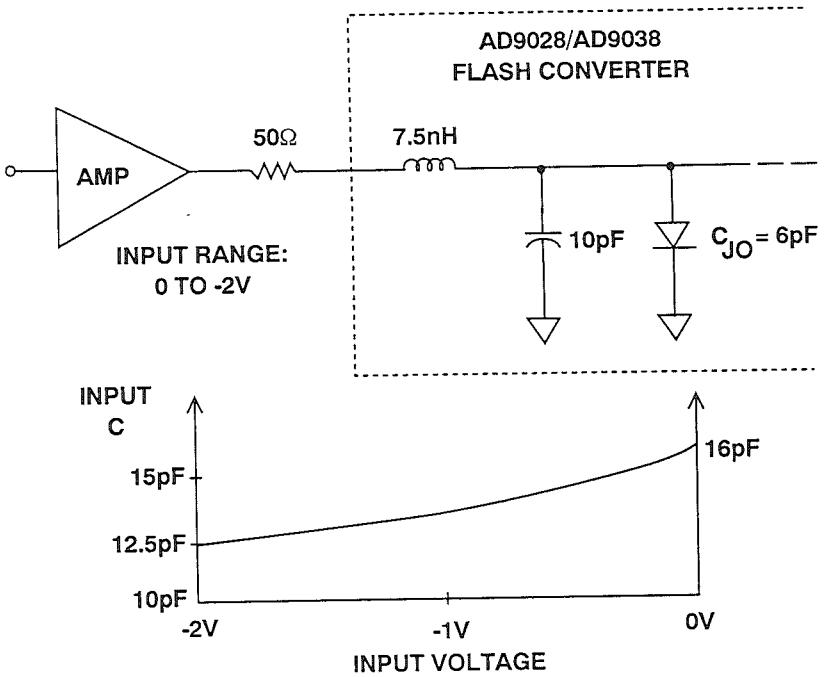


Figure 7.70

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SIMULATED THD DUE TO SIGNAL-DEPENDENT INPUT CAPACITANCE

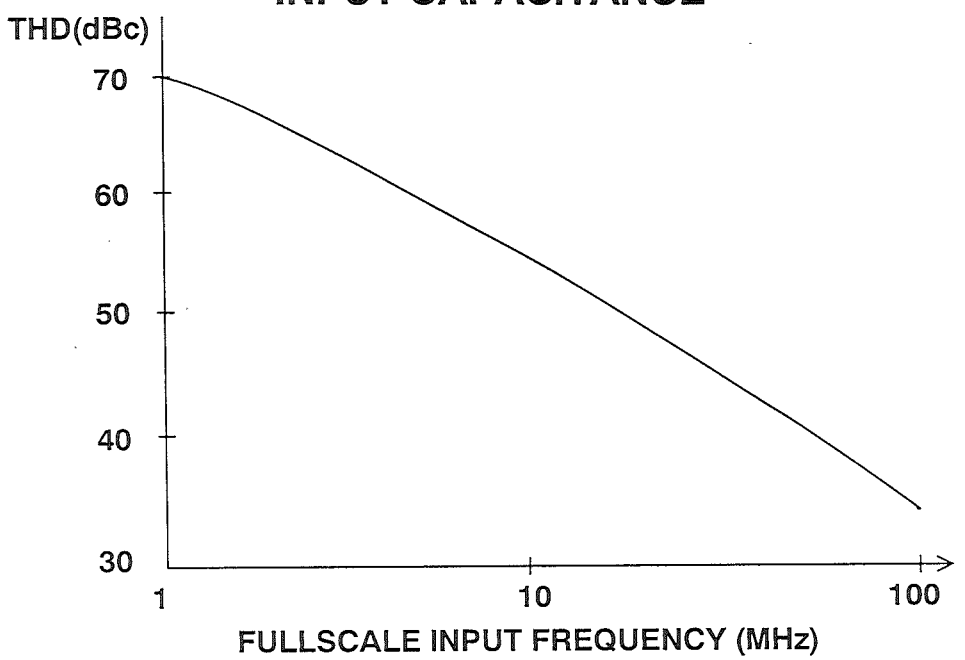
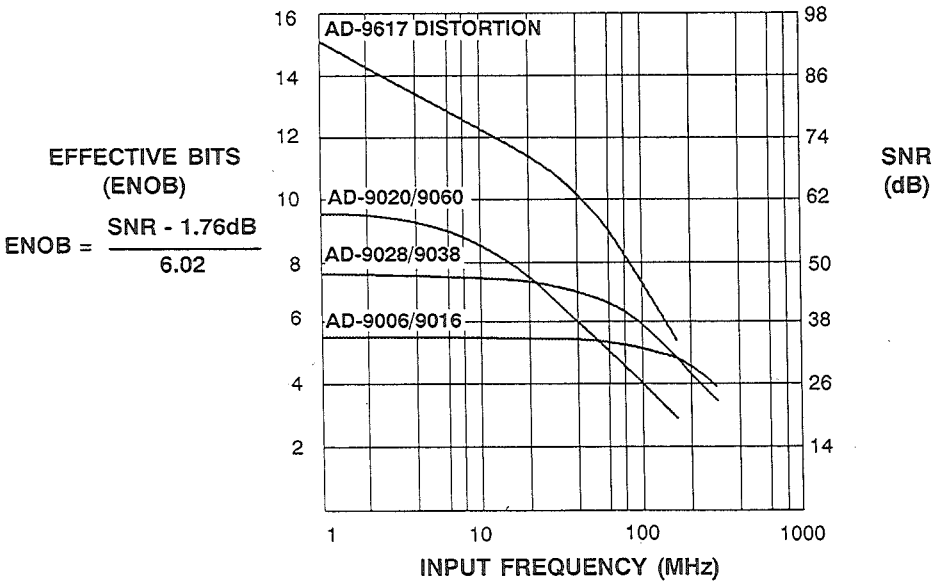


Figure 7.71

FLASH ADC AND OP AMP DYNAMIC PERFORMANCE



FLASH ADC	RESOLUTION	SAMPLING RATE
AD9020	10 BITS	40 MSPS
AD9060	10 BITS	60 MSPS
AD9028/9038	8 BITS	250 MSPS
AD9006/9016	6 BITS	400 MSPS

Figure 7.72

Figure 7.72 shows the SNR and ENOB performance of several flash converters including the AD9028/AD9038. Also shown on the figure is the harmonic distortion performance of the AD9617 current feedback amplifier. Note that the amplifier performance is better than that of the ADCs over a wide range of input frequencies.

DRIVING PRECISION 16 BIT SAMPLING ADCS (AD676)

The AD676 is a precision 16 bit, 100kSPS ADC which utilizes a switched-capacitor charge redistribution architecture. Overall performance is optimized by digitally correcting internal nonlinearities through on-chip autocalibration, thereby eliminating the need for laser trimming. A block diagram of the AD676 is shown in Figure 7.73, and key specifications are summarized in Figure 7.74.

The AD676 employs a successive approximation technique to determine the value of the analog input voltage. However, instead of the traditional laser trimmed resistor ladder approach, this device uses a capacitor array, charge redistribution technique. Binary-weighted capacitors subdivide the input sample to perform the actual analog to digital conversion. The capacitor array eliminates variation in the linearity of the device due to temperature-induced mismatches of resistor values. Since a capacitor array is used to perform the data conversions, the SHA function is included without the need for additional circuitry.

Initial errors in capacitor matching are eliminated by an autocalibration circuit. This circuit employs an on-chip microcontroller and a calibration DAC to measure and compensate capacitor mismatch errors. As each error is deter-

AD676 16-BIT, 100kSPS SAMPLING ADC BLOCK DIAGRAM

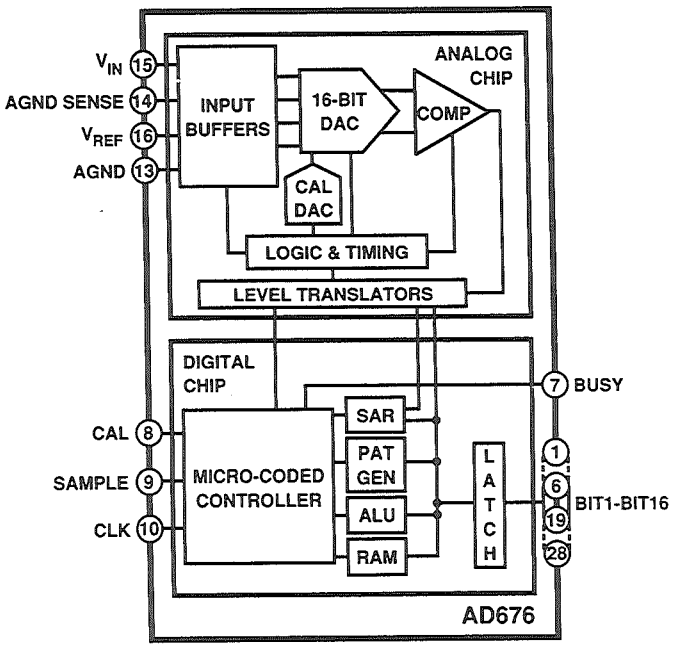


Figure 7.73

7

AD676 ADC KEY SPECIFICATIONS

- 16 Bits, 100kSPS Sampling SAR ADC
- Switched-Capacitor, Charge-Redistribution Architecture
- On-Chip Autocalibration Circuits
- AC and DC Specifications
- ±1 LSB INL
- 90dB S/(N+D)
- 1MHz Full Power Bandwidth
- 95dBc THD

Figure 7.74

mined, its value is stored in on-chip RAM. Subsequent conversions use these RAM values to improve conversion accuracy. The autocalibration routine may be invoked at any time. Autocalibration insures high performance while eliminating the need for any user adjustments.

Designing with high resolution converters requires careful attention to board layout. Trace impedance is a significant issue. A 1.22mA current through a 0.5Ω trace will develop a voltage drop of 0.6mV, which is 4 LSBs at the 16-bit level for a 10V fullscale span.

The AD676 provides an Analog Ground Sense (AGND SENSE) pin that can be used to compensate for small voltage drops (<100mV) in the analog input signal return line as shown in Figure 7.75. The AGND SENSE pin is used to remotely sense the ground potential of the signal source, and is especially useful if the signal has to be carried some distance to the ADC. Figure 7.76 shows how the signal wires should be shielded in a noisy environment to avoid capacitive coupling. The AGND and DGND of the AD676 should be both tied together at the device and connected to the PCB Analog Ground Plane.

The AD676 is designed to provide superior S/(N+D) performance as shown in the curves in Figure 7.77.

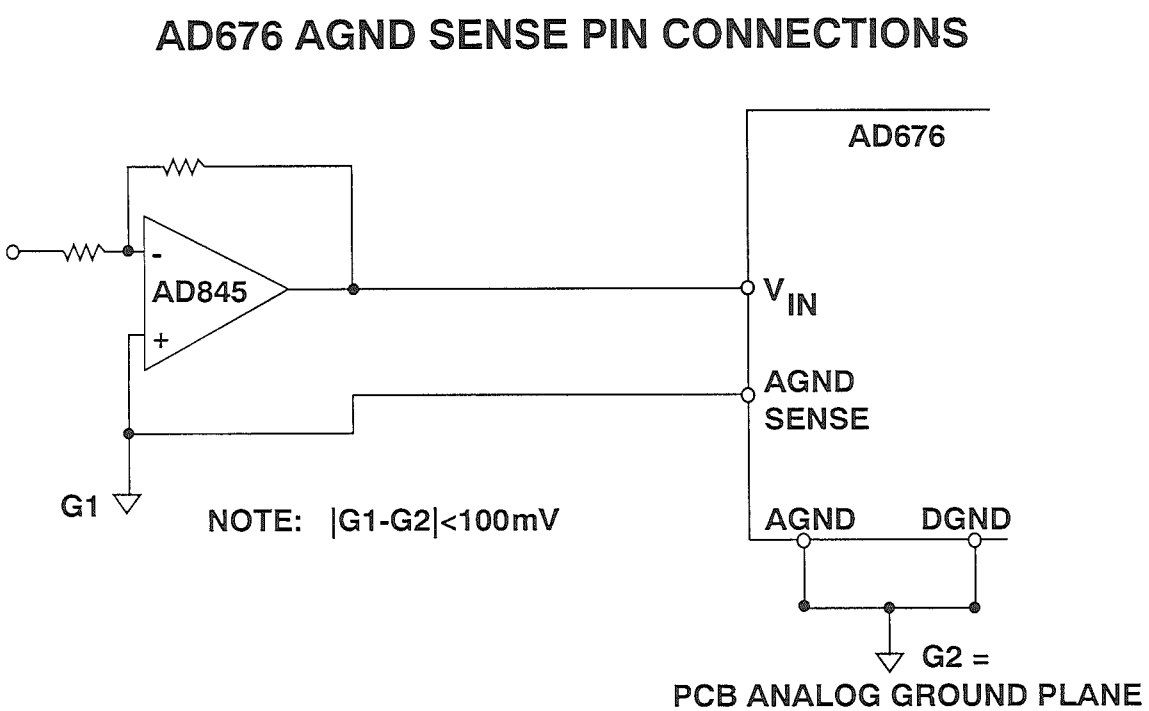


Figure 7.75

AD676 AGND SENSE PIN CONNECTIONS FOR SHIELDED TWISTED PAIR CABLE

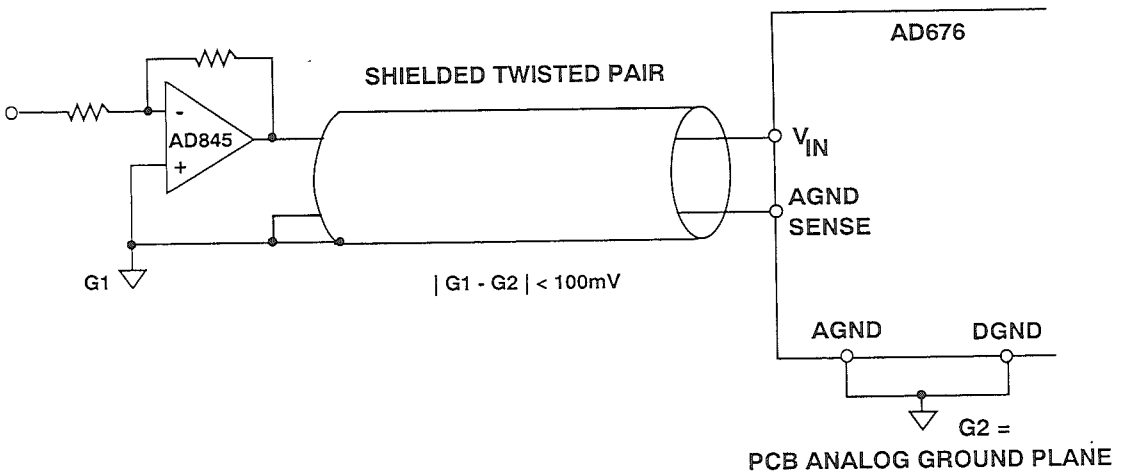


Figure 7.76

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AD676 16-BIT, 100kSPS SAMPLING ADC S/N + D AND EFFECTIVE BIT PERFORMANCE

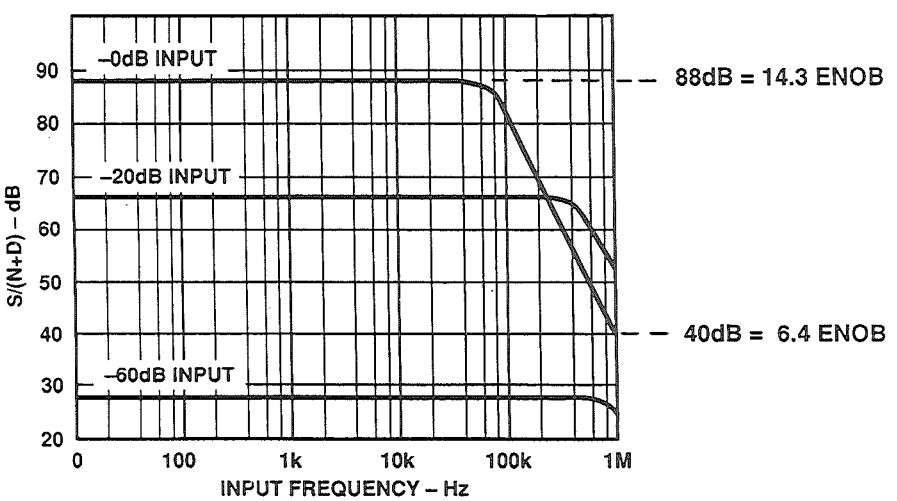


Figure 7.77

AD676 EQUIVALENT INPUT CIRCUIT

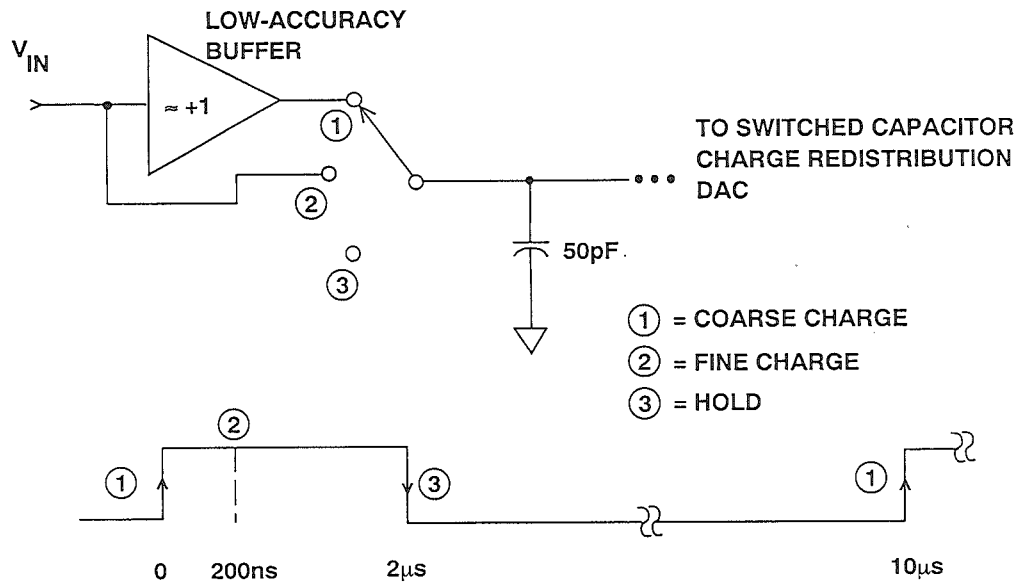


Figure 7.78

A simplified schematic of the input circuit of the AD676 is shown in Figure 7.78. All of the inputs (V_{in}, V_{ref}, and AGND SENSE) produce transient load currents which must be absorbed by their respective drivers. When a conversion cycle begins, each analog input is connected to an internal, discharged 50pF capacitor which then charges to the voltage present at the corresponding pin. The capacitor is disconnected when the SAMPLE line is taken LOW, and the stored charge is used in the subsequent conversion. In order to limit the demands placed on the external source by this high initial charging current, an internal low-accuracy buffer amplifier is connected between the input and this capacitance for a few hundred nanoseconds. During this time the input pin exhibits typically 20kΩ| |10pF and ±40mA bias current. Next, the input is switched directly to the now precharged capacitor and allowed to fully settle. During this time, the input sees only a 50pF capacitor. Once the sample is taken, the input is internally floated so that the external input source sees a very high input resistance and a parasitic input capacitance of only 2pF. As a result, the only dominant input characteristic which must be considered is are the high current steps which occur when the internal buffers are switched in an out.

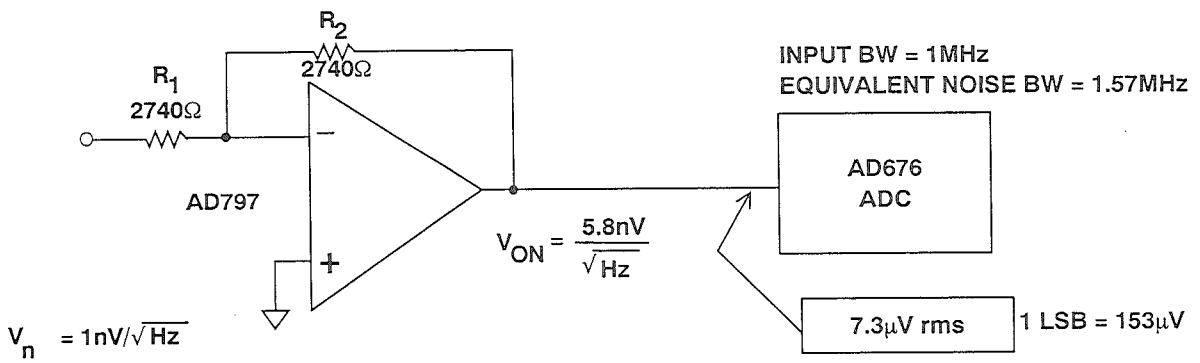
The drive amplifier for the AD676 must have fast settling time, low distortion and 16-bit dc accuracy. The AD797 low distortion bipolar op amp is an excellent choice for this application. Key specifications are summarized in Figure 7.79.

AD797 PRECISION LOW DISTORTION BIPOLAR OP AMP KEY SPECIFICATIONS

- 0.1mV Input Offset Voltage
- 0.2μV/°C Offset Voltage Drift
- 100nA Input Offset Current
- 1,000,000 dc Open Loop Gain
- 100MHz Gain Bandwidth Product
- 110dB THD @ 20kHz, 3Vrms into 600Ω
- 0.9nV/$\sqrt{Hz}$, 2pA/$\sqrt{Hz}$ Input Noise at 1kHz

Figure 7.79

AD797 DRIVING AD676 16 BIT, 100kSPS ADC



$$V_{ON} = \sqrt{BW}\sqrt{V_n^2\left[1+\frac{R_2}{R_1}\right]^2 I_{n-}^2 R_2^2}$$

$$V_{ON} = \sqrt{BW}\sqrt{(1\times10^{-9})^2(2)^2 + (2\times10^{-12})^2(2740)^2}$$

$$V_{ON} = \sqrt{BW}\sqrt{4\times10^{-18} + 30\times10^{-18}}$$

$$V_{ON} = \sqrt{BW}\,(5.8nV/\sqrt{Hz}) = \sqrt{1.57\times10^6}(5.8nV/\sqrt{Hz}) = 7.3\mu V\ rms$$

Figure 7.80

Figure 7.80 shows the calculations for the total output noise of the AD797 over the 1MHz input bandwidth of the AD676. The total noise is computed to be only 7μV rms compared to the theoretical 16-bit quantization noise (10V fullscale range) of 44μV rms.

For less demanding applications, the AD845 may be used as a drive amplifier for the AD676 yielding a total output noise of 63μV rms.

DRIVING SIGMA-DELTA AUDIO ADCs (AD1879)

The AD1879 is a state-of-the-art dual 18 bit sigma-delta ADC designed to meet the stringent requirements of professional digital audio. A block diagram of the device is shown in Figure 7.81, and performance specifications are summarized in Figure 7.82. The input sigma-delta modulator is a fifth-order differential switched capacitor design which performs the quantization noise shaping function. The oversampling ratio is 64x, which places the oversampling frequency at 3.072MHz for the standard audio sampling rate of 48kSPS. Because of the high oversampling ratio, a single-pole analog antialiasing filter is sufficient at the input of the ADC.

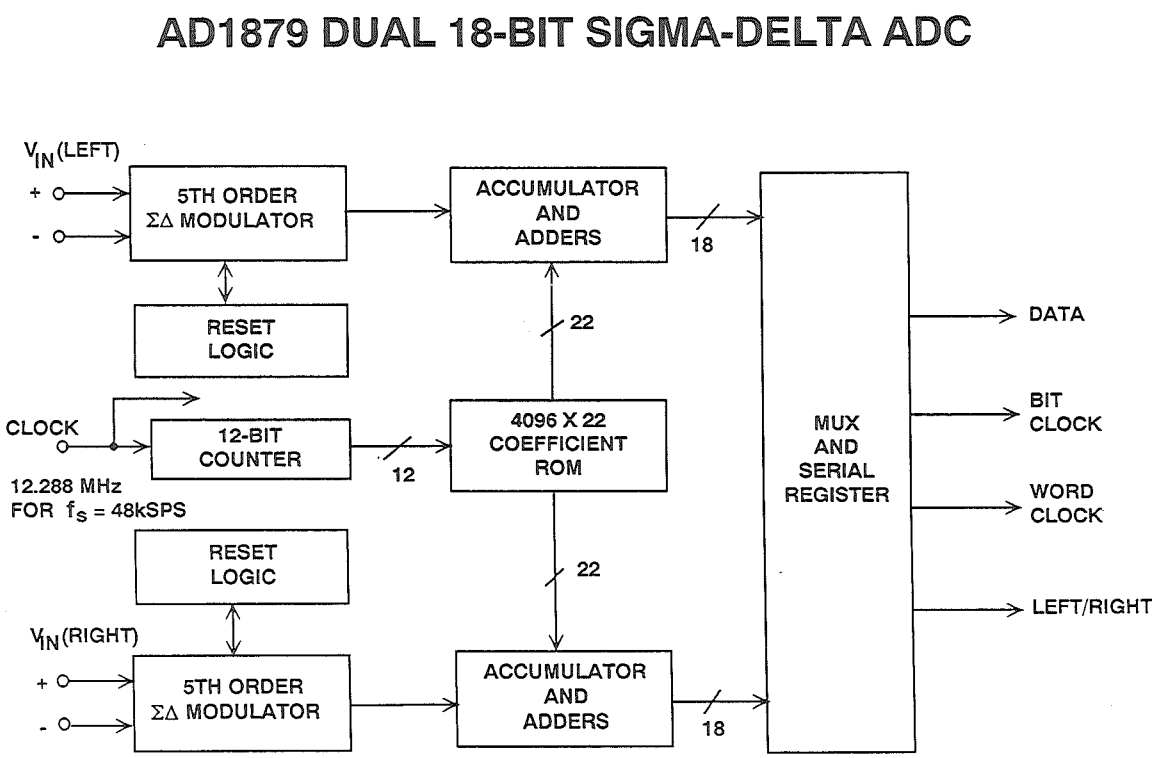


Figure 7.81

AD1879 18 BIT SIGMA-DELTA ADC KEY SPECIFICATIONS

- Two 18 Bit Channels for Stereo Digital Audio
- Interchannel Crosstalk: -110dB @ 1kHz
- SNR: 103dB
- THD: 98dB
- Oversampling Ratio: 64x
- Output Word Rate: 55kHz Maximum
- Linear Phase Digital Filter: 4095 Taps, 0.0004dB Passband Ripple, 115dB Stopband Attenuation
- Power: 600mW
- Package: 28 Pin, 600-mil Plastic

Figure 7.82

A switched capacitor input circuit presents a special set of problems for the drive amplifier because of signal-dependent transient input currents. In order to understand the phenomenon better, Figure 7.83 shows the basic circuit for a single-ended switched capacitor integrator. The capacitor is switched at the oversampling rate, f_S, and acts as a resistor having a resistance equal to $1/Cf_S$.

The integrator time constant is therefore determined by capacitance *ratios* which can be accurately controlled in a CMOS process. The switched capacitor is implemented in CMOS using the T-switch circuit shown in Figure 7.84. Because the input signal to the switch modulates the FET bias voltages, the charge injected into the drive amplifier is signal dependent.

SINGLE-ENDED SWITCHED CAPACITOR INTEGRATOR

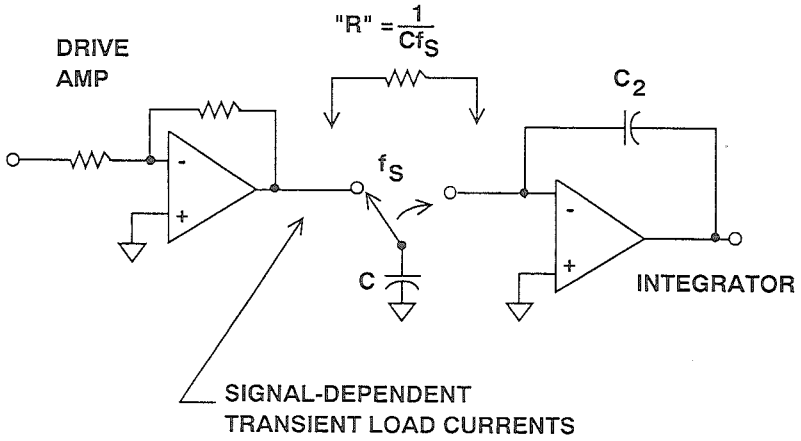


Figure 7.83

CMOS IMPLEMENTATION OF SWITCHED CAPACITOR

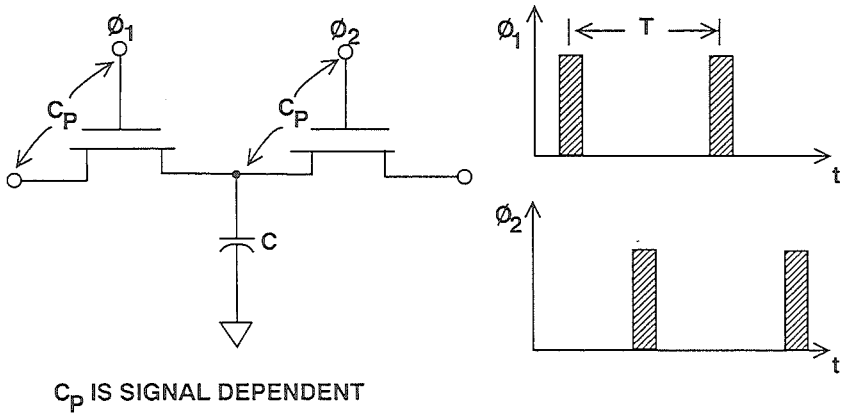


Figure 7.84

DIFFERENTIAL DRIVER (ONE CHANNEL) FOR AD1879 SIGMA-DELTA AUDIO ADC

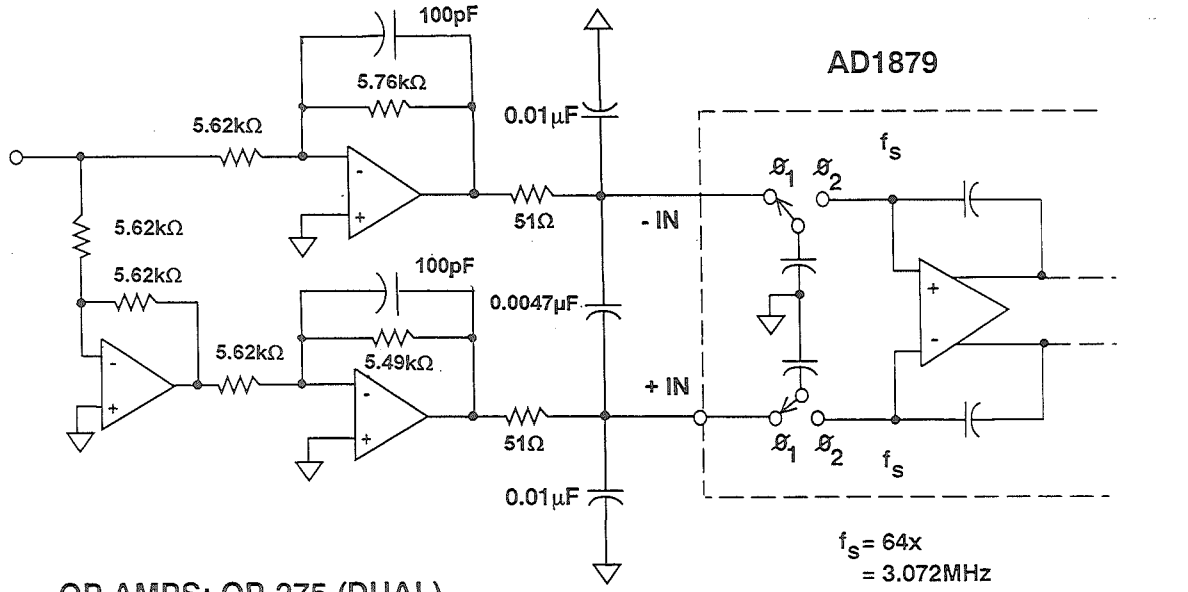


Figure 7.85

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The sigma-delta modulator in the AD1879 is fully differential and has the equivalent input circuit shown in Figure 7.85 (only one input channel shown). For optimum common mode rejection of transient load currents, the input should be driven differentially. The differentially connected 0.0047µF capacitor supplies most of the differential-mode transient currents, while the 0.01µF capacitors connected to ground absorb spike currents which are common mode. The 51Ω series resistors isolate the remaining transient current from the drive amplifiers as well as isolate the capacitive loads from the op amp outputs. These resistors must be small, however, in order to avoid distortion because of the signal-dependent transients caused by charge injection. The OP-275 (dual) op amp is recommended as precision low-distortion drive amplifier for demanding professional audio applications.

ADC INPUT CLAMPING AND PROTECTION CIRCUITS

Most ADCs will tolerate moderate out-of-range signals in the order of 50% or so without damage to the input circuit. The exception to this are certain flash converters which have unipolar negative input ranges. This will be discussed shortly.

For example, an ADC with an input range of ±5V should tolerate an input signal up to ±7.5V. It is usually true, however, that the overvoltage recovery time of an ADC (shown in Figure 7.86) increases as the input signal moves further out of range.

It may be desirable, therefore, to clamp the ADC input so that the input signal is limited to small overrange values. This is especially true if large out-of-range signals are frequently expected. Clamping therefore not only protects the internal ADC input circuits from damage, but also reduces the overvoltage recovery time.

Because the clamping circuit is in the signal path (between the drive amplifier and the ADC), care must be taken to insure that the clamp circuit does not degrade the system performance for normal in-range signals.

The circuit shown in Figure 7.87 utilizes low capacitance (1.2pF), low leakage (100nA @ 15V reverse bias) Schottky diodes (1N5712) to clamp the ADC input to adjustable levels. The series resistor must be chosen so that the drive amplifier output current is limited to acceptable values for overrange signals. A single Schottky diode is capable of withstanding up to 50mA of forward current for short periods of time. If additional current-handling capability is required, two diodes may be paralleled at the expense of additional capacitance and reverse leakage current.

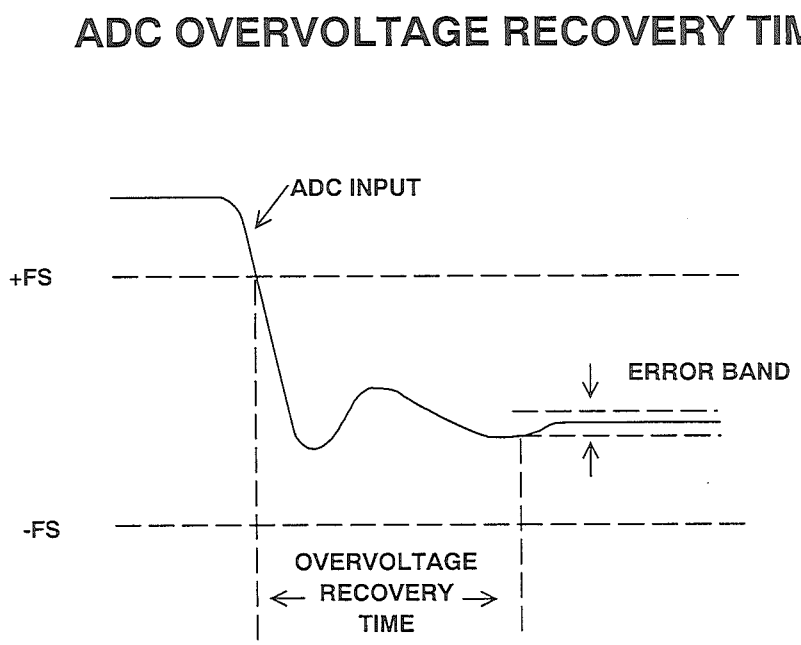

Figure 7.86

ADJUSTABLE POSITIVE AND NEGATIVE CLAMP CIRCUIT

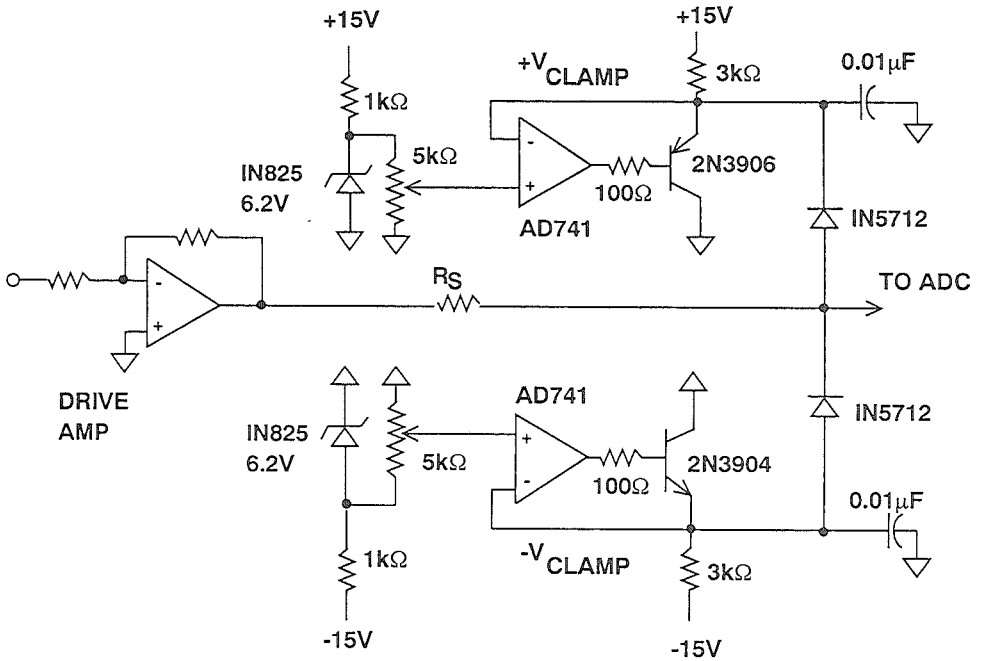

Figure 7.87

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PROTECTION AGAINST LATCH-UP AND DAMAGE DUE TO SUPPLY SEQUENCING

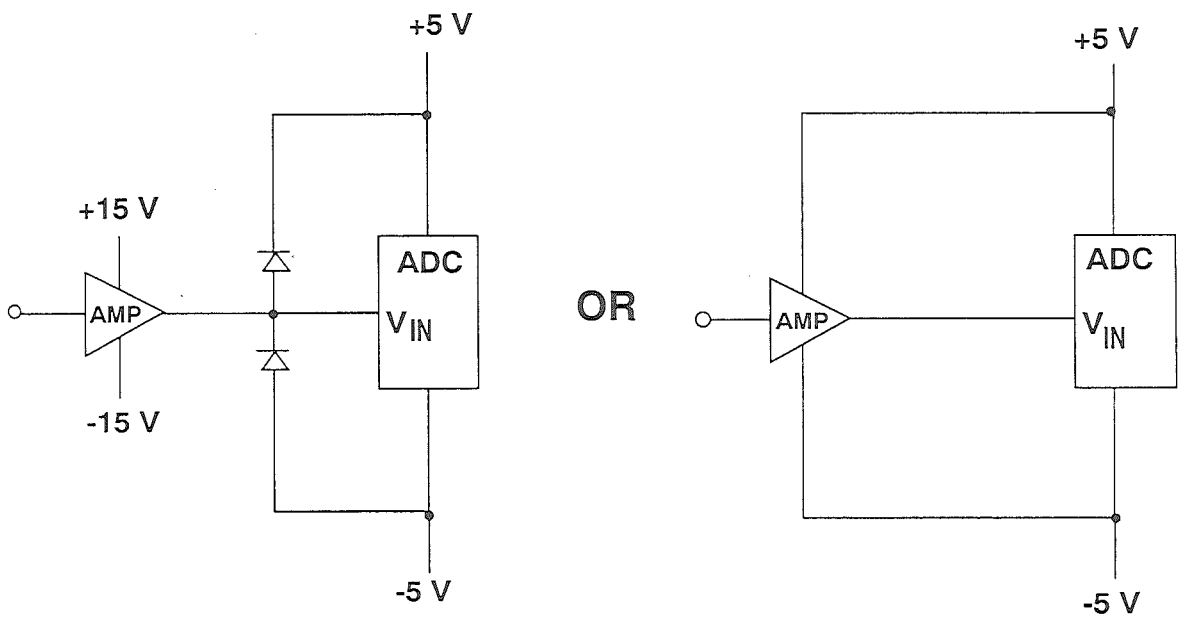

Figure 7.88

Other conditions of temporary overvoltage may occur because of power supply sequencing. Several possibilities will be discussed briefly.

Figure 7.88 shows an op amp powered by ±15V supplies driving an ADC which is powered by ±5V supplies (typical of many CMOS ADCs). If the op amp supplies are brought up before the ADC supplies, an overvoltage condition on the ADC input may cause latch up and destroy the device. In addition, the analog input voltage to a CMOS ADC should never exceed the supply voltages, or a latch-up condition may occur. The diodes shown in the figure will protect against this condition. In fact, many CMOS ADCs have the protection diodes on-chip.

An alternative is also shown in Figure 7.88. If a ±5V supply op amp is chosen, then both the ADC and the op amp may be powered from the same supplies, thereby eliminating the potential latch-up problem. It should be noted that many op amps have specifications for both ±15V and ±5V supply operation. If a ±15V op amp must be used, the ±5V for the CMOS ADC may be derived from a three-terminal voltage regulator as shown in Figure 7.89. This is relatively efficient because most CMOS ADCs are low power devices. This scheme also has the advantage of isolating the ADC from the noise on the ±5V supplies in a system which is used to power digital circuitry.

Many flash converters are designed to operate on a single -5.2V power supply and have a negative input voltage range of 0 to -2V. If the input goes positive, the substrate silicon diode begins to conduct. Any amount of forward current above a few mA may permanently degrade the performance of the flash converter. Input Schotkky diodes should be installed as shown in Figure 7.90 to prevent this condition. Most amplifiers suitable for driving flash converters (such as the AD9617) operate on dual 5V supplies and can deliver 50 to 100mA of output current. The series resistor should be chosen to limit this current to an acceptable level. Two diodes should be paralleled if more than 50mA current is expected from the drive amplifier.

USING 3-TERMINAL REGULATORS AS ADC SUPPLIES

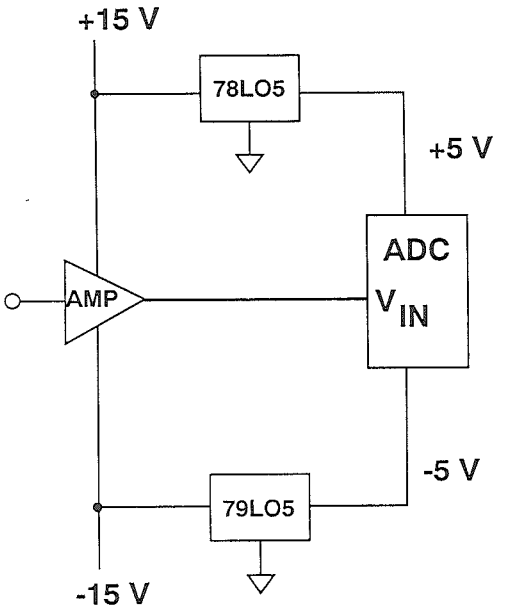

Figure 7.89

PROTECTING FLASH CONVERTER INPUTS WITH SCHOTTKY DIODES

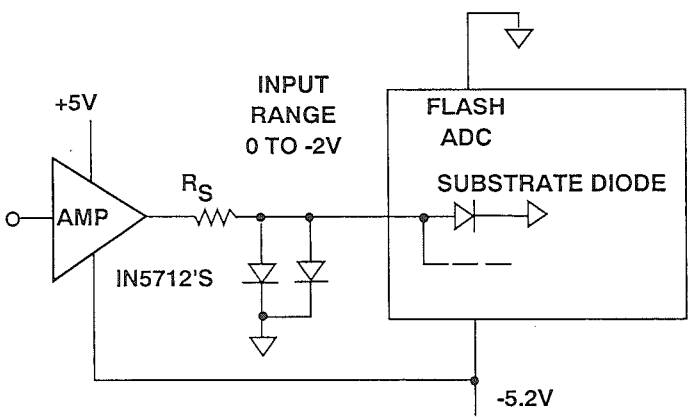

Figure 7.90

REFERENCES

1. Thomas M. Fredrickson, **Intuitive Operational Amplifiers**, McGraw-Hill, 1988.

2. Paul R. Gray and Robert G. Meyer, **Analysis and Design of Analog Integrated Circuits, Second Edition**, John Wiley, 1984.

3. Walter G. Jung, **IC Op-Amp Cookbook, Third Edition**, SAMS (Division of Macmillan, Inc.), 1986

4. J. K. Roberge, **Operational Amplifiers-Theory and Practice**, John Wiley, 1975.

5. Ralph Morrison, **Grounding and Shielding Techniques in Instrumentation, Third Edition**, John Wiley, Inc., 1986.

6. Henry W. Ott, **Noise Reduction Techniques in Electronic Systems, Second Edition**, John Wiley, Inc., 1988.

7. Analog Devices, **High Speed Design Seminar, 1990.**

8. Analog Devices, **Mixed Signal Design Seminar, 1991.**

9. Joe Buxton, *Careful Design Tames High-Speed Op Amps*, **Electronic Design**, April 11, 1991, pp. 81-97.