SECTION IV

SINGLE SUPPLY, LOW POWER APPLICATIONS

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■ Single Supply Design Considerations:
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SECTION IV

SINGLE SUPPLY, LOW POWER APPLICATIONS

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SINGLE SUPPLY DESIGN CONSIDERATIONS

Single supply operation is becoming an increasingly important requirement as systems get smaller, cheaper, and more portable. Portable systems rely on a battery as the primary power source. Consequently power consumption and therefore operating time per battery charge are high on the designers' priority list. This makes low voltage operation and low power consumption critical.

However, most op amps are designed to operate with ±15V supplies. Trying to make them work at low voltages may require special attention because few are specified to operate at lower voltages.

Many will not even function at 5V or less. Thus the choice of devices narrows rapidly as the supply voltage is reduced.

The +12V supply is popular because of the ubiquitous automobile battery and its wide range of size and capacity. Even more popular is the +5V supply voltage that powers virtually all TTL or CMOS logic based systems. There are also special applications that run on one or two 1.5V cells. The lower the supply voltage, the more difficult the circuit design task becomes: the signal range gets compressed, and fewer components are able to operate.

SINGLE SUPPLY DESIGN CONSIDERATIONS

■ Low Signal Swing Compresses Signal-To-Noise Performance

■ Noise Floor Tends To Rise at Low Currents

■ Choosing "Ground Reference" Important

■ Fewer Precision Op Amp Choices Available

■ Bandwidth Suffers As Supply Current Drops

■ Limitations of Zero-Volt Output Amplifiers

■ Noise Pickup from Logic Supplies

■ Tradeoffs to Achieve Desired Performance May Be Necessary

Figure 4.1

Besides these limitations, many design considerations that otherwise are minor issues suddenly become important. For example, signal-to-noise (SNR) performance degrades as a result of swing limitation. "Ground reference" is no longer a simple choice, as one reference voltage may work for some devices, but not others. System noise usually increases dramatically as operating current drops and bandwidth decreases. Therefore, achieving adequate bandwidth and required precision with a somewhat limited selection of amplifiers presents significant design challenges in single-supply, low power applications. The following sections discuss each of these issues.

REDUCED SIGNAL-TO-NOISE PERFORMANCE

The most immediate effect on an amplifier circuit when operating with a single supply at a reduced voltage is the reduction in signal swing. Even if the noise floor remains constant (highly unlikely), the signal-to-noise performance will drop as the signal amplitude decreases.

Most op amps that are designed to operate from ±15V usually do not have problems with output headroom: 3V to 4V is sufficient for most applications. However, if the supply voltages drop to, say +12V, a 3V headroom requirement (at each rail) would limit the signal swing to 6Vp-p (from +3V to +9V). Dropping the voltage further to +5V will render these op amps inoperable, as there is no output swing capability left.

For this reason and others, low voltage single supply op amps are designed so that their output stage is designed to swing as close to both rails as possible. This helps to restore some of the lost SNR performance. It is useful if the output can swing to the negative rail. Many op amps do have this capability. More on this subject in the next sections. On the positive rail side, most single supply op amps still require 1V to 2V of headroom because of junction voltages and biasing circuits. Others require even less by designing the output stage such that there are no junction voltages to limit headroom. Thus a 3V to 4V or more swing is possible for a 5V supply. The drawback is that most of these op amps are not designed to source much output current, usually 5mA maximum.

Besides being compressed at high levels end by signal reduction, SNR performance is generally squeezed from the bottom end as well as noise floor tends to rise. This is because single supply usually accompanies an inevitable drive toward lower supply current consumption, which tends to increase noise up.

The designer must decide how these issues affect the final performance target of the system and make the necessary tradeoffs.

WHERE IS "GROUND"?

Most of us take "ground" reference for granted. Most analog circuits scale their input and output ranges about a ground reference. For ±15V supply operation, a reference that splits the supplies is very convenient, as there is ample supply headroom to work with. Indeed, being a de facto standard also helps ease the choice.

Such is not the case for single supply circuits. Ground reference can be chosen anywhere within the supply range of the circuit. There is no standard to follow. Indeed, the choice of ground reference depends on the type of signals used. To illustrate the point, choosing the negative rail as the ground reference may optimize the signal dynamic range of an op amp

that is designed to swing to zero volts. On the other hand, the signal may have to be level shifted in order to be compatible with another device that is not designed to operate at 0V input because the signal can no longer be inverted. These limitations can force an inefficient design, thus increasing the cost of the system.

It is prudent to sit back and think through the design requirements, roughly sketch out the circuit configurations of various stages that fit together, and get an idea of what devices might be used before deciding on the ground reference.

CHOOSING THE NEGATIVE RAIL AS THE GROUND REFERENCE

This is the simplest and the most natural choice for setting the ground reference. Since the negative rail is the return of the supply, its impedance is very low and it makes an ideal ground reference. All signals can be returned to this point without the concern about its ability to sink the current - assuming the current is within the rated capability of the supply. Nevertheless the voltage drop in negative rail ground returns can be a problem, and their resistance must be kept low.

Setting ground reference at the negative rail usually allows the maximum signal dynamic range, as it establishes the limit of one end of the signal range. However, this may present a problem interfacing with other devices as their inputs or outputs are not designed to operate near the negative rail. Therefore it is important to know what type of devices are needed for the application, knowing that the signal will swing to the negative rail.

AN ISOLATED DIGITALLY PROGRAMMABLE, LOOP-POWERED 4-TO-20mA PROCESS CONTROLLER
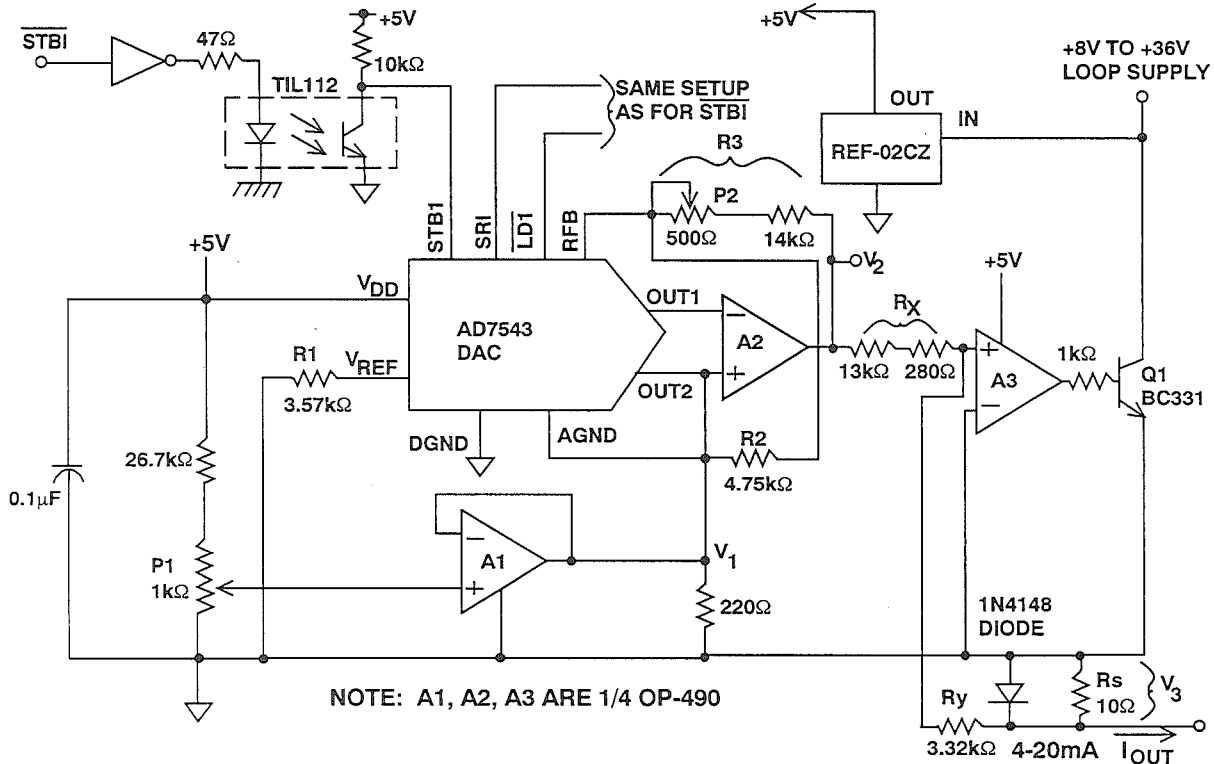

Figure 4.2

Quite often a non-single supply device can be made to operate in a single supply environment. For example, Figure 4.2 shows a CMOS DAC operating with a single supply in a loop-powered 4-to-20mA process control application. Note that while the op amp uses the negative rail as the reference voltage, the DAC is biased up from the negative rail with a separate reference voltage V_1. This allows a non-single supply device to interface properly with a single supply op amp.

Power for the controller circuit is derived from the loop supply, which can range from +8V to +36V. Since the controller is intended to be isolated, all control signals must be opto-isolated before being applied to the DAC. To limit the power and the number of isolators and components, a serial input loading DAC is preferable.

The AD7543/PM7543 is a 12-bit DAC that can be loaded and controlled with only three lines, STB1, SRI and $\overline{LD1}$. Since the opto-isolators act as signal inverters, the microcontroller, PC, or whatever is supplying the control signals must take this into account and generate the appropriate logic levels to the opto-isolators. The serial data is clocked into the input register on the rising edge of STB1. Data is loaded with the MSB as the first bit in the data stream. Once the new data word has been clocked in, it is transferred to the DAC register by strobing $\overline{LD1}$. Refer to the AD7543/PM7543 data sheet for more details.

The DAC output voltage at V_2 is given by:

$$V_2 = V_1 + V_1 \times D \, (1 + R_3/R_2).$$

where D is the normalized value of the DAC digital input code in decimal and can vary from 0 to almost unity (4095/4096). This output voltage is transformed into a loop current by means of A3 and Q1. Amplifier A3 drives the NPN transistor Q1, configured as an emitter follower in the feedback loop, to maintain a current necessary to keep the voltage V_3 across R_S, the sense resistor, equal to the voltage across R_Y, the feedback resistor. Since the ratio of R_X to R_Y is 4 so the ratio of voltages across R_X and R_Y must be the same, i.e. $V_3 = V_2/4$.

Thus V_3, and ultimately the loop current, follows the DAC output voltage V_2. In order to operate from low loop voltages, the voltage V_3 should be as small as practical. With the 10 Ω used for R_S in Figure 4.2, V_3 varies from approximately 40 mV (at 4 mA loop current) to approximately 200 mV (at 20 mA loop current).

From the above equation, with all 0's in the DAC,

$$V_2 = V_1,$$

and with all 1's in the DAC and $(1 + R_3/R_2) = 4$,

$$V_2 \sim 5V_1.$$

Thus as the loop current changes from 4 mA to approximately 20 mA, V_2 changes from V_1 to approximately $5V_1$ and, because of the x4 attenuation due to the R_X/R_Y ratio, the sense voltage V_3 correspondingly changes from $V_1/4$ to $5V_1/4$.

The zero-scale loop current is calibrated by adjusting potentiometer P1, with all 0's in the DAC, until a current of 4 mA is measured flowing in the loop. The full-scale loop current is calibrated by adjusting potentiometer P2, with all 1's in the DAC, until a current of 20 mA - 3.9 μA is measured flowing in the loop. (One LSB of current is equal to 16/4096 mA or 3.9 μA.) The zero-scale adjustment is unaffected by the full-scale adjustment.

Resistor R_1 is chosen to be equal to the parallel combination of resistors R_2 and R_3. This avoids the absolute value of the DAC ladder resistance, which may vary from device to device, from appearing in the output expression for V_2 (assuming $R_{FB} = R_{ladder}$, i.e. , no DAC gain error). Ideally resistors R_1, R_2, and R_3 should be the same type and from the same manufacturer to ensure that their TCs match and track each other. However since it is necessary to provide full-scale adjustment, R_3 consists of a fixed 14 kΩ metal film resistor and a 500 Ω 10-turn potentiometer P2. Although the TCs of the potentiometer and the metal film resistor will almost certainly not match, the additional drift will not be significant since the TC of the much larger fixed resistor will dominate.

The 220 Ω resistor on the output of A1 acts as a pull-down resistor and helps to keep the voltage V_1 constant as the DAC's digital input code changes.

The actual loop current that flows is given by:

$$I_{OUT} = V_3 \left(1/R_S + 1/R_Y \right)$$

R_S is set at 10 Ω and R_Y is set at 3 kΩ. With 4 mA flowing (I_{OUT} = 4 mA), using the above equation we see that V_3 = 39.867 mV (V_2 = 159.468mV). Similarly, $V_2 = V_1$ at the all-0's code. This voltage, as mentioned above, is set by P1.

At full-scale (I_{OUT} = 30 mA - 3.9 μA), using the above output current equation, we see that V_3 = 199.336 mV (V_2 = 797.344 mV). This voltage is set by P2.

The diode across R_S serves to clamp the voltage to 0.6V such that it limits the loop current to no more than 60 mA during power-on, where transient voltages may be present on the base of Q1. When this condition occurs, Q1 can momentarily turn on and cause excessive current to flow through R_S. If a sufficiently large voltage drop develops across R_S, the non-inverting input of amplifier A3 may pull 0.6V more negative than the inverting input (negative rail). This may cause A3's output to invert its phase (go   positive) which keeps Q1 on, causing a positive feedback circuit lock-up. The diode clamp prevents this condition from occurring. If a smaller current limit is required, a low-leakage Schottky diode may be used in place of the silicon diode.

USING A FALSE-GROUND REFERENCE

Not all single supply circuits work well with the 0V ground system. For example, audio signals or video signals may be best handled using a false-ground system by biasing the amplifiers to the mid-point of the supply. Then the signal can be AC coupled through the amplifier chain. This removes the necessity of level shifting at each amplifier stage as would otherwise be required if the 0V ground system is used. It also saves the cost of additional components to do level shifting.

It is often assumed that a false-ground circuit need only be a simple buffer amplifier without the bypass capacitors and compensation. In some cases, one can get by without them as long as the false-ground node does not see any dynamic or transient load changes. These can occur when driving the ground pin of a D-A or an A-D converter. In these applications, the false-ground node must hold its voltage constant with minimum perturbation. If reference "bounce" is present, conversion error may result, or noise may be injected into the circuit.

The choice of the quality of the false-ground rests on whether the circuit is sensitive to the false-ground perturbation, both in DC and AC terms. Not all applica-

tions necessarily require a high-quality, low impedance false ground. In fact, in some cases, it may be sensible to use both false-ground as well as negative rail ground references in different parts of the circuit. One needs to observe the level shifting requirement when interfacing the two. It depends on what works best.

A solid false-ground can be easily implemented using a voltage divider or a reference voltage buffered by an amplifier. The choice of the op amp and the implementation is critical to a good reference node without reference "bounce". An example is shown in Figure 4.3.

These circuits have elaborate compensations to allow for heavy capacitive bypasses at the false-ground output. The benefit of a big capacitor is that not only does the false-ground present a very low DC resistance to the load, its AC impedance is low as well. The capacitor serves as a "charge reservoir" to absorb any momentary load current surges, thus minimizes reference "bounce". A reasonably fast settling op amp also helps to replenish the discharge quickly for rapid recoveries from disturbances.

Proper recovery requires the op amp to have sufficient output current sinking as well as sourcing capabilities. Furthermore, the amplifier's output current level should not operate close to the current limit point as a surge of current can easily push it over the limit. Undesirably long recovery will result.
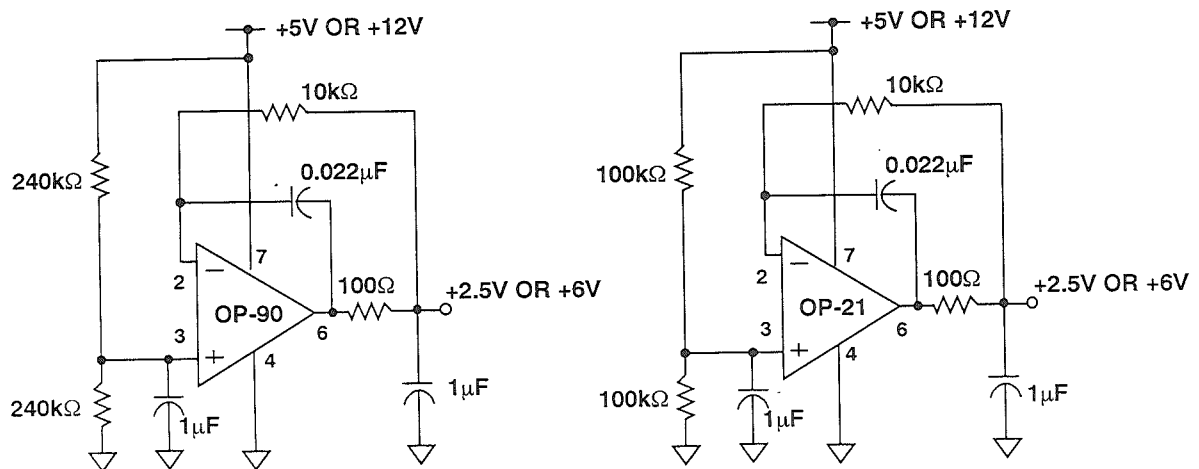
SUPPLY SPLITTER REFERENCE GENERATORS

Figure 4.3

A 50/60Hz NOTCH FILTER USES FALSE-GROUND

To process AC signals, it can be easier to use false-ground bias. A 50/60Hz notch filter for eliminating line noise in a patient monitoring equipment having several kilohertz bandwidth may not be sensitive to false-ground perturbations. Such an application might use a simple false-ground circuit as shown in Figure 4.4 that biases the amplifiers to the midpoint of a +12V supply. This notch filter achieves nearly 40dB rejection of 60Hz pickup at a Q of 0.75. To reject 50Hz frequency, simply change the resistors in the twin-T section (R1 through R5) from 2.67kΩ to 3.16kΩ.

This circuit helps reject 50Hz or 60Hz power line frequency pick-up that tends to obscure low frequency physiological signals, such as heart rates, blood pressures, EEGs, ECG, etc. The notch filter achieves almost 40dB (at a Q=0.75) of rejection using standard off-the-shelf components.

The filter uses a pair of the OP-482's quad op amps in a twin-T configuration whose frequency selectivity is very sensitive to the relative matching of the capacitors and resistors in the twin-T section. Mylar is a good choice for the twin-T's capacitors, and the relative matching of the capacitors and resistors determines the filter's passband symmetry. Using 1% resistors and 5% capacitors produced satisfactory results.

The amount of rejection and the Q of the filter is solely determined by one resistor, and is as shown in Figure 4.5. For example, at a Q=1, the filter measured 35dB rejection of 60Hz noise. Additional rejection beyond 40dB at 60Hz can be achieved by cascading identical filter sections.

The third of the OP-482 amplifier, A3, buffers the supply splitter to create a false-ground reference voltage at +6V. No special output bypassing is necessary to
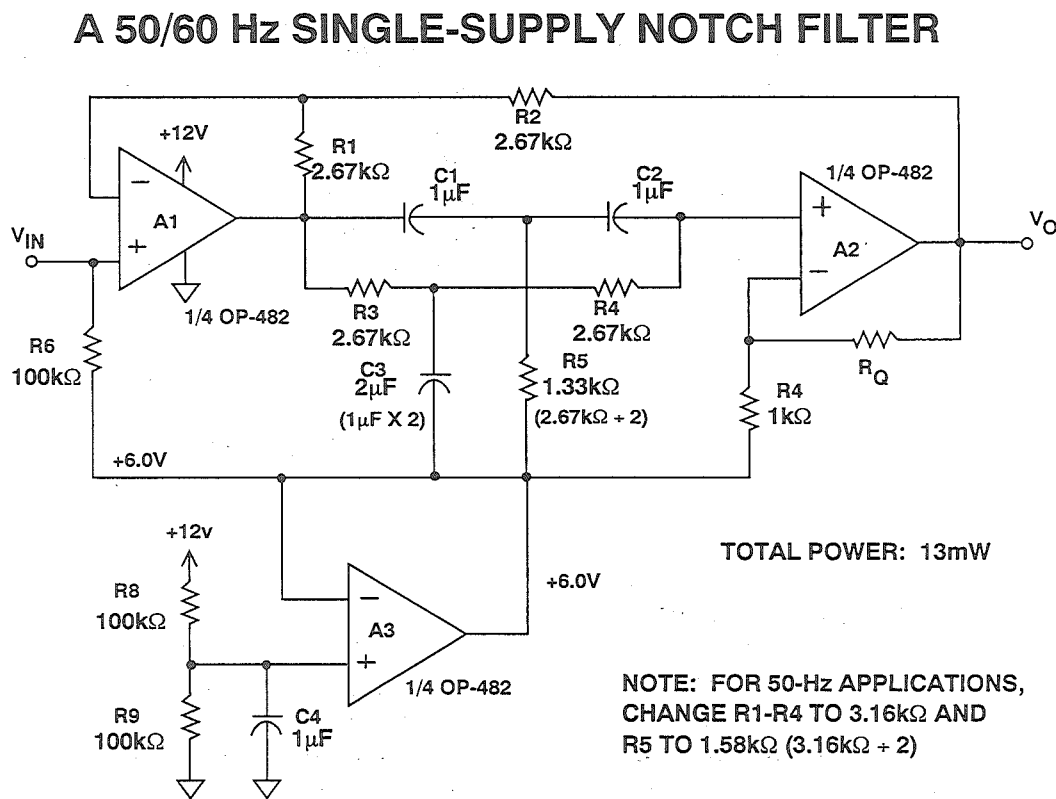
A 50/60 Hz SINGLE-SUPPLY NOTCH FILTER

Figure 4.4

RQ, REJECTION AT 60 Hz, AND FILTER'S VOLTAGE GAIN AS A FUNCTION OF THE FILTER Q

Filter Q	R_Q (kΩ)	Rejection (dB)	Voltage Gain
0.75	1.0	40	1.33
1.00	2.0	35	1.50
1.25	3.0	30	1.60
2.50	8.0	25	1.80
5.00	18	20	1.90
10.0	38	15	1.95

Figure 4.5.

OP-282 / OP-482 DUAL AND QUAD LOW POWER, HIGH SPEED JFET OP AMP PERFORMANCE FEATURES

■ High Slew Rate: 9 V/μs

■ Low Supply Current: 250 μA / Amplifier

■ Wide Bandwidth: 4 MHz

■ Unity Gain Stable

Figure 4.6

improve the quality of the false ground as the op amp buffer has more than sufficient bandwidth and fast settling characteristics that are well beyond the signal bandwidth.

The OP-482 is chosen because it can pass signals more than 1 MHz at a Q of 1 while consuming a relatively low power of

13 mW, making it suitable for battery operated or portable medical instrumentation. In addition, the OP-482's FET input has low current noise that interfaces well with the high impedance of ECG and EEG probes. Some OP-482's features are shown in Figure 4.6.

AN ULTRASONIC CLAMPING RECEIVER USING A FALSE GROUND REFERENCE

Another application example where it makes sense to use false ground reference is an ultrasonic sensor amplifier as shown

in Figure 4.7 where simple diode feedback provides crude but effective gain compression for wide dynamic signal range.

A 40kHz ULTRASONIC CLAMPING/LIMITING RECEIVER
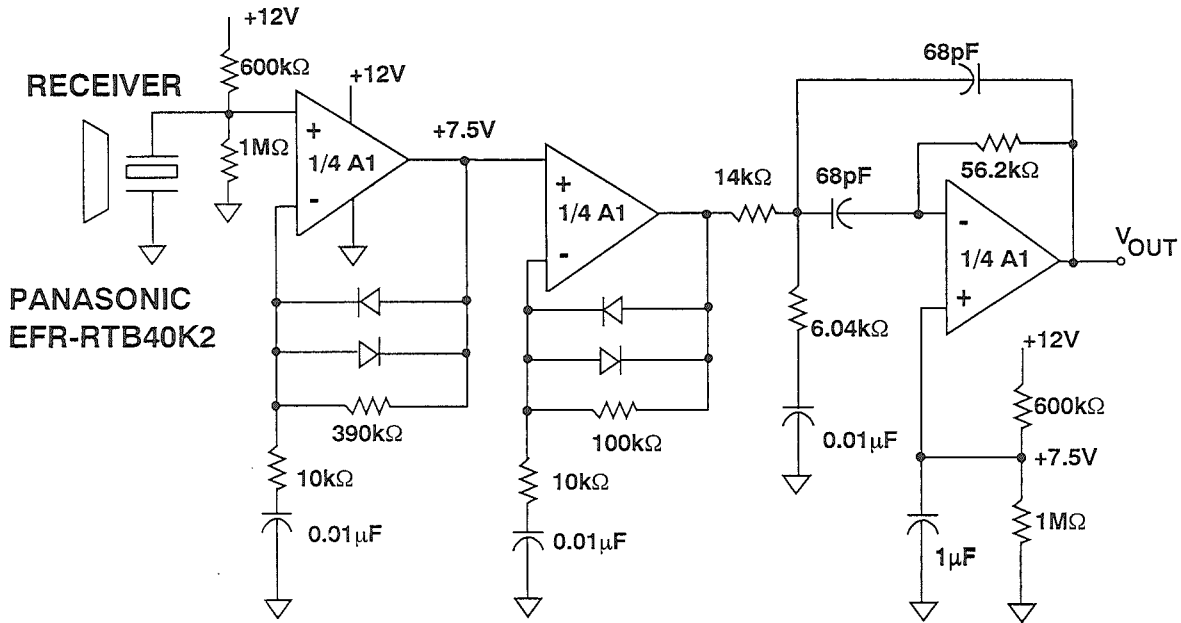
NOTE: A1 IS OP-482
DIODES ARE IN914

Figure 4.7

This circuit amplifies a 40kHz ultrasonic wave signal through a pair of low-cost clamping amplifiers before feeding a bandpass filter to extract a clean 40kHz signal for processing. The ultra-sound signal is AC-coupled into the false-ground bias node by virtue of the capacitive piezoelectric sensing element. Rather than using a supply splitter (1/2 the supply voltage) bias, the false-ground is set at 7.5V, which is halfway between the input and output range of the op amp to get the maximum signal swing. The 600 kΩ and the 1 MΩ divider provides the bias.

Each amplifier stage provides AC gain while passing on the DC self-bias. As long as the output signal at each stage is less than a diode's forward voltage, each amplifier has unrestricted gain to amplify low level signals. However, as the signal strength increases, the feedback diodes begin to conduct, shunting the feedback current, and thus reducing the gain. Although distorting the waveform, the diodes effectively maintain a relatively constant amplitude even with large signals that otherwise would saturate the amplifier. In addition, the this design is considerably more stable than feedback type AGC.

The overall circuit has a gain range from -2 to -400, where the inversion comes from the bandpass filter stage. Operating with a Q of 5, the filter restores a clean, undistorted signal to the output. Total supply current draws 1 mA maximum for the entire circuit making battery operation feasible.

HANDLING ZERO-VOLT INPUT SIGNALS

Most op amps are designed to operate with two supplies and usually cannot handle signals that are at or near the negative rail. These amplifiers typically have NPN input transistor pairs, requiring at least 2V to 3V of headroom at either rails. Operating at or near the negative rail would cause the amplifier to go nonlinear as saturation is approached. Even worse, it may cause the output to reverse its phase.

Op amps that are designed for single supply operation typically use PNP input pairs to allow the input to operate linearly at or near the negative rail. An example of such an op amp's input stage is shown in Figure 4.8.

Another input architecture that can operate at zero volt is to use MOSFET transistors in a CMOS amplifier. With a P-channel input pair, the input common-mode range extends to the negative rail. Figure 4.9 shows such an amplifier.

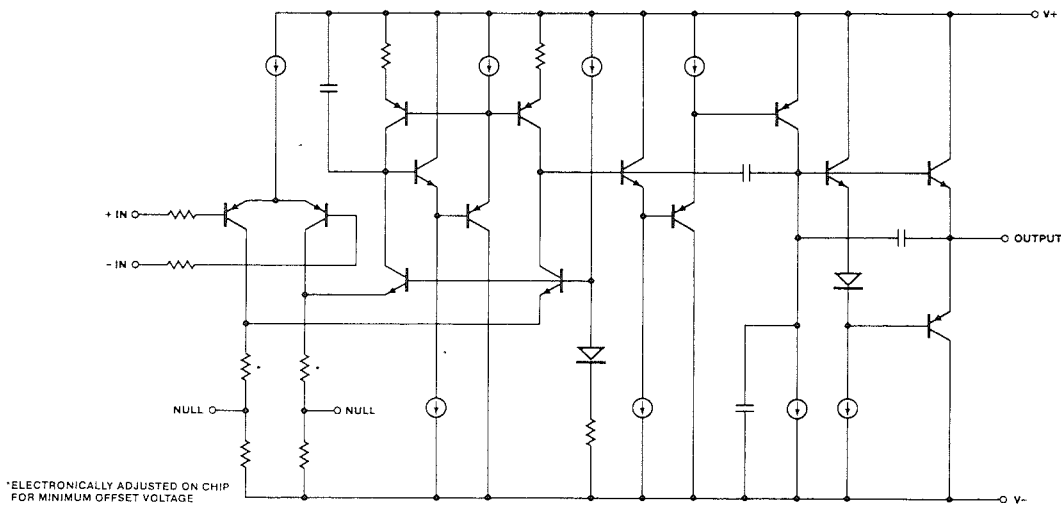# OP-90 PNP INPUT STAGE DESIGN ALLOWS ZERO-VOLT INPUT OPERATION

Figure 4.8
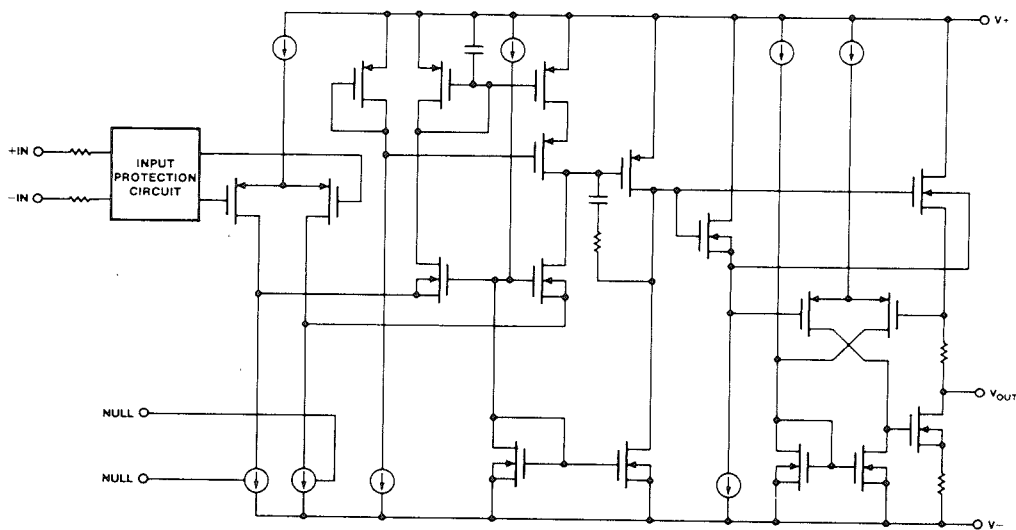
OP-80 CMOS OP AMP ALLOWS ZERO VOLT INPUT OPERATION

Figure 4.9

HANDLING ZERO-VOLT OUTPUT SIGNALS

Ideally a single supply op amp's output should be capable of swinging to the negative rail, especially if it is feeding into the input of the next stage that can operate at zero volts.

Beware that as the output swings very near the negative rail, the output accuracy can drop off rapidly as a function of the load current the output must sink. This is because a single supply amplifier's output stage usually have either an active transistor pull-down, or it may require a resistor to pull-down to the negative rail. Whatever the means, the pull-down's

finite resistance develops a voltage drop that prevents the output from swinging fully to the negative rail. If accuracy is required at or near zero volts, the load current must be kept as small as practical. Always keep in mind that the total load current also includes the current flow in the feedback resistor.

As mentioned above, some op amps have active output drive to the negative rail. Others require a resistor pull-down to achieve complete swing to zero volt. Figure 4.10 shows both topologies.

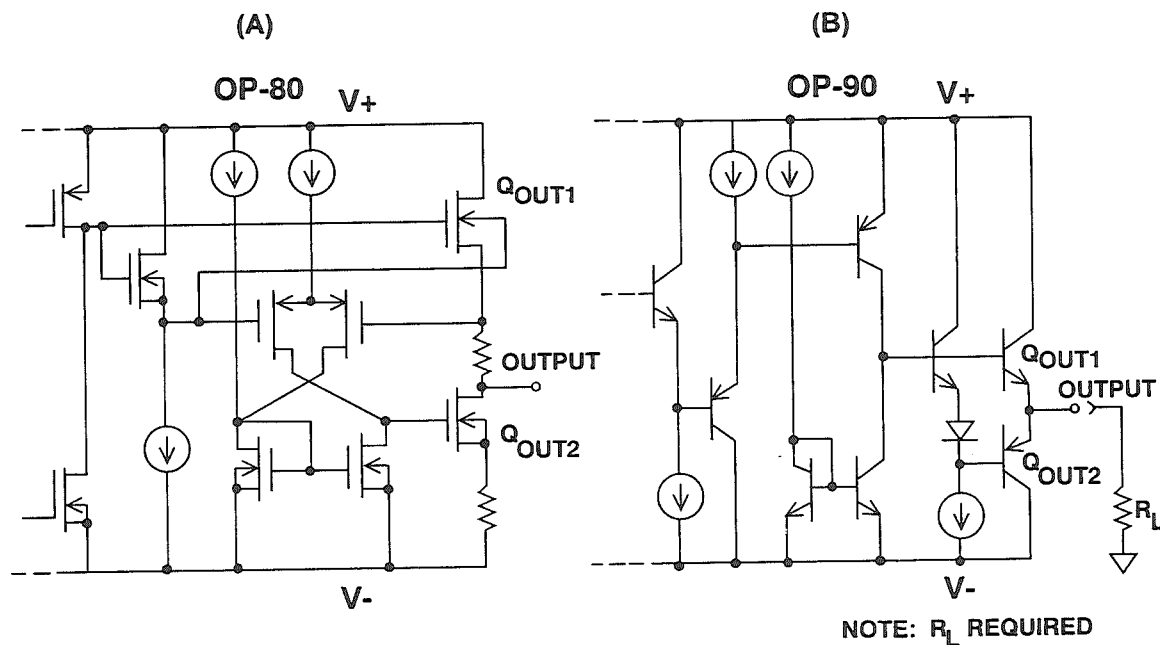## ZERO-VOLT SWING OUTPUT STAGE DESIGNS

Figure 4.10

Figure 4.10(a)'s OP-80 output stage relies on the Q_{OUT2}'s internal ON-resistance to pull the output down to the negative rail. Including a source resistance, the total pull-down resistance is typically 400 Ω. As long as the load currents is less than 1 μA, its output will swing to within 1mV of the negative rail.

The OP-90 utilizes a conventional push-pull emitter-follower output stage as shown in Figure 4.10(b). It provides low impedance drive except for output voltages less than 0.5V to the negative rail.

Below this voltage, the bottom output transistor Q_{OUT2} saturates, clamping the output at a base-emitter voltage above the negative rail. If no external pull-down resistor is provided, the top output transistor Q_{OUT1} turns off completely as its base voltage tends to pull less than its base-emitter voltage, cutting off the base drive. However, a pull-down resistor would keep the Q_{OUT1} active, and therefore linear operation continues as the output swings to the negative rail.

THE KEY IS ZERO-VOLT SWING WITH LINEARITY

It is not sufficient for a single supply amplifier to just swing to zero volts. Accuracy can only be assured if its linearity does not drop off significantly, at least to within millivolts to the rail. The best way is to measure an amplifier's linearity as its output swings to the negative rail using a circuit as that in Figure 4.11.

A small amount of nonlinearity, such as a "bowing" or an irregular "S" shape may not be significant enough to cause concern. However, if the curve shows a radical discontinuity or exhibits a large "glitch", that may be an indication that the amplifier is not suited to operate at or

near the negative rail. The designer must determine whether such behavior is acceptable in the application.

A good measurement should look something like that in Figure 4.12. The example measurement was made using the OP-90 with an output resistor pull-down to a negative bias of -5V. The OP-90 exhibits excellent linearity below 0.5V and indeed behaves well as its output swings to 0.0V. No appreciable offset fall-off was evident. This type of amplifier provides accurate measurement of low level signal while operating at zero-volt input and zero-volt output.

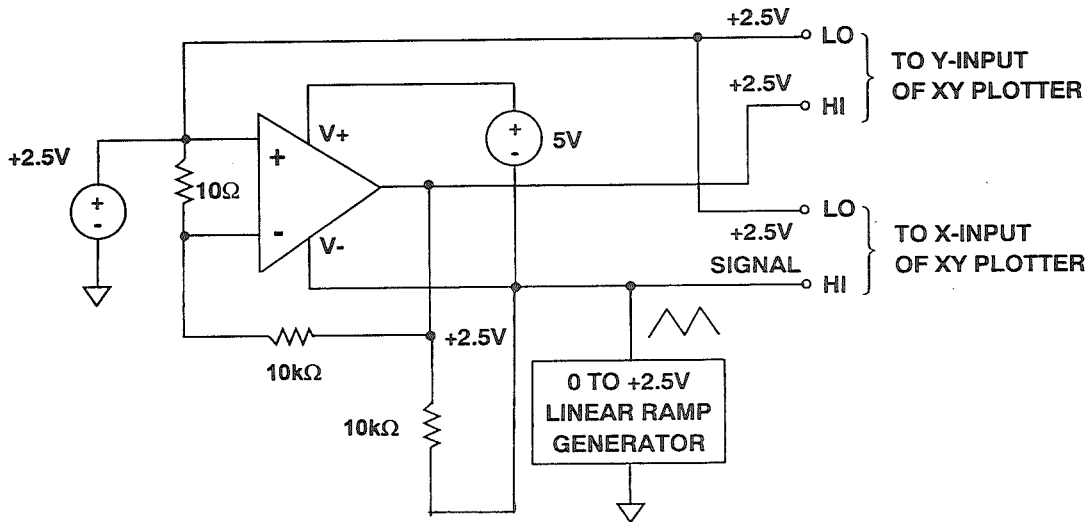# TEST CIRCUIT TO MEASURE SINGLE-SUPPLY AMPLIFIER'S LINEARITY NEAR ZERO-VOLTS

Figure 4.11

A ZERO-IN / ZERO-OUT, SINGLE SUPPLY AMPLIFIER SHOULD EXHIBIT LINEAR PERFORMANCE NEAR ZERO VOLTS OUTPUT
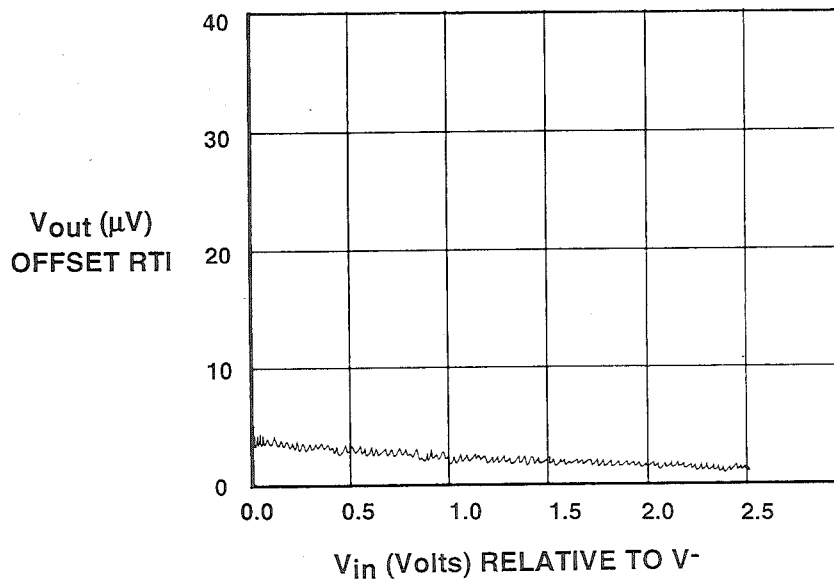
Figure 4.12

APPLICATION EXAMPLE: DESIGNING A TRUE SINGLE-SUPPLY INSTRUMENTATION AMPLIFIER

It is not straight forward to design a true instrumentation amplifier that has zero-in and zero-out capabilities. A standard 2 op amp instrumentation amplifier, shown in Figure 4.13, requires special considerations when operating with the negative supply pin at ground.

The main issue is that amplifier "A" needs to be able to sink any current that flows through resistor R_3. With -IN at 0.0V, the output V_{OA} will be at ground potential. Any voltage on the +IN will cause current I_{SINK} to flow through R_3 and into V_{OA}. If V_{OA} changes with changing current, this error will be gained up to the circuit's output V_{OB}, by the ratio of R_4 to R_3. Typical values for a gain of 100 are $R_2 = R_3 = 20$ kΩ and $R_1 = R_4 = 99R_2 = 1.98$ MΩ. Assuming a +5V supply and a maximum differential voltage of 40 mV, the maximum amount of sink current is $I_{SINK} = 2$ μA, which occurs when -IN = 40 mV. While this seems like a very small amount, it is significant because amplifier "A" needs to maintain $V_{OA} = 0.000$V. Even as little as a 1 mV error on V_{OA} will lead to a 99 mV error at the output.

While the OP-90 has zero-in / zero-out operation, its output is not able to sink current when its voltage is at 0.000V. Normally a pull-down resistor on the output allows the voltage to swing to around 100 μV. However, since $R_3 = 20$ kΩ, the pull-down resistor would need to be less than 400 Ω. Using this value will result in up to 10 mA of extra supply current at high common-mode voltages. Obviously 10mA is unacceptable in a low power design. Thus, how can a true instrumentation amplifier be made when it is used in single supply? One answer to this challenge is an addition of two discrete CMOS N-channel FET transistors configured as a current mirror as shown in Figure 4.14.

The 10 kΩ resistor in combination with Q_1 set up the quiescent current in the mirror, which is approximately 340 μA with a gate-to-source voltage of 1.6V. This keeps Q2 turned on and provides a very low resistance current sink that pulls V_{OA} down to ground. A desirable feature is that this resistance does not shift appreciably as I_{SINK} changes, thus resulting in accurate operation of the instrumentation amplifier.

The benefit of using this method over a simple pull-down resistor is that as the common mode voltage is increased the sink current is limited to just 340 μA by the current mirror. Thus the most current that will be consumed by the two transistors is 680 μA. For example, a common mode voltage of 4.0V results in a V_{OA} voltage of 4.0V. This condition would require the OP-290 to source 10mA with a 400 Ω pull-down in contrast to only 340μA in the case of with the current mirror, producing significant saving in power supply current.

4

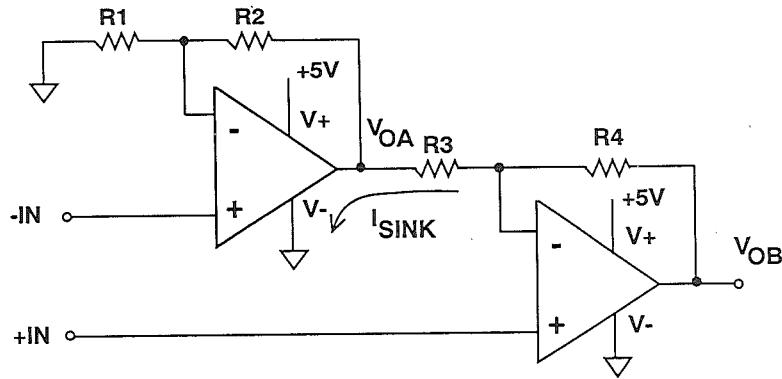# A TRADITIONAL 2 OP-AMP INSTRUMENTATION AMPLIFIER

Figure 4.13

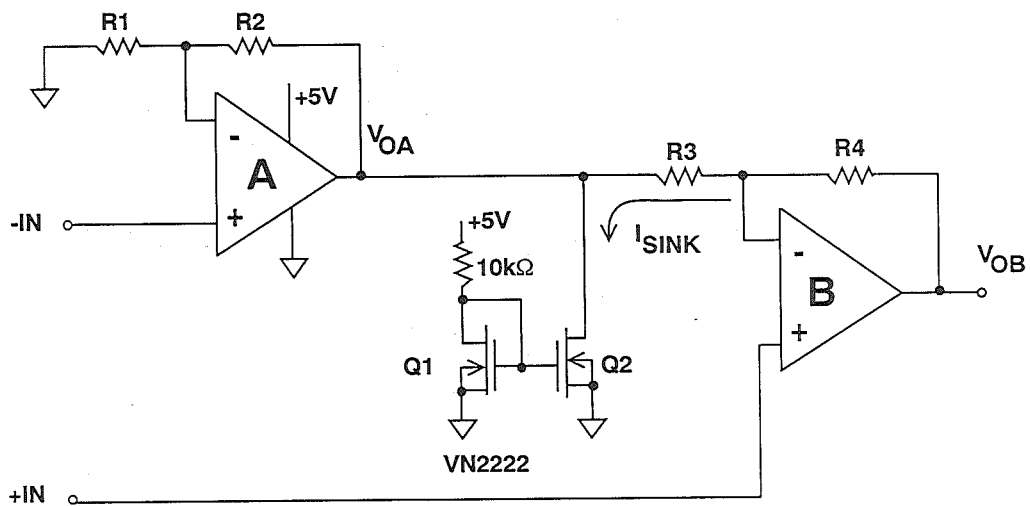# A TRUE SINGLE-SUPPLY, ZERO IN/ZERO OUT INSTRUMENTATION AMPLIFIER USING THE OP-290

Figure 4.14

OTHER LIMITATIONS OF ZERO-VOLT OUTPUT AMPLIFIERS

No Inverting Amplifier. While the simple non-inverting amplifier configuration serves most amplification functions, grounded rail does not lend itself to inverting a signal. That is, an inverting amplifier usually cannot be implemented unless the input is biased up to a "false-ground" voltage other than the rail.

Unipolar Operation Only. Another way of saying it is that ground-referred single supply non-inverting amplifiers cannot amplify negative signals. They can, but only if used in the inverting mode. This is obvious yet when required, makes the design considerably more complex. An example of a unipolar-only signal conditioning circuit is the thermocouple amplifier in Figure 4.15. This amplifier limits the temperature measurement range from 0°C to 200°C by scaling the amplifier output from 0V to 2.00V, respectively. Clearly the amplifier is not designed to measure temperature below 0°C, that is, below zero volts by virtue of having only one supply. If a negative signal needs to be measured, it is possible to level shift such that the amplifier can deal with negative polarity.

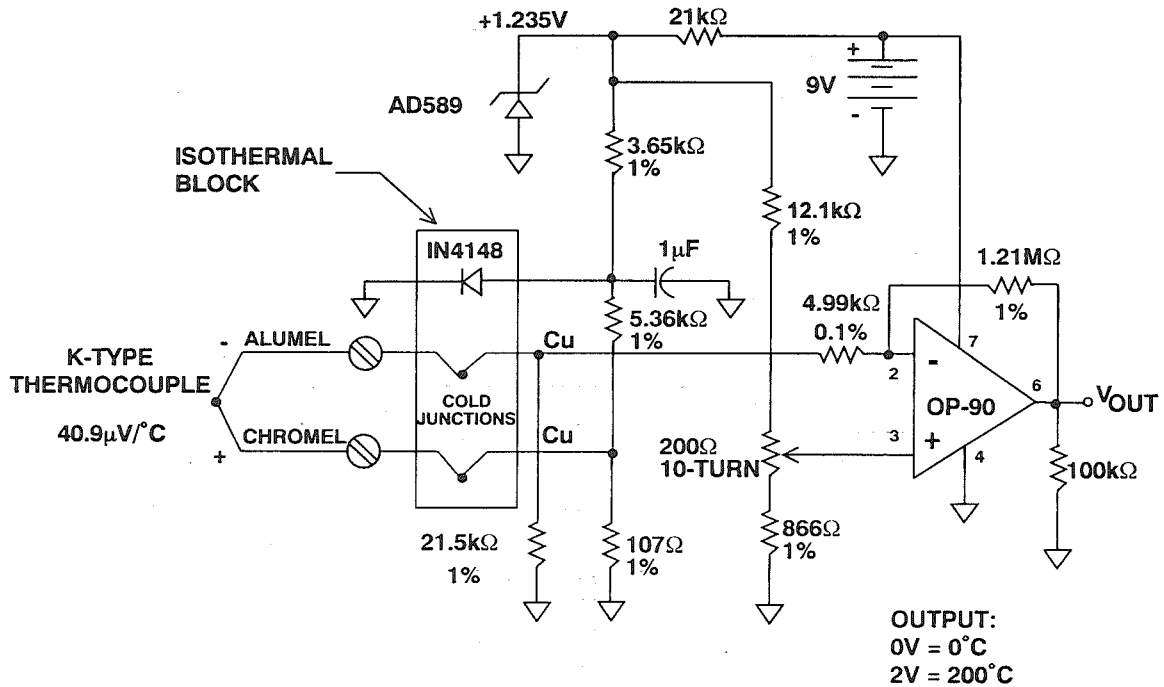# A COLD JUNCTION COMPENSATED BATTERY POWERED THERMOCOUPLE AMPLIFIER

Figure 4.15

This amplifier utilizes the linear portion of the K type thermocouple from 0°C to 200°C. Within this temperature range, the thermocouple's Seebeck coefficient centers at 40.9 μV/°C with a variation of +0.5 μV/°C and -0.44μV/°C. This corresponds to a maximum error of ±1°C at any temperature within this range.

Compensating the cold-junction is made easier by terminating the junctions at the PC board. The operation of cold-junction compensation circuits has been described in the temperature transducer section of this seminar. The object is to keep both terminating junctions at the same temperature at all times regardless of the ambient change. The compensation is accomplished by sensing the junctions temperature with an inexpensive 1N4148 diode, by placing it as close to the junctions as possible. Its temperature coefficient of -2.1mV/°C is divided down by the 107 Ω and the 5.36 kΩ divider to yield a -40.9μV/°C that would exactly cancel the cold-junction T.C. of the thermocouple. Thus any ambient temperature change does not induce an error in the measurement.

The measuring junction's Seebeck TC is amplified by a factor of 244.5 such that a full-scale of 200°C is equivalent to 2.000 volts at the output. This voltage range is compatible with most low-cost single-chip integrating A/D converter for panel meter applications. The 1.235V reference provides stable biasing for the cold-junction compensator as well as for offsetting the amplifier.

A single calibration can be made by adjusting the 200 Ω potentiometer for a 0.00V output with the thermocouple immersed in 0°C ice bath. Although the potentiometer resistance makes up a small part of the 121 kΩ resistor leg, its temperature coefficient should be chosen such that it is smaller than that of the fixed resistors to minimize its overall drift effect.

During normal operation, the 21.5 kΩ resistor is part of the cold-junction compensation circuit whose parallel combination with the 107 Ω resistor forms the T.C.-correction voltage dividing ratio with the 5.36 kΩ. However, it is purposely placed in the "-" side of the thermocouple so that if the thermocouple is disconnected or open-circuited, the 21.5 kΩ pull-down will cause the output to saturate to the positive rail, thus indicating an equipment failure.

Clearly, with zero volts established as the zero scale, this design cannot make negative signal measurements.

RAIL-TO-RAIL OUTPUT SWING OP AMP

Op amps whose outputs are designed to swing from one rail to the other are ideally suited for single, reduced supply operation. Theoretically the maximum signal-to-noise performance for a given supply voltage can be achieved. One such rail-to-rail device is the OP-295 dual operational amplifier.

Similar to zero-out op amps, how close a rail-to-rail op amp can swing to either supply depends on its finite output resis-tance and the load current it must source or sink. In order to be sure the amplifier swings as close to the rail as possible, keep the load current small.

Figure 4.17 shows a D-to-A converter analog channel that takes advantage of the wide output swing of a rail-to-rail op amp. The entire circuit operates off a single +5V supply, and its output swings from 0V to 4.095V full-scale, in 1 mV per LSB increments. Thus the op amp must

OP-295 DUAL RAIL-TO-RAIL
OP AMP KEY FEATURES

■ **Rail-to-Rail Output Swing**

■ **Sinks and Sources Current at the Rails**

■ **Single-Supply Operation** .... +3V to +36V

■ **Low Offset Voltage** .... 300µV Max

■ **Low Supply Current** .... 300µA Max

■ **Gain-Bandwidth Product** .... 85 kHz

■ **Unity-Gain Stable**

Figure 4.16

faithfully reproduce accurate voltages from less than 500 μV to the full-scale of 4.095V in order to preserve the 12-bit performance of the DAC.

In this design, the CMOS D-to-A converter is connected in a voltage switching output mode rather than the normal current output mode so that its output is positive.

In the voltage output mode, the R-2R ladder functions as a voltage divider. A 1.23V reference is selected so that the I_{OUT} pin of the CMOS DAC is biased up no more than 1.25V. The purpose of this is to preserve the full 12-bit linearity performance of the DAC. This is because the I_{OUT} pin is the summing node to which all the R-2R ladder branches are switched by a bank of CMOS transistors whose channel ON-resistances are part of each 2R resistance leg. A minimum of 3.5V gate drive is necessary to fully turn on each transistor. If the I_{OUT} voltage increases beyond 1.25V, the gate drive voltage is correspondingly reduced and hence increases the 2R resistance. Even a slight shift results in poor DAC linearity performance.

The output voltage at the V_{REF} pin exhibits a constant impedance, typically 11 kΩ. The output swings from zero volts for all 0's code to a full-scale reference voltage of 1.23V. The OP-295 serves as a buffer and provides gain up the full-scale output voltage of 4.096V. Overall, the circuit provides 1mV per bit of programmable control. The OP-295 allows the output swing to within 100 μV of ground. In addition, its offset contributes less than 250 μV error. Thus full 12 bit performance is realized.

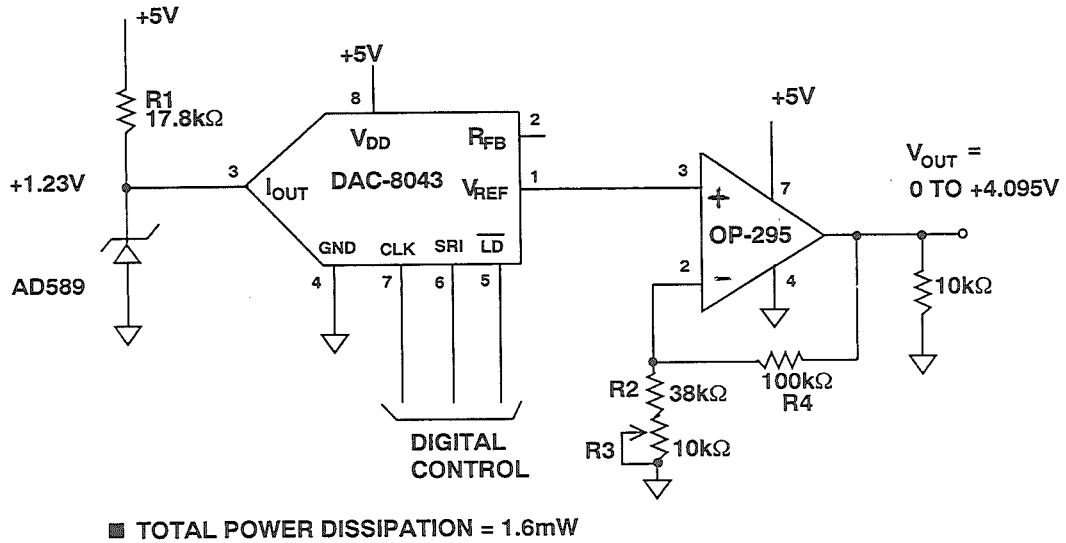# A 5-VOLT 12-BIT DAC
WITH 0 TO +4.095V OUTPUT SWING

■ TOTAL POWER DISSIPATION = 1.6mW

Figure 4.17

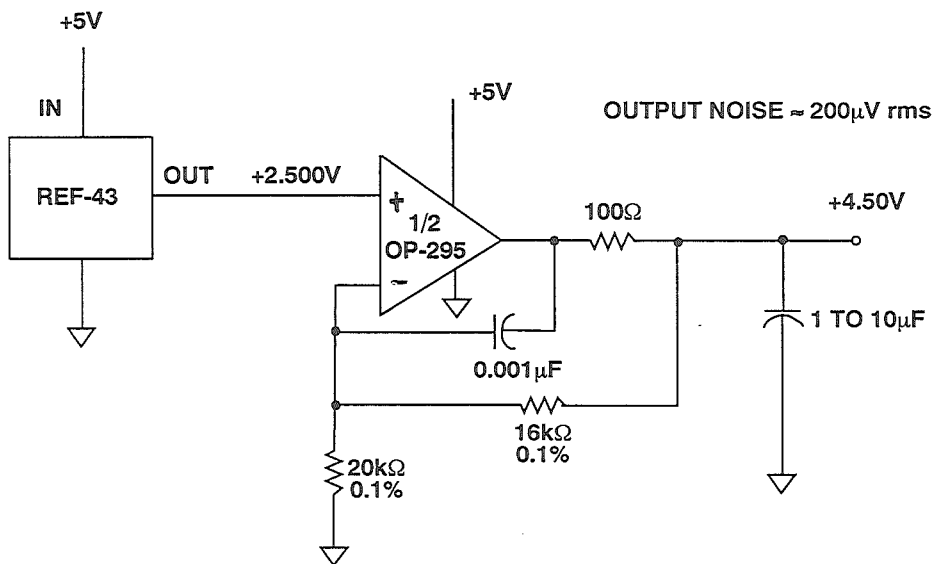# A 4.5V REFERENCE REGULATOR
WITH <20mV NO-LOAD DROPOUT

Figure 4.18

The op amp's rail-to-rail swing capability insures the full-scale output will always meet specifications regardless of supply tolerance.

Another useful application is a 4.5V reference that is powered by a single +5V supply as in Figure 4.18. The REF-43 provides a temperature-stable 2.500V reference to the OP-295. It in turn amplifies the signal to 4.50V output.

The amplifier is frequency compensated so that it can drive a 1µF to 10µF output capacitance without oscillation. Furthermore, a large capacitor provides a charge reservoir to keep the output stable in the event of a sudden load current surge.

PRECISION SINGLE-SUPPLY OP AMP CHOICES ARE LIMITED

The industry-standard precision op amps such as the OP-07, OP-77, OP-177, AD707/708, etc. are designed to operate with dual, higher voltage (±15V) supplies. Their precision performance is optimized for these supply voltages. As such, trying to operate them at lower voltages may be inadvisable as their specifications may no longer apply. Indeed many do not even function if their inputs are forced to the negative rail, or if they are powered by a single +5V supply.

Very few single-supply op amps exhibit sufficiently low input offset and offset drift to qualify them as precision op amp. The OP-90/OP-290/OP490 come close to precision performance yet can operate off single supply. A comparison of single-supply op amps is given in Figure 4.19.

4

SINGLE SUPPLY PRECISION OP AMPS

		Max V_{OS}	Max TC V_{OS}	Max I_S (/Amplifier)
Single	OP-20	250µV	1.5µV/°C	80µA
Single	OP-21	100µV	1.0µV/°C	300µA
Single	OP-80	1.5mV	-	325µA
Single	OP-90	150µV	2.5µV/°C	20µA
Dual	OP-220	150µV	1.5µV/°C	85µA
Dual	OP-221	150µV	1.5µV/°C	400µA
Dual	OP-290	200µV	3.0µV/°C	20µA
Dual	OP-213	150µV	0.2µV/°C typ	2mA
Dual	OP-295	300µV	<10µV/°C	150µA
Quad	OP-420	2.5mV	10µV/°C	450µA
Quad	OP-421	2.5mV	10µV/°C	450µA
Quad	OP-490	0.5mV	5µV/°C	20µA

Figure 4.19

USING PRECISON OP AMPS IN SINGLE-SUPPLY, LOW VOLTAGE APPLICATIONS

If low offset is required in a single supply, low voltage application, then it may be necessary to choose dual supply, precision op amps to do the job. As mentioned before, most precision op amps do not guarantee their specifications at lower supply voltages. Under these circumstances, the rule to follow is to design conservatively. If the application calls for conditions that are beyond the recommended ranges, most likely the device manufacturer will not be able to guarantee devices' performance — at least not

without some additional testing cost. However, often their applications engineering staff may be able to provide sufficient insight as to how to derate from the performance specifications so that appropriate error budgeting can be done.

Most manufacturers' data sheets do provide sufficient information and characteristics of the device to allow for proper "derating" for worst case designs. The following sections provides some guidelines.

HOW LOW CAN THE SUPPLY VOLTAGE GO?

Some device data sheet provides a supply voltage versus supply current curve or a supply voltage range specification that indicate what the device can operate. Furthermore, it is important to decide for the application where the input voltage range and output voltage swing range need to be in order that an op amp choice can be made. Remember that most precision op amps do require a certain amount of supply headroom for both rails. At low supply voltages this means a greatly reduced signal swing.

For example, the industry standard OP-177's input voltage is guaranteed to have a ±13V range with a ±15V supply. At this voltage, the output is guaranteed to swing ±12V into 2 kΩ load. For all practical purposes at reduced supply voltages, the headroom required can be considered to remain constant. Consequently, at ±5V (or +10V) supply, the OP-177's input linear range drops to only ±3V. Similarly its worst-case output swing is expected to have a minimum of ±2V.

INPUT OFFSET VOLTAGE DERATED BY POWER SUPPLY REJECTION

Precision op amps' input offset voltage specification is normally based on a symmetrical, dual supply, and with an input common-mode voltage at zero. At reduced supplies, additional error sets in,

in the form of input offset that is introduced by the supply reduction. Consequently the worst-case input offset voltage at reduced supplies can be derated by this additional error.

HOW LOW THE SUPPLY VOLTAGE CAN GO DEPENDS ON:

■ THE AMPLIFIER'S INPUT/OUTPUT SWING REQUIREMENT AND CAPABILITY OVER THE FULL TEMPERATURE RANGE

Example: OP-177E (-40°C to +85°C)

	Guaranteed @ ±15V Supply	Expected @ ±5V Supply
Input Voltage Range	±13V	±3V
Output Swing Range	±12V	±2V

Rule to remember: Input/Output headroom is fixed regardless of supply

■ THE DEVICE'S MINIMUM SUPPLY OPERATING SPECIFICATION

Figure 4.20

DERATE INPUT OFFSET VOLTAGE ERROR BY THE POWER SUPPLY REJECTION ERROR

■ Example: OP-177E @ -40°C to +85°C, V_S Reduced from ±15V to ±5V

Initial Input Offset Voltage:	20μV
Power Supply Rejection Error: ($1μV/V × 20V$ V_S Change)	20μV
Derated Input Offset Voltage:	40μV

Figure 4.21

SUPPLY CURRENT DROPS AS SUPPLY VOLTAGE DECREASES

Generally the op amp's supply current will drop as the supply voltage is reduced, but usually not linearly. Most data sheets specify the maximum supply current at a given supply voltage. But it only gives a *typical* characteristic curve showing the supply current level as a function of supply voltage. The question is what can be counted on as the *worst-case* supply current at a reduced voltage?

It is unlikely any op amp manufacturer has the ready answer to this question and would not be willing to guarantee this or other out-of-the-ordinary specification without conducting an exhaustive characterization and yield studies, which are both expensive and time-consuming. Short of this, one can approach this problem by conservatively derating the specification. An example is shown in Figure 4.22.

ESTIMATE WORST-CASE SUPPLY CURRENT BY CONSERVATIVELY DERATING THE SPECIFICATION

■ Example: OP-177E @ -40°C To +85°C

	Typ	Max
Supply Current @ ±15V	1.6mA	2.0mA

Typical Supply Current: 0.75mA @ ±5V
(From Characteristic Curve)

Normal Derating: (1.25 × 0.75mA):   0.938mA

Apply Additional 30% Derating: 1.22mA
(1.3 X 0.938mA)

Figure 4.22

DERATING INPUT OFFSET VOLTAGE DRIFT

Input offset voltage drift is more difficult to derate, as generally little or no data sheet information is provided to indicate how it behaves as the supply voltage is reduced. In these cases, there are two ways to approach the problem. The more accurate approach is to measure the drift of a sample of devices at both the rated supply voltages as well as at reduced supply. Then apply statistical projection to derive a high-confidence worst-case drift. However, this approach is costly and time-consuming.

The other approach is to derate based on known guaranteed specifications.

Similar to derating the input offset voltage as described in above, the supply rejection ratio provides a good indicator of the behavior of the input offset drift characteristic at reduced supplies. Worst-case offset drift can be calculated based on the guaranteed initial V_{OS} @ 25°C assuming it is at one polarity drifting to the opposite polarity of the data sheet's guaranteed maximum V_{OS} error due to temperature plus reduced supply voltages. This is shown in Figure 4.23 for the OP-177G.

DERIVING INPUT OFFSET VOLTAGE DRIFT AT REDUCED SUPPLY VOLTAGES

■ Example: OP-177G @ -40°C To +85°C, V_S Reduced From ±15V To ±5V

Initial V_{OS} (@ 25 C) = 60µV

Total V_{OS} (over temp):
Maximum V_{OS} = 100µV
PSRR (106dB) Error = 100µV
_____
200µV

Worst-Case V_{OS} Drift = (60µV + 200µV) / 65°C
(+25°C To -40°C) = 4µV/°C

Figure 4.23

The above worst-case analysis assumes that the drift is linear, although in reality it is almost never linear over the entire temperature range. However, the nonlinear behavior generally is not radical enough to significantly affect the worst-case estimate.

NOISE INCREASES AS SUPPLY VOLTAGES DECREASE

As the supply voltages decrease, the corresponding reduction in supply current causes the op amp's input stage current to decrease. The consequence of it is the input voltage noise tends to increase.

How much the voltage noise increases is difficult, if not impossible, to predict as usually no information is given to indicate its noise level as a function of the supply voltage. Furthermore, one cannot assume the input stage current is linearly proportional to the total supply current, and hence provide a reliable prediction of the current noise level.

The best way is to measure the noise voltage at the supplies that one intends to operate. A simple voltage noise test circuit is shown in Figure 4.24 below.

VOLTAGE NOISE TEST CIRCUIT AT REDUCED SUPPLIES
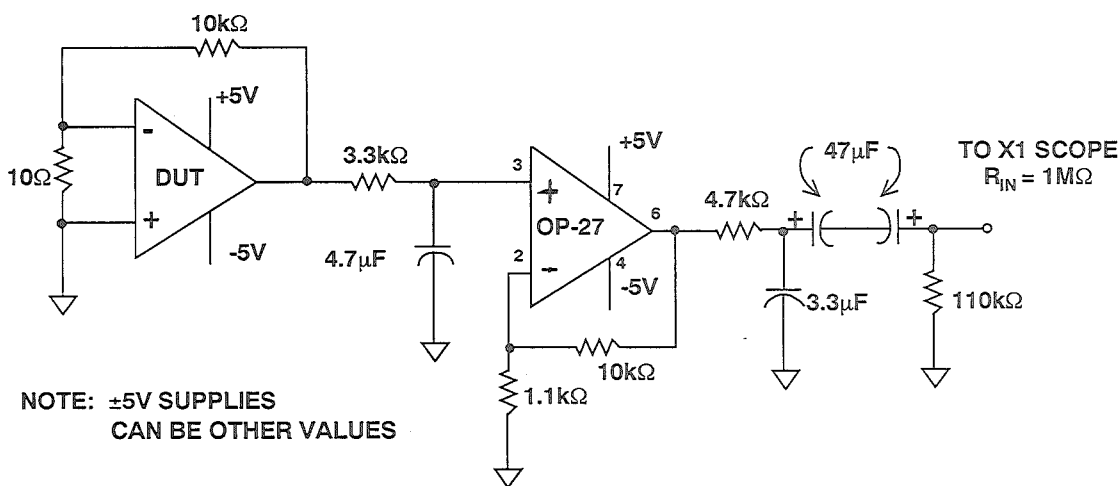## 0.1Hz TO 10Hz
VOLTAGE GAIN = 10,000

Figure 4.24

Be aware that the DUT stage has a gain of 1,000. If the op amp under test has an offset voltage more than 200 μV, it may be enough to drive one or both op amp stages into saturation. In that case, an erroneously low noise will be measured at the output. High offset op amps can be measured by reducing the D.U.T. stage's feedback resistance from 10 kΩ to 2 kΩ. In which case, the test circuit can accommodate op amps that have up to 1 mV offset.

REDUCED BANDWIDTH AND SLEW RATE

All AC parameters tend to get worse with reduced supply voltages. Most notable are bandwidth and slew rate. That is because the op amp's supply currents tend to decrease, pushing the internal transistors' operating points lower. Some op amp data sheets do show AC characteristic curves or have specifications at lower supply voltages. This is usually true for single supply op amps as they are specifically designed for low voltage operations.

However, most precision op amps that are designed for ±15V do not offer much AC information at reduced supplies. Consequently, one must measure these performance characteristics at the appropriate voltages.

Generally most precision measurement applications do not call for any stringent bandwidth or slew rate performance. In fact, a reduced bandwidth may provide built-in noise band filtering.

LOW SUPPLY CURRENT INCREASES NOISE

Most single supply op amps are designed to draw low supply current, at the expense of having higher voltage noise. This tradeoff may be necessary because the system must be powered by a battery. However, this condition is worsened because all circuit resistances tend to be higher. As a result, in addition to the op amp's voltage noise, Johnson noise (resistor thermal noise) is also a significant contributor to the total noise of the system.

The choice of monolithic op amps that combine the characteristics of low noise and single supply operation is rather limited. Most single supply op amps have noise on the order of 30 to 60 nV/$\sqrt{Hz}$. On the other hand, a dual-supply, 5 nV/$\sqrt{Hz}$ op amp's input and output voltage ranges require at least a couple of volts from either supply rails.

In order to achieve both low noise and low supply voltage operation, discrete designs may provide the solution. The circuit in Figure 4.25 uses a rail-to-rail op amp (OP-295) and a discrete PNP matched transistor pair (MAT-03) to achieve true zero-in / zero-out single supply operation with an input voltage noise of 3.1nV/$\sqrt{Hz}$ at 100 Hz. R_5 and R_6 yield a gain of 1000, making this circuit ideal for maximizing dynamic range when amplifying low level signal in single supply. The OP-295 provides rail-to-rail output swings allowing this circuit to operate with 0 to 5V outputs. Only half of the OP-295 is used leaving the other uncommitted op amp for use elsewhere.

A LOW NOISE SINGLE SUPPLY PREAMPLIFIER

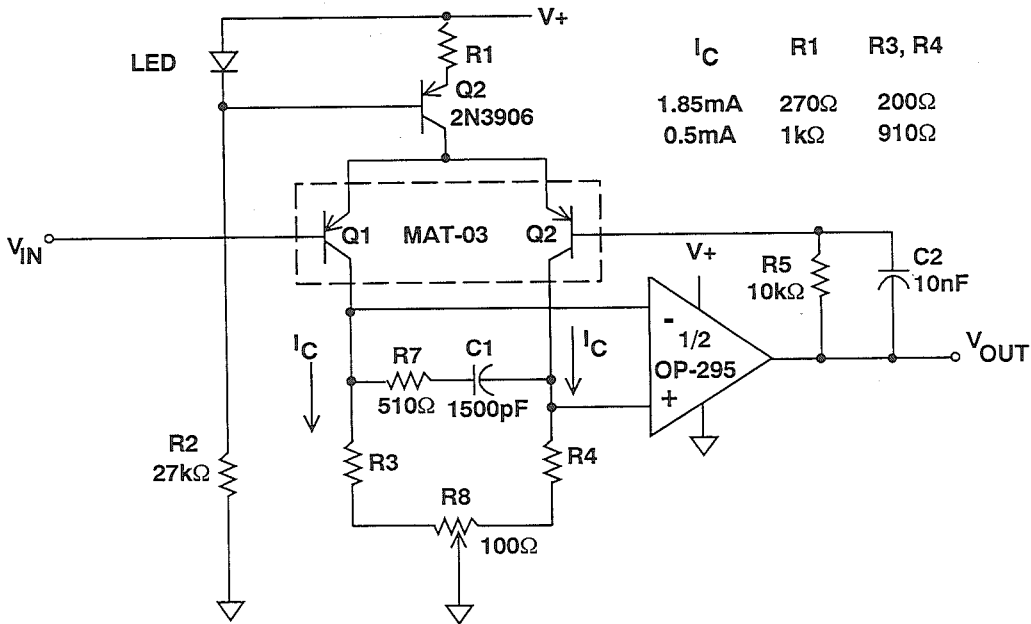| I_C	R1	R3, R4
1.85mA	270Ω	200Ω
0.5mA	1kΩ	910Ω

Figure 4.25

The input noise is controlled by the MAT-03 transistor pair and its collector current level. Increasing the collector current reduces the voltage noise. This particular circuit was tested with 1.85 mA and 0.5 mA of current. Under these two cases, the input voltage noise measured 3.15nV/$\sqrt{Hz}$ and 8.6 nV/$\sqrt{Hz}$ at 100Hz, respectively. The high collector currents lead to higher supply current consumption, higher input bias current, and higher current noise. For example, the MAT-03's typical h_{FE} of 165 produces bias currents of 11 μA and 3 μA, respectively. Based on the high bias currents, this circuit is best suited for applications requiring low source impedances, such as magnetic pick-ups or low impedance strain gauge sensors. In addition, high source impedance will degrade the noise performance. For example, a 1 kΩ resistor generates 4nV/$\sqrt{Hz}$ of broadband noise, which is already greater than the preamp by itself.

The collector current is set by R_1 in combination with the LED and Q2. The LED provides a 1.6V reference whose temperature coefficient closely matches that of Q2's base-emitter junction TC, thus producing a constant 1.0V drop across R_1. With R_1 equal to 270 Ω, the tail current is 3.7 mA, and the collector current is half that, or 1.85 mA. The value of R_1 can be altered to adjust the collector current.

Whenever R_1 is changed then R_3 and R_4 should also be adjusted. To maintain a common-mode input range that includes ground, the collectors of Q1 and Q2 should not go above 0.5V, otherwise they could saturate. Thus R_3 and R_4 have to be small enough to prevent this condition. Their values and the overall performance for two different values of R_1 are summarized in Figure 4.26.

Lastly, the potentiometer R_8 is needed to null the offset voltage to zero. Similar performance can be obtained using an OP-90 as the output amplifier with a savings of about 185 μA of supply current. However, the output swing will not include the positive rail, and the bandwidth will reduce to approximately 250 Hz.

SINGLE SUPPLY LOW NOISE
PREAMP PERFORMANCE

	$I_C = 1.85mA$	$I_C = 0.5mA$
R1	270Ω	$1.0k\Omega$
R3,R4	200Ω	910Ω
e_n @ 100Hz	$3.15nV/\sqrt{Hz}$	$8.6nV/\sqrt{Hz}$
e_n @ 10Hz	$4.2nV/\sqrt{Hz}$	$10.2nV/\sqrt{Hz}$
I_{SY}	4.0mA	1.3mA
I_B	$11\mu A$	$3\mu A$
Bandwidth	1kHz	1kHz
Closed Loop Gain	1000	1000

Figure 4.26

OUTPUT DRIVE CAPABILITY LIMITED

Low power op amps typically operate on very low levels of quiescent stage currents. Consequently, their output transistors' base drive is usually small. As a result, the output drive capability is limited as well. Typical low power op amps can handle several milliamps before the output transistor becomes base-current starved. Most will limit at about 10 mA.

Indeed, low power op amps are primarily designed for applications that conserve power, and therefore are not often called upon to deliver much current. Output voltage swing is usually much more of a concern.

HIGH CIRCUIT IMPEDANCES ARE SUSCEPTIBLE TO NOISE PICKUP

Since low power circuits tend to use high value resistors to conserve power, this tends to make the circuit more susceptible to externally induced radiated noise and conducted noise. Even a small amount of parasitic capacitance can create a significant conduction path for noise to penetrate.

For example, as little as 1 pF of parasitic capacitance allows a 5V logic transition to cause a large disturbance in a $100k\Omega$ circuit as illustrated in Figure 4.27.

HIGH CIRCUIT IMPEDANCES INCREASE SUSCEPTIBILITY TO NOISE PICKUP

C_S = 1pF STRAY
CAPACITANCE

VERT. SCALE: 5V/DIV (TOP)
20mV/DIV (BOTTOM)
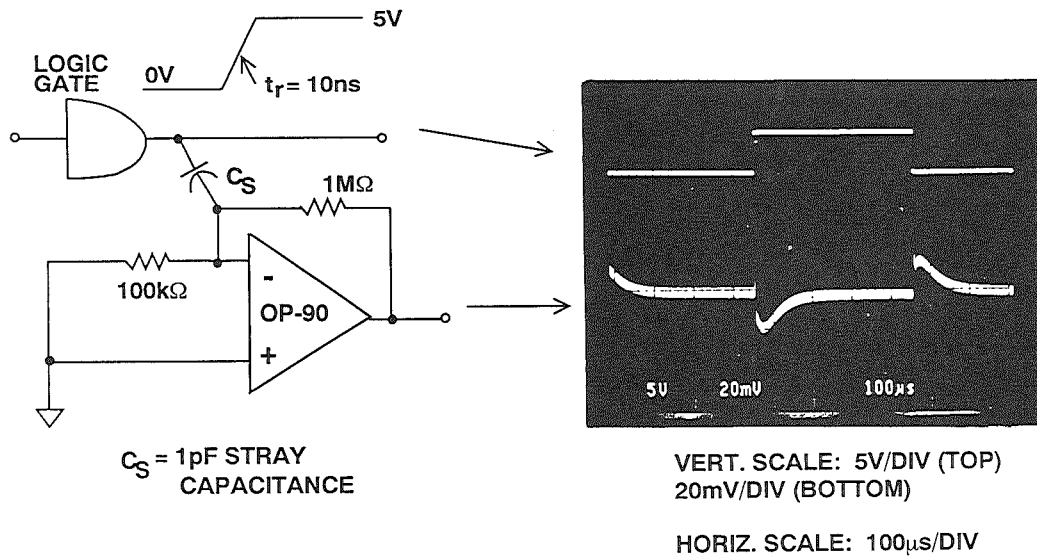
HORIZ. SCALE: 100μs/DIV

Figure 4.27

   This serves to illustrate that high impedance circuits are full of potential parasitics which can cause a good paper design to perform poorly when actually implemented. One needs to pay particular attention to the routing of signals. Interestingly, many high-frequency layout techniques for eliminating parasitics can also be applied here for low frequency, low power circuits — for different reasons. While circuit parasitics cause unwanted phase shifts and instabilities in high frequency circuits, the same parasitics pick up unwanted noise in low power precision circuits.

CIRCUIT LAYOUT GUIDELINES TO MINIMIZE NOISE PICKUP PROBLEMS

■ Keep Circuit Trace Interconnection Short

■ Keep Circuit Compact

■ Keep Summing Junction Component Leads Short

■ Bypass Power Supplies

■ Keep Digital Circuit Traces Away From Analog Circuits

■ Use Single Point Ground Where Possible

Figure 4.28

## HOW TO POWER ANALOG CIRCUITS USING A +5V LOGIC SUPPLY

Since +5V is ubiquitous and universally available in every system, we are constantly tempted to use it to power analog circuits. With a bit of sound engineering and careful filtering, there is no reason why this cannot be accomplished in most cases.

The first mistake often made is to tap the supply close to the logic circuit, usually because of convenience, without re-routing the supply connections. The problem starts when the fast logic transition edges induce high current pulses which last nanoseconds to sub-nanoseconds. With the logic circuits located some distance away from the supply, as little as a few inches of conductor can have significant resistance and inductance allowing the current pulse to generate several 100 millivolts of voltage glitches.

These spikes usually permeate throughout the logic circuit's ground and the supply lines. Figure 4.29 shows what a typical computer system's +5V supply at the logic circuit looks like with all the noise riding on it. Tapping the logic supply at this point will corrupt the analog circuits with unwanted high frequency spike noise. Much of this noise is not common-mode (same amplitude and phase) to the supply and ground lines. Therefore, the analog circuit cannot reject it easily. Filtering them becomes very difficult.

DO NOT USE +5V LOGIC SUPPLIES
TO POWER ANALOG CIRCUITS
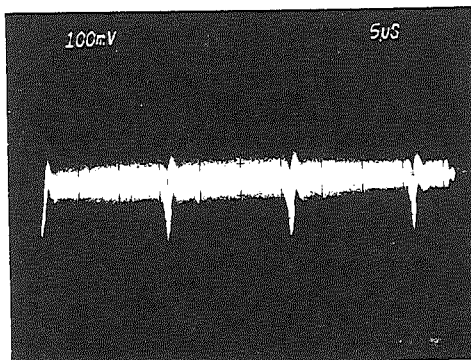
VERTICAL SCALE: 100mV / div.
HORIZONTAL SCALE: 5μs / div.

Figure 4.29

DIFFERENTIAL LC FILTER TURNS NOISY LOGIC
SUPPLIES INTO NOISE-FREE ANALOG SUPPLIES

Ferrite Beads: 2 Turns, Fair-Rite #2677006301   +5V

TTL/CMOS
LOGIC
CIRCUITS

100μF
ELECT.

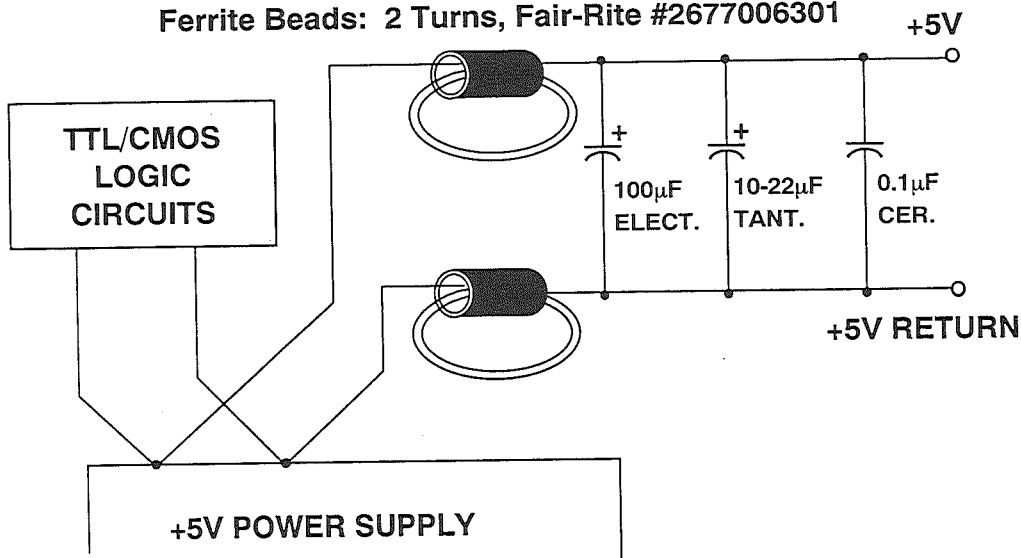10-22μF
TANT.

0.1μF
CER.

+5V RETURN

+5V POWER SUPPLY

Figure 4.30

However, glitch noise directly at the power supply output is usually much less than it is directly at the noisy logic circuit interface. However, some glitch noise may still be present directly at the power supply output, not due to the logic circuit noise, but because of the power supply's high energy switching circuit (typical of a switching power supply). For these reasons, all analog circuits should be powered directly from the power supply outputs using appropriate filtering between the power supply output and the analog circuits. A clean, analog-grade supply can be generated from a +5V logic supply using a differential LC filter with separate power supply and return lines as shown in Figure 4.30.

The supply output is virtually free of any glitch noise as evident in the scope photo in Figure 4.31, which compares the input and output sides of the filter. All capacitors used were selected from commonly available types. Lower noise can be attained using low ESR (Equivalent Series Resistance) type electrolytic and tantalum capacitors.

The circuit as shown can easily handle 100 mA of load current without the risk of saturating the ferrite core. Higher current capacity can be designed using correspondingly larger ferrites. The same or similarly valued circuit can also be used for higher supply voltages such as +12V and +15V.

4

(Note: The ferrite beads shown in Figure 4.30 are manufactured by Fair-Rite Products, P.O. Box J, Wallkill, NY, 12589)

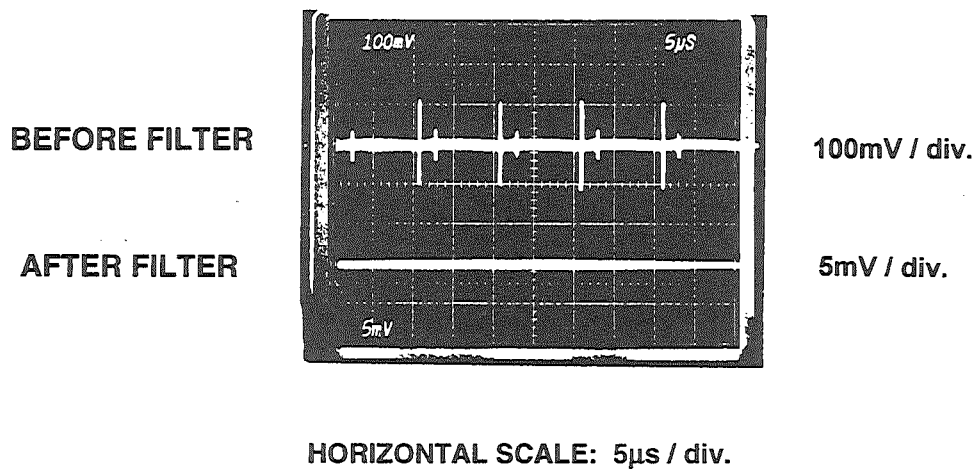## LC FILTER VIRTUALLY ELIMINATES ALL GLITCH NOISE

BEFORE FILTER   100mV / div.

AFTER FILTER   5mV / div.

HORIZONTAL SCALE: 5µs / div.

Figure 4.31

+3V SUPPLY OPERATION?

The current trend is for systems to move from +5V supply to +3V supply in order to accommodate higher speed logic circuits at reduced levels of power consumption. Actual implementations have so far been confined to certain specific applications such as camcorders, cellular communications, etc. Although these applications are relatively few in comparison to other applications for low supply amplifiers, they are growing and increasing in popularity. Perhaps in the future, +3V operation for analog circuits will become an important requirement.

Going to +3V or less will narrow op amp and component selection even further. All the above design considerations and tradeoffs will become more complex.