SECTION III
HIGH IMPEDANCE, LOW CURRENT APPLICATIONS

- Precision Photodiode Preamplifier Design Analysis: Photodiode Characteristics, DC Analysis, AC Analysis, Noise Analysis, Circuit Tradeoffs, "T" Network Analysis

- High Speed Photodiode Preamplifiers: Characteristics of High Speed Photodiodes, Determining Circuit Frequency Response, Selecting the Proper Op Amp, Noise Analysis, Achieving More Bandwidth by Using Two Stages, Using a Composite Amplifier to Increase the Gain Bandwidth Product, High Speed Fiber Optic Receivers

- Other High Impedance Transducer Applications: A pH Probe Buffer Amplifier, High Impedance Charge Output Transducers, Accelerometer Amplifiers, Hydrophone Amplifiers, Op Amp Performance: JFET Versus Bipolar, Using Decompensated Op Amps as I/V Converters, A High Performance Audio I/V Converter

SECTION III

HIGH IMPEDANCE, LOW CURRENT APPLICATIONS

WALT KESTER, SCOTT WURCER, CHUCK KITCHIN

PRECISION PHOTODIODE PREAMPLIFIER CIRCUIT ANALYSIS

WALT KESTER

In this portion of the seminar we will conduct a detailed design analysis of a precision photodiode preamplifier circuit. This particular application was chosen because it illustrates most of the key points which must be considered when dealing with precision low-noise op amps. The circuit designed is extremely useful in converting any precision low-level current into a voltage.

PHOTODIODE APPLICATIONS AND CHARACTERISTICS

Photodiodes generate a small current which is proportional to the level of illumination. They have many applications ranging from precision light meters to high-speed fiber optic receivers.

The equivalent circuit for a photodiode is shown in Figure 3.2. One of the standard methods for specifying the sensitivity of a photodiode is to state its short circuit photocurrent (I_{SC}) at a given light level from a well defined light source. The most commonly used source is an incandescent tungsten lamp running at a color temperature of 2850K. At 100 fc (foot-candles) illumination (approximately the light level on an overcast day), the short circuit current is usually in the picoamps to hundreds of microamps range for small area (less than $1mm^2$) diodes.

PHOTODIODE APPLICATIONS

- Optical: Light Meters, Auto-Focus, Flash Controls
- Medical: CAT Scanners (X-Ray Detection), Blood Particle Analyzers
- Automotive: Headlight Dimmers, Twilight Detectors
- Communications: Fiber Optic Receivers
- Industrial: Bar Code Scanners, Position Sensors, Laser Printers

Figure 3.1

PHOTODIODE EQUIVALENT CIRCUIT

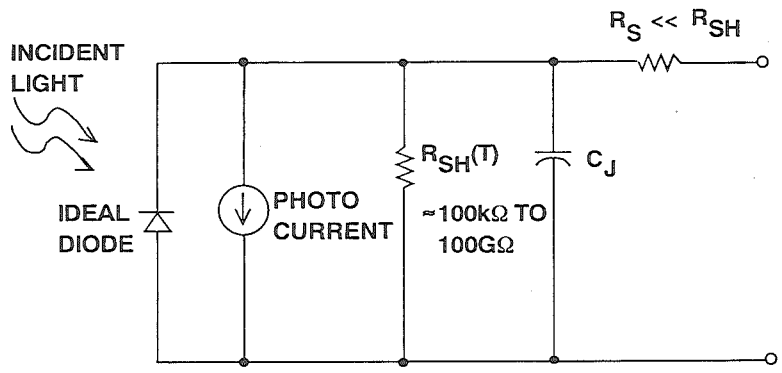
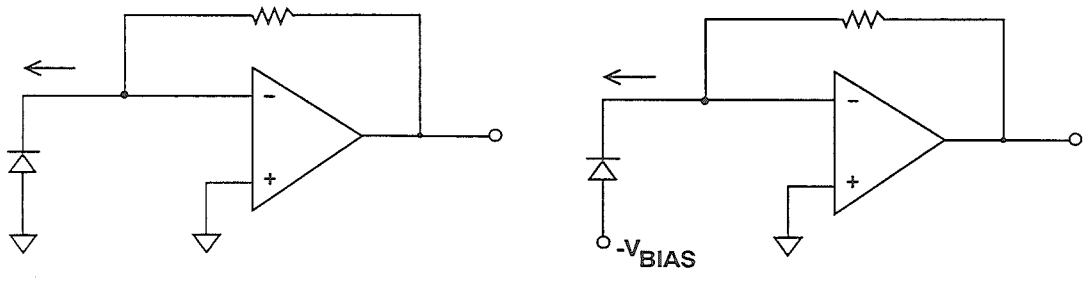


Figure 3.2

PHOTODIODE MODES OF OPERATION



PHOTOVOLTAIC

- Zero Bias
- No Dark Current
- Precision Applications
- Low Noise (Johnson)

PHOTOCONDUCTIVE

- Reverse Bias
- Dark Current Exists
- High Speed Applications
- Higher Noise (Johnson + Shot)

Figure 3.3

The short circuit current is very linear over 6 to 9 decades of light intensity, and is therefore often used as a measure of absolute light levels. The open circuit forward voltage drop across the photodiode varies logarithmically with light level, but, because of its large temperature coefficient, the diode voltage is seldom used as an accurate measure of light intensity.

The shunt resistance is usually in the order of 1000MΩ at room temperature, and decreases by a factor of 2 for every 10°C rise in temperature. Diode capacitance is a function of junction area and the diode bias voltage. A value of 50pF at zero bias is typical for small area diodes.

Photodiodes may either be operated with zero bias (*photovoltaic* mode) or reverse bias (*photoconductive* mode) as shown in Figure 3.3. The most precise linear operation is obtained in the photovoltaic mode, while higher switching speeds are realizable when the diode is operated in the photoconductive mode. Under reverse bias conditions, a small amount of current called *dark current* will flow even when there is no illumination. There is no dark current in the photovoltaic mode. In the photovoltaic mode, the diode noise is basically the thermal noise generated by the shunt resistance. In the photoconductive mode, shot noise due to conduction is an additional source of noise. Photodiodes are usually optimized during the design process for use in either the photovoltaic mode or the photoconductive mode, but not both.

Figure 3.4 shows the photosensitivity for a small photodiode (Silicon Detector Part Number SD-020-12-001), and specifications for the diode are summarized in Figure 3.5.

SHORT CIRCUIT CURRENT VERSUS LIGHT INTENSITY FOR PHOTODIODE (PHOTOVOLTAIC MODE)

ENVIRONMENT	ILLUMINATION (fc)	SHORT CIRCUIT CURRENT
Direct Sunlight	1000	30μA
Overcast Day	100	3μA
Twilight	1	0.03μA
Full Moonlit Night	0.1	3000pA
Clear Night / No Moon	0.001	30pA

Figure 3.4

PHOTODIODE SPECIFICATIONS
Silicon Detector Part Number SD-020-12-12-001

- Area: 0.2mm^2
- Capacitance: 50pF
- Shunt Resistance at 25°C: 1000 megohms
- Maximum Linear Output Current: 40mA
- Response Time: 12ns
- Photosensitivity: 0.03μA / fc

Figure 3.5

PHOTODIODE PREAMP CIRCUIT CONSIDERATIONS

A convenient way to convert the photodiode current into a usable voltage is to use an op amp as a current-to-voltage converter as shown in Figure 3.6. The diode bias is maintained at zero volts by the virtual ground of the op amp, and the short circuit current is converted into a voltage. If we wish to operate at maximum sensitivity, we must be able to detect a diode current of 30pA. This implies that the feedback resistor must be very large. For example, 1000MΩ will yield a corresponding voltage of 30mV for this amount of current. Larger resistor values are impractical, so we will use 1000MΩ for the most sensitive range. This will give an output voltage range of 10mV for 10pA of diode current and 10V for 10nA of diode current. This yields a range of 60dB. For higher values of light intensity, the gain of the circuit must be reduced by using a smaller feedback resistor. For this range of maximum sensitivity, we should be able to easily distinguish between the light intensity on a clear moonless night (0.001fc) and that of a full moon (0.1fc)!

Notice that we have chosen to get as much gain as possible from one stage, rather than cascading two stages. This is in order to maximize the signal-to-noise ratio (SNR). If we halve the feedback resistor value, the signal level decreases by a factor of 2, while the noise due to the feedback resistor (Noise Voltage = $\sqrt{4kTR \cdot \text{Bandwidth}}$) decreases by only $\sqrt{2}$. This reduces the SNR by 3dB, assuming the closed loop bandwidth remains constant. Later in the analysis, we will see that the resistors are one of the largest contributors to the overall output noise.

SIMPLIFIED OP-AMP CURRENT-TO-VOLTAGE CONVERTER

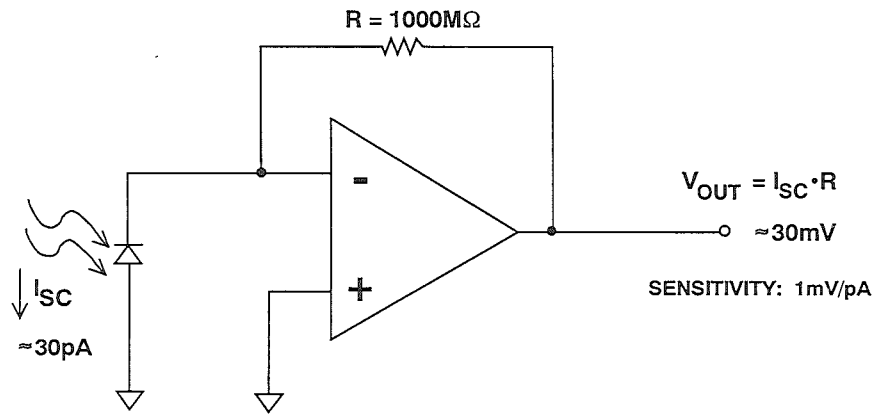


Figure 3.6

PRECAUTIONS FOR PICOAMPERE CIRCUITS

Since the diode current is measured in terms of picoamperes, extreme attention must be given to potential leakage paths in the actual circuit. Two parallel conductor stripes on a high-quality well-cleaned epoxy-glass PC board 0.05 inches apart running parallel for 1 inch have a leakage resistance of approximately 10^{11} ohms at +125°C (Reference 4, p.293). If there is 15 volts between these runs, there will be a current flow of 150pA.

The critical leakage paths for the photodiode circuit are enclosed by the dotted lines in Figure 3.7. The feedback resistor should be thin film on ceramic or glass with glass insulation. The compensation capacitor across the feedback resistor should have a polypropylene or polystyrene dielectric. All connections to the summing junction should be kept short. If a cable is used to connect the photodiode to the preamp, it should be kept as short as possible and have Teflon insulation.

Guard rings (on both sides of the PC board) should be used around the inverting input pin of the op amp as shown in Figure 3.8. The case ground of the op amp (usually Pin 8) should also be connected to the grounded guard ring. Maintaining the guard ring potential the same as the inverting input potential minimizes any leakage current due to PC board resistance.

Ideally, all connections to the summing input of the op amp should be made to a virgin Teflon standoff insulator ("Virgin" Teflon is a solid piece of new Teflon material which has been machined to shape and has not been welded together from powder or grains). If mechanical and manufacturing considerations allow, the inverting input pin of the op amp should be soldered directly to the Teflon standoff

LEAKAGE CURRENT PATHS

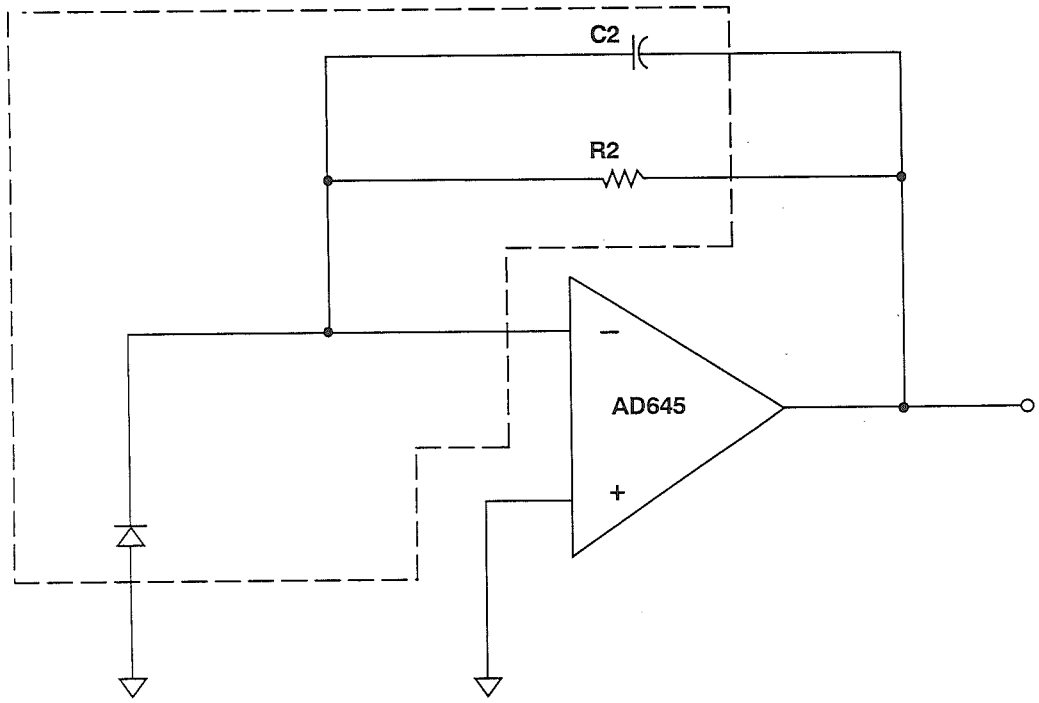
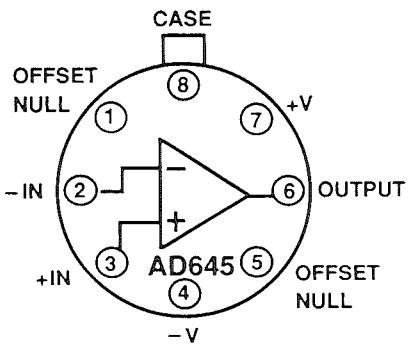


Figure 3.7

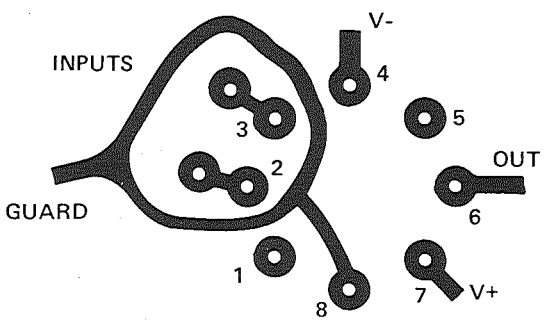
PC BOARD LAYOUT FOR GUARDING TO-99 PACKAGE

TOP VIEW



NOTE: CASE IS CONNECTED TO PIN 8

BOTTOM VIEW



SAME PATTERN SHOULD BE LAID OUT ON BOTH SIDES OF P.C. BOARD

Figure 3.8

(see Figure 3.9) rather than going through a hole in the PC board. The PC board itself must be cleaned carefully and then sealed against humidity and dirt using a high quality conformal coating material.

In addition to minimizing leakage currents, the entire circuit should be well shielded with a grounded metal shield to prevent stray signal pickup. Details regarding proper grounding, shielding, and noise reduction techniques are given in References 8 and 9 at the end of this section.

A VIRGIN TEFLON STANDOFF INSULATOR HAS MUCH LOWER LEAKAGE THAN A PCB TRACK

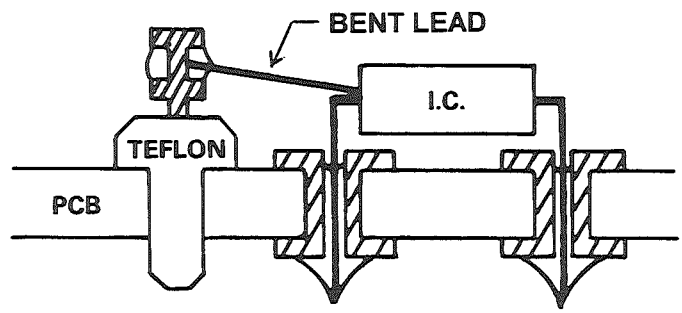


Figure 3.9

AMPLIFIER SELECTION AND DC CIRCUIT ANALYSIS

If we wish to accurately measure photodiode currents in the tens of picoamps range, the bias current of the op amp should be no more than a few picoamps. This narrows the choice considerably. The industry-standard AD OP-07 is an ultra-low offset voltage (10μV) bipolar op amp , but its bias current is 4nA (4000pA!). Even super-beta bipolar op amps with bias current compensation (such as the AD OP-97) have bias currents of 100pA at room temperature. For this reason, an FET-input electometer-grade op amp such as the AD645 is required for our photodiode preamp. The AD645 utilizes a BiFET process in conjunction with laser wafer trimming to achieve the specifications shown in Figure 3.10.

AD645 BiFET OP AMP KEY SPECIFICATIONS

- Offset Voltage: 250μV Maximum at 25°C
- Offset Voltage Drift: 1μV/°C Maximum (C Grade)
- Input Bias Current: 1.5pA at 25°C
- 2.5μV p-p Noise, 0.1Hz to 10Hz
- 20nV/$\sqrt{Hz}$ Noise at 100Hz
- 11fA p-p Current Noise, 0.1Hz to 10Hz
- 0.6fA/$\sqrt{Hz}$ Current Noise at 20kHz
- 90mW Power Dissipation at ± 15V
- 1MHz Gain Bandwidth Product

Figure 3.10

ANALYSIS OF OUTPUT DC OFFSET VOLTAGE AND DRIFT

The general offset voltage and bias current model for an op amp is shown in Figure 3.11. This model can be modified as needed to fit any particular application circuit which uses an op amp either in the inverting or the non-inverting mode. In our example, R_p=0, R_2=1000MΩ, and R_1=photodiode shunt resistance. Unfortunately, the diode shunt resistance is a function of temperature (halves every 10°C rise) which complicates our analysis somewhat.

At this point, we need to define the *noise gain* of our circuit. The noise gain is the gain the amplifier circuit presents to the input offset voltage and the input noise voltage. For dc, its value is $1 + R_2/R_1$. Noise gain must be distinguished from *signal gain*! In the inverting mode, the signal gain of an op amp for dc is $-R_2/R_1$. In the non-inverting mode, the signal gain is $1 + R_2/R_1$. In both cases, the noise gain is $1 + R_2/R_1$.

In our example, since R_1 is a function of temperature, the noise gain will also be a function of temperature. In fact, at -25°C the noise gain is 1.03, while at +85°C it increases to 64.7 (corresponding to R_1 going from 31,920MΩ to 15.7MΩ).

All the individual dc error sources and their sum are shown in Figure 3.12. This curve assumes a room temperature offset voltage of 0.250mV, a temperature coefficient of 1μV/°C, and a room temperature

bias current of 1.5pA. The majority of the output voltage drift comes from the effects of the op amp bias current which, even though it is very low at room temperature (1.5pA), nevertheless, doubles for every 10°C rise in temperature (at +85°C, the bias current is 96pA). For this reason, every attempt should be made to minimize the self-heating of the op amp. An adequate heatsink should be used to minimize the junction temperature rise above ambient, and output loading should also be minimal to prevent increased chip power dissipation due to load current. In the next sections we will explore several methods to improve the dc drift over temperature.

OFFSET VOLTAGE AND BIAS CURRENT MODEL

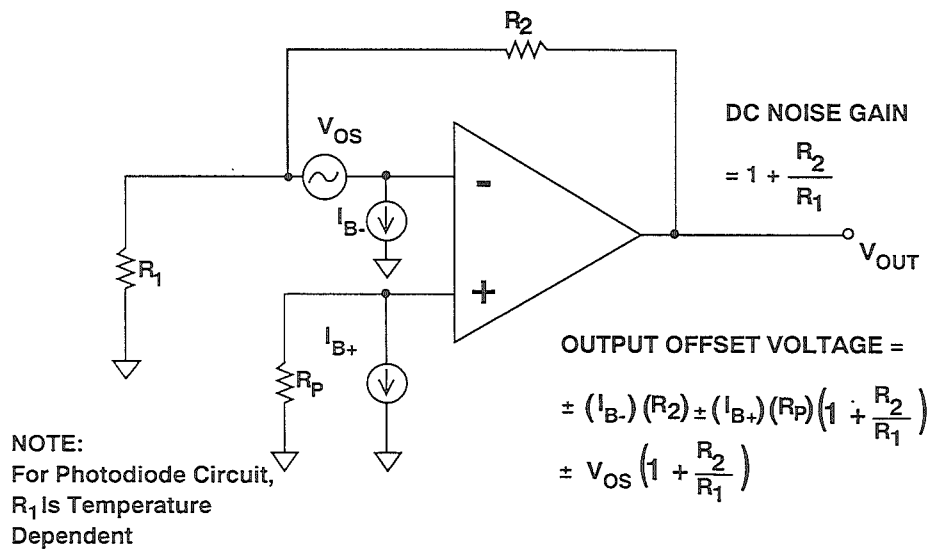


Figure 3.11

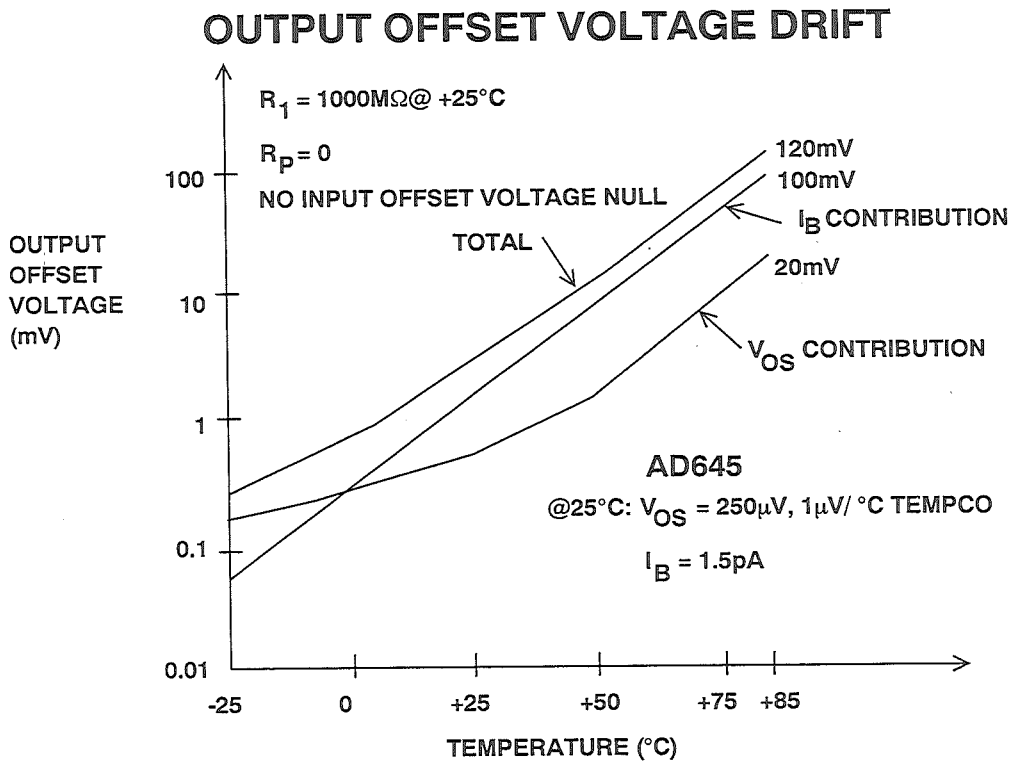


Figure 3.12

BIAS CURRENT COMPENSATION

In circuits where R_1 is a constant value and where $I_{b+} \approx I_{b-}$ (i.e. the offset current is low), the effects of bias current on the output voltage offset can be cancelled by inserting a resistor in the non-inverting input whose value is equal to the parallel combination of R_1 and R_2. This is shown in Figure 3.13. Normal practice is to bypass this resistor with a capacitor so that the resistor noise is not multiplied by the noise gain and combined with the output noise. This scheme works very well for bipolar op amps where the input bias currents tend to be well matched. FET-input devices have the lowest bias currents, although on a percentage basis, their offset currents are not as low as those of bipolar devices. Their input and offset currents are, however, low enough in absolute level that in many circuits they do not need bias-current compensation. A disadvantage of FET-input devices is the temperature dependence of bias current, which roughly doubles for every 10°C of temperature rise. If very high operating temperatures are required, this characteristic tends to defeat their low-input-current superiority somewhat, although the degree to which this is true depends, of course, on the device and at how high a temperature one must operate it.

If we apply this bias current compensation technique to the photodiode circuit using the room temperature value of R_1 (1000MΩ) to calculate R_p, we find that R_p = 500MΩ (See Figure 3.14). If, however, we run through the calculations at +85°C, we find that R_1 = 15.7MΩ, Noise Gain = 64.7, I_b = 96pA, and the output offset voltage is 3V !! Also, the 96pA of bias current flowing through Rp develops a voltage of 48mV which appears across the photodiode. The effect of this voltage is to cause non-linearity in the diode response to light intensity.

INPUT BIAS CURRENT CANCELLATION

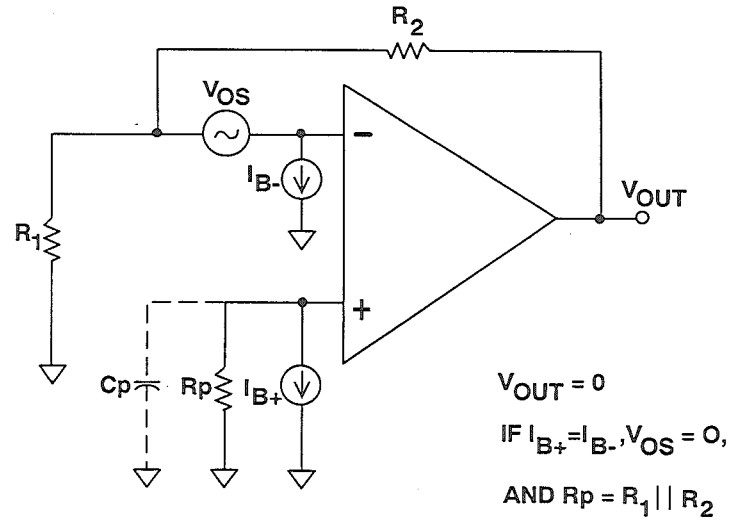


Figure 3.13

A BIAS CURRENT CANCELLATION DISASTER

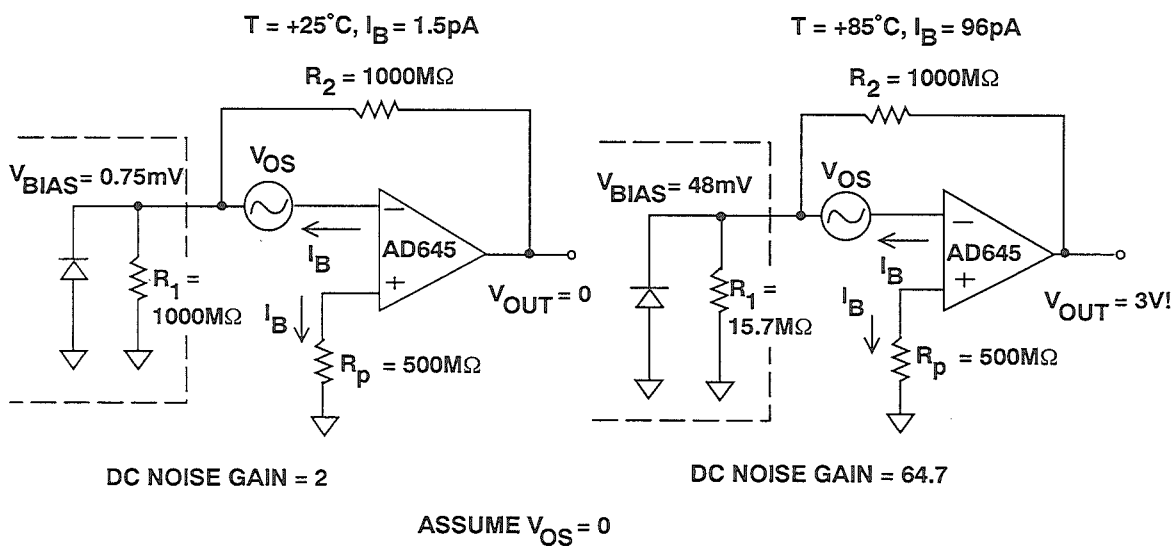


Figure 3.14

Rather than select Rp based on the room temperature value of R_1, it should be selected based on R_1's value at +85°C which is 15.7MΩ. For this value of R_1, R_p should be 15.4MΩ. Output voltage versus drift versus temperature is now improved over the case where $R_p = 0$. The small amount of bias voltage developed across the photodiode due to I_b flowing in R_p (1.5mV) is not sufficient to cause linearity problems. Figure 3.15 shows output voltage drift due to I_b with and without the compensating resistor.

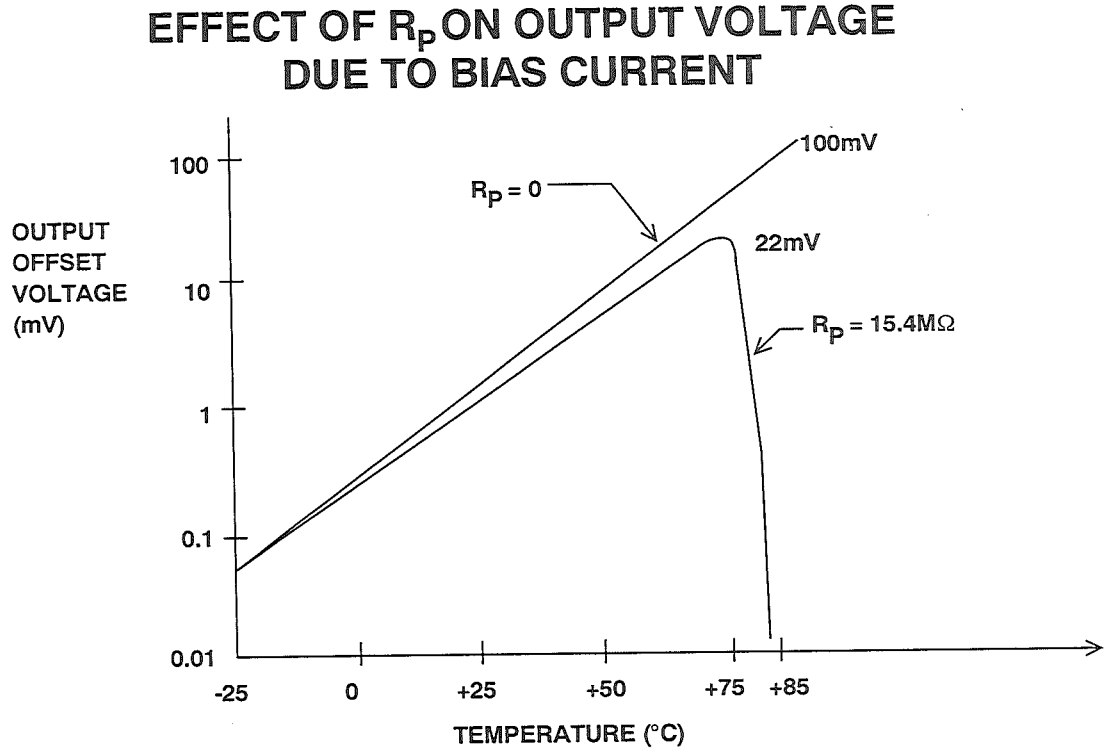


Figure 3.15

INPUT OFFSET VOLTAGE NULLING

Several techniques exist for nulling out the effects of the op amp input offset voltage. In the case of the AD645, the initial room temperature offset is only 250μV maximum. A simplified schematic of the input circuit for the AD645 is shown in Figure 3.16. The device is actively trimmed at the wafer level for both drift and room temperature offset. The devices are first probed at high temperature, and the offset voltage measured and recorded. The devices are probed a second time at room temperature, and the offset voltage is again measured and recorded. Based on the amount of offset shift, the currents in the input differential pair are then trimmed to minimize drift over temperature. Finally, the appropriate source resistor is trimmed for minimum input offset voltage.

One common method for nulling out the input offset voltage is to make use of an external potentiometer tied to the *offset null* pins of the op amp as shown in Figure 3.17. Unfortunately, this method of nulling will actually increase the temperature coefficient of offset voltage

BiFET OP AMP SIMPLIFIED INPUT CIRCUIT

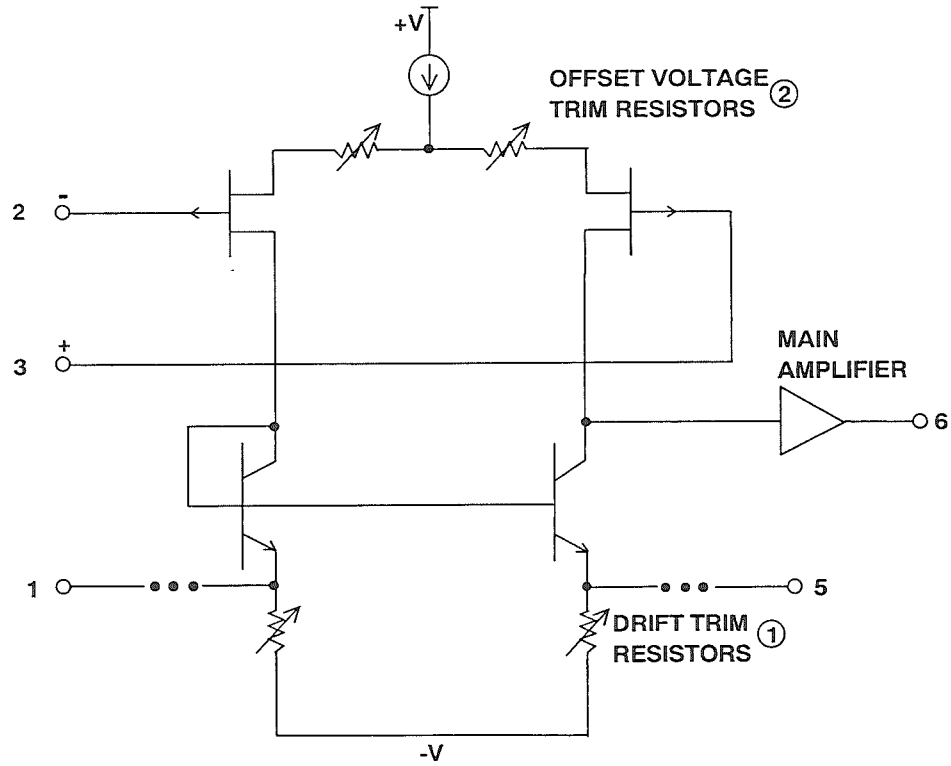
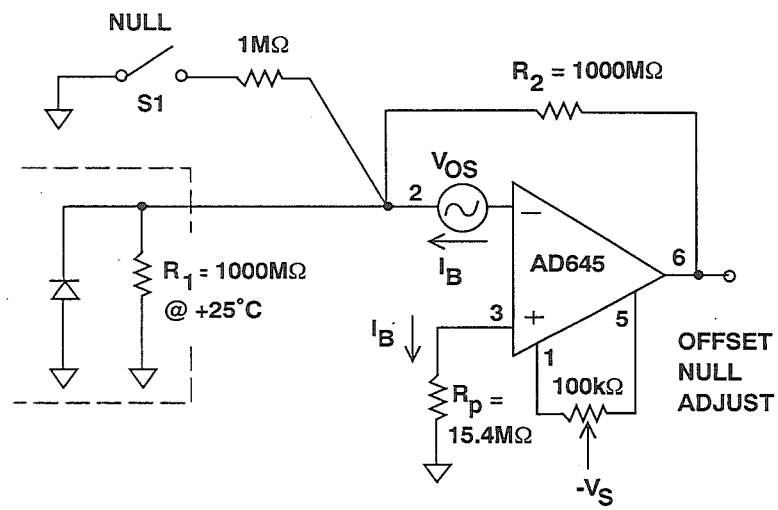


Figure 3.16

USING OFFSET VOLTAGE NULL PINS



- S1 ALLOWS V_{OS} NULL INDEPENDENT OF I_B
- V_{OS} TEMPCO INCREASES 4μV/°C/mV NULL

Figure 3.17

because the nulling is achieved by creating an imbalance in the differential input FET currents. Therefore, this method should be used with extreme caution and should only be used to null out the op amp input offset voltage and never for nulling out large system offset voltages. In the case of the AD645, the offset drift specification is 1μV/°C maximum with an input offset voltage specification of 0.250mV maximum. Nulling out the input offset voltage using the offset null pins will actually introduce an additional drift component of approximately 4μV/°C per millivolt of offset nulled. Therefore, nulling out 0.250mV of input offset will increase the temperature coefficient from 1μV/°C to 2μV/°C!!

The nulling procedure for the photodiode preamp circuit is complicated by effects of the output voltage offset due to the room temperature bias current (typically 1pA). The null for offset voltage should not correct for the nominal offset (2mV at the output) due to the 1pA input bias current. Otherwise, the amount of overcorrection introduced will be multiplied by the high noise gain at the high temperature. A method to null the offset voltage independently of the bias current is shown in Figure 3.18. The 1MΩ resistor is switched in before the offset voltage is nulled. This increases the noise gain to 1001. The relative effects of the input bias current on the output voltage are now negligible. After the null is accomplished, the 1MΩ resistor is switched out of the circuit.

Another method commonly used to null out the effects of input offset voltage is shown in Figure 3.18. In addition to creating leakage current problems in high impedance applications (such as the photodiode preamp) the extra summing resistor increases the dc noise gain of the circuit. A much preferred method for offset nulling is shown in Figure 3.19, where the offset is introduced across a small resistor which is inserted in the non-inverting input.

OFFSET VOLTAGE NULLING USING INVERTING INPUT

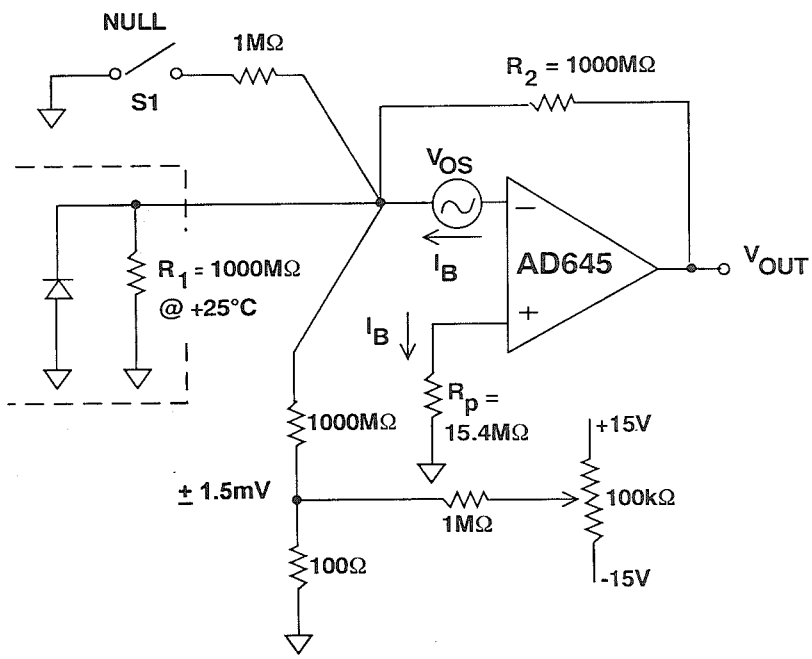


Figure 3.18

OFFSET VOLTAGE NULLING USING NON-INVERTING INPUT

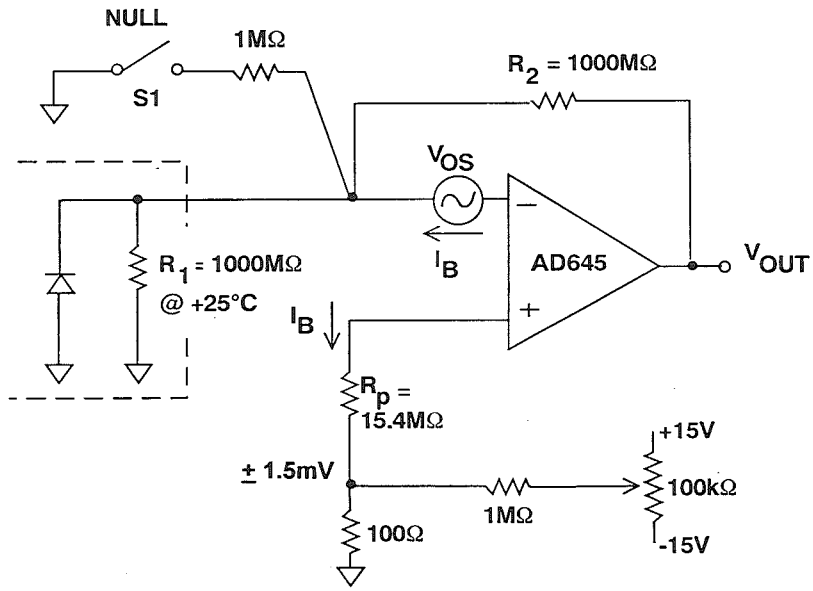


Figure 3.19

OUTPUT OFFSET VOLTAGE DUE TO V_{OS}

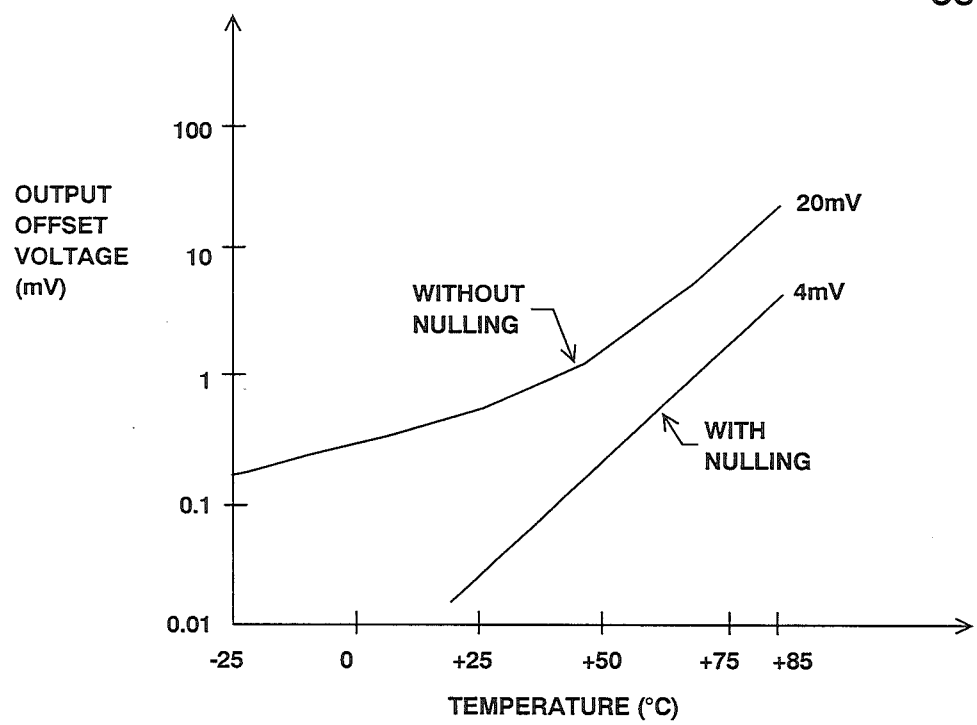


Figure 3.20

In applications where all the external feedback resistors are fixed, offset nulling (using the non-inverting input) will have no effect on the overall amount of output voltage drift over temperature. The amount of drift over temperature remains the same, but it is now centered about zero volts at room temperature. In the case of the photodiode circuit, however, where the diode shunt resistance (and hence the noise gain) is a function of temperature, offset nulling actually improves the drift characteristic as shown in Figure 3.20. This improvement is because the absolute value of the offset voltage over temperature has been reduced by the nulling process.

DC PERFORMANCE OF PHOTODIODE PREAMP

The final dc design for the photodiode preamp is shown in Figure 3.21. The resistor in the non-inverting input was chosen based on the high-temperature value of the diode shunt resistance, R_1. Performance of the final design is shown in Figure 3.22. The individual error components are shown as well as the total output error as a function of temperature. The total output voltage drift from -25 to +85°C is approximately 25mV.

THERMOELECTRIC VOLTAGES AS SOURCES OF INPUT OFFSET VOLTAGE

Thermoelectric potentials are generated by electrical connections which are made between different metals at different temperatures. For example, the copper PC board electrical contacts to the kovar input pins of an IC can create an offset voltage of 40μV/°C when the two metals are at different temperatures. Common lead-tin solder, when used with copper, creates a thermoelectric voltage of 1 to 3μV/°C. Special cadmium-tin solders are available that reduce this to 0.3μV/°C. (Reference 4, p. 127). The solution to this problem is to insure that the connections to the inverting and non-inverting input pins of the IC are made with the same material and that the PC board thermal layout is such that these two pins remain at the same temperature. In the case where a Teflon standoff is used as an insulated connection point for the inverting input (as in the case of the photodiode preamp), prudence dictates that connections to the non-inverting inputs be made in a similar manner to minimize possible thermoelectric effects.

FINAL DC DESIGN FOR PHOTODIODE PREAMP

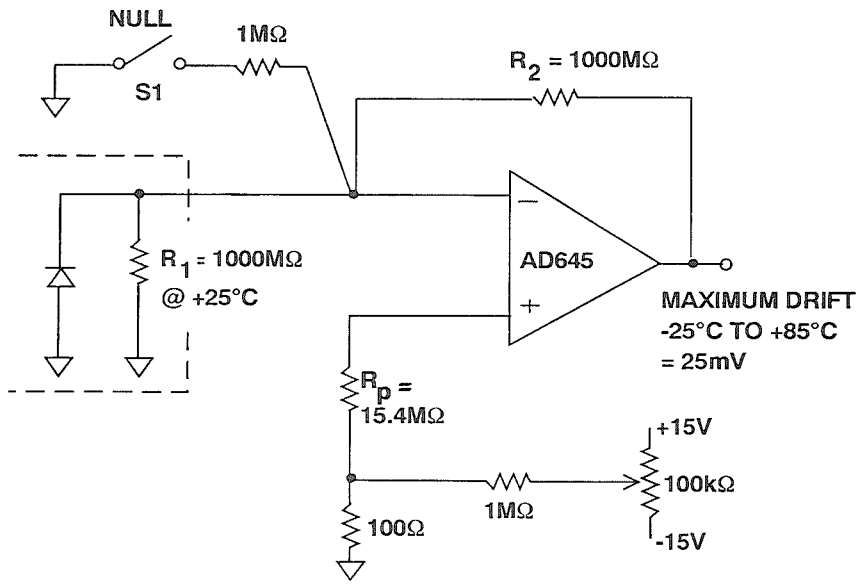


Figure 3.21

OUTPUT VOLTAGE OFFSET FOR FINAL DESIGN

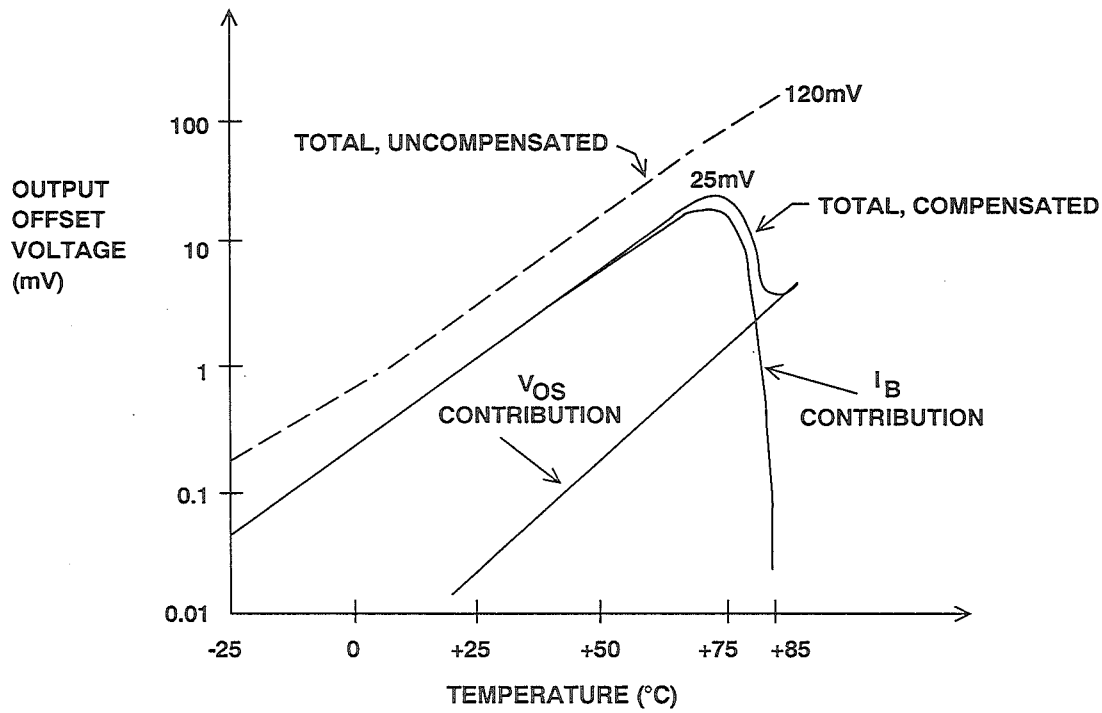


Figure 3.22

THERMOELECTRIC VOLTAGES AS SOURCES OF OP AMP INPUT OFFSET VOLTAGE

- **Different metals at Different Temperatures:**

  Copper/Kovar: 40μV/°C
  Copper/Lead-Tin Solder: 3μV/°C

- **Minimize Temperature Gradients Between Inverting and Non-Inverting Inputs**

- **Use Same Metals to Connect to Each Input**

Figure 3.23

AC DESIGN, BANDWIDTH, AND STABILITY

The important reactive elements of the photodiode circuit are shown in Figure 3.24. The bypass capacitor C_p is 0.1μF, and in parallel with R_p gives a cutoff frequency of $1/2\pi R_p C_p$ or 0.1Hz. For ac analysis purposes, therefore, it will be assumed that the non-inverting input of the op amp is grounded.

The key to the ac design is an understanding of the circuit Bode plot. A typical Bode plot for an op amp is shown in Figure 3.25. The definitions of each portion of the curve are given in Figure 3.26 (Reference 6, p. 24). The noise gain is the reciprocal of the feedback loop attenuation, β, where $\beta = Z_1/(Z_1 + Z_2)$. It should be noted that Z_1 and Z_2 may contain reactive elements, therefore, the noise gain may be a function of frequency.

Stability of the system is determined by the net slope of the noise gain and the open loop gain where they intersect. For unconditional stability, the noise gain curve must intersect the open loop response with a net slope of less than 12dB/octave (20dB per decade). The dotted line shows a noise gain which intersects the open loop gain at a net slope of 12dB/octave, indicating an unstable condition. This is what would occur in our photodiode circuit if there were no feedback capacitor (i.e. $C_2 = 0$).

The noise gain Bode plot for a generalized circuit is shown in Figure 3.27. A zero in the noise gain transfer function occurs at a frequency of $1/2\pi\tau_a$, where $\tau_a = R_1 \| R_2(C_1 + C_2)$. The pole of the transfer function occurs at a corner frequency of $1/2\pi\tau_2$, where $\tau_2 = R_2C_2$. The signal bandwidth is equal to the pole corner frequency. At low frequencies, the noise gain is $1 + R_2/R_1$. At high frequencies, it is $1 + C_1/C_2$.

REACTIVE PORTION OF PHOTODIODE CIRCUIT

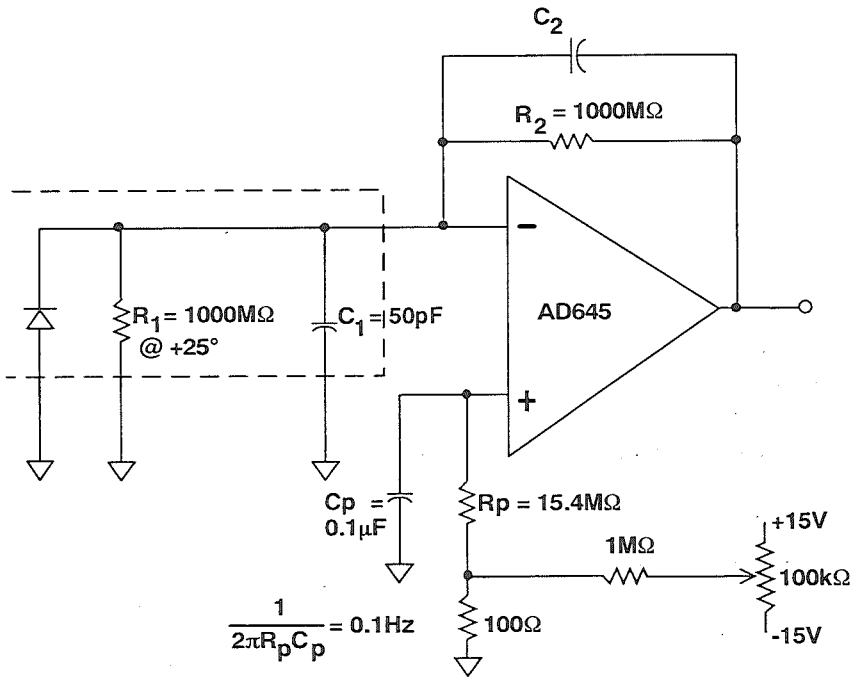


Figure 3.24

BODE PLOT

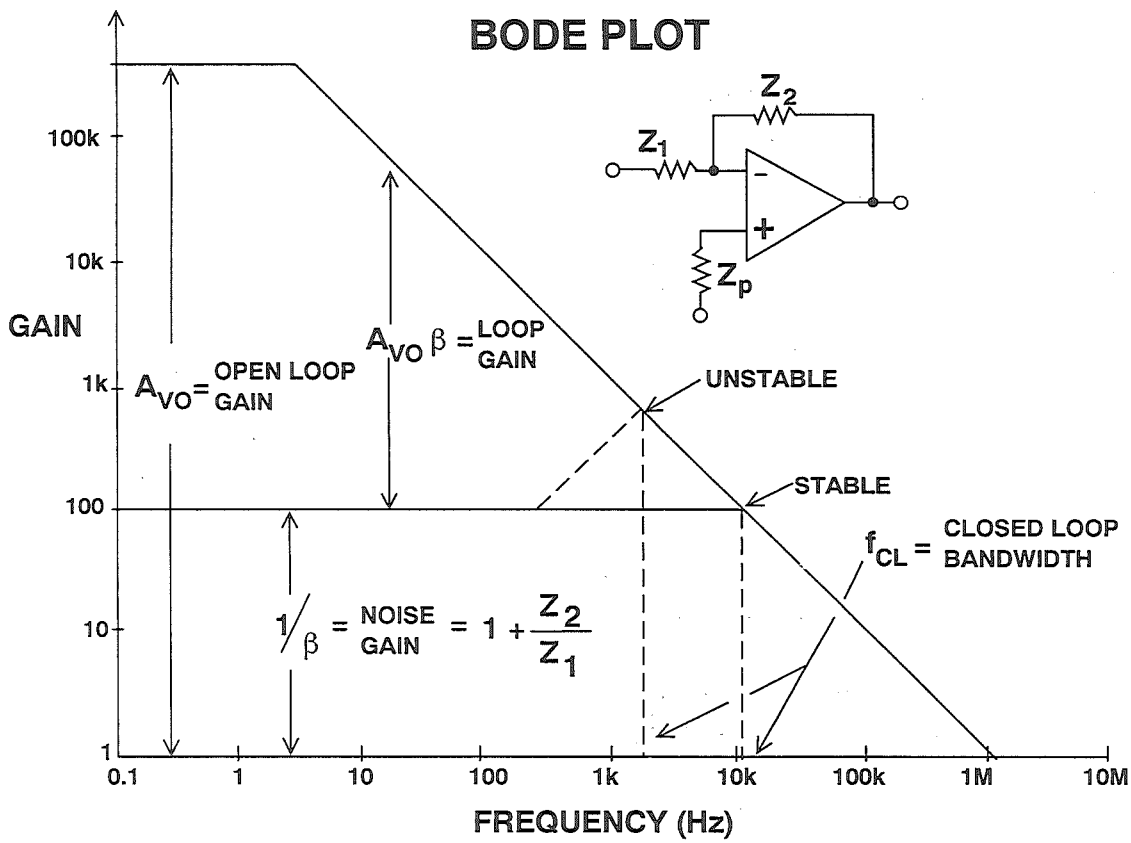


Figure 3.25

BODE PLOT DEFINITIONS

- Open Loop Gain (A_{VO}) = The open loop voltage gain of the basic amplifier without feedback but with loading. This includes frequency dependence.
- Signal Gain (A_V) = The closed loop voltage gain of the amplifying circuit for signals applied, as appropriate to the configuration.
- Feedback Loop Attenuation (β) = The voltage attenuation of the feedback network including all impedances.
- Noise Gain ($1/\beta$) = The voltage gain response given by the inverse of the feedback loop attenuation.
- Loop Gain ($A_{VO}\,\beta$) = The net gain around the broken feedback loop as seen from the feedback network input terminal back to the amplifier output. This includes frequency dependence.
- Closed Loop Gain (A_{CL})=The noise gain including the effects of loop gain.
- Closed Loop Bandwidth (f_{CL}) = The frequency at which the noise gain intersects the open loop gain.

Figure 3.26

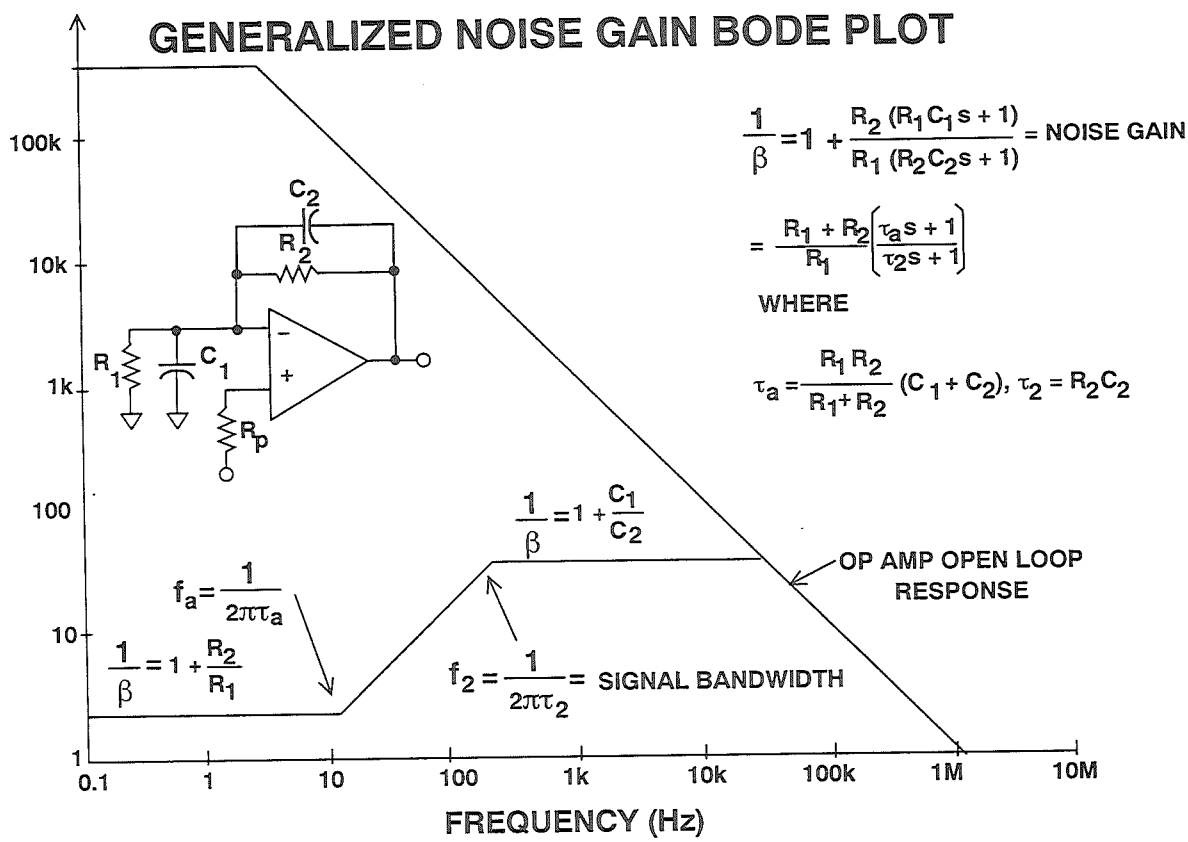


Figure 3.27

In our circuit, the diode capacitance C_1 = 50pF. If we select the feedback capacitor C_2 such that $R_1C_1 = R_2C_2$, the noise gain curve will be flat across the frequency of interest. Remember, however, that since R_1 is a function of temperature, the noise gain curve will be also. If we select C_2 = 50pF, the room temperature noise gain curve will be flat. Figure 3.28 shows the resulting noise gain curve for -25°C, +25°C, and +85°C. Note that the circuit is unconditionally stable at all temperatures.

With C_2 = 50pF, the signal bandwidth is only 3.2Hz. Signal bandwidth can be increased by lowering the value of C_2. This will cause a small amount of peaking in the noise gain. If we choose C_2 = 10pF, the signal bandwidth is increased to 16Hz. The corresponding noise gain curves are shown in Figure 3.29. The penalty for increasing the signal bandwidth is to increase the total amount of noise. This tradeoff will be examined more closely in the next section.

3

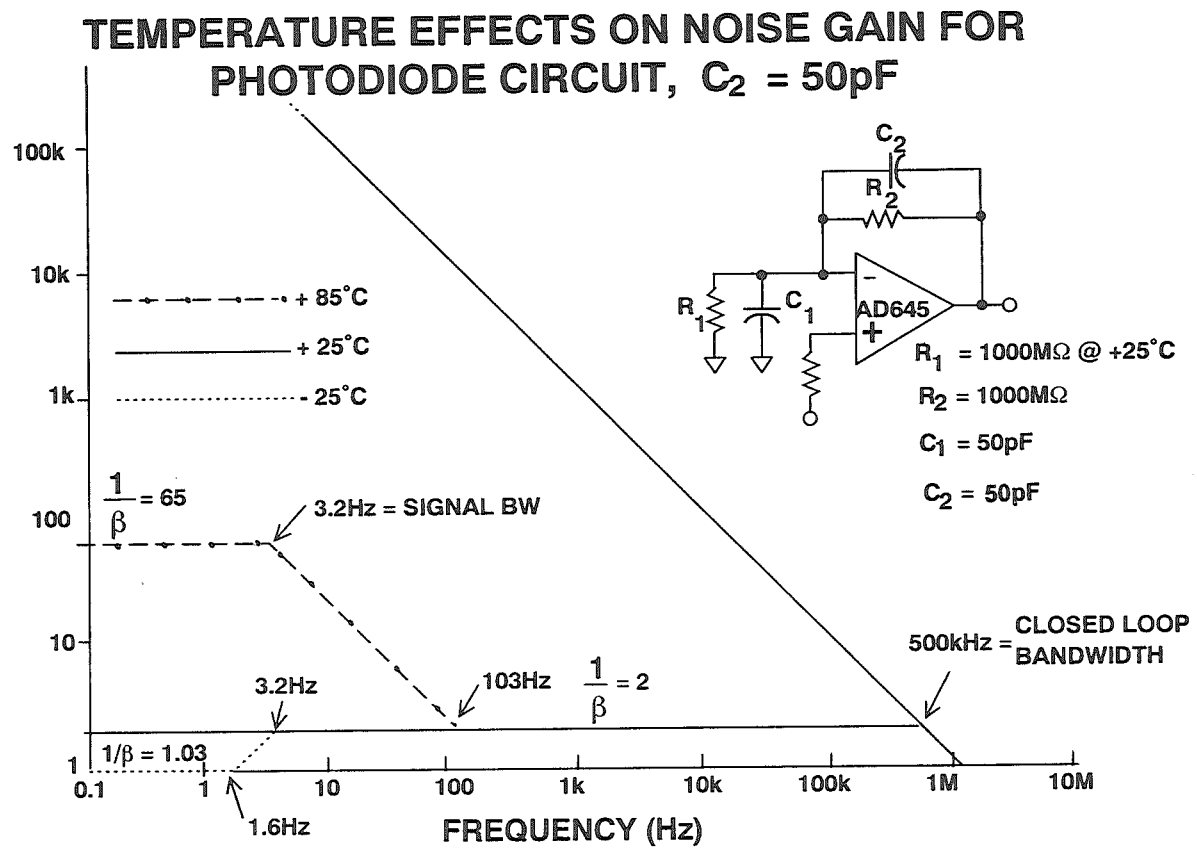


Figure 3.28

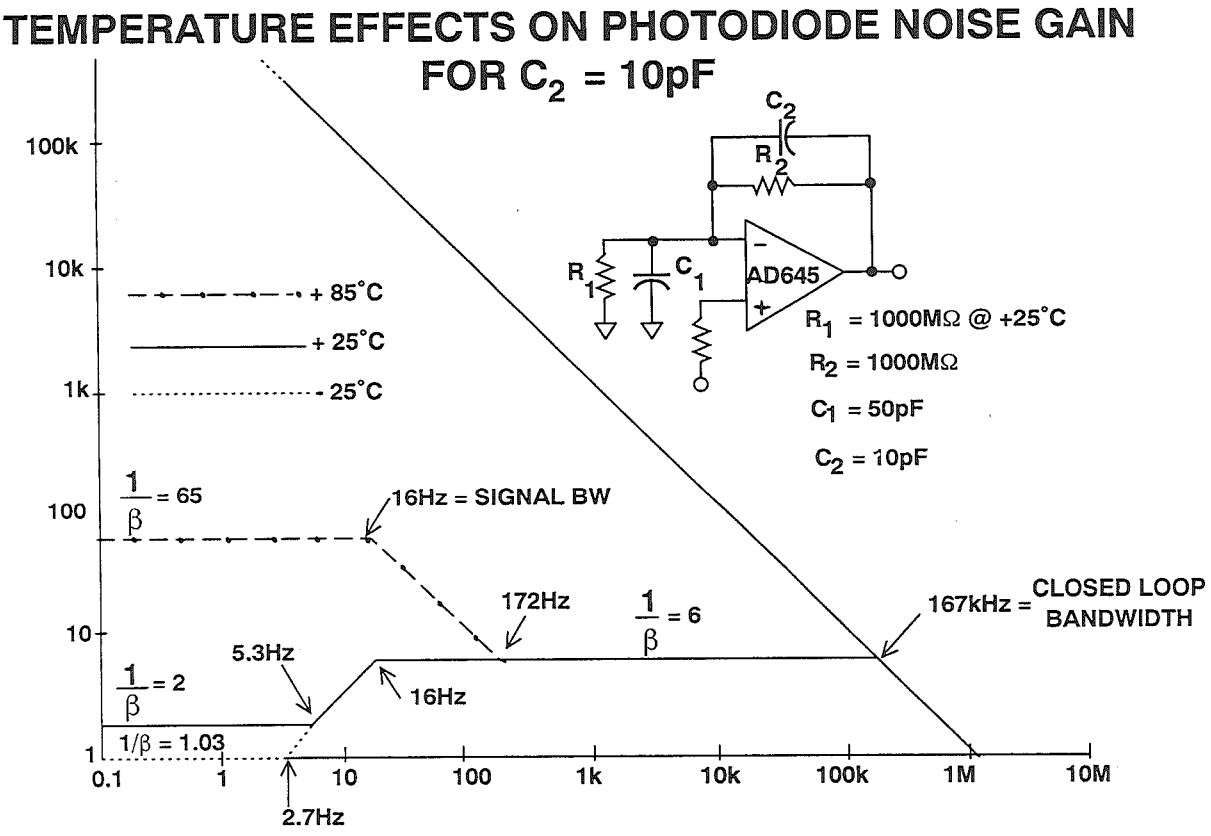


Figure 3.29

PHOTODIODE PREAMPLIFIER CIRCUIT NOISE ANALYSIS

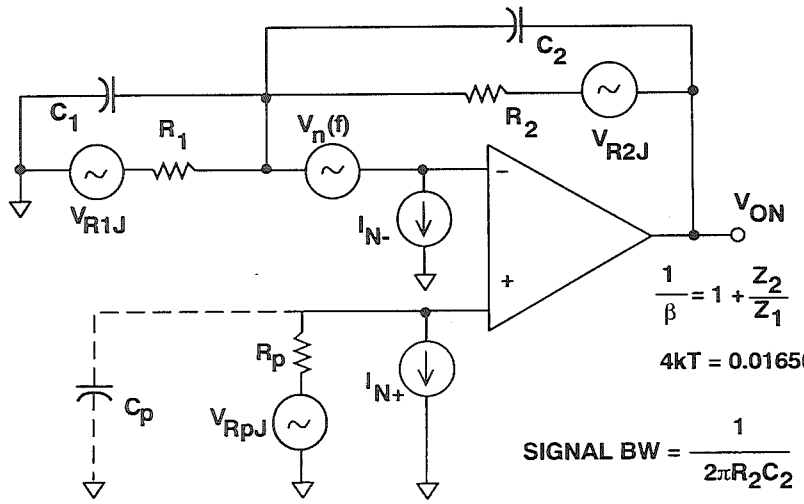
All noise sources associated with an op amp circuit are shown in Figure 3.30. The op amp itself generates both voltage noise and current noise. There is also Johnson (or thermal) noise generated by the external resistors. The total op amp output noise is obtained by first calculating the individual contributions of each of the sources, reflecting them to the output, and then taking the square root of the sum of their squares.

Johnson noise is broadband, and its spectral density is constant with frequency. Op amp voltage and current noise are usually specified as a function of frequency in terms of noise spectral density plot. These noise spectral density curves for the AD645 are shown in Figure 3.31 and are given in the units of $nV/\sqrt{Hz}$ and $fA/\sqrt{Hz}$. Each noise component must be multiplied by an appropriate factor to reflect it to the output. The output spectral densities of the individual components are then integrated over the appropriate bandwidth to obtain the rms contribution. The total output noise is then calculated by taking the square root of the sum of the squares of the individual components. We will now discuss each source which contributes to the output noise.

INPUT VOLTAGE NOISE

In order to obtain the output voltage noise spectral density plot due to the input voltage noise, the input voltage noise spectral density plot is multiplied by noise gain plot. This is easily accomplished using Bode plots on a log-log scale. The total rms output voltage noise due to the input voltage noise is then obtained

OP AMP NOISE MODEL



$$\frac{1}{\beta} = 1 + \frac{Z_2}{Z_1}$$

$$4kT = 0.01656\frac{(nV)^2}{Hz \cdot \Omega} \text{ @+25°C}$$

$$\text{SIGNAL BW} = \frac{1}{2\pi R_2 C_2}$$

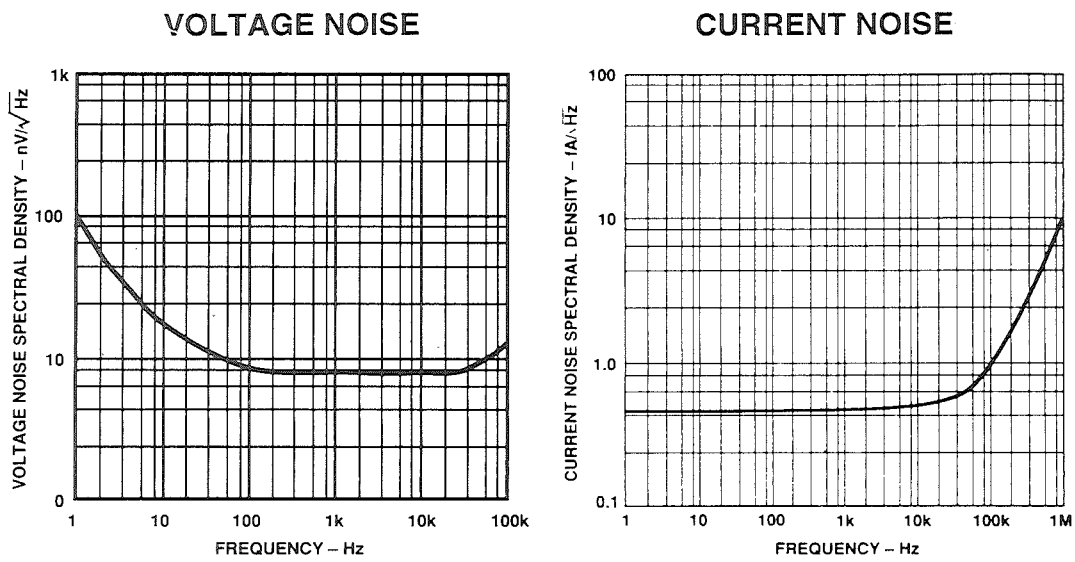
$$V_{on} = \left\{ \int_{f_1}^{f_2} V_n^2(f)\left(1 + \frac{Z_2}{Z_1}\right)^2 df + I_{n+}^2 R_p^2 \int_{f_1}^{f_2}\left(1 + \frac{Z_2}{Z_1}\right)^2 df + 4kTR_p \int_{f_1}^{f_2}\left(1 + \frac{Z_2}{Z_1}\right)^2 df \right.$$

$$\left. + I_{n-}^2 R_2^2 BW + 4kTR_2 BW + 4kTR_1\left(\frac{R_2}{R_1}\right)^2 BW \right\}^{\frac{1}{2}}$$

f_1 = 0.01Hz, f_2 = CLOSED LOOP BW•1.57, BW = SIGNAL BW•1.57

Figure 3.30

AD645 INPUT NOISE SPECTRAL DENSITIES



$\frac{1}{f}$ CORNER FREQUENCY = 12Hz

Figure 3.31

by integrating the square of the output voltage noise spectral density plot and then taking the square root. In most cases, this integration may be approximated. A lower frequency limit of 0.01Hz in the 1/f region is normally used. If the bandwidth of integration for the input voltage noise is greater than a few hundred Hz, the input voltage noise spectral density may be assumed to be constant. Usually, the value of the input voltage noise spectral density at 1kHz will provide sufficient accuracy.

It is important to note that the input voltage noise contribution must be integrated over the entire closed loop bandwidth of the circuit (the closed loop bandwidth, f_{cl}, is the frequency at which the noise gain intersects the op amp open loop response). This is also true of the other noise contributors which are reflected to the output by the noise gain (namely, the non-inverting input current noise and the non-inverting input resistor noise).

INVERTING INPUT CURRENT NOISE

The inverting input noise current flows through the feedback network to produce a noise voltage contribution at the output The input noise current is approximately constant with frequency, therefore, the integration is accomplished by multiplying the noise current spectral density (measured at 1kHz) by the noise bandwidth which is 1.57 times the signal bandwidth ($1/2\pi R_2C_2$). The factor of 1.57 arises when single-pole 3dB bandwidth is converted to equivalent noise bandwidth (See Reference 4, p. 137).

JOHNSON NOISE DUE TO FEEDFORWARD RESISTOR R_1

The noise current produced by the feedforward resistor R_1 also flows through the feedback network to produce a contribution at the output. The noise bandwidth for integration is also 1.57 times the signal bandwidth.

NON-INVERTING INPUT CURRENT NOISE

The non-inverting input current noise develops a voltage noise across R_p which is reflected to the output by the noise gain of the circuit. The bandwidth for integration is therefore the closed loop bandwidth of the circuit. However, there is no contribution at the output if $R_p = 0$ or if R_p is bypassed with a large capacitor which is usually desirable when operating the op amp in the inverting mode.

JOHNSON NOISE DUE TO RESISTOR IN NON-INVERTING INPUT

The Johnson voltage noise due to R_p is also reflected to the output by the noise gain of the circuit. If R_p is bypassed sufficiently, it makes no significant contribution to the output noise.

SUMMARY OF PHOTODIODE CIRCUIT NOISE PERFORMANCE

Figure 3.32 shows the output noise spectral densities for each of the contributors at +25°C. The various contributors to the output noise along with appropriate multiplying factors and integration bandwidths are summarized in Figure 3.33. The specific results for the photodiode circuit at +25°C are summarized in Figure 3.34.

OUTPUT VOLTAGE NOISE COMPONENTS SPECTRAL DENSITIES AT +25°C

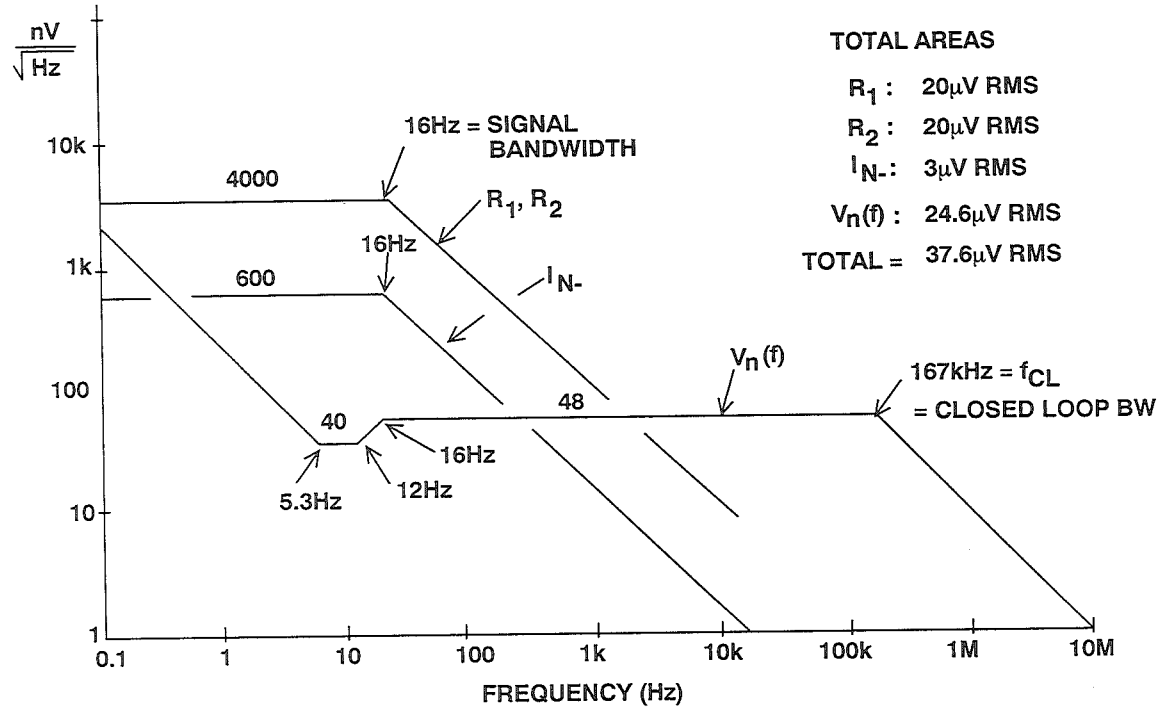


Figure 3.32

SUMMARY OF CONTRIBUTORS TO OUTPUT NOISE

NOISE SOURCE	SPECTRAL DENSITY OF VOLTAGE NOISE	REFLECTED TO OUTPUT	BANDWIDTH FOR INTEGRATION
$V_n(f)$	Frequency Dependent	$V_n(f)$*Noise Gain	1.57*Closed Loop BW
I_{n+}	Constant	$I_{n+}R_p$*Noise Gain	1.57*Closed Loop BW
I_{n-}	Constant	$I_{n-}R_2$	1.57*Signal BW
R_1	Constant	$V_{nR1}(R_2/R_1)$	1.57*Signal BW
R_2	Constant	V_{nR2}	1.57*Signal BW
R_p	Constant	V_{nRp}*Noise Gain	1.57*Closed Loop BW

Figure 3.33

SUMMARY OF NOISE CONTRIBUTORS FOR PHOTODIODE CIRCUIT AT +25°C

NOISE SOURCE	BANDWIDTH FOR INTEGRATION	RMS OUTPUT CONTRIBUTION
$V_n(f)$	167*1.57 = 262kHz	24.6μV
R_1, R_2	16*1.57 = 25Hz	20μV
I_{n-}	16*1.57 = 25Hz	3μV
I_{n+}	0	0
R_p	0	0
TOTAL		37.6μV

Figure 3.34

The effects of high temperature on the noise performance of the circuit are shown in Figure 3.35. There are three factors which cause an overall increase in the output noise. First, the overall noise gain increases considerably at frequencies less than 172Hz. This is due to the temperature dependence of R_1 which has been previously discussed. The second factor is that the output noise contribution due to the current noise of the op amp increases from 600nV/$\sqrt{Hz}$ to 4000nV/$\sqrt{Hz}$. This information comes from the AD645 data sheet. Lastly, the Johnson resistor noise spectral density increases from 4000nV/$\sqrt{Hz}$ to 4500nV/$\sqrt{Hz}$ due to the increase in temperature. Total output noise at +85°C is 50.5μV rms compared to 37.6μV rms at +25°C.

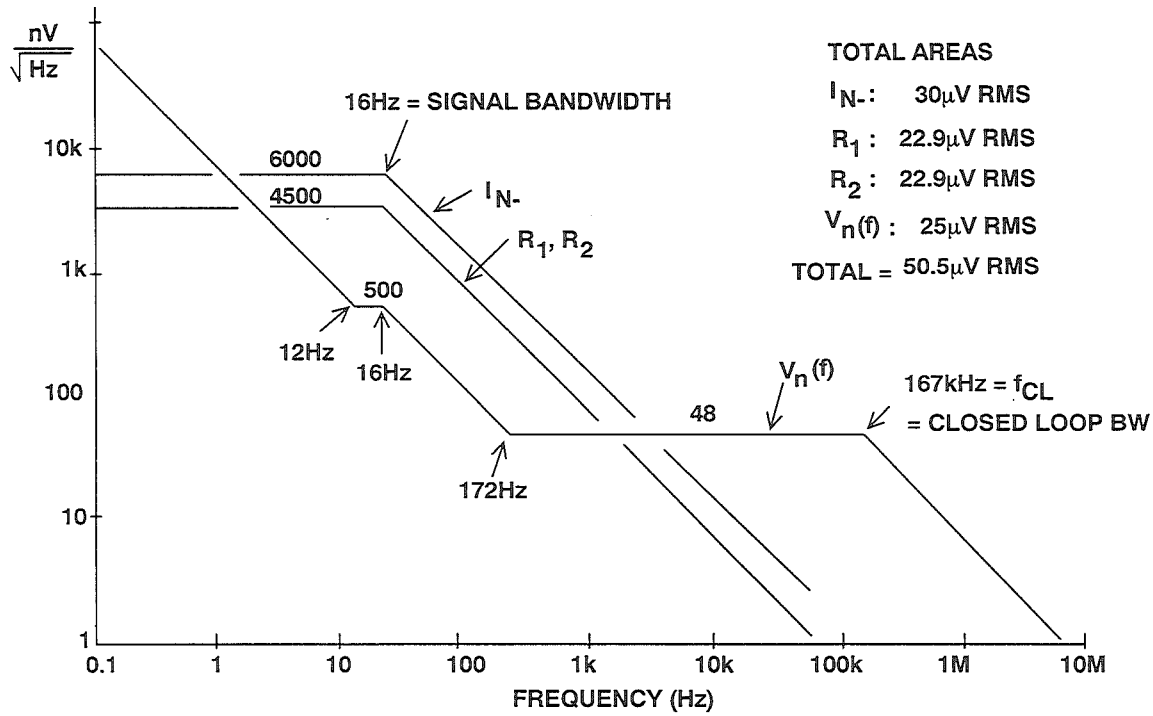
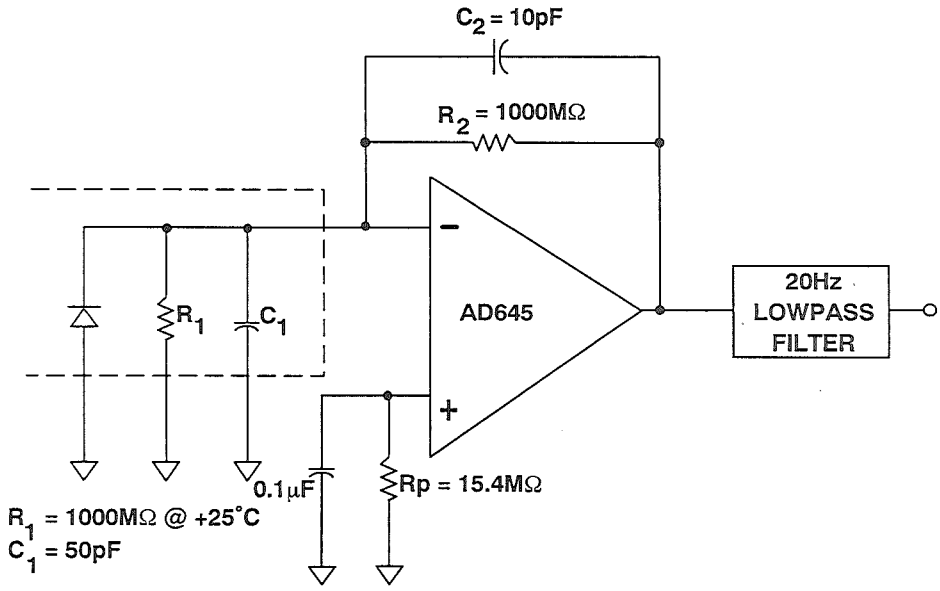


Figure 3.35

NOISE REDUCTION USING OUTPUT FILTERING

From the above analysis, the largest contributor to the output noise voltage at +25°C is the input voltage noise of the op amp reflected to the output by the noise gain. This contributor is large primarily because the noise gain over which the integration is performed extends to a bandwidth of 167kHz (the intersection of the noise gain curve with the open-loop response of the op amp). If the op amp output is filtered by a single pole filter (as shown in Figure 3.36) with a 20Hz cutoff frequency (R = 80MΩ, C = 0.1μF), this contribution is reduced to less than 1μV rms. Notice that the same results would not be achieved simply by increasing the feedback capacitor, C_2. Increasing C_2 lowers the high frequency noise gain, but the integration bandwidth becomes proportionally higher. Larger values of C_2 may also decrease the signal bandwidth to unacceptable levels. The addition of the simple filter reduces the output noise to 28.5μV rms; approximately 75% of its former value. After inserting the filter, the resistor noise and current noise are now the largest contributors to the output noise.

OUTPUT FILTER REDUCES INPUT VOLTAGE NOISE CONTRIBUTION TO OUTPUT NOISE



	UNFILTERED	20Hz FILTER (IGNORE $V_n(f)$)
+25°C	37.6μVrms	28.5μVrms
+85°C	50.5μVrms	44.1μVrms

Figure 3.36

SUMMARY OF CIRCUIT PERFORMANCE

The diagram for the final optimized design of the photodiode circuit is shown in Figure 3.37. Performance characteristics are summarized in Figure 3.38. The total output voltage drift over -25 to +85°C is 25mV. This corresponds to 25pA of diode current, or approximately 0.001 foot-candles. (The level of illumination on a clear moonless night). Limiting the upper operating temperature to +50°C reduces the output voltage drift to only 10mV.

The input sensitivity based on a total output voltage noise of 44μV is obtained by dividing the output voltage noise by the value of the feedback resistor R_2. This yields a minimum detectable diode current of 44fA. If a 12 bit ADC is used to digitize the 10V fullscale output, the weight of the least significant bit (LSB) is 2.5mV. The output noise level is much less than this.

OPTIMIZED PHOTODIODE PREAMP

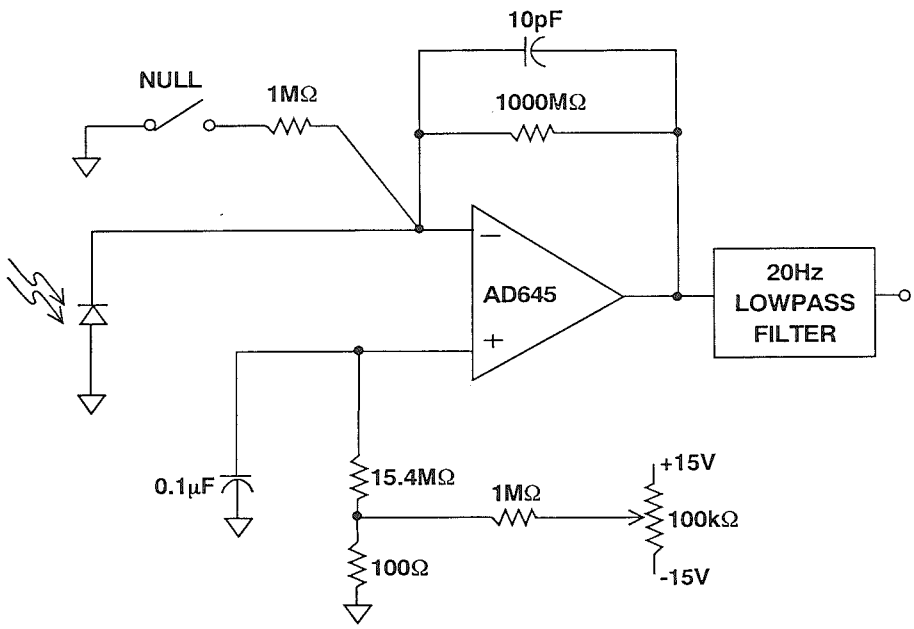


Figure 3.37

PHOTODIODE CIRCUIT PERFORMANCE

- Output Voltage Drift (-25 to +85°C) : 25mV
- Photosensitivity Drift (-25 to +85°C) : 0.001fc
- Output Photosensitivity: 30V/foot-candle
- Total Output Noise: 44μV rms at +85°C
- Output Noise Referred to Input Current: 44fA rms
- Range with R_2 = 1000MΩ: 0.001 to 0.33fc
- Bandwidth: 16Hz

Figure 3.38

PHOTODIODE CIRCUIT TRADEOFFS

There are many tradeoffs which could be made in the basic photodiode circuit design we have described. More signal bandwidth can be achieved in exchange for a larger output noise level. Reducing the feedback capacitor C_2 to 1pF increases the signal bandwidth to approximately 160Hz. Further reductions in C_2 are not practical because the parasitic capacitance is probably in the order of 1 to 2pF. A small amount of feedback capacitance is also required to maintain stability.

If the circuit is to be operated at higher levels of illumination (greater than approximately 0.3 fc), the value of the feedback resistor can be reduced thereby resulting in further increases in circuit bandwidth and less resistor noise. If gain-ranging is to be used to measure the higher light levels, extreme care must be taken in the design and layout of the additional switching networks to minimize leakage paths.

PHOTODIODE CIRCUIT TRADEOFFS

- Signal Gain / Signal Bandwidth
- Bandwidth / Noise
- Sensitivity / Gain Ranging

Figure 3.39

T NETWORK ANALYSIS

A popular circuit using "T" feedback for converting small currents into voltages is shown in Figure 3.40. The equations relating the input current to the output voltage as well as the equations for the noise gain, $1/\beta$, are given. Notice that R_3 and R_4 constitute an attenuator which attenuates the output voltage by an amount equal to approximately $R_3/(R_3 + R_4)$. The attenuated voltage is then applied to the op amp summing junction through R_2. The effect of the attenuator is to increase the signal gain by an amount equal to approximately $1 + R_4/R_3$ (assuming that $R_2 >> R_3$). The transimpedance "gain" of the circuit is increased from R_2 to approximately $R_2(1+R_4/R_3)$.

This circuit may be useful especially when amplifying very low input currents such as in the photodiode preamp. In Figure 3.41, the 1000MΩ feedback resistor is replaced with a 100MΩ resistor and a 10X attenuator. The overall transimpedance gain remains approximately 1000MΩ, but the need for the extremely large resistor is eliminated. Notice, however, that the noise gain of the circuit is increased by a factor of 5.6. The T-network circuit will therefore be 5.6 times as sensitive to input offset voltage drift and also input noise voltage.

The effect on output noise due to the feedback resistor is even more interesting. Reducing the 1000MΩ resistor to 100MΩ reduces the resistor Johnson noise by a factor of $\sqrt{10}$. However, this noise is gained up by a factor of 10 due to the T network attenuator. The net effect is to *increase* the overall output noise due to the feedback resistor by a factor of $\sqrt{10}$.

In the photodiode design example just completed, we could probably tolerate an increase in output noise due to the increase in noise gain, but the increase in sensitivity to input offset voltage would be undesirable.

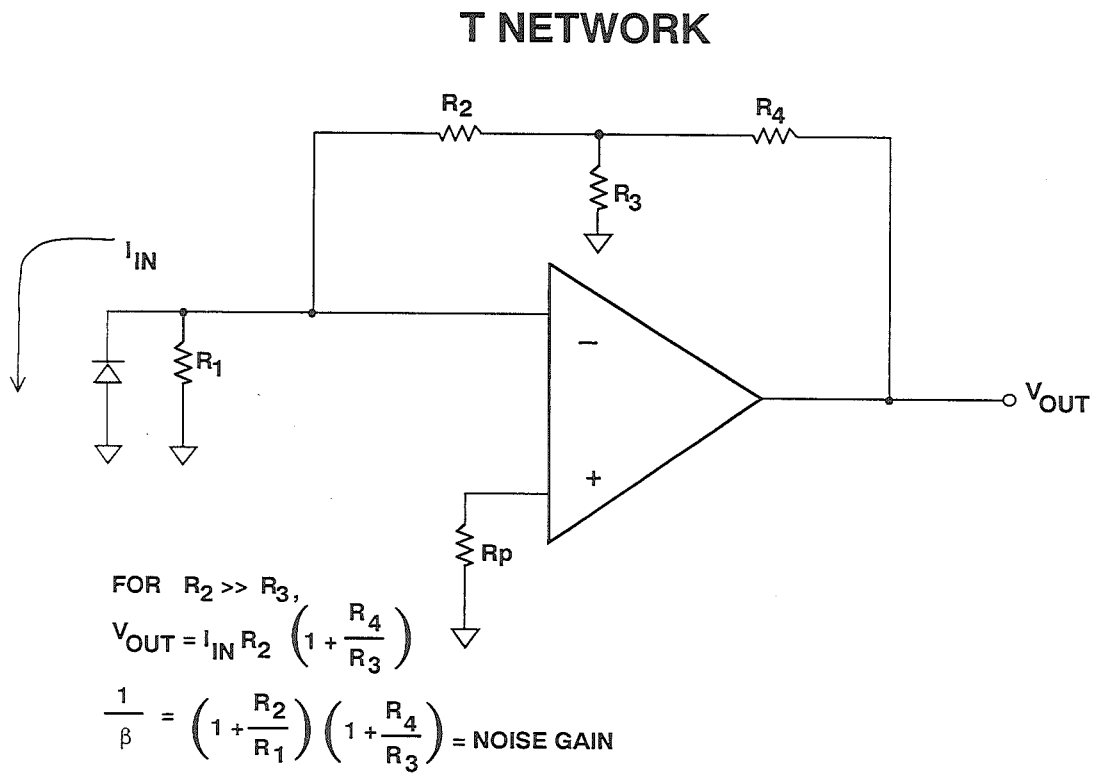


Figure 3.40

T NETWORK INCREASES RESISTOR NOISE AND NOISE GAIN

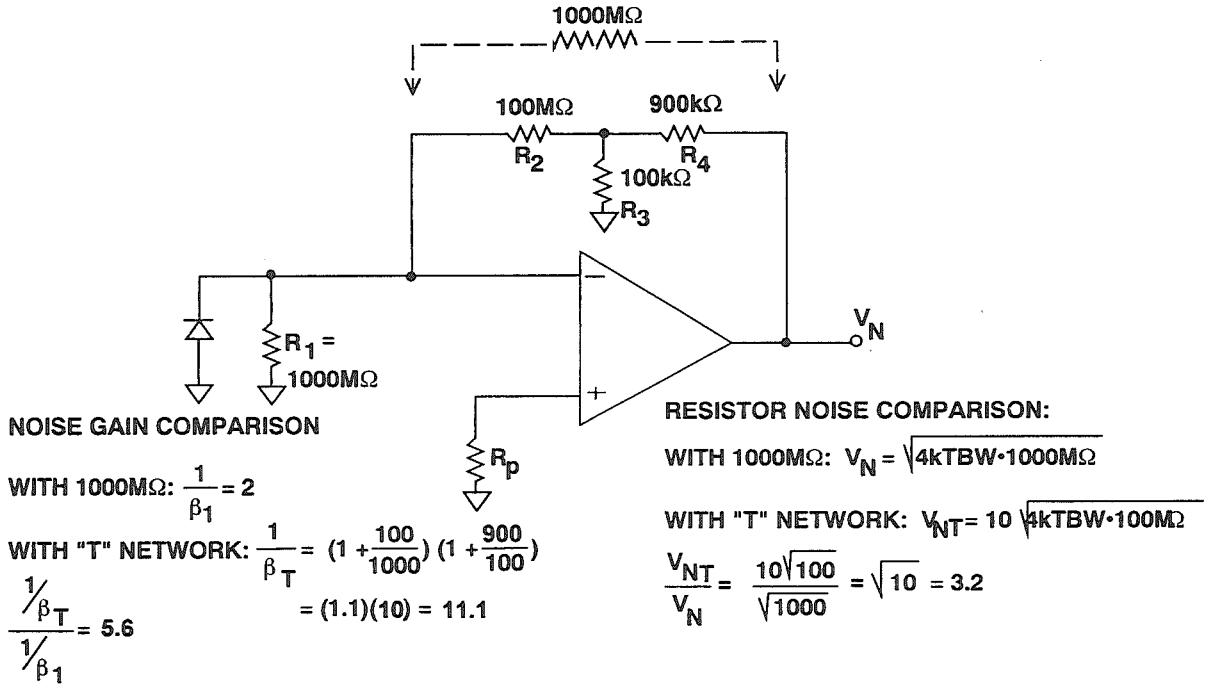


Figure 3.41

HIGH SPEED PHOTODIODE PREAMPLIFIERS

WALT KESTER, SCOTT WURCER

The precision photodiode preamp previously described was designed for maximum sensitivity at low illumination levels with little consideration for overall signal bandwidth. There are many applications, however, which require less sensitivity to illumination levels but more bandwidth. These applications present significant design challenges because of the many tradeoffs which are possible.

We will use the simple model shown in Figure 3.43 as the basis for our analysis. The sensitivity of the circuit is determined by the amount of photodiode current multiplied by the feedback resistor R_2.

The key parameters of the diode are its sensitivity (output current I_d as a function of illumination level), dark current (the amount of current which flows due to the reverse bias voltage when the diode is not illuminated), risetime t_r, shunt capacitance C_S, and shunt resistance R_{sh}. The key parameters of the op amp are its input voltage and current noise, bias current, unity gain-bandwidth product, f_u, and input capacitance C_{in}. As we shall see, the design of a high-speed preamp involves many tradeoffs, therefore this discussion will only touch on a few possibilities.

APPLICATIONS OF WIDE BANDWIDTH PHOTODIODE CIRCUITS

- Ring Laser Gyro Systems
- Bar Code Readers
- Fast Scanners
- Document Scanners
- Fax Machines
- Fiber Optic Receivers

Figure 3.42

HIGH BANDWIDTH PHOTODIODE PREAMP EQUIVALENT CIRCUIT

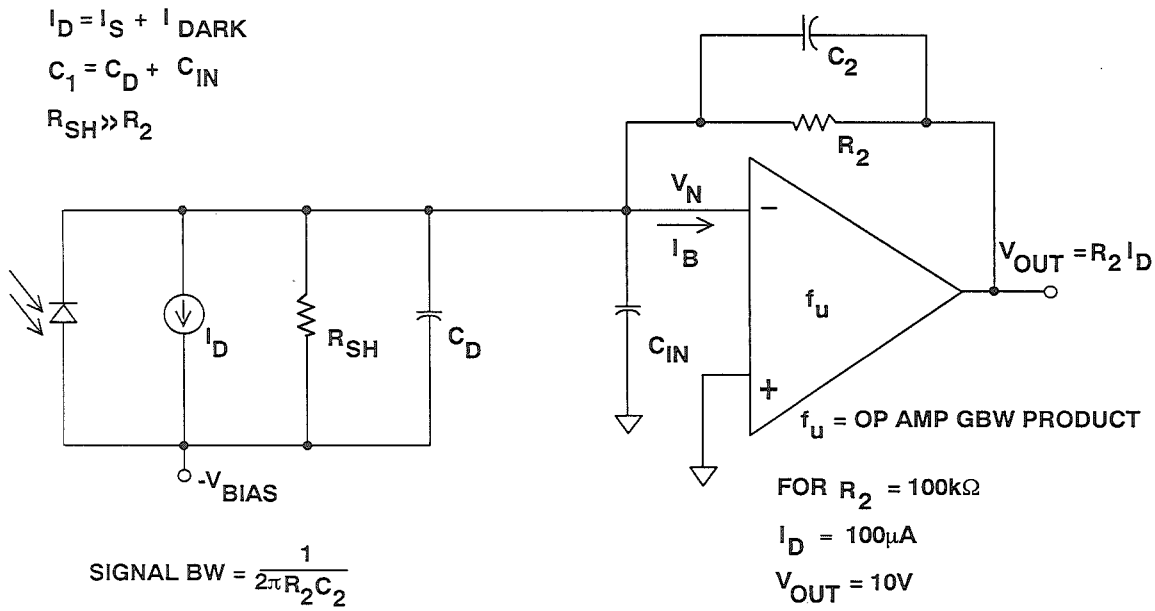


Figure 3.43

CHARACTERISTICS OF HIGH SPEED PHOTODIODES

The Motorola 5082-4204 PIN Photodiode will be used as an example for our discussion. Its characteristics are given in Figure 3.44. It is typical of many commercially available PIN photodiodes. As in most high speed photodiode applications, the diode is operated in the reverse-biased or *photoconductive* mode. This greatly lowers the junction capacitance, but causes a small amount of *dark current* to flow even when the diode is not illuminated.

It is, therefore, the combination of dark current and noise which usually determines the lowest level of detectable light. Photodiodes are linear with illumination level up to approximately 50 to 100μA of output current. With a dark current of 600pA, this give a possible dynamic range of approximately 100,000, or 100dB, neglecting the effects of noise.

Using the simple circuit shown in Figure 3.43, assume that we wish to have a fullscale output of 10V for a diode current of 100μA. The value of the feedback resistor R_2 must therefore be:

$$R_2 = 10V/100\mu A = 100k\Omega.$$

CHARACTERISTICS OF TYPICAL HIGH SPEED PIN PHOTODIODE OPERATED IN PHOTOCONDUCTIVE MODE

- Sensitivity: 350μA @ 1mW, 900nm
- Maximum Linear Output Current: 50-100μA
- Area: 0.002cm^2 (0.2mm^2)
- Capacitance: 4pF @ -10V Bias
- Shunt Resistance: $10^{11}\Omega$
- Risetime: 1-10ns
- Dark Current: 600pA @ -10V Bias

Figure 3.44

DETERMINING CIRCUIT FREQUENCY RESPONSE

The simple model shown in Figure 3.43 may also be used to determine the overall frequency response of the photodiode circuit. The total input capacitance C_1 is the sum of the diode capacitance C_d and the op amp input capacitance C_{in}. This capacitance creates a feedback pole in the frequency response. Noise gain plots for the circuit are shown in Figure 3.45, and Bode gain and phase plots in Figure 3.46.

With no compensation capacitor (C_2 = 0), the circuit is unstable because the phase shift at unity loop gain (see Figure 3.45) is 180°, corresponding to zero phase margin. The effects of adding the compensation capacitor C_2 are also shown in the Figure 3.45 and 3.46.

At this point, we should distinguish between the *signal bandwidth* and the *closed loop bandwidth*. The signal bandwidth is the frequency at which the output voltage divided by the diode current is attenuated by 3dB. The closed loop bandwidth, on the other hand, is the frequency at which the noise gain curve intersects the open loop gain curve.

The absolute maximum signal bandwidth achievable in this circuit f_{max} is the geometric mean of $1/2\pi R_2C_1$ and the unity gain-bandwidth frequency of the op amp f_u:

$$f_{max} = \sqrt{\frac{f_u}{2\pi R_2 C_1}}$$

The circuit may be stabilized by adding a feedback capacitor C_2 which creates a zero in the transfer function as shown in the noise gain plot of Figure 3.45. If we desire the maximum signal bandwidth, select C_2 such that the signal bandwidth, $1/2\pi R_2C_2$ is equal to f_{max}, or

$$\frac{1}{2\pi R_2 C_2} = \sqrt{\frac{f_u}{2\pi R_2 C_1}} \quad ,$$

EFFECT OF COMPENSATION ON PREAMP NOISE GAIN AND SIGNAL BANDWIDTH

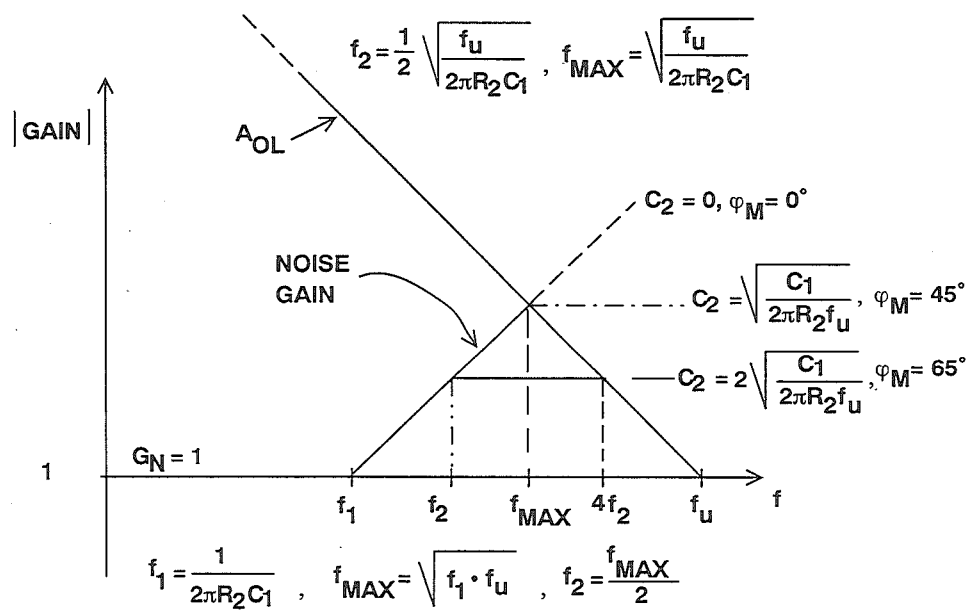


Figure 3.45

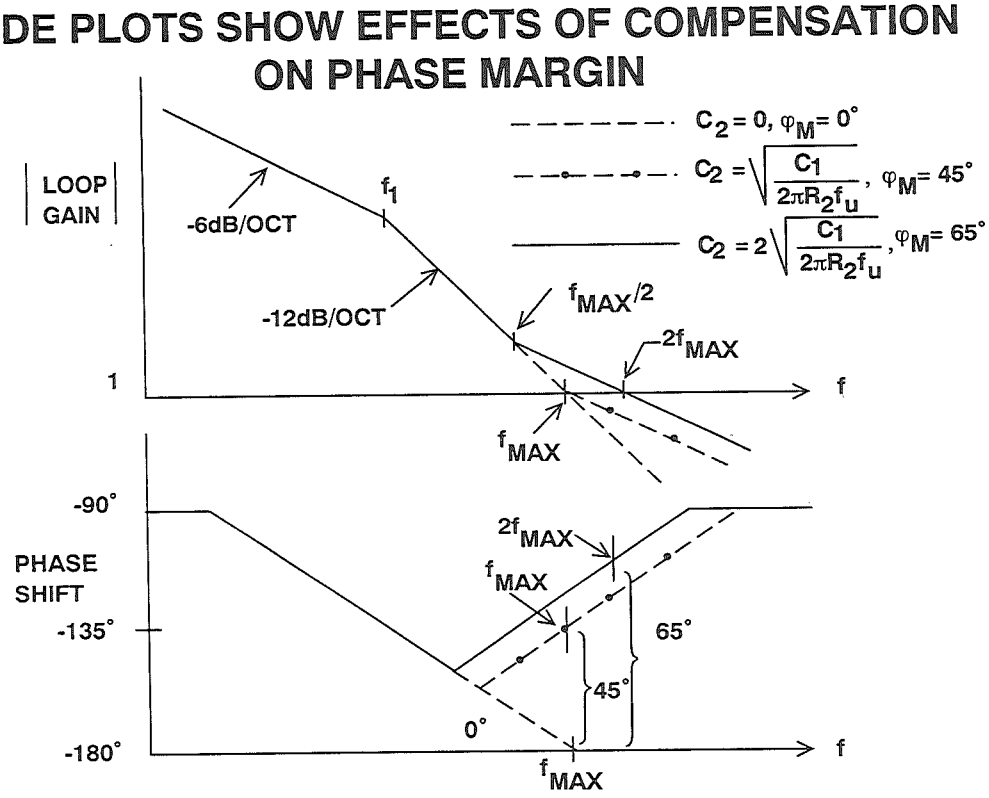


Figure 3.46

and solving for C_2 :

$$C_2 = \sqrt{\frac{C_1}{2\pi R_2 f_u}}$$

The value of C_2 chosen from the above equation will result in a phase margin of approximately 45°, step response overshoot of about 16%, and signal frequency response gain peaking of about 2dB. These numbers are derived from standard feedback control loop theory regarding second-order systems. (See in particular, Reference 11 for details of the analysis and easy methods to construct the Bode plot gain and phase approximations).

More phase margin, less overshoot, and flatter signal frequency response may be obtained by increasing the value of C_2. In fact, if flat signal frequency response is desired, C_2 should be approximately doubled from the value calculated above. This will reduce the signal bandwidth to $f_{max}/2$ and yield a phase margin of approximately 65° with 5% step response overshoot.

The value of C_2 which is computed from the equation should only be used as a starting point. Because of the approximations made and the effects of circuit parasitics, component variations, etc., C_2 should be optimized in the actual circuit to provide the best compromise between frequency and pulse response.

CONDITIONS FOR MAXIMALLY FLAT SIGNAL FREQUENCY RESPONSE WITH APPROXIMATELY 65° PHASE MARGIN AND 5% STEP FUNCTION OVERSHOOT

- $C_2 \approx 2\sqrt{\frac{C_1}{2\pi R_2 f_u}}$, and

- Signal Bandwidth $\approx \frac{1}{2}\sqrt{\frac{f_u}{2\pi R_2 C_1}}$.

Figure 3.47

SELECTING THE PROPER OP AMP

The relationship between the various circuit parameters and the signal bandwidth it given by the following approximate equations:

$$C_2 \approx 2\sqrt{\frac{C_1}{2\pi R_2 f_u}} \quad \text{, and}$$

Signal Bandwidth =

$$\frac{1}{2\pi R_2 C_2} = \frac{1}{2}\sqrt{\frac{f_u}{2\pi R_2 C_1}}$$

The equation for signal bandwidth can be simplified to show proportionality only, as shown in the general selection process given in Figure 3.48.

Since R_2 has already been determined by sensitivity requirements, the ratio f_u/C_1 may be used along with bias current and voltage noise to evaluate various op amps for maximum signal bandwidth in this application. Note that $C_1 = C_d + C_{in}$, where C_{in} is the op amp's input capacitance. In any event, making $C_{in} < C_d$, and maximizing the ratio f_u/C_1 provides the greatest signal bandwidth in the circuit, assuming the other parameters of the op amp are acceptable. If you plug in some typical numbers, you will quickly find that the op amp and not the diode is the chief element limiting the frequency response of the circuit. A comparison table between various low bias current FET-input op amps is given in Figure 3.49 to assist in the selection process.

Because the feedback resistor R_2 is normally between 100 and 300kΩ, the effects of the amplifier input current noise may usually be neglected, especially when using FET-input op amps which have inherently low input current noise specifications.

GENERALIZED OP AMP SELECTION FLOW CHART FOR HIGH SPEED PHOTODIODE PREAMP

- SIGNAL BW ~ $\sqrt{\frac{f_u}{R_2 C_1}}$, f_u = Op Amp Unity Gain Bandwidth
  C_1 = Input Capacitance = $C_d + C_{in}$.
- Minimize Value of R_2 Based on Gain Requirements
- Minimize op amp input capacitance: $C_{in} \leq C_d$
- Maximize f_u/C_{in}, Minimize Voltage and Current Noise
- Calculate C_2 and Signal Bandwidth
- Examine Bias Current and Noise Effects on Circuit

Figure 3.48

OP AMP COMPARISON TABLE FOR WIDE BANDWIDTH PHOTODIODE PREAMP APPLICATIONS

	Unity GBW Product, f_u (MHz)	Input Capacitance C_{in} (pF)	f_u/C_{in} (MHz/pF)	Input Bias Current I_b (pA)	Voltage Noise @10kHz (nV/$\sqrt{Hz}$)
AD645	1	1	1	1.5	8
AD743	4.5	20	0.2	250	2.9
AD745*	20	20	1	250	2.9
AD744	13	5.5	2.4	100	16
AD845	16	8	2	500	18
AD843	34	6	5.7	600	19
AD829	500	5	100	7000	2

* Stable for Noise Gains ≥ 5. Usually the Case, Since High Frequency Noise Gain = $1 + C_1/C_2$, and C_1 Usually $\geq 4C_2$.

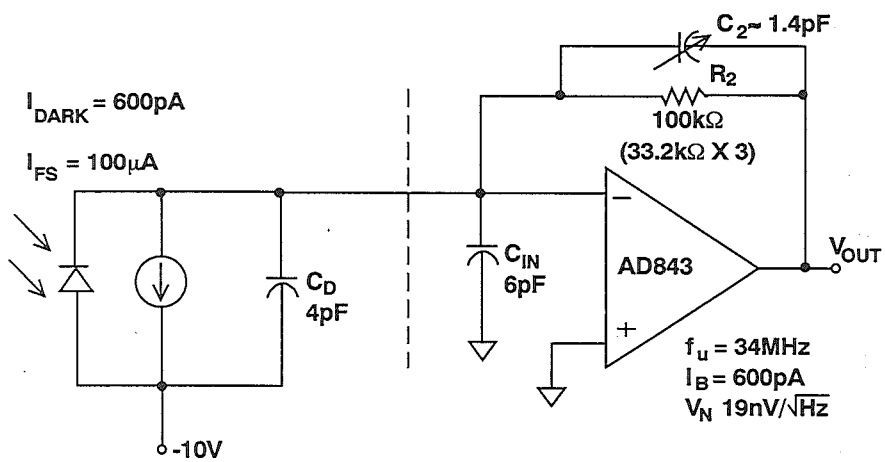
Figure 3.49

For the example under consideration, we will choose the FET-input AD843 op amp which has a unity gain-bandwidth product of 34MHz and an input capacitance of 6pF. Using the circuit parameters: $C_1 = C_d + C_{in} = 4 + 6 = 10pF$, $f_u = 34MHz$, $R_2 = 100k\Omega$, we find that $C_2 \approx 1.4pF$. This yields a signal bandwidth of 1.14MHz. In actual practice, C_2 should be a 2pF low leakage variable capacitor so that the circuit may be optimized for best compromise between frequency and transient performance. The 100kΩ resistor should be made up of three 33.2kΩ film resistors to minimize the associated stray capacitance. The circuit is shown in Figure 3.50.

ESTIMATING CIRCUIT NOISE PERFORMANCE

Performing exact noise calculations for op amp circuits can become a very tedious matter. It is much more productive to make intelligent approximations and simplify the process by identifying the chief noise contributors and neglecting the others.

1 MHz PHOTODIODE PREAMP USING AD843 OP AMP



SIGNAL BW ≈ 1.14 MHz
PHASE MARGIN ≈ 65°

Figure 3.50

STEPS IN ESTIMATING TOTAL AMPLIFIER OUTPUT NOISE

- Approximate the Noise Gain Curve for the Circuit
- Multiply the Noise Gain Curve by the Input Voltage Noise Spectral Density (Use Value at 1 or 10kHz) to Obtain the Output Noise Voltage Spectral Density
- Use Approximation Techniques to Integrate the Output Noise Voltage Spectral Density
- Calculate the Output Voltage Noise Due to the Feedback Resistor
- Calculate the Output Voltage Noise Due to the Amplifier Input Current Noise (May be Neglected in This Example)
- Calculate the Total Output Voltage Noise by Taking the Square Root of the Sum of the Squares of the Individual Components

Figure 3.51

1.1 MHz PREAMP OUTPUT VOLTAGE NOISE COMPONENTS SPECTRAL DENSITIES

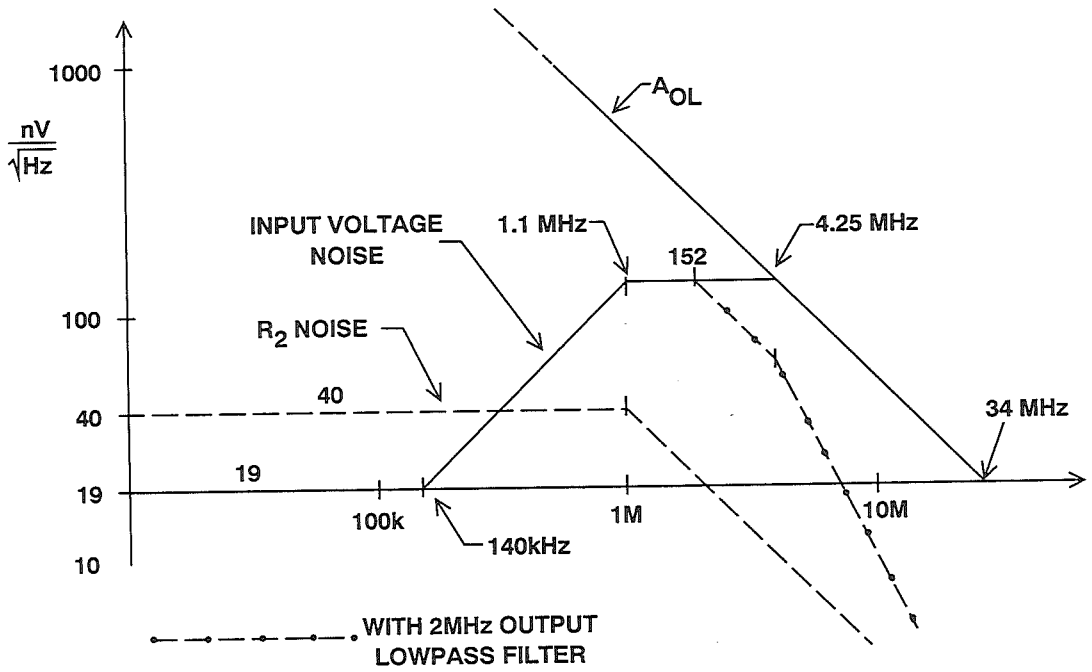


Figure 3.52

The steps used in calculating the total output noise are summarized in Figure 3.51. The total output voltage noise spectral density for the circuit using the AD843 op amp is shown in Figure 3.52. The most significant contributor to the total output noise is the input voltage noise of the op amp. The voltage noise of the 100kΩ feedback resistor should also be considered, but the contribution due to the op amp's input current noise may be neglected. The input voltage noise contribution must be integrated over the output voltage noise spectral density plot shown in Figure 3.52.

For simplicity, we will use the input voltage noise spectral density at 10kHz (19nV/$\sqrt{Hz}$) for all frequencies in the calculations. The output voltage noise over the three regions of interest are given in Figure 3.53. The noise gain is assumed to be unity in Region 1 between dc and 140kHz. In Region 2, between 140kHz and 1.1MHz, the noise gain is approximated by the geometric mean of the two noise gains: 1 and 8, or = 2.8. This yields an output noise spectral density of 54nV/$\sqrt{Hz}$. This point was somewhat arbitrarily chosen to simplify the mathematics, but the approximation contributes negligible error. The noise gain is 8 between 1.1MHz and 4.25MHz yielding an output noise spectral density of 152nV/$\sqrt{Hz}$. The correction factor of 1.57 is needed to convert the single-pole closed loop bandwidth into its equivalent noise bandwidth.

Now, we must calculate the output noise due to the 100kΩ resistor. Since a 1000Ω resistor has a noise spectral density of 4nV/$\sqrt{Hz}$, the noise of the 100kΩ resistor integrated over the signal bandwidth of 1.1MHz is given by:

$$R_2 \text{ Output Noise} = \frac{4nV}{\sqrt{Hz}}\sqrt{\frac{100000}{1000}}\sqrt{1.1x10^6x1.57Hz} = 53\mu V \text{ rms.}$$

Total output voltage noise is the root-sum of the squares of the three contributing voltage noise regions plus the feedback resistor noise, or approximately 346μV rms.

Notice that the largest contributor to the total output voltage noise is due to the noise within the gain-peaking region between 1.1MHz and 4.25MHz. In fact, this contribution itself is 338μV rms, making the other contributors negligible.

This calculation illustrates another important principle in making approximate noise calculations which essentially says that if there is a significant amount of noise at the higher frequencies of interest, the error caused by neglecting lower frequency contributors is small.

The total output voltage noise is now reflected to the input as an equivalent input noise current by dividing by the feedback resistor R_2.

This value should now be compared with the op amp input bias current of 600nA and the diode dark current of 600nA. For this example, the noise becomes the chief factor limiting the resolution of the system and not the bias current or the dark current.

A single pole external lowpass filter may be used to reduce the total high frequency output noise contribution as shown in Figure 3.55. The total output noise is reduced to 196μV rms using a single pole external 2Mhz filter, and the equivalent input current noise becomes 1960pA rms.

SUMMARY OF OUTPUT VOLTAGE NOISE CONTRIBUTIONS

Noise Source	Output Spectral Density, $nV/\sqrt{Hz}$	Bandwidth for Integration,MHz	Output Voltage Noise μV rms
V_n, dc to 140kHz	19×1 = 19	0.140	7.1
V_n, 140kHz to 1.1MHz	19×2.8 = 54	0.996	54
V_n, 1.1MHz to 4.25MHz	19×8 = 152	3.15×1.57	338
Resistor, R_2	40	1.1×1.57	53
TOTAL			346

Figure 3.53

REFLECTING OUTPUT VOLTAGE NOISE TO AN EQUIVALENT INPUT NOISE CURRENT

- Equivalent Input Current Noise = 346μV rms/100,000Ω = 3460pA rms.
- Op Amp Input Bias Current = 600pA
- Photodiode Dark Current = 600pA
- Dynamic Range $= 20\log_{10}\left(\frac{100\mu A}{3460pA}\right) = 89dB.$

Figure 3.54

EFFECT OF OUTPUT FILTER ON NOISE

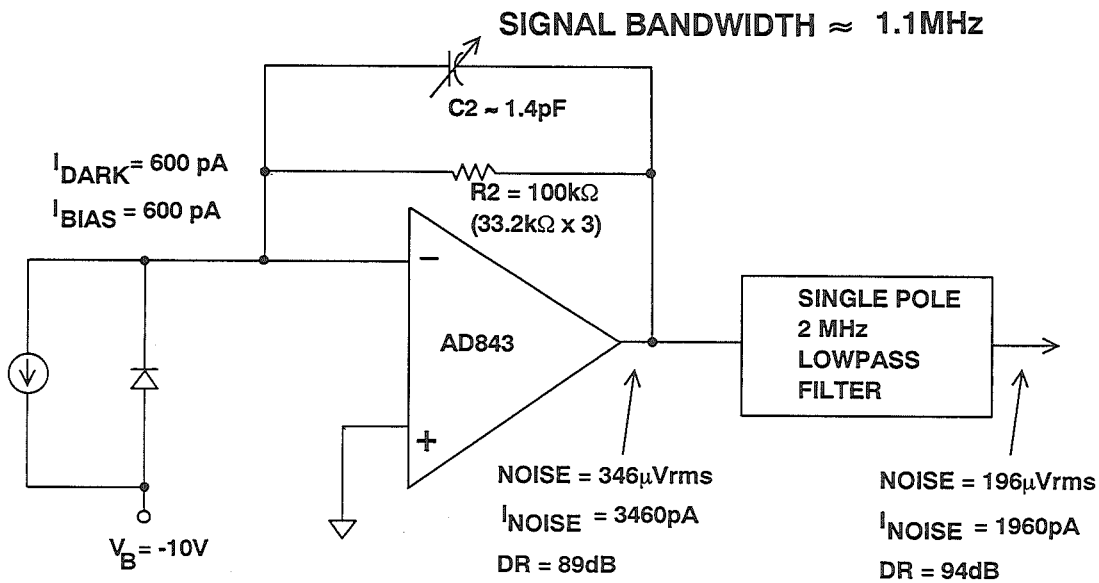


Figure 3.55

EFFECTS OF 2MHz OUTPUT FILTER ON OUTPUT VOLTAGE NOISE

- Equivalent Input Current Noise = 196μVrms/100,000Ω = 1960pA rms.
- Op Amp Input Bias Current = 600pA
- Photodiode Dark Current = 600pA
- Dynamic Range $= 20\log_{10}\left[\frac{100\mu A}{1960pA}\right] = 94dB.$

Figure 3.56

The external 2MHz lowpass filter will not have a significant effect on the signal bandwidth, but reduces the effective output rms noise by a factor of almost two. If the filter is to be used, its effects on the circuit's pulse response must be evaluated during the optimization process.

ACHIEVING MORE BANDWIDTH BY USING TWO STAGES

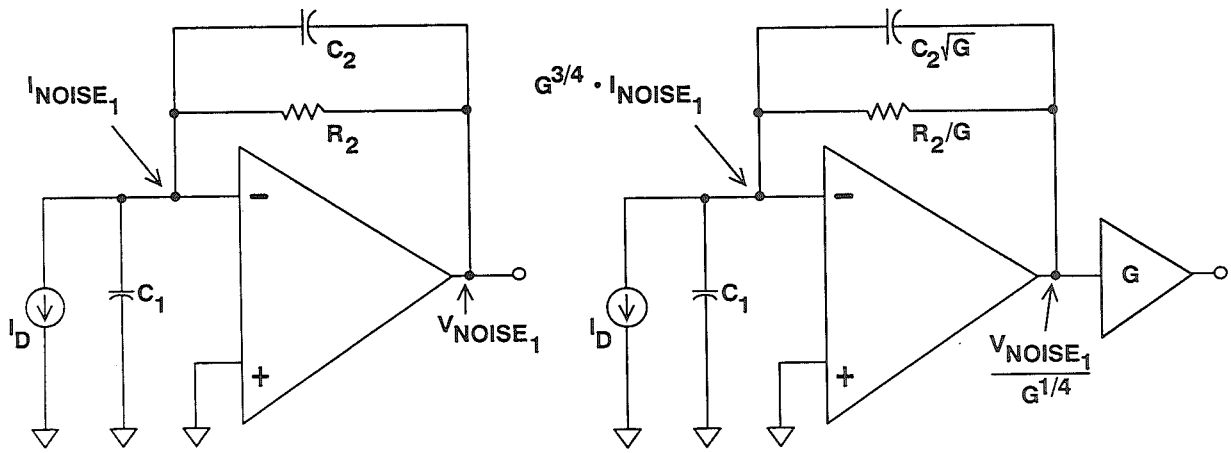
Circuit bandwidth may be increased at the expense of increased noise by splitting the gain into two stages as shown in Figure 3.57.

As can be seen in the illustration, decreasing the feedback resistor R_2 by the gain factor G increases the first-stage bandwidth by the factor $G^{1/2}$ The second-stage amplifier should be a low noise amplifier with a gain bandwidth product at least 10 times that of the desired signal gain. The extra amount of noise injected by the second-stage amplifier can usually be neglect.

The noise penalty due to this approach may be explained as follows. The gain of the first stage is decreased by the factor G, while the voltage noise at the output is only decreased by a factor equal to $G^{1/4}$ The noise reflected to the input of the first stage is therefore increased by a factor equal to $G^{3/4}$ The normal noise penalty one would expect to pay for increasing the bandwidth of a circuit is a factor which is equal to the square root of the bandwidth increase. In the simple case of a resistor, for instance, the voltage noise is proportional to the square root of the bandwidth:

Resistor Voltage Noise $= (4kTR \cdot Bandwidth)^{1/2}$.

USING TWO GAIN STAGES INCREASES BANDWIDTH BUT INCURS NOISE PENALTY WHEN REFLECTED TO INPUT



IN GENERAL, NOISE ~ $\sqrt{BW}$

$\therefore$ NOISE "PENALTY" = $\sqrt{G}$

Figure 3.57

If the bandwidth increases by a factor of $G^{1/2}$, then one would expect the noise voltage to increase by a factor equal to $(G^{1/2})^{1/2} = G^{1/4}$. The noise "penalty" paid in the above photodiode is therefore proportional to $G^{1/2}$, since the actual increase is $G^{3/4}$.

USING A COMPOSITE AMPLIFIER CONFIGURATION TO INCREASE THE EFFECTIVE GAIN-BANDWIDTH PRODUCT

Figure 3.58 shows a circuit configuration which takes advantage of the low bias current of a FET input amplifier such as the AD843 and the high gain-bandwidth product (600MHz) of a bipolar op amp such as the AD829. The AD829 is configured and compensated for a gain of 2. The signal bandwidth of the AD829 in this configuration is approximately 71MHz, which is much greater than the unity gain bandwidth product of the AD843 of 34MHz. The net result is that the unity gain bandwidth product f_u of the composite amplifier is increased by approximately a factor of 2. The equations developed previously indicate that if f_u is doubled, the signal bandwidth increases by a factor equal to $\sqrt{2}$.

The composite circuit may be best optimized initially by using ADSpice models of the amplifiers, and final optimization done on the actual circuit.

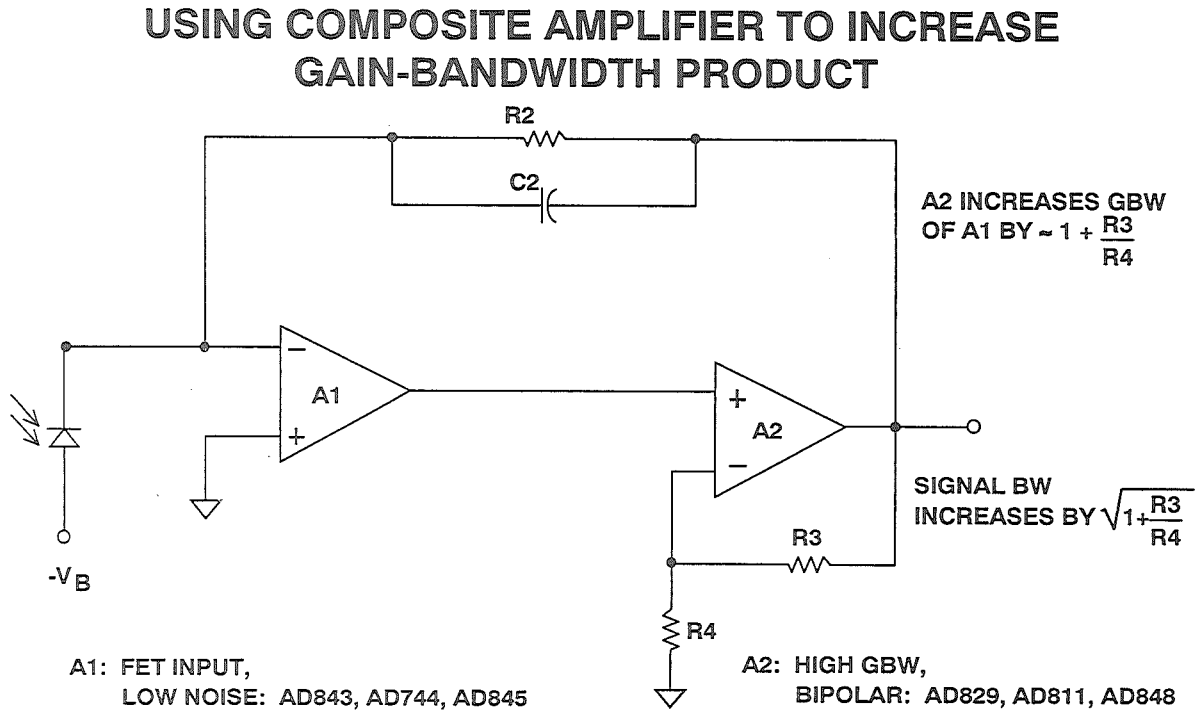


Figure 3.58

HIGH SPEED FIBER OPTIC RECEIVERS

When the primary function of the photodiode preamp is to amplify digital data from a fiber optic link, even more tradeoffs become possible in achieving higher speeds. In a fiber optic data transmission system such as the one shown in Figure 3.59, the primary purpose of the preamp is to amplify the photodiode current to a voltage level which is sufficient to drive the input of threshold comparator. In these applications, the data is coded in such a manner that the average duty cycle of the data is always 50% regardless of the actual bit pattern. A Manchester coding scheme is one way to accomplish this. Since the average duty cycle of the data stream is always 50%, ac coupling is possible, and the need for wideband precision op amps is eliminated. The preamp does not have to be a traditional dc-coupled op amp with feedback, and may be a low noise open loop GaAs "gain block". The photodiode, preamp, and the comparator are often fabricated on the same substrate in a hybrid package in order to minimize parasitics. Data transmission rates of greater than 100MHz are possible using this approach.

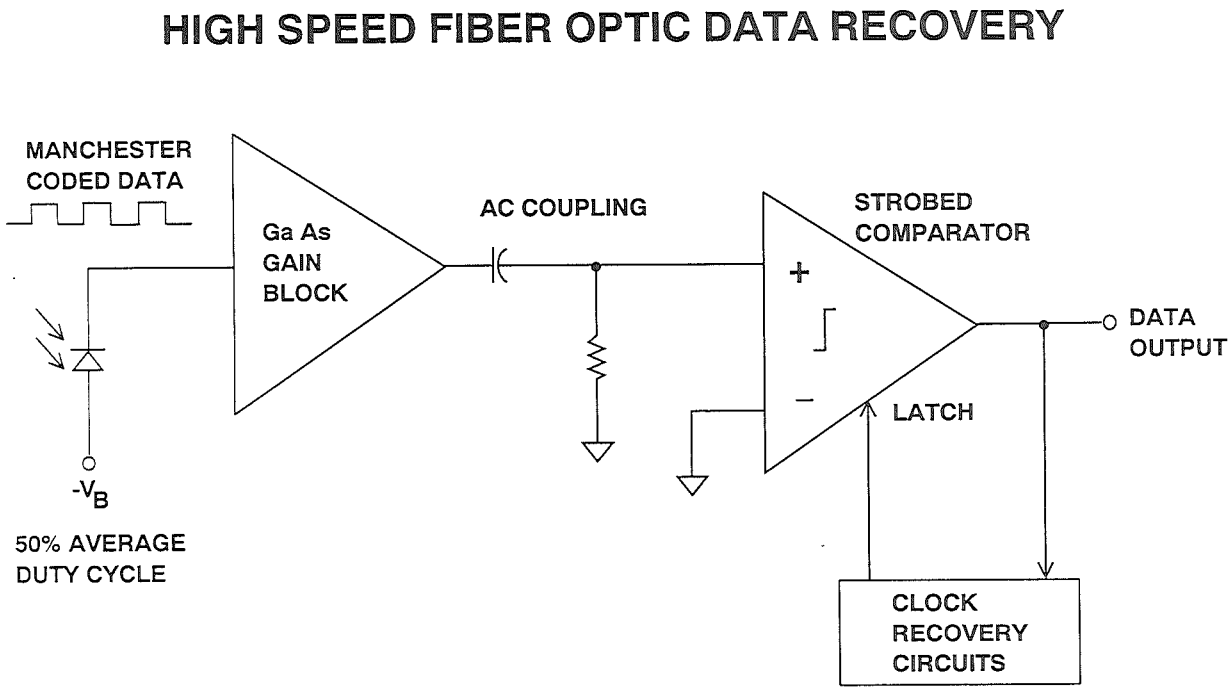


Figure 3.59

OTHER HIGH IMPEDANCE TRANSDUCER APPLICATIONS

SCOTT WURCER, CHUCK KITCHEN

A pH PROBE BUFFER AMPLIFIER

A typical pH probe requires a buffer amplifier to isolate its 10^6 to 10^9 Ω source resistance from external circuitry. Such an amplifier is shown in Figure 3.60. The low input current of the AD645 allows the voltage error produced by the bias current and electrode resistance to be minimal. The use of guarding, shielding, high insulation resistance standoffs, and other such standard picoamp methods used to minimize leakage are all needed to maintain the accuracy of this circuit.

The slope of the pH probe transfer function, 50mV per pH unit at room temperature, has a +3300ppm/°C temperature coefficient. The buffer shown in Figure 3.60. provides a gain of 20 and yields an output voltage equal to 1 volt/pH unit. Temperature compensation is provided by resistor RT which is a special temperature compensation resistor, part number Q81, 1kΩ, 1%, +3500ppm/°C, available from Tel Labs Inc.

A pH PROBE BUFFER AMPLIFIER WITH A GAIN OF 20 USING THE AD645 PRECISION OP AMP

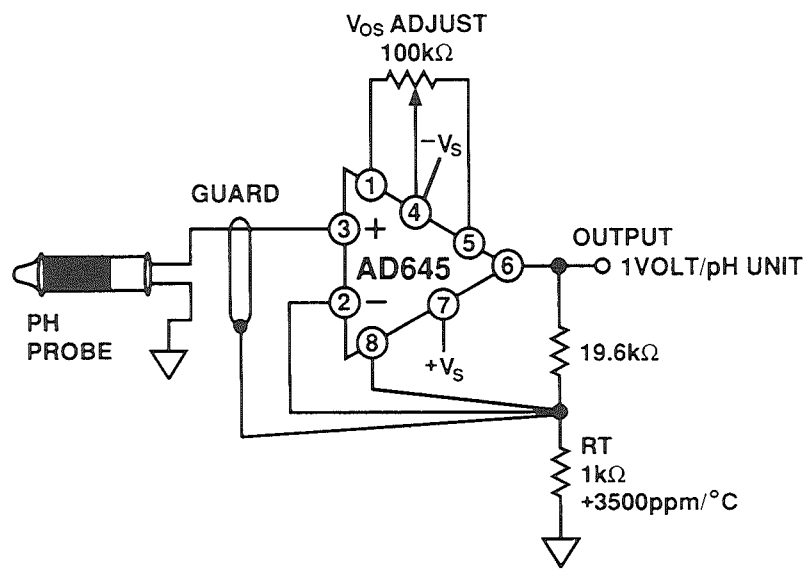


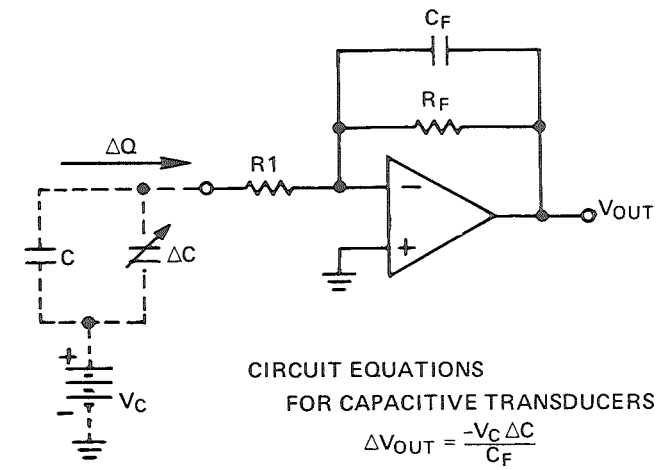
Figure 3.60

HIGH-IMPEDANCE CHARGE OUTPUT TRANSDUCERS

High impedance transducers such as hydrophones and some accelerometers require an amplifier which converts a transfer of charge into a change of voltage. Because of the high dc output impedance of these devices, appropriate buffers are required. The basic circuit for an inverting charge sensitive amplifier is shown in Figure 3.61. There are basically two types of charge transducers: capacitive and charge-emitting. In a capacitive transducer, the voltage across the capacitor (V_c) is held constant. The change in capacitance ,ΔC, produces a change in charge, $\Delta Q = \Delta CV_c$. This charge is transferred to the op amp output as a voltage, $\Delta V_{out} = -\Delta Q/C_f = \Delta CV_c/C_f$.

Charge-emitting transducers produce an output charge, ΔQ, and their output capacitance remains constant. This charge would normally produce an open-circuit output voltage at the transducer output equal to $\Delta Q/C$. However, since the voltage across the transducer is held constant by the virtual ground of the op amp (R1 is usually small), the charge is transferred to capacitor C_f producing an output voltage $\Delta V_{out} = -\Delta Q/C_f$.

CHARGE-SENSITIVE AMPLIFIER



CIRCUIT EQUATIONS

FOR CAPACITIVE TRANSDUCERS

$$\Delta V_{OUT} = \frac{-V_C \Delta C}{C_F}$$

FOR CHARGE-EMITTING TRANSDUCERS

$$\Delta V_{OUT} = \frac{-\Delta Q}{C_F}$$

LOWER CUTOFF FREQUENCY (-3dB)

$$f_{o1} = \frac{1}{2\pi R_F C_F}$$

UPPER CUTOFF FREQUENCY (-3dB)

$$f_{o2} = \frac{1}{2\pi R_1 C}$$

Figure 3.61

LOW NOISE CHARGE AMPLIFIER CIRCUIT CONFIGURATIONS

Figure 3.62 shows two ways to buffer and amplify the output of a charge output transducer. Both require using an amplifier which has a very high input impedance, such as the AD745. The AD745 provides both low voltage and low current noise. This combination makes this device particularly suitable in applications requiring very high charge sensitivity, such as capacitive accelerometers and hydrophones.

The first circuit in Figure 3.62 uses the op amp in the inverting mode. Amplification depends on the principle of conservation of charge at the inverting input of amplifier A1. The charge on capacitor C_S is transferred to capacitor C_F, thus yielding an output voltage of $\Delta Q/C_f$. The amplifier's input voltage noise will appear at the output amplified by the ac noise gain of the circuit, $1 + C_S/C_f$.

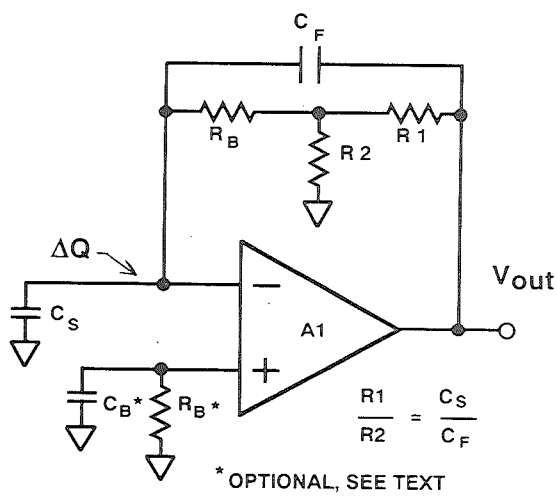
The second circuit shown in Figure 3.62 is simply a high impedance follower with gain. Here the noise gain (1 + R1/R2) is the same as the gain from the transducer to the output. Resistor R_B, in both circuits, is required as a dc bias current return.

To maximize dc performance over temperature, the source resistances should be balanced on each input of the amplifier. This is represented by the optional resistor R_B shown in Figure 3.62. For best noise performance, the source capacitance should also be balanced with the capacitor C_B. In general, it is good practice to balance the source impedances (both resistive and reactive) as seen by the inputs of a precision low noise BIFET amplifiers such as the AD743/AD745. Balancing the resistive components will

3

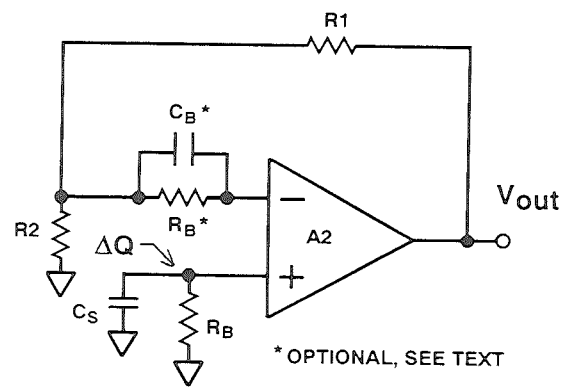
CHARGE AMPLIFIER CONFIGURATIONS

CHARGE OUTPUT MODE



$$\Delta V_{out} = \frac{-\Delta Q}{C_F}$$

VOLTAGE OUTPUT MODE



$$\Delta V_{out} = \frac{\Delta Q}{C_S}\left(1 + \frac{R1}{R2}\right)$$

Figure 3.62

optimize dc performance over temperature because balancing will mitigate the effects of any bias current errors. Balancing the input capacitance will minimize ac response errors due to the amplifier's nonlinear common mode input capacitance, and as shown in Figure 3.63, noise performance will be optimized. Figure 3.63 shows the required external components for both inverting and noninverting configurations. For values of C_B greater than 300pF, there is a diminishing impact on noise, and C_B can then be simply a large mylar bypass capacitor of 0.01μF or greater.

BALANCING SOURCE IMPEDANCES MINIMIZES EFFECTS OF BIAS CURRENTS AND REDUCES INPUT NOISE

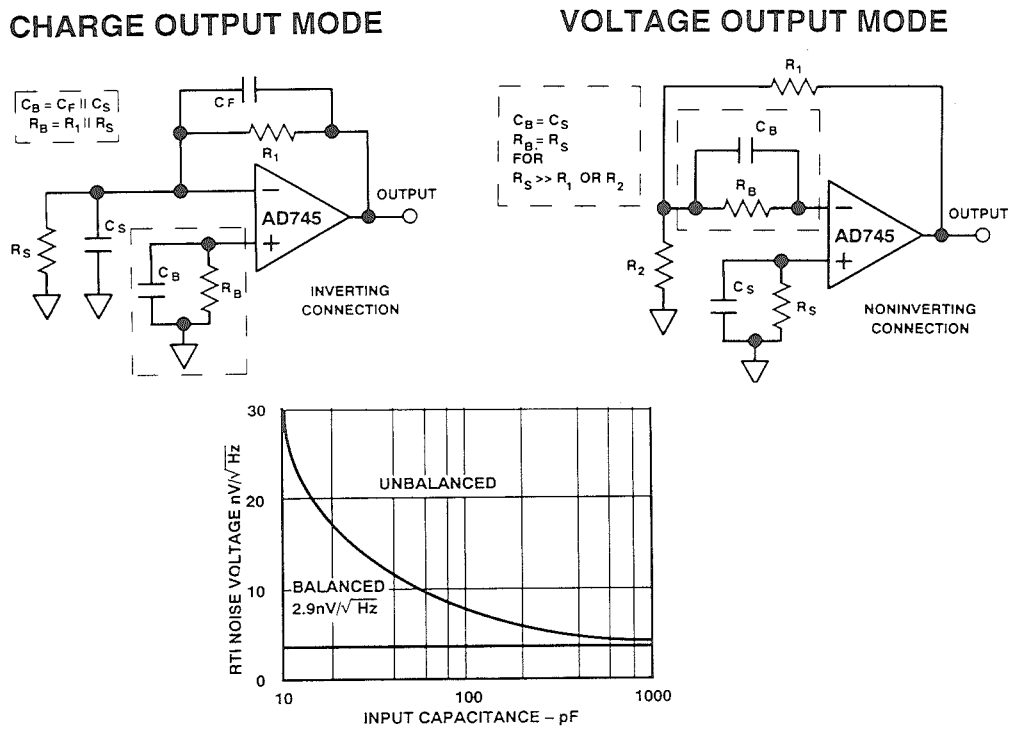


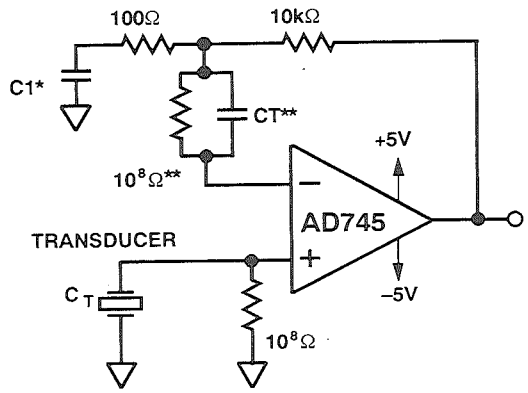
Figure 3.63

A 40dB Gain Piezoelectric Transducer Amplifier Operates on Reduced Supply Voltages for Lower Bias Current

Figure 3.64 shows a piezoelectric transducer amplifier connected in the voltage-output mode. Reducing the power supplies to ±5V reduces the effects of bias current in two ways: first, by lowering the total power dissipation and, second, by reducing the basic gate-to-junction leakage current. The addition of a clip-on heat sink such as the Aavid #5801will further limit the internal junction temperature rise.

Without the ac coupling capacitor C1, the amplifier will operate over a range of -40°C to +85°C. If the optional ac coupling capacitor C1 is used, the circuit will operate over the entire -55°C to +125°C temperature range, but dc information is lost.

A GAIN OF 100 PIEZOELECTRIC TRANSDUCER AMPLIFIER



*OPTIONAL DC BLOCKING CAPACITOR
**OPTIONAL, SEE TEXT

- ±5V Power Supplies Reduce I_b for 0°C to +85°C Operation
- C1 Allows -55°C to +125°C Operation

3

Figure 3.64

HIGH PERFORMANCE ACCELEROMETER AMPLIFIERS

Two of the most popular charge-out transducers are hydrophones and accelerometers. Precision accelerometers are typically calibrated for a charge output measured in picocoulombs (pC) per g, where g is the Earth's gravitational constant. Figure 3.65 shows two ways to configure the AD745 as a low noise charge amplifier for use with a wide variety of piezoelectric accelerometers. The output voltage, ΔV_{out} ,of these circuits will be determined by the value of capacitor, C1, and the transducer charge output ,ΔQ, or

$$\Delta V_{out} = \frac{\Delta Q}{C1}$$

HIGH PERFORMANCE ACCELEROMETER AMPLIFIERS

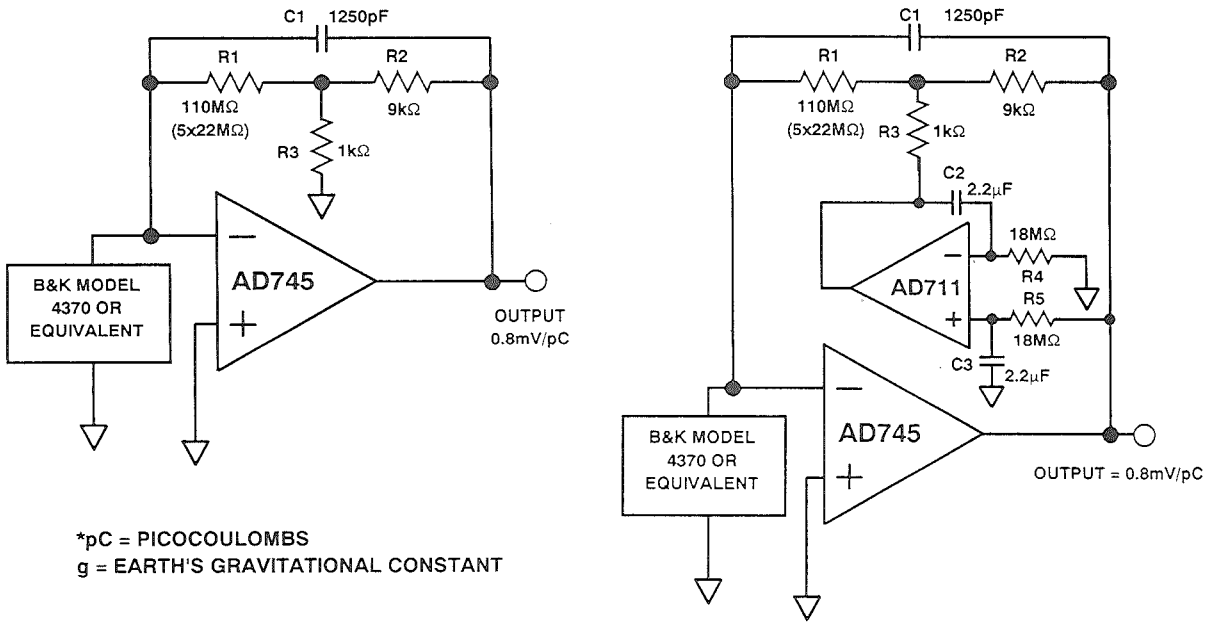


Figure 3.65

The ratio of capacitor C1 to the internal capacitance C_T of the transducer determines the ac noise gain of the circuit, $1 + C_T/C1$. The amplifier's voltage noise will appear at its output amplified by this amount. The low frequency bandwidth of these circuits will be dependent on the value of resistor R1. If a "T" network is used, the effective value is R1(1+R2/R3).

The addition of a dc servo loop as shown in Figure 3.65 can be used to assure a dc output less than 10mV without the need for a large compensating resistor when dealing with bias currents as large as 100nA. For optimal low frequency performance, the time constant of the servo loop (R4C2 = R5C3) should be:

Time Constant = R4C2 =

$$R5C3 \geq 10R1\left(1 + \frac{R2}{R3}\right)C1 .$$

HYDROPHONES

Interfacing the outputs of highly capacitive transducers such as hydrophones, some accelerometers, and condenser microphones to the outside world presents many problems. Previously designers had to use costly hybrid amplifiers consisting of discrete low-noise JFETs in front of conventional op amps to achieve the low levels of voltage and current noise required by these applications. Now, using the AD743 and AD745, designers can achieve new levels of system integration and performance.

In sonar applications, a piezo-ceramic cylinder is commonly used as the active element in the hydrophone as shown in Figure 3.66. A typical cylinder has a nominal capacitance of around 6,000pF with a series resistance of 10Ω. The output impedance is typically $10^8\Omega$ or 100MΩ

Since the hydrophone signals of interest are inherently ac in nature, noise is the overriding concern among sonar system designers. The noise floor of the hydrophone and the hydrophone preamplifier together limit the sensitivity of the system and therefore the overall usefulness of the hydrophone. Typical hydrophone bandwidths are in the 1kHz to 10kHz range. The AD743 and AD745 op amps, with their low noise figures of $2.9nV/\sqrt{Hz}$ and high input impedance of $10^{10}\Omega$ (or 10GΩ) are ideal for use as hydrophone amplifiers.

The AD743 and AD745 are companion amplifiers with different levels of internal compensation. The AD743 is internally compensated for unity gain stability. The AD745, stable for noise gains of 5 or greater, has a much higher bandwidth and slew rate. This makes the AD745 especially useful as a high-gain preamplifier where it provides both high gain and wide bandwidth. The AD743 and AD745 also operate with extremely low levels of distortion: less than 0.0003% and 0.0002% (at 1kHz), respectively.

HYDROPHONE AMPLIFIERS

Hydrophone amplifiers are usually connected in the voltage-out mode rather than charge-out mode shown in Figure 3.66. The circuits shown in Figure 3.67 can be used to amplify the output of a typical hydrophone connected in the voltage-out mode.

If the optional ac coupling capacitor, C_C, is used, the circuit on the left-hand side of Figure 3.8 will have a low frequency cutoff (F_L) :

$$F_L = \frac{1}{2\pi C_C 100\Omega} ,$$

which is determined by the time constant R_3C_C. With the ac coupling capacitor, the gain at dc is 1, and the gain above the low frequency cutoff will be a maximum of (1 + R2/R3) or 26dB.

A second type of hydrophone amplifier circuit is shown in the right-hand diagram in Figure 3.67. It uses a DC servo loop to force the dc output to 0V, within the input offset limits of the op amp, thereby maintaining full dynamic range. Power supply voltages should be reduced and heatsinking used to keep the input bias current of the AD745 below 100nA over the full military temperature range. For a smooth, low frequency response, the time constant of R7 and C1 should be at least 10x larger than that of R1 and C_T.

The transducer shown has a source capacitance of 7500pF. For smaller transducer capacitances (≤300pF), the lowest noise can be achieved by adding a parallel RC network (R4 = R1, C_T = C1) in series with the inverting input of the AD745. Balancing the source impedances (both resistive and reactive) is good practice as has been previously described.

HYDROPHONE AMPLIFIERS

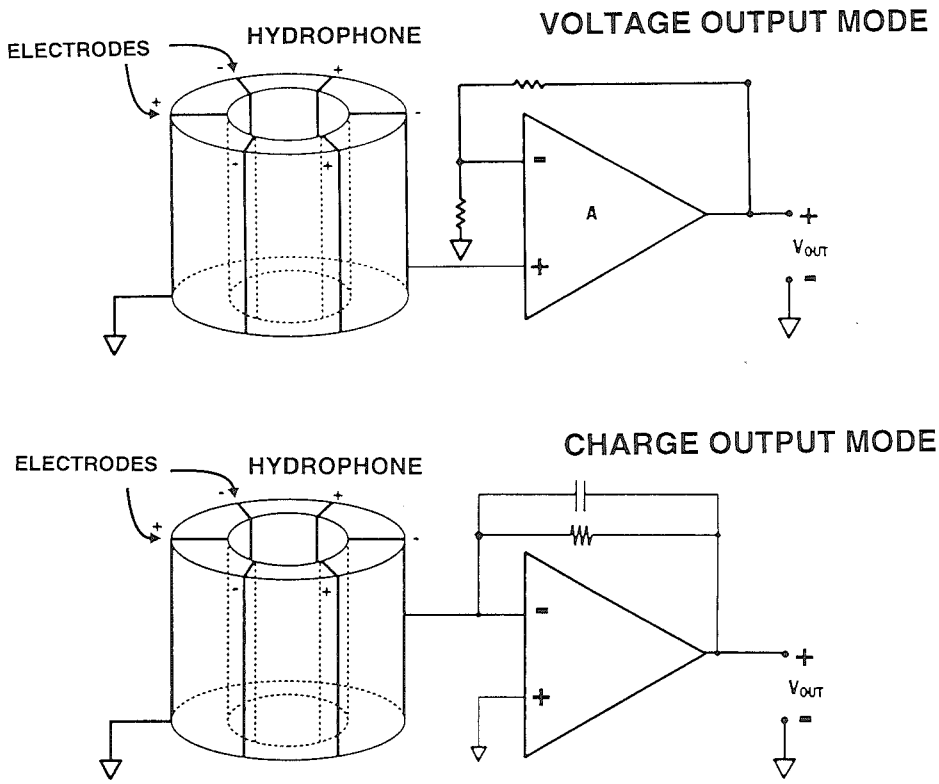


Figure 3.66

HYDROPHONE AMPLIFIER CONFIGURATIONS

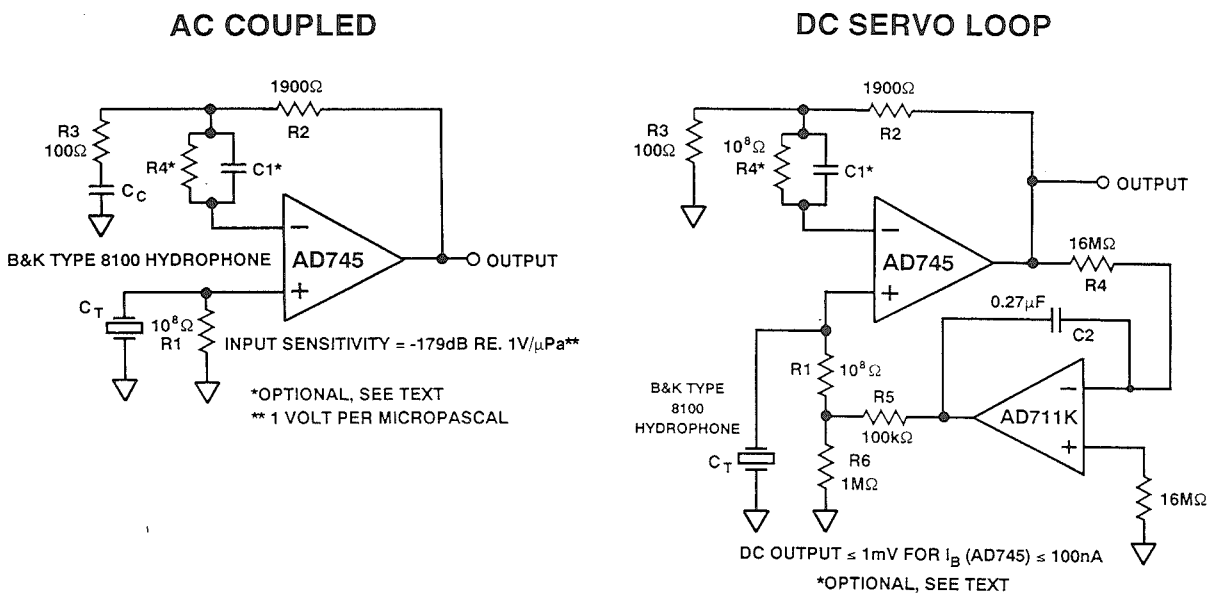


Figure 3.67

OP AMP PERFORMANCE: JFET VERSUS BIPOLAR

The AD743 and AD745 op amps are the first monolithic JFET devices to offer the low input voltage noise of an industry standard bipolar op amp without the high input bias currents typically associated with bipolar op amps. Figure 3.68 shows input voltage noise versus input source resistance of the OP-37 and the AD745 op amps. Note that the noise levels of the AD743 and the AD745 are identical. From this figure, it is clear that at high source impedances, the low current noise of the AD745 also provides total lower noise than the typical bipolar op amp. It is also important to note that, with the AD745, this noise reduction extends all the way down to low source impedances. At high source impedances, the lower dc current errors of the AD745 also reduce errors due to offset and drift as shown in Figure 3.68.

EFFECTS OF SOURCE RESISTANCE ON OUTPUT NOISE AND EFFECTIVE INPUT OFFSET VOLTAGE FOR OP-37 (BIPOLAR) AND AD745 (BiFET) OP AMPS

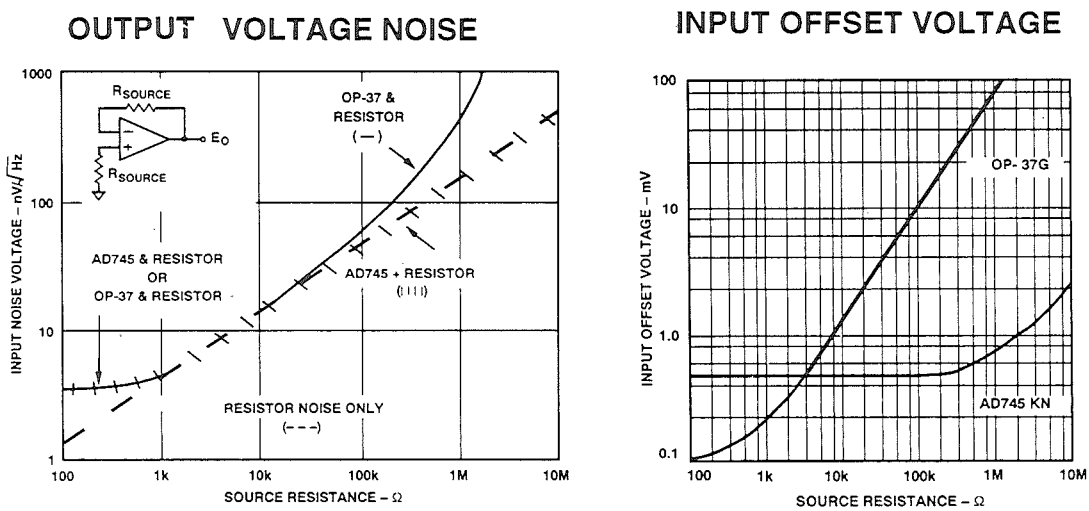


Figure 3.68

USING DECOMPENSATED AMPLIFIERS AS I/V CONVERTERS: DESIGN CONSIDERATION SUMMARY

As we have seen in the previous discussions regarding high speed photodiode preamps, there are some simple rules of thumb when designing an I/V converter where there is significant source capacitance and the bandwidth needs to be optimized. The basic circuit is shown in Figure 3.69. The high frequency noise gain ($1 + C_S/C_L$) is usually greater than 5, so a decompensated amplifier such as the AD745 with its higher slew rate and bandwidth is ideally suited to this application.

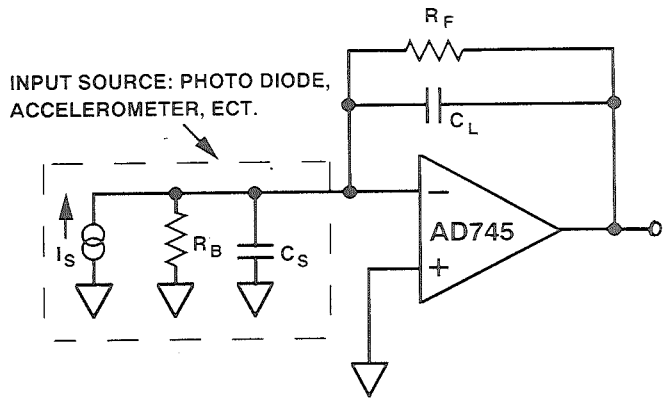
Here both the low current and low voltage noise of the AD745 can be taken advantage of, since it is desirable in some instances to have a large R_F (which increases sensitivity to input current noise) and , at the same time, operate the amplifier at high noise gain.

In Figure 3.69, the time constant $R_F C_S$ limits the practical bandwidth over which flat response can be obtained. The maximum signal bandwidth obtainable is given by the geometric mean of $1/2\pi R_F C_S$ and the op amp unity gain bandwidth produce f_C:

$$f_{max} = \sqrt{\frac{f_c}{2\pi R_F C_S}} .$$

The proper selection of the value of the stabilization capacitor, C_L, is critical to the performance of the circuit. If R_B and R_F are of the same order of magnitude, C_L is chosen such that $R_F C_L = R_B C_S$. If, however, the source is largely capacitive, and $R_B >> R_F$, then the optimum value of C_L is chosen in a different manner.

GENERALIZED CURRENT-TO-VOLTAGE CONVERTER



For $R_B >> R_F$, or Large C_S

$$\sqrt{\frac{C_S}{2\pi R_F f_C}} \leq C_L \leq 2\sqrt{\frac{C_S}{2\pi R_F f_C}}$$

$$f_{max} = \sqrt{\frac{f_C}{2\pi R_F C_S}}$$

$$\frac{f_{max}}{2} \leq f_{3dB} \leq f_{max}$$

Figure 3.69

For the case of a high impedance source, C_L should be chosen such that the phase margin of the two-pole circuit is between is between 45° and 65°, or

$$\sqrt{\frac{C_S}{2\pi R_F f_c}} \leq C_L \leq 2\sqrt{\frac{C_S}{2\pi R_F f_c}}$$

Optimizing the value of C_L within this range will result in a signal bandwidth between f_{max} and $f_{max}/2$ for the two-pole system. The actual value should be chosen in the circuit by adjusting C_L to provide the best tradeoff between frequency and pulse response.

A HIGH PERFORMANCE AUDIO I/V CONVERTER USING THE AD745

This principle can also be used to apply the AD745 in a high performance audio application. Figure 3.70 shows that an I/V converter of a high performance DAC, here the AD1862, can be designed to take advantage of the low voltage noise of the AD745 (2.9nV/ as well as the high slew rate and bandwidth provided by decompensation. This circuit, with component values shown, has a 3dB bandwidth of 531kHz, with a passband ripple of less than 0.001dB and a phase deviation of less than 2 degrees at 20kHz. The feedback capacitor value is initially chosen using the formulas in Figure 3.69, which indicate a value between 72pF and 144pF. The final circuit value of 100pF was selected by optimizing the actual circuit performance. An important feature of this circuit is that high frequency energy, such as clock feedthrough, is shunted to ground via a high quality 2000pF capacitor and not the output stage of the amplifier, thereby greatly reducing the error signal at the input of the amplifier and subsequent opportunities for intermodulation distortion.

HIGH PERFORMANCE AUDIO DAC CURRENT-TO-VOLTAGE CONVERTER USING AD745

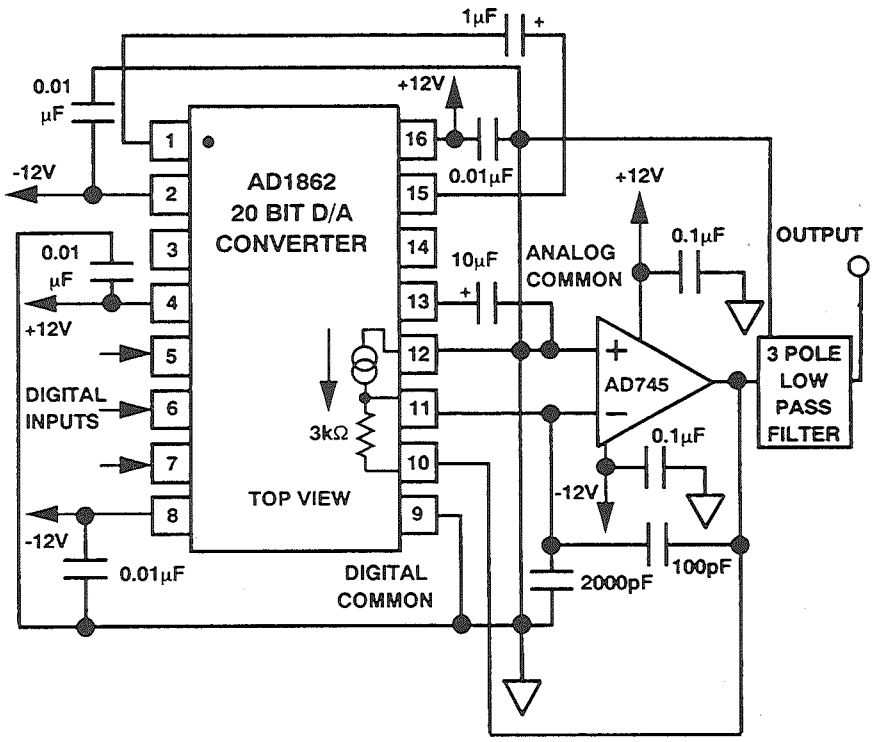


Figure 3.70

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