# SECTION XIII
# ANALOG CIRCUIT SIMULATION

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# SECTION XIII

# ANALOG CIRCUIT SIMULATION

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In the past few years, circuit simulation has been taking on an increasingly important role in the design of analog circuits, and SPICE, in its multiple forms, continues to be the most popular simulation tool. However, to achieve accurate and meaningful results, designers need accurate models of the many devices and components in their systems. In answer to this need, Analog Devices developed an advanced SPICE model for operational amplifiers. By utilizing an innovative open architecture, the gain and phase response can be fully modelled, enabling designers to accurately predict their circuits' AC and transient behavior as well as DC performance. Since then, this modelling methodology has been extended to such varied devices as instrumentation amplifiers, references, and analog multipliers.

The popularity of SPICE simulation has led to the release of op amp macromodels from many different sources, such as device manufacturers and SPICE software vendors. With the many versions comes confusion as to what is modelled, what is not modelled, and how accurate the model is. All of which are important to understand in order to know whether or not the simulation results are believable. Thus, it is important to verify each model before using it. This involves checking the model and comparing it to the actual device under various conditions such as a transient response.

## SIMULATION IS A POWERFUL TOOL WHEN USED WISELY

- Understand the Goals of the Simulation
- Evaluate the Models Accordingly
- Know the Capabilities for Each Op Amp Model From Different Sources
- Breadboarding is Necessary in Addition to Simulation

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Figure 13.1

An accurate model alone does not guarantee accurate simulations. Instead, each circuit needs to be verified in the lab by breadboarding. A breadboard of the circuit can often reveal behavior that was not predicted by SPICE either because of an incomplete model, external circuit parasitics, or numerous other reasons. By using SPICE and breadboarding together, a circuit can be efficiently and quickly designed with good assurance of working properly on the final PC board.

## MACROMODEL VS. MICROMODEL

The distinction between macromodel and micromodel is often unclear. A micromodel is the actual transistor level model of the device with all the active devices fully characterized according to the process the device is built on. Typically, a micromodel is used in the actual design of an IC. In contrast, a macromodel looks at a finished device and uses ideal elements to model its observed behavior. In other words, in developing a macromodel a device is measured in the lab, and then the model is adjusted to match this behavior.

There are advantages and disadvantages to both approaches. A micromodel can give a complete and accurate model of the circuits behavior under almost all conditions. However, because of the large number of transistors with their multiple internal nodes, the simulation time is very long. Also, manufacturers are reasonably reluctant to release these models because they contain proprietary information about the process and design of the IC. Lastly, even though all the transistors are included, this is not a guarantee that the model will be accurate. The transistor models themselves do not cover all regions of operation or may have inaccuracies in their characterization. Any small errors in the transistor models can translate into larger errors in the complete device model. Futhermore, because the number of nodes is high, SPICE has more difficulty in DC and transient convergence calculations, which may cause the simulation to fail.

On the other hand, if carefully developed, a macromodel can produce accurate results while saving considerable simulation time. With an advanced model such as the ADSpice model (described in the next section), the transient and AC performance of the device can be closely replicated. Furthermore, much of an op amp's non-linear behavior can also be included, such as short circuit current limits and output voltage swing. However, because the macromodel is a simplified version of the device, not all non-linearities are modelled. For example, the ADSpice model does not include the common mode input voltage range, which would most likely be part of a micromodel. This is not to say that such effects could not be included, but a choice was made to concentrate on more critical parameters such as AC and transient response. Adding every possible op amp characteristic would lead to a macromodel that was overly large, slow, and could possibly have convergence problems. Thus, the ADSpice macromodel includes an op amp's behavior that is critical to a circuit's performance under normal operating conditions, but does not necessarily model some of the non-linear behavior.

# MACROMODEL OR MICROMODEL??

| | METHODOLOGY | ADVANTAGES | DISADVANTAGES |
|---|---|---|---|
| MACROMODEL | Ideal Elements Model the Device Behavior | Fast Simulation Time, Easy to Modify | May Not Model All Characteristics |
| MICROMODEL | Fully Characterized Transistor Level | Most Complete Model | Slow Simulation, Difficulty in Convergence |

Figure 13.2

## THE ADSPICE MODEL

The ADSpice model was developed to advance the state-of-the-art in op amp macromodelling and provide a tool for designers to accurately simulate their circuits. Previously, the dominant model architecture was the Boyle model.[1] However, this model was developed over 15 years ago and does not accurately model many of today's higher speed amplifiers. The primary reason for this is that the Boyle model has only two frequency shaping poles and no zeroes. In contrast, the ADSpice model has an open architecture that allows for unlimited poles and zeroes, leading to much more accurate AC and transient responses.

The ADSpice model is comprised of three main portions, the input and gain stage, the pole / zero stages, and the output stage. The input stage shown in Figure 13.3 uses the only two transistors in the entire model. These are needed to properly model an op amp's differential input stage characteristics. Although the example here uses NPN transistors, the input stage can easily be modified to include PNP, JFET, or CMOS devices. The rest of the input stage uses simple SPICE elements such as resistors, capacitors, and controlled sources. An example of a controlled source is Gm1 in the gain stage, which is a voltage controlled current source. It senses the differential collector voltage from the input stage and converts that to a current. When the current flows through $R_7$, a single ended voltage is produced. By making the product of $gm_1$ and $R_7$ equal to the open loop gain, the entire open-loop gain is produced in the gain stage, which means that all other stages are unity gain. This leads to significant flexibility in adding and deleting stages.

## INPUT AND GAIN STAGES

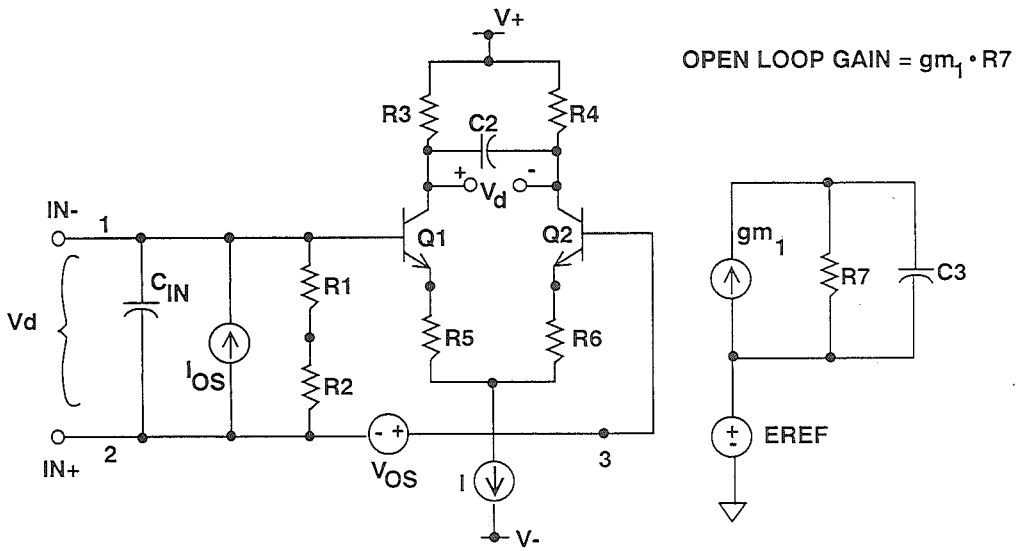



Figure 13.3

## POLE AND ZERO STAGE

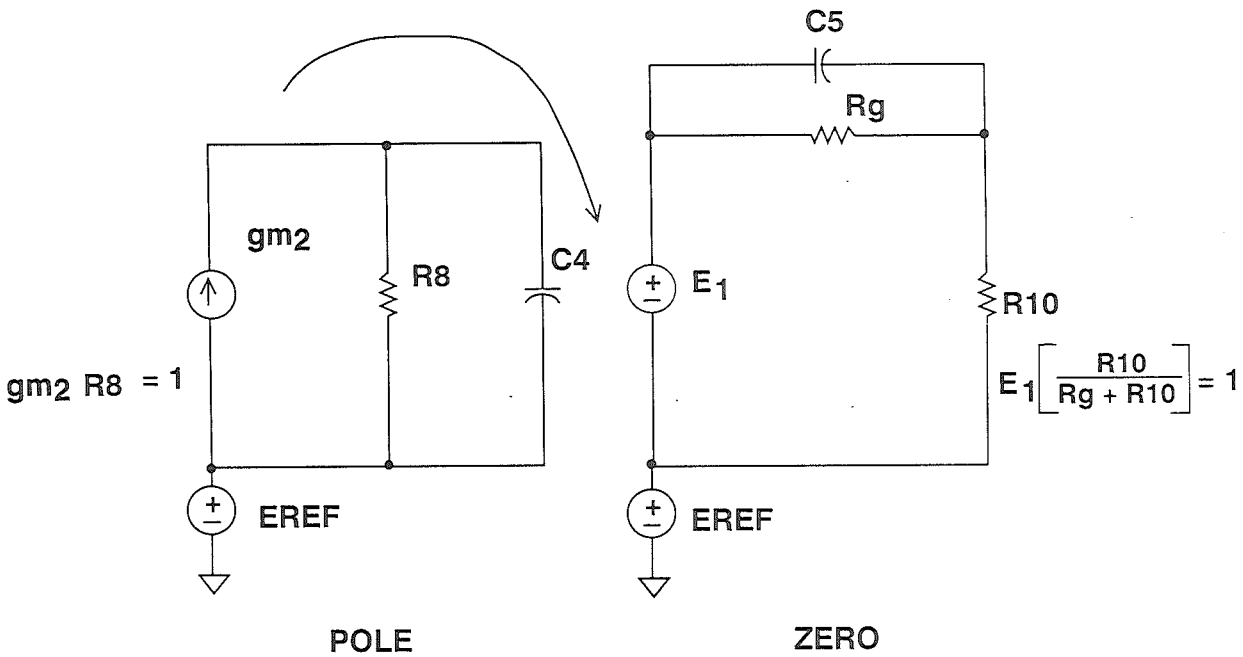



Figure 13.4

Following the gain stage are an unlimited number of pole / zero stages. The typical topology of these stages is shown in Figure 13.4, which is similar to the gain stage. The main difference is that now the product of $gm_2$ times $R_8$ is equal to unity. The pole or zero frequency is set by the parallel combination of the resistor and capacitor, $R_8$ $C_4$ for the pole and $R_9$ $C_5$ for the zero. Because these stages are unity gain, any number of them can be added or deleted without affecting the low frequency response of the model. Instead, the high frequency gain and phase response can be tailored to accurately match the actual amplifier's response. The benefits are especially apparent in closed loop pulse response and stability analysis.

The output stage in Figure 13.5 not only models the open loop output impedance at DC but with the inclusion of an inductor also models the rise in impedance at high frequencies. Additionally, the output current is correctly reflected in the supply currents. This is a significant improvement over the Boyle model because now the power consumption of the circuit under load can be analyzed accurately. Furthermore, circuits that use the supply currents for feedback can also be simulated.

All of these improvements satisfied our goal of providing an accurate state-of-the-art macromodel that can predict a circuit's behavior under many different conditions including the difficult AC and transient analysis. A comparison in Figure 13.6 of the ADSpice model, the Boyle model, and an actual op amp reveals the improved performance from the unlimited number of poles and zeros. The difference is easily apparent from a transient analysis plot for a simple unity gain follower circuit. In this case an OP-249 amplifier is used with the output connected to the inverting input and a 260pF capacitive load to produce the ringing seen in the response. The ADSpice model accurately predicts the amount of overshoot and frequency of the damped ringing in contrast to the Boyle model, which predicts about half the overshoot and significantly less ringing.

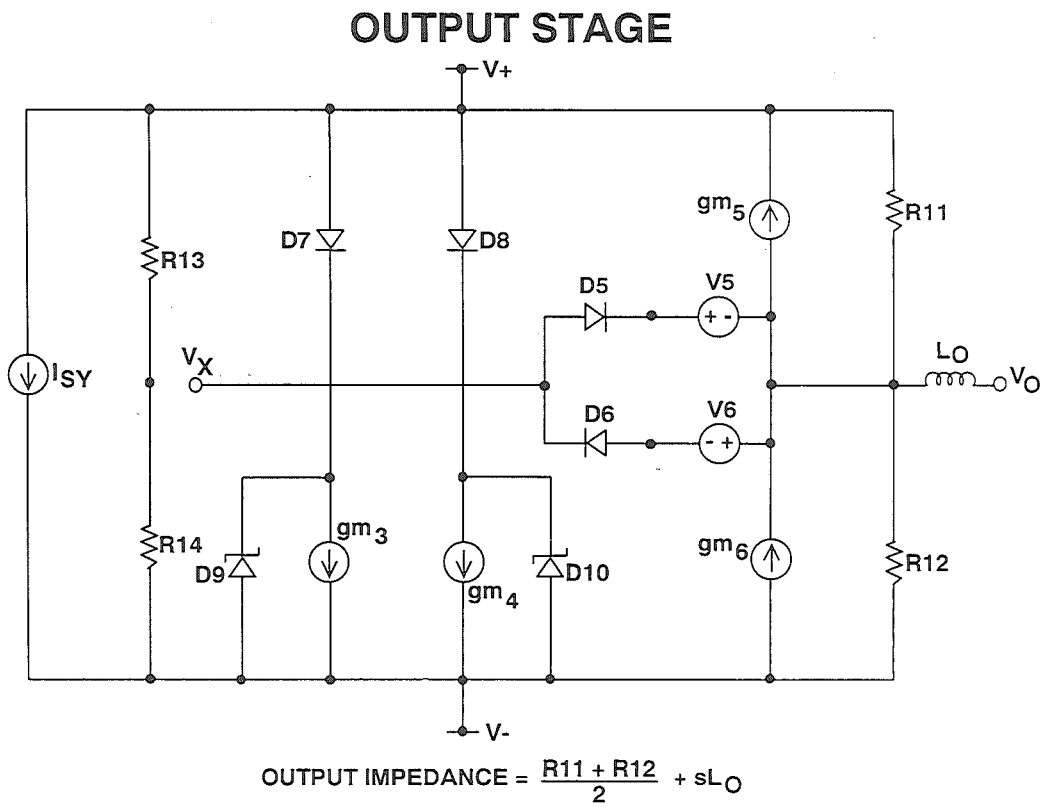



Figure 13.5

## OP-249 TRANSIENT RESPONSE TEST

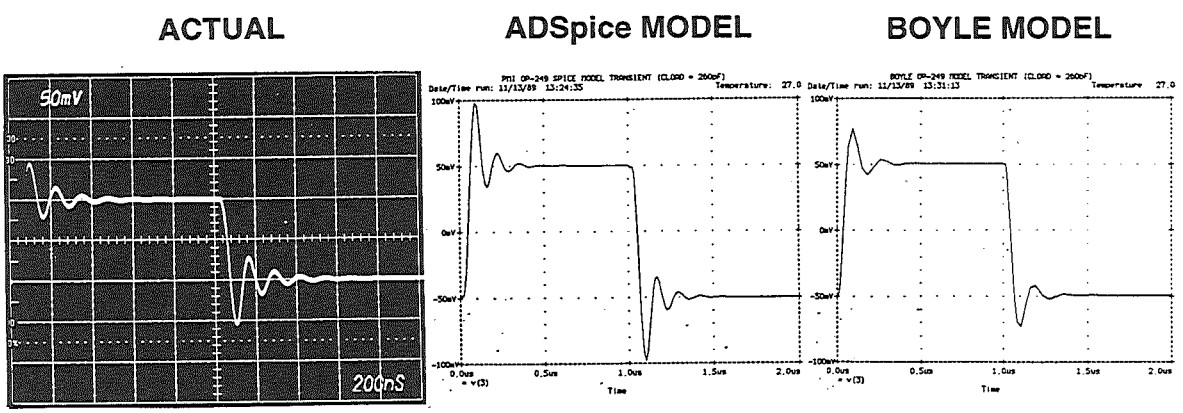



Figure 13.6

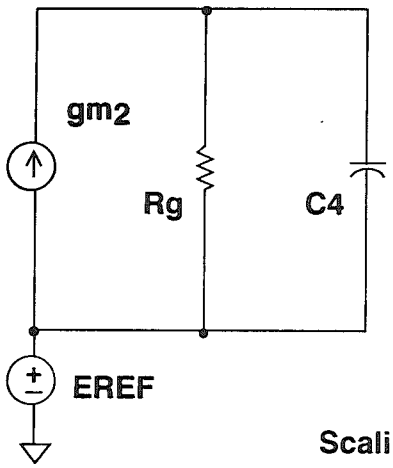
## THE NOISE MODEL

In addition to the basic model described above, there have been many enhancements to the ADSpice model such as noise modelling and a current feedback amplifier topology. The capability to model a circuit's noise in SPICE can be appreciated by anyone who has tried to analyze noise by hand. A complete analysis is a very involved and tedious task that involves adding all the individual noise contributions from all semiconductor devices and all resistors, and referring them to the output or input. This is further complicated by the frequency response from any one of these noise sources to the output.

To greatly simplify and speed this task, the ADSpice model was enhanced to include noise generators that accurately mimic the broadband and 1/f noise of an actual op amp. This involves first making the existing model noiseless and then adding discrete noise generators. The first step is mainly an exercise in scaling the internal impedances. Because of high resistance in the base model, it generates noise that is orders of magnitude too large compared to the actual device. For example, by reducing the resistances in the pole stages from 1E6Ω to 1Ω the total noise can be reduced to under $200pV/\sqrt{Hz}$.

As figure 13.7 illustrates, the noise from a simple pole stage with the large resistor in place is $129nV/\sqrt{Hz}$, but when the resistor is scaled down to 1Ω, the noise becomes $129pV/\sqrt{Hz}$. Notice that gm2 and C4 were also scaled by the same factor to maintain unity gain and the pole frequency. Extending this technique to the entire model renders it essentially noiseless.

# NOISE FROM A POLE STAGE

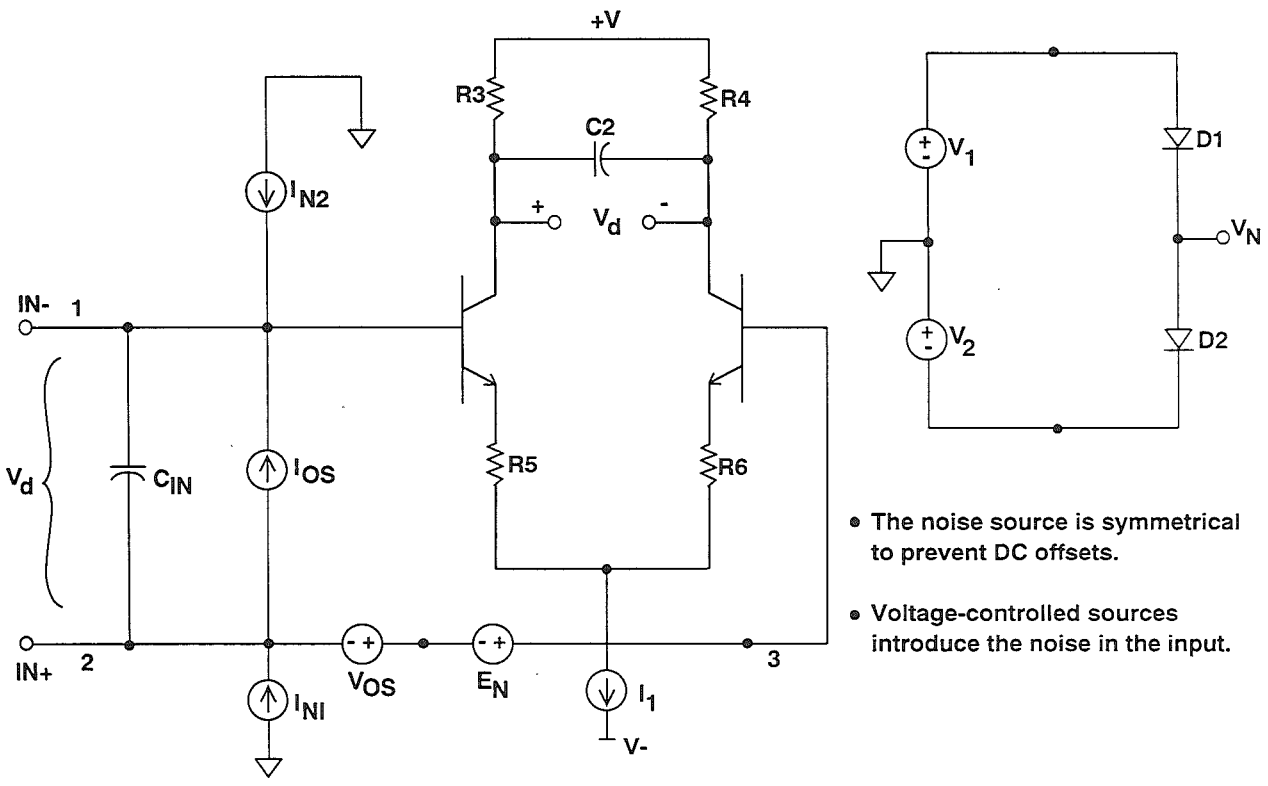



| | CASE | |
|---|---|---|
| | "NOISY" | "NOISELESS" |
| Rg | $1x10^{6}\ \Omega$ | $1\ \Omega$ |
| $gm_2$ | $1x10^{-6}$ | 1.0 |
| C4 | $159x10^{-15}F$ | $159x10^{-9}F$ |
| Noise | $129nV/\sqrt{Hz}$ | $129pV/\sqrt{Hz}$ |

Scaling the resistors down greatly reduces noise

Figure 13.7

# ADDING NOISE TO THE INPUT STAGE




- The noise source is symmetrical to prevent DC offsets.
- Voltage-controlled sources introduce the noise in the input.

Figure 13.8

Once this is achieved, three independent noise sources are added, one for voltage noise and two for current noise. All three noise sources have the same topology shown in Figure 13.8. In SPICE, semiconductor models have the built in ability to generate both broadband (thermal) noise and 1/f (flicker) noise. The noise generators use diodes mainly because they are the simplest to work with. By properly specifying the series impedance (RS) to get the broadband noise and the flicker coefficients (KF and AF) for the 1/f noise, this topology can achieve any amount of input noise. The noise is then introduced into the input stage using a voltage controlled voltage source for voltage noise and two voltage controlled current sources for current noise. Three independent sources are needed so that the input noise is not correlated, which would reduce the overall noise for the op amp. Lastly, the noise generators are symmetrical around ground so that the controlled sources will not introduce a DC bias into the input stage.

## NOISE MODEL SIMPLIFIES FULL NOISE ANALYSIS

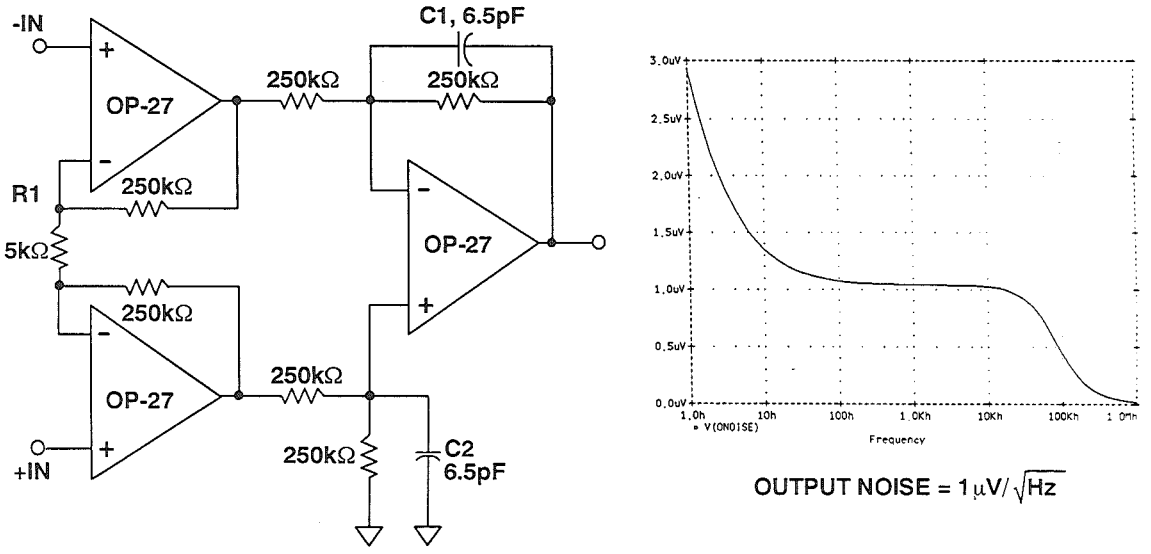



Figure 13.9

Running a noise analysis in SPICE can reveal substantial information about a circuit's noise performance. The broadband and 1/f noise referred to output or input can be plotted, as well as the total RMS noise. SPICE can also print out the noise contribution due to each element to determine the dominant sources. A simple three op amp instrumentation amplifier with a gain of 100 is a good example of how the ADSpice noise model can predict the total noise of a system. Figure 13.9 shows the topology, which in this case uses OP-27 op amps because of their low noise performance of $3nV/\sqrt{Hz}$. Running a SPICE analysis results in a broadband noise of $1\mu V/\sqrt{Hz}$ and a 1/f corner at 10Hz.

An even more useful number is the total RMS noise. This can be plotted in such programs as MicroSim's Probe by integrating the noise over the circuit's entire bandwidth. Figure 13.10 shows the total output noise as $270\mu V_{RMS}$. As can be seen from this graph, noise is being collected all the way up to 55kHz; however, if the circuit only needs a bandwidth of 1kHz, then much of the noise can be filtered out by increasing the value of C1 and C2 to 640pF. Doing so results in a total noise figure of $40\mu V_{RMS}$, which is also plotted in Figure 13.10. Already the noise has been improved by a factor of 7, but there may still be room for improvement. Looking at the SPICE output file for each component's contribution to total noise reveals that the input resistor, R1, dominates. Reducing it to 500Ω, and all the other resistors by the same factor of 10, further lowers the total noise to $20\mu V_{RMS}$ as shown on the bottom trace of the graph. As this example illustrates, the ADSpice noise model greatly simplifies a complete noise analysis, which further speeds the design of a circuit.

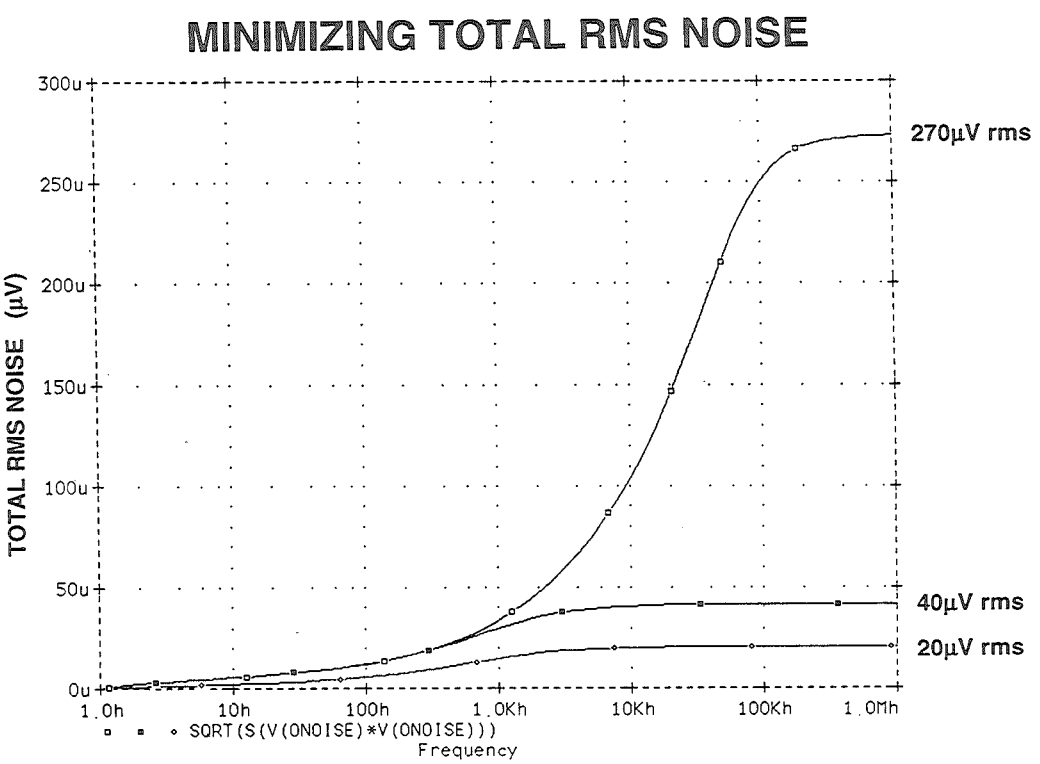



Figure 13.10

## CURRENT FEEDBACK AMPLIFIER MODEL

A new model topology had to be developed for current feedback amplifiers to accommodate their unique input stage structure. The model uses the topology shown in Figure 13.11 for the input stage, and the rest of the model containing the gain stage, pole / zero stages, and output stage are essentially the same as for voltage feedback amplifiers. The input stage resembles that of most actual current feedback amplifiers with a high impedance non-inverting input and a low impedance inverting input. The slew rate is very high in current feedback amplifiers because large amounts of current can flow in the inverting input, which is then available to charge the compensation capacitor by using current mirrors. The current mirrors in the ADSpice model is actually the voltage controlled current sources in the gain stage. These sense the voltage drops across the input stage resistors (R1 and R2) and translates this into a current to charge C3. By making the value of G1 and G2 equal to the reciprocal of R1 and R2, the currents will be identical. Clamping the voltage drops across R1 and R2 limits the total current and thus the amplifier's slew rate.

One of the unique properties of current feedback amplifiers is that the bandwidth is a function of the feedback resistor and the internal compensation capacitor C3. The lower the feedback resistor, the higher the bandwidth. The lower limit of the resistor is the value at which the part oscillates. Because the model also includes the low impedance inverting input, it will accurately mimic the actual parts behavior as the resistor is altered. Figure 13.12

## CURRENT FEEDBACK AMPLIFIER INPUT AND GAIN STAGE

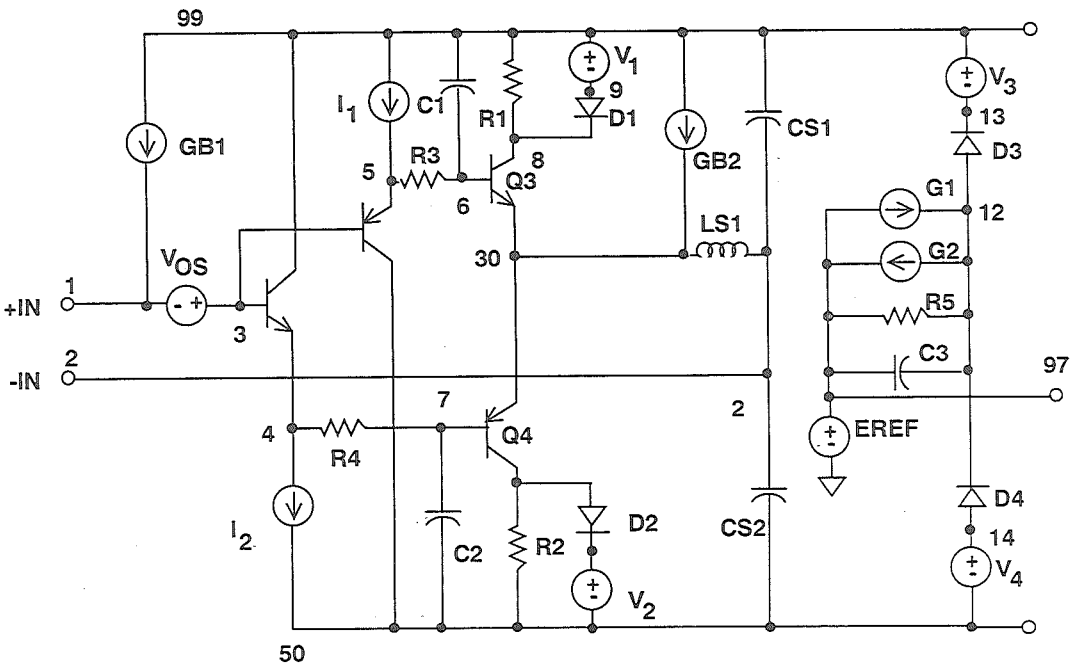



Figure 13.11

compares the ADSpice model to the actual device for an AD811 video amplifier. As the graphs show,the ADSpice model accurately predicts the gain roll off at the much lower frequency for the 1kΩ feedback resistor than for the 500Ω resistor.

The current feedback amplifier input stage is yet another enhancement to the ADSpice model that further increases its flexibility in modelling different types of devices to increase a design cycle's speed.

## VOLTAGE REFERENCE MODEL

ADI is committed to continually expanding the library into new device types to make complete system analysis possible. One recent addition is a voltage reference model. This model was designed to accurately simulate most reference parameters such as DC accuracy, output noise, temperature drift, turn on time, and transient load settling time. The topology is actually very simple, consisting of an ideal 1.23V bandgap reference voltage, a gain stage, and an output stage as labelled in Figure 13.13. Again the macromodel approach is used to simplify the development and speed the simulation time. For example, the bandgap reference is simply a current source and a resistor to develop the required 1.23V. The additional controlled sources accurately predict line and load regulation. This is a great simplification of the actual device, without sacrificing accuracy.

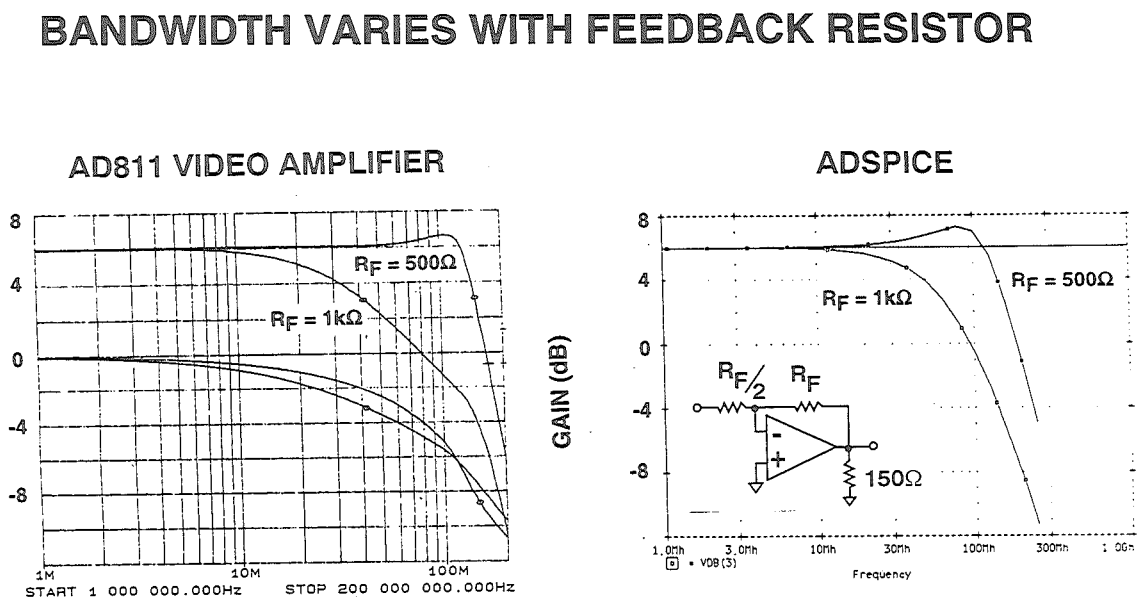



Figure 13.12

# ADSPICE VOLTAGE REFERENCE MODEL

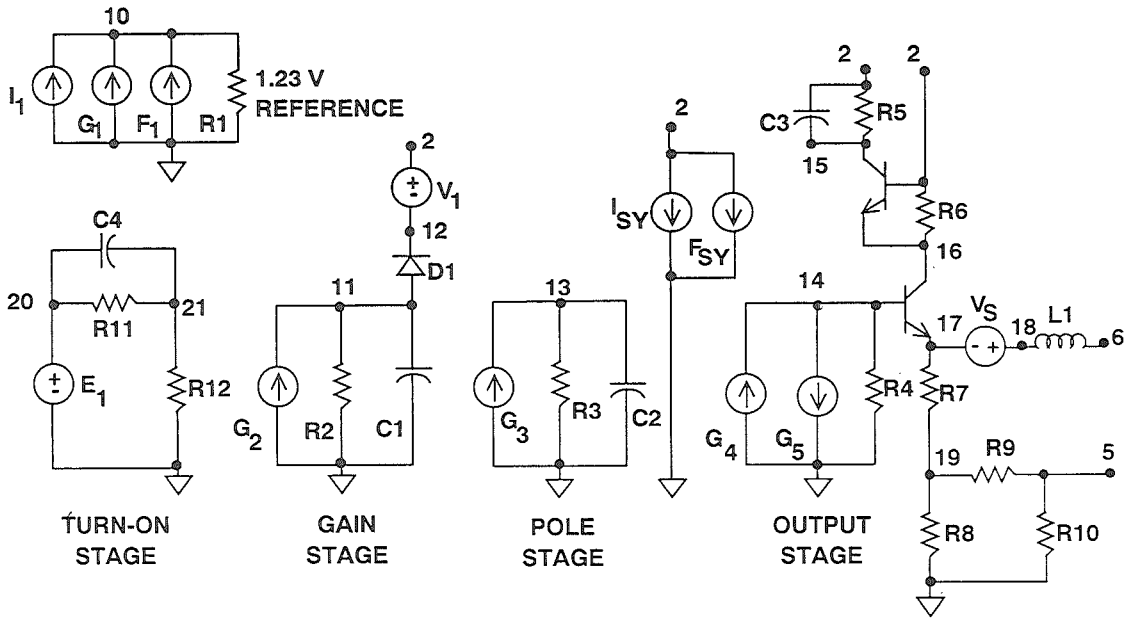
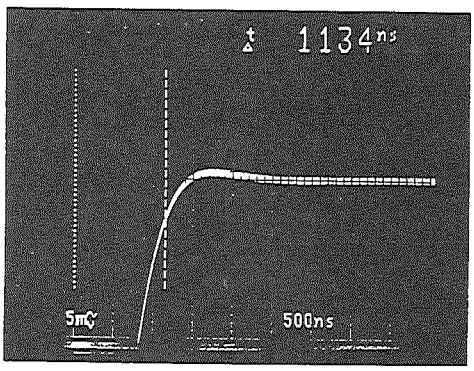


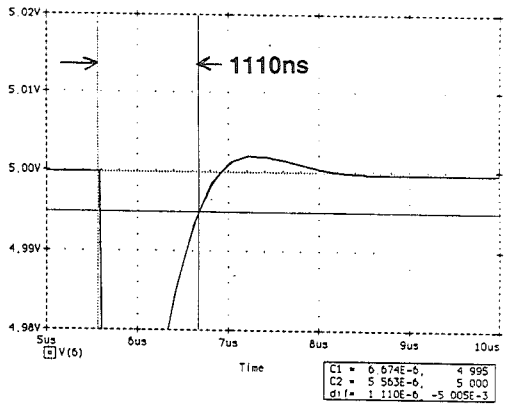

Figure 13.13

# TRANSIENT LOAD RESPONSE

REF-02




ADSpice




SETTLING TIME TO 0.1% FOR A 1mA STEP IN LOAD CURRENT

Figure 13.14

An important characteristic for voltage references is their ability to recover from transient load current pulses on their outputs. For example, some analog to digital converters produce a step change in load current on the reference during conversion. In such a case the reference needs to settle to its correct output voltage before the next conversion decision. This can affect the accuracy of the system making it important for the reference model to predict this. Figure 13.14 compares the response to a 1mA step change in the output current of the REF-02 to the SPICE model of the part. The two results show excellent agreement.

Another key parameter that can affect the accuracy of a system, especially as the resolution increases, is the output voltage noise. By properly setting the internal impedance of the 1.23V reference stage, the model can accurately simulate output noise. Figure 13.15 shows the broadband noise as well as the total noise for a 0.1 to 10Hz bandwidth. This correlates to the typical data sheet specification for the REF-02 noise of 10μVp-p, by using the standard multiplication factor of 6 to convert RMS to peak-to-peak noise.

Voltage references are required to maintain their accuracy over the full operating temperature range of the system. Thus, the drift needs to be very low, and any SPICE model needs to be able to predict this critical parameter. This is easily done by adding temperature dependance to the resistor in the bandgap reference stage. Temperature dependency in resistor models is a standard feature for all versions of SPICE and is set as follows:

```
R1  10  4  1000E3  [TC = 3E-6]
```

where the TC coefficient is the change in resistor value per degree Celsius. This

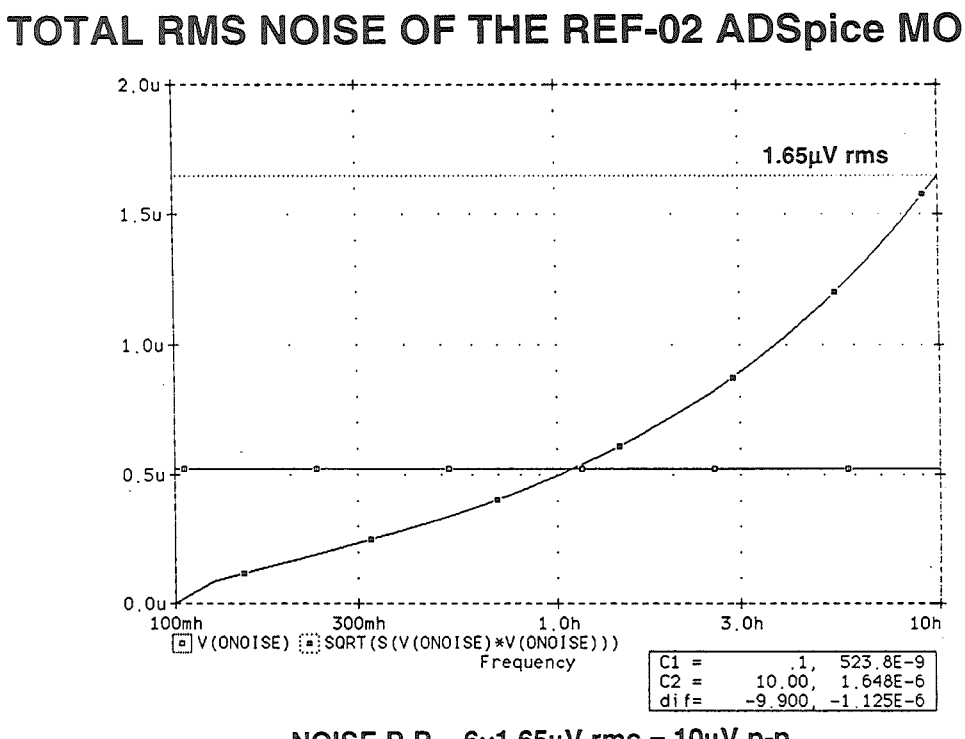


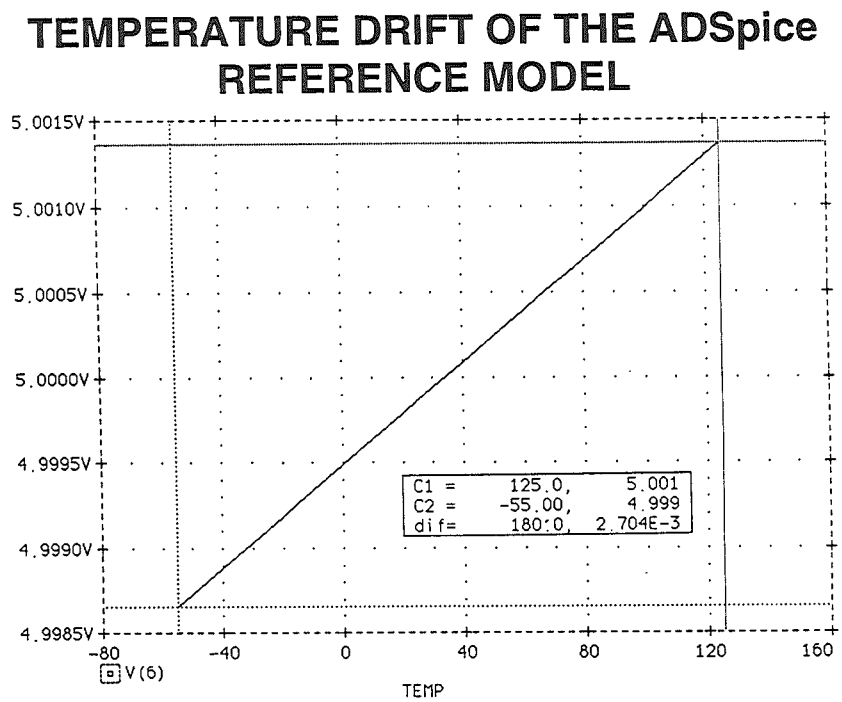

Figure 13.15

produces a linear variation of the output voltage with temperature. The actual device does have a somewhat non-linear temperature variation, but simplifying this to a linear coefficient still gives a good indication of the overall variation. The output plot in Figure 13.16 shows the typical temperature drift, which matches the data sheet parameter of 3ppm/°C. This new model is a complete reference model that yields accurate results under many real world input and loading conditions. Furthermore, it is one more significant piece in a system level analysis.

## ANALOG MULTIPLIER MODEL

Like the voltage reference model, ADI has also developed the world's first analog multiplier macro model based on the AD734, a wideband, 4-quadrant analog multiplier. The development of the model offers significant benefits to system designers. Predicating the behavior of analog functions such as modulation/demodulation, frequency doubling, and high-speed RMS-to-DC conversion is a complex task by analytical means. However, with the new model, designers can, by computer simulation, quickly evaluate complex circuit responses under real world transient and small-signal conditions, thus saving time during the design cycle.

The topology of the macro model follows very closely to the block diagram of the AD734 which is shown in Figure 13.17. Each subsection of the model, including the denominator control and an internal voltage reference, was designed using techniques developed for the



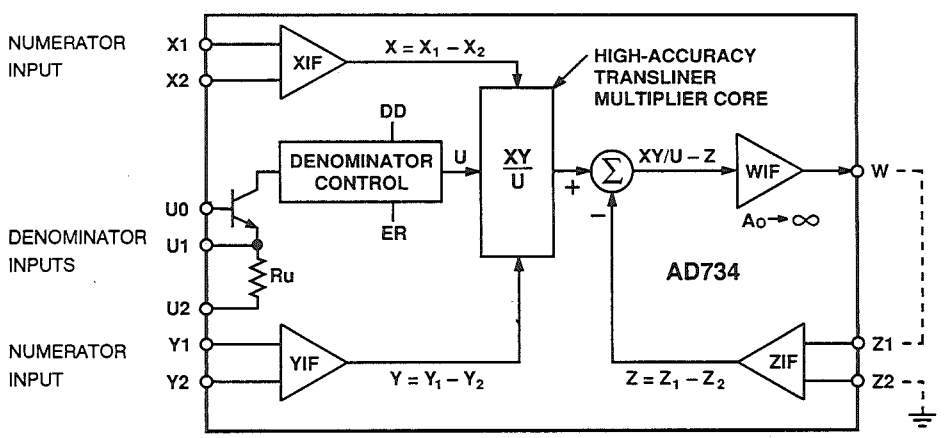

$$\text{TEMPERATURE DRIFT} = \frac{\Delta V_{out}}{\Delta T} = \frac{2.704V}{180°C} = 15\mu V/°C = 3ppm/°C$$

Figure 13.16

ADSpice op amp model. Only controlled sources and as few active devices as possible are used throughout the model to speed simulation time. For example, the macro model's input X-, Y-, and Z-interfaces were designed using only resistors, capacitors, and controlled sources to model the AD734's input offset voltages, input bias currents, common-mode rejection, and 40-MHz input bandwidth. Similarly, the design of macro model's output amplifier (the AD734's W-interface) was based on the op amp macro model's gain and output stage topology and accurately predicts the AD734's output voltage swing, open-loop voltage gain, short circuit current, 10 MHz 3-dB bandwidth, and 450-V/μs slew rate.

At the heart of the AD734 is a translinear multiplier core which exhibits a 250 MHz gain-bandwidth product and is based on the Gilbert multiplier cell. In its monolithic form, the AD734's core requires approximately 50 active and passive components to derive the transfer function, W = XY/U. Using a transistor level model for the translinear core would slow simulation time down so much as to make computer analysis of complex analog functions (for example, a frequency doubler) very CPU intensive and time consuming. As shown in Figure 13.18, the macro model's multiplier core was synthesized using only 8 ideal components to derive the same transfer function and gain-bandwidth product.

## AD734 MULTIPLIER BLOCK DIAGRAM




$$W = \left[\frac{(X1 - X2)(Y1 - Y2)}{U1 - U2} - (Z1 - Z2)\right] A_0$$

Figure 13.17

To understand how the multiplier core works, KVL equations will be used. The voltage at node A is given by:

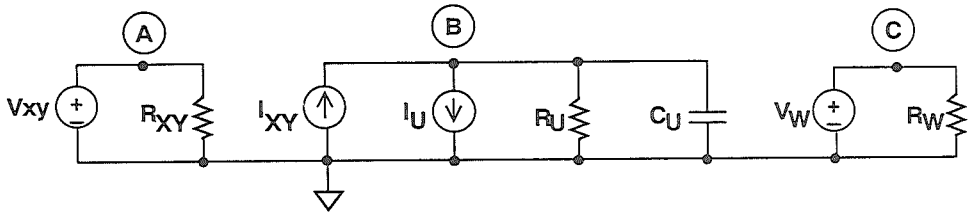
$$V_A = E_{XY} \cdot (V_{X1} - V_{X2}) \cdot (V_{Y1} - V_{Y2}) = V_{XY}$$

where the coefficient of $E_{XY}$ is set to 1.

To arrive at the KVL equation for node B, $V_A$ is first converted to a current by $G_{XY}$, such that $I_{XY} = G_{XY} \cdot V_A$. Then, a second controlled source, $G_U$ (a second order polynomial), is used to generate a current such that $I_U = G_U \cdot (V_U \cdot V_B)$. The KVL equation at Node B is given by:

$$V_B = R_U \cdot (I_{XY} - I_U)$$

## AD734 SPICE MACRO MODEL MULTIPLIER CORE WITH 250 MHz GAIN-BANDWIDTH PRODUCT




- KVL @ Node A: $V_A = E_{XY}[(V_{X1}-V_{X2}) \cdot (V_{Y1}-V_{Y2}) = V_{XY}$
- KVL @ Node B: $V_B = R_U(I_{XY} - I_U)$

$$V_B = \frac{R_U \cdot G_{XY} \cdot V_U}{1 + R_U \cdot G_U \cdot V_U} \Rightarrow \frac{V_{XY}}{V_U} = V_{XY/U}$$

- KVL @ Node C: $V_C = V_{XY/U} - V_Z = V_W$

$$W = \frac{XY}{U} - Z$$

Figure 13.18

Substituting $G_{XY} \cdot V_A$ for $I_{XY}$ and $G_U \cdot (V_U \cdot V_B)$ for $I_U$ yields:

$$V_B = R_U \cdot (G_{XY} \cdot V_A - G_U \cdot V_U \cdot V_B)$$

Simplifying the equation by solving for $V_B$ yields:

$$V_B = \frac{R_U G_{XY} V_U}{1 + R_U G_U V_U}$$

Setting $G_{XY}$ and $G_U$ to 1 and $R_U$ to 1E12 simplifies the expression for the voltage at node B to:

$$V_B = = V_{XY/U}$$

Lastly, the AD734 high-gain output op amp nulls the difference between XY/U and an additional input, Z = Z1 - Z2, to generate the final output, W. This is done in the macro model by subtracting the Z input signal from XY/U using another controlled source, $E_W$. Hence, the voltage at node C is given by:

$$V_C = E_W \cdot (V_{XY/U} - V_Z)$$

and, as was done for $E_{XY}$, the coefficient of $E_W$ is set to 1.

To complete the multiplier core, a capacitor, $C_U$, was added across $R_U$ to model the 250 MHz gain-bandwidth product of the AD734. The versatility of the AD734 to be configured as a three-variable analog multiplier/divider (shown in Figure 13.19) by using direct denominator control permitted evaluation of the macro model's small-signal response. The model's performance (Figure 13.20b) shows excellent agreement to the actual measured data (Figure 13.20a) for four denominator settings.

# THREE VARIABLE MULTIPLIER/DIVIDER USING DIRECT DENOMINATOR CONTROL

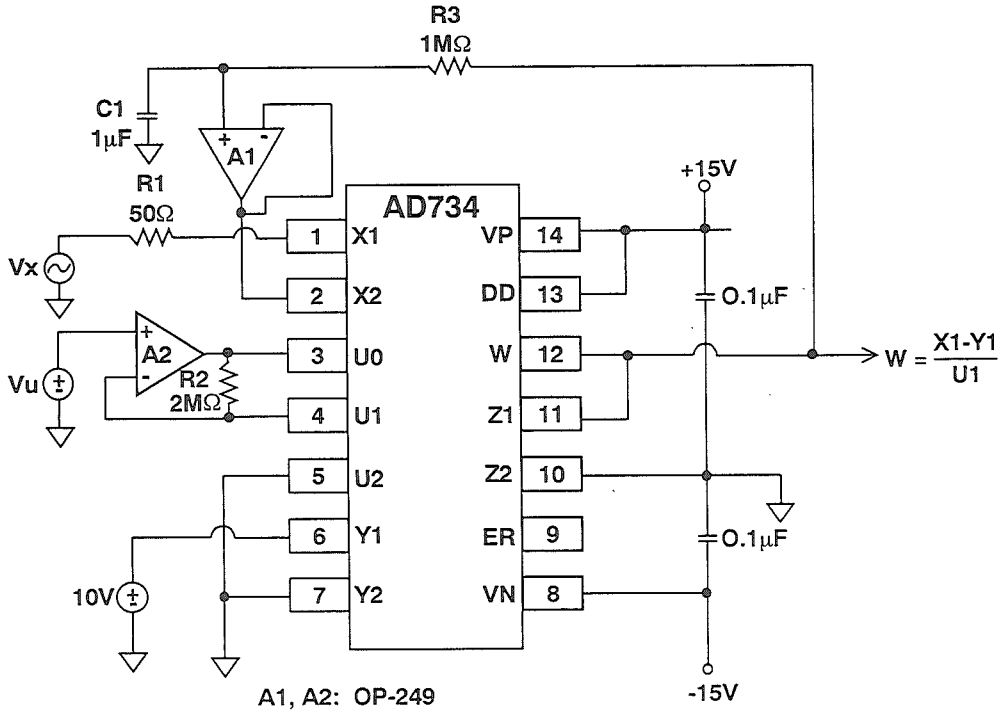



Figure 13.19

# SMALL SIGNAL AC RESPONSE COMPARISON FOR AD734 THREE-VARIABLE MULTIPLIER

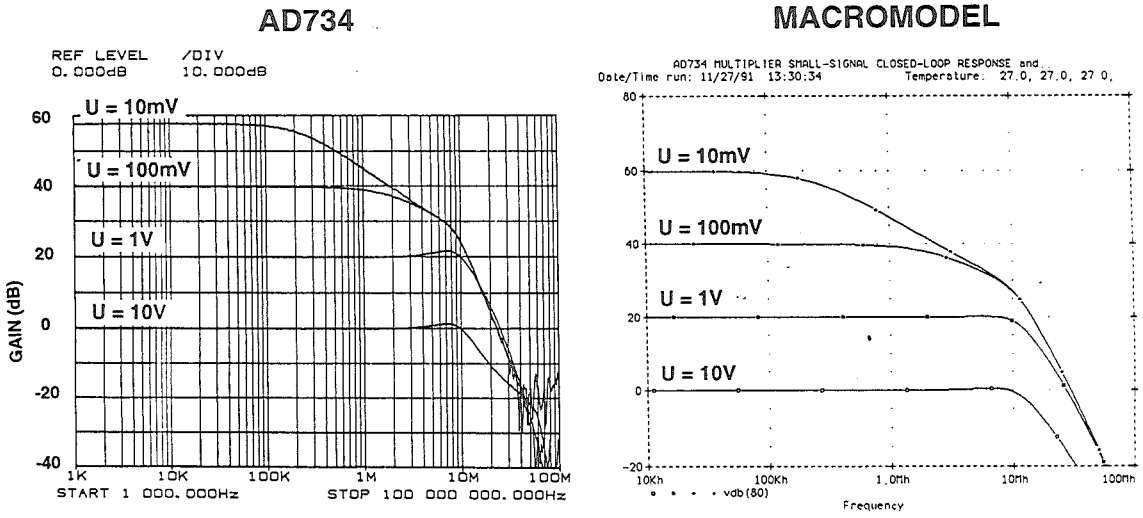



Figure 13.20

In avionics and communications, one of the most important characteristics of an analog multiplier is its transient response. It is important in these applications that an analog multiplier exhibit high slew rates to maintain high full-power bandwidths with low distortion. The AD734 is the ideal device for these applications and the macro model accurately simulates the AD734's transient response. The comparisons were done using the circuit in Figure 13.21 where the load circuit consisted of 500 ohms in parallel with 20 pF. The use of frequency shaping stages in the macro model permitted custom tailoring of the AD734's small-signal and transient response with a high degree of accuracy, as Figure 13.22 shows.

It is the accurate modeling of AD734's small-signal and transient response, as well as incorporating its DC parameters, that makes the macro model a very powerful tool in evaluating and analyzing complex analog circuits and systems. Accurately predicting real circuit behavior under small-signal and transient conditions provides a high level of confidence in the design of an analog system. To this end, Analog Devices is committed to developing new macro models for other non-linear analog building block circuits.

## CIRCUIT DIAGRAM OF THE AD734 USED TO EVALUATE TRANSIENT RESPONSE

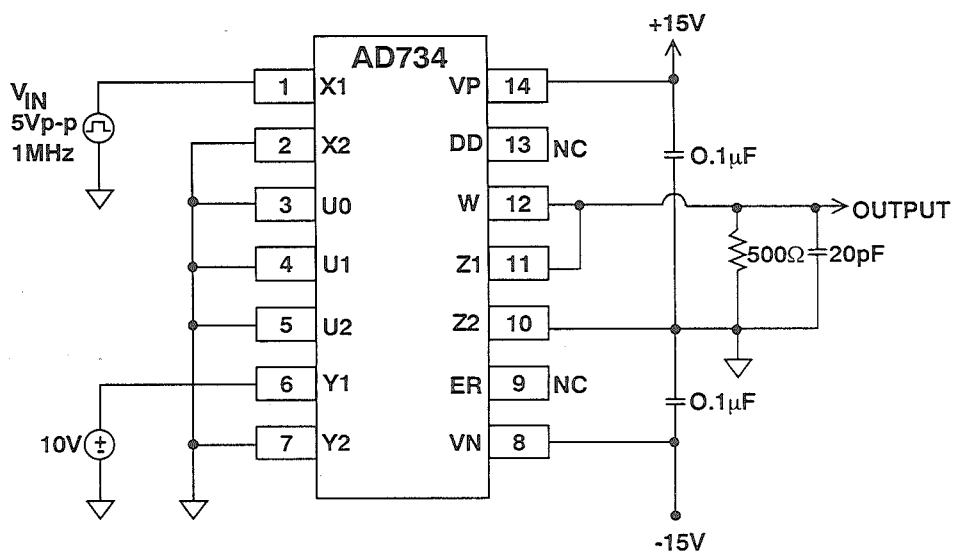
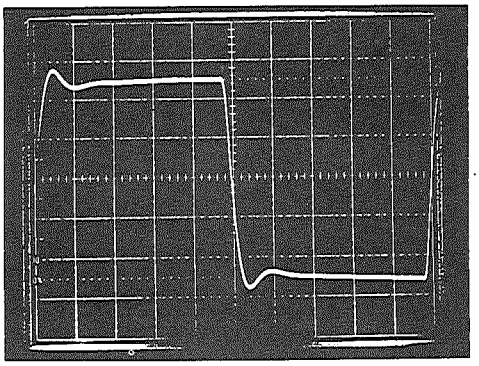



Figure 13.21

# AD734 ACTUAL VERSUS SIMULATED TRANSIENT RESPONSE COMPARISON

**AD734**



**VERTICAL = 1V/div.**
**HORIZONTAL = 100ns/div.**

**MACROMODEL**

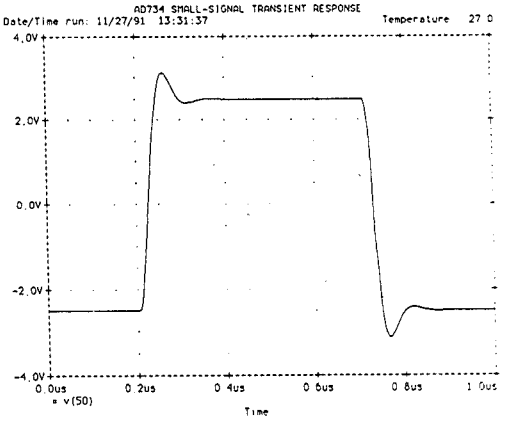



**Figure 13.22**

## SIMULATION DOES NOT REPLACE BREADBOARDING

No matter how accurate the model is, or how much confidence there is with the simulation, SPICE does not replace breadboarding. In the layout and the actual device, there are many second and third order effects that are caused by such things as parasitic capacitances, inductances, and resistances, and it is nearly impossible to include all of these effects in a simulation. Furthermore, no macromodel includes all characteristics of an op amp. For example, exceeding the input voltage range can cause non-linear behavior in an op amp, which is not necessarily included in its model. Because of such effects that a simulation might not predict, it is necessary to breadboard the circuit.

Even with a model as comprehensive as the ADSpice macromodel, other external effects can cause the circuit to work improperly. For example, PC board parasitics can significantly alter the frequency performance, especially for high speed designs. A few picofarads of stray capacitance can easily exist between the input traces and the ground plane. While this may make no difference in lower frequency circuits, at high frequencies this could make the difference between a circuit that is stable and one that oscillates. Such parasitics are easily overlooked in a SPICE simulation, but a breadboard can reveal the instability. Ultimately, simulation and breadboarding should be used together to maximize the design efficiency.

## BREADBOARDING AND SPICE

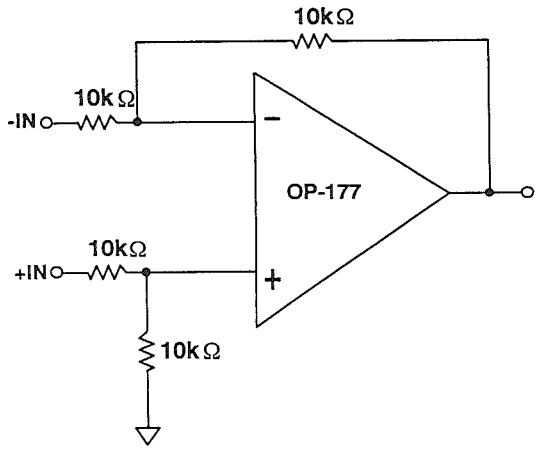
- Use Breadboarding as THE Final Design Verification
- Be Aware of Op Amp Characteristics that are not Modelled
- Pay Attention to PC Board Parasitics that could Impact the Circuit's Behavior

Figure 13.23

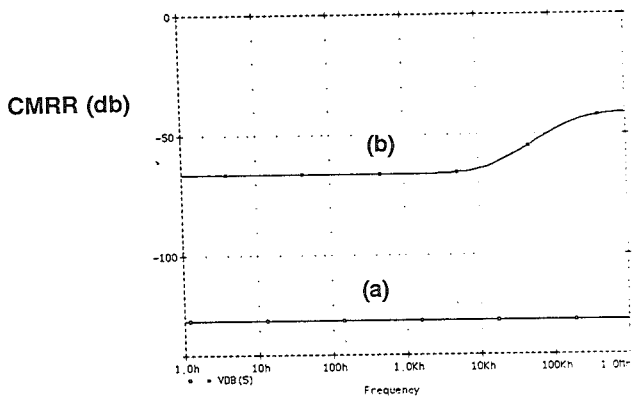
### USE SIMULATION WISELY

Simulation is an extremely powerful tool, but it must be used wisely to realize all its benefits. This includes knowing the models well, understanding PC board effects, and anticipating the results. For example, consider a simple differential instrumentation amplifier (Figure 13.24a) comprised of an op amp and four resistors that needs to be analyzed for common mode rejection ratio(CMRR) performance. The CMRR at low frequencies will be dominated by resistor mismatch and at higher frequencies by the op amp's CMRR performance. However, the simulation will only show this if the external resistors are mismatched and the op amp properly models not only CMRR at DC but also the reduction in CMRR at higher frequencies. If these two important points are overlooked then the bottom plot in Figure 13.24b results. This shows excellent CMRR performance over the entire bandwidth of the circuit. Unfortunately, it is not correct. In contrast, substituting an ADSpice model, which has CMRR modelled as a function frequency, and substituting mismatched resistors results in the top plot in Figure 13.20b Now the picture is very different, showing realistic CMRR performance including the expected rise at higher frequencies.

# KNOW WHAT IS AND IS NOT MODELLED




CMRR Test Circuit




(a) Resistors not mismatched and SPICE model not complete.

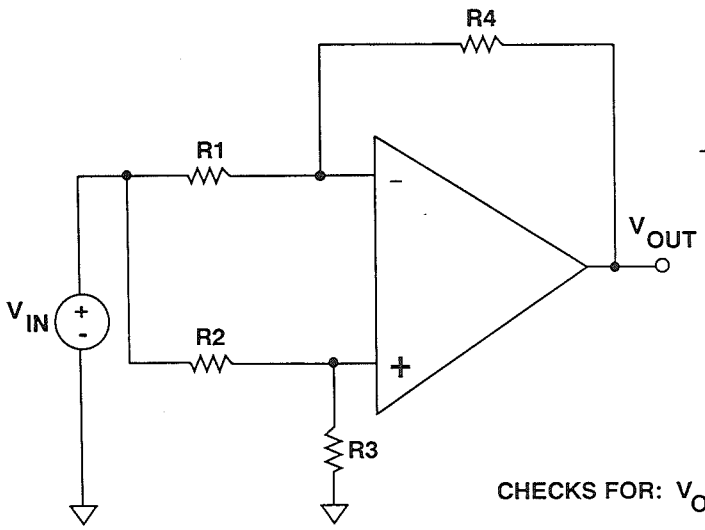
(b) Resistor with 0.1% tolerance and OP-177 ADSpice model includes CMRR vs. Frequency.

Figure 13.24

## KNOW THE MODELS

The above example illustrates the importance of knowing the goals of a simulation and evaluating the models accordingly. In fact, one of the first steps in doing a simulation should be to check each model for its accuracy and what is included. Perhaps even more important is to understand what is not modelled in order to anticipate situations where the simulation may not yield the correct results. The best way to check a model is to actually perform simulations and check the results. Figure 13.25 shows a simple configuration to check DC parameters such as offset voltage and input currents. The accompanying table shows the values for the resistors and the resulting output. For the first three tests no input voltage source is needed, and the input resistors are tied to ground. A value of 0Ω in the table indicates a short, and infinity Ω indicates an open. The DC bias solution for the output voltage gives the result listed for the first three tests. The CMRR test is the only one that requires an AC sweep over the frequency range of the amplifier. This test reveals both the DC value and the high frequency roll off if it is included, as in the ADSpice models. Similar simple tests can be devised to check many other DC and AC parameters.

# A SIMPLE TEST CIRCUIT FOR DC PARAMETERS



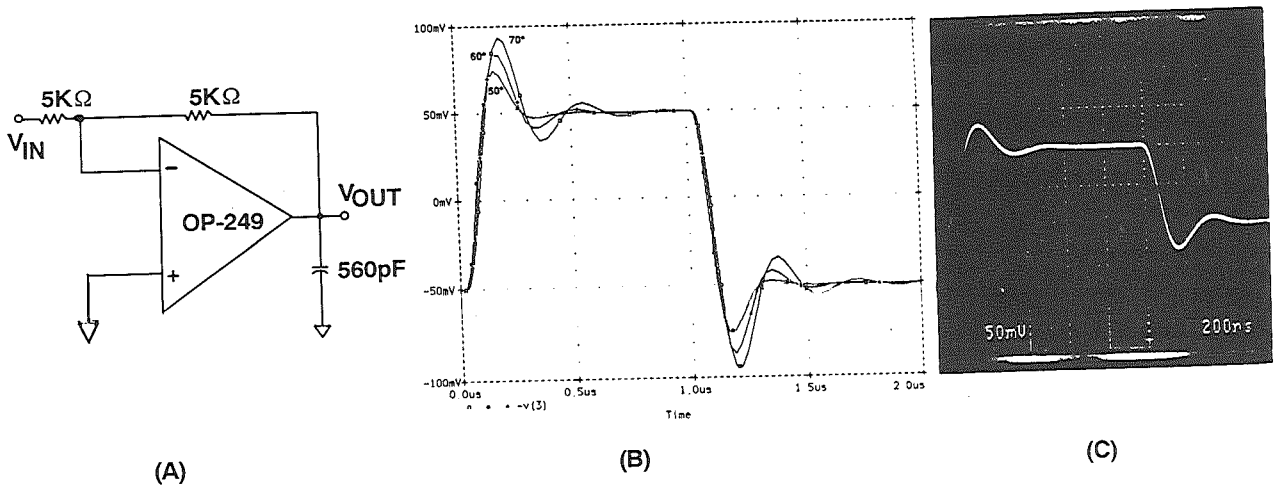

| R1 | R2 | R3 | R4 | $V_{OUT}$ |
|---|---|---|---|---|
| ∞ | ∞ | 0 | 0 | $V_{OS}$ |
| ∞ | ∞ | 1MΩ | 0 | $I_B = V_{OUT}/R3$ |
| ∞ | ∞ | 1MΩ | 1MΩ | $I_{OS} = V_{OUT}/R3$ |
| 10kΩ | 10kΩ | 10kΩ | 10kΩ | CMRR |

Figure 13.25

The gain and phase margin of a circuit determines many important performance characteristics such as overshoot, settling time, and oscillation. For the simulation to accurately predict these parameters, the model must have an accurate open-loop gain and phase response. Having an accurate AC SPICE model increases the confidence level that the desired response of the actual circuit will behave close to the simulation results.

Using a simple inverting amplifier configuration, the open-loop gain and phase can be determined by dividing the output voltage by the error voltage on the inverting input. The simulation output can then be compared to data sheet graphs. Unfortunately, many data sheets only show the amplifier's dominant pole. This leaves many questions about the actual characteristics of the gain and phase, especially near the op amp's unity gain crossover. The same test can be performed on the actual device using a network analyzer; however, this may not be a feasible option. Fortunately, a transient response test reveals much of the same information in the amount of overshoot, frequency of ringing, and the damping characteristics.

# TRANSIENT RESPONSE REVEALS PHASE MARGIN




(A) (B) (C)

• 60° phase curve agrees with actual device

**Figure 13.26**

Figure 13.26 shows the transient response of the OP-249 SPICE model with a capacitive load to induce ringing. The phase margin is adjusted for the different simulations as labelled next to each curve. As can be seen, a 10° decrease in phase margin leads to a significant change in the amount of overshoot and frequency of ringing on the output. A photo of the actual device's performance is also shown for comparison, which shows good agreement with the 60° curve. This result correlates with comparisons of the frequency response of the OP-249 to its SPICE model, which both show a phase margin of 60°. Thus, checking the transient response can reveal the accuracy of a model's phase response.

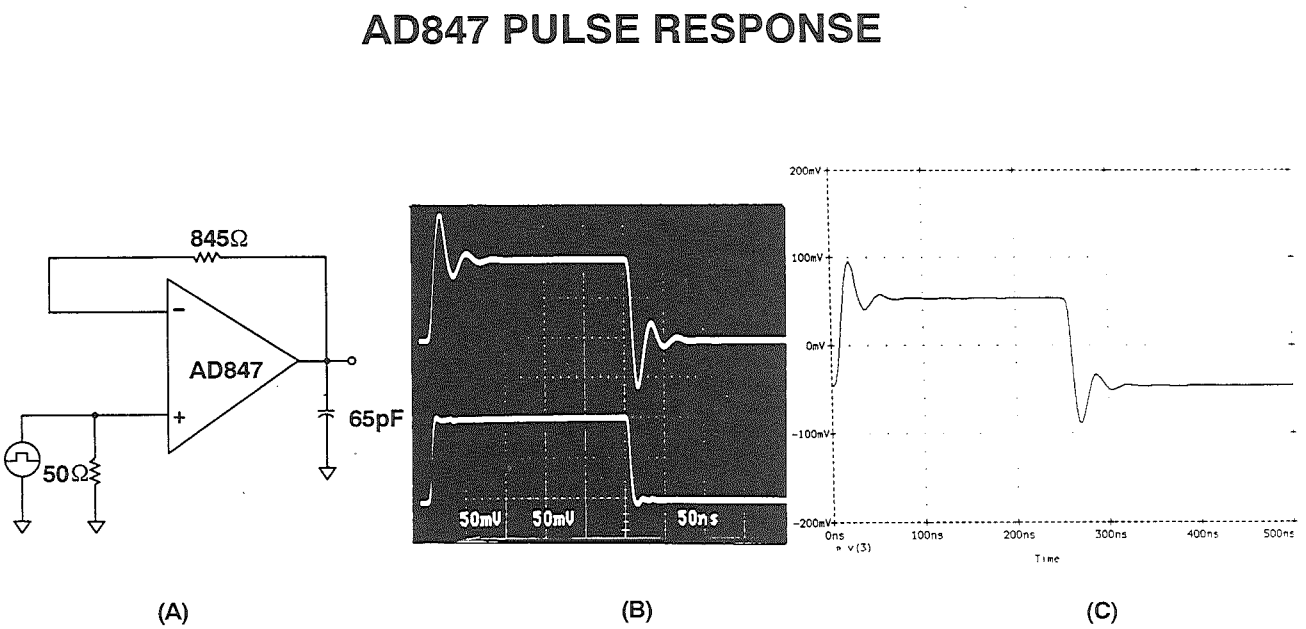
The small signal transient response is one of the most important of all the tests in determining a model's AC accuracy. Even if a network analyzer is available to check the frequency response, the small signal pulse response should still be compared. It is also informative to check how the model behaves with a capacitive load. Placing varying capacitances on the output and looking at the change in overshoot and ringing further verifies the model.

Using the above tests, an op amp macromodel, regardless of source, can be checked for accuracy. Further tests can be devised for other op amp parameters that may be important for a particular simulation. All of which is important because knowing the model's capabilities ahead of time can help prevent many headaches later.

## UNDERSTAND PC BOARD PARASITICS

Even if the model passes all the above tests, caution still needs to be exercised. As discussed above, PC board parasitics can have significant impact on a circuit's performance. This is especially true for high speed circuits. A few picofarads of capacitance on the input node can make the difference between a stable circuit and one that oscillates. Thus, these effects need to be carefully considered when simulating the circuit to achieve meaningful results.

To illustrate the impact of parasitics, the simple circuit shown in Figure 13.27 was built twice, first on a carefully laid out PC board and second on a plug-in type of protoboard. The AD847 is used because of its wide bandwidth of 50 MHz, which makes any parasitics much more critical. The properly laid out PC board has a clean response with less overshoot and ringing (Figure 13.27b). The SPICE model results are in close agreement with the actual circuit showing an accurate simulation (Figure 13.27c). On the other hand, the circuit built on the plug-in board shows much worse performance and no agreement with either the PC board or the SPICE model (Figure 13.28a). However, when PC board parasitics are included in the SPICE file, the simulation results do agree with the actual circuit (Figure 13.28b). This example illustrates two points. One, board parasitics can make the actual circuit behave much differently from the SPICE model, and two, a clean layout that minimizes parasitics is very important for high speed designs. One interesting point is that the simulation can be used as a rough measure of the PCB layout design. If the simulation, without any parasitics, agrees with the PC board, then there is a reasonable assurance that PC board is well laid out.

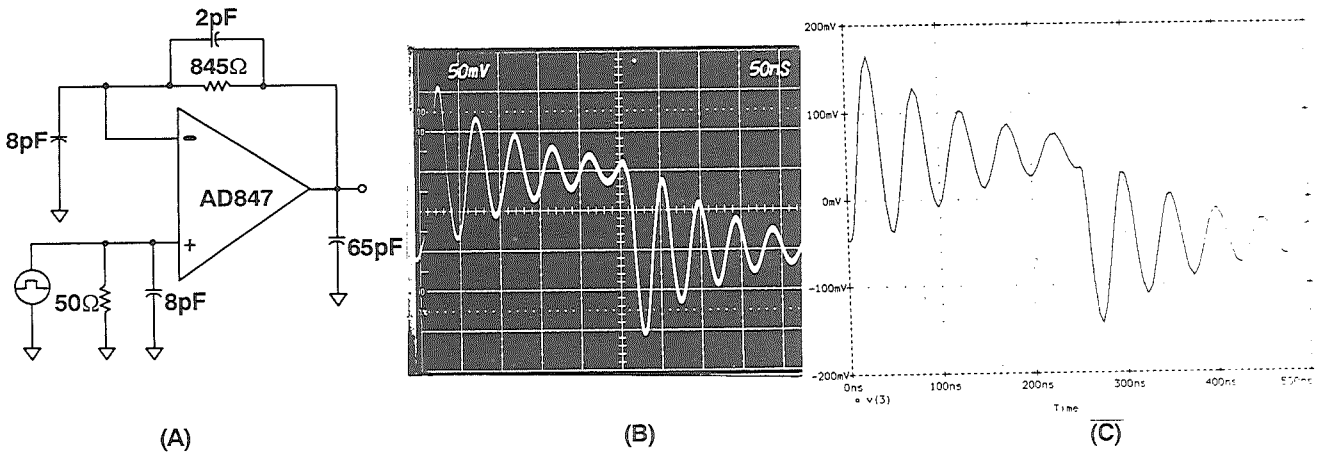



Properly laid out PC board and simulation agree closely

13

Figure 13.27

# PC BOARD PARASITICS WILL ALTER THE RESULTS




- Parasitic capacitances worsen the circuit's response
- Properly modelling the parasitics in SPICE yields good results

Figure 13.28

Parasitic PC board elements are not the only area that may cause differences between the simulation and the breadboard. Perhaps the circuit exhibits nonlinear behavior during power-on that will cause a devices to lock-up. Perhaps the device will oscillate due to insufficient power supply decoupling or lead inductance. It is impossible to anticipate all normal or abnormal operating conditions that an amplifier could be subjected to. Thus, it is very important the circuit be breadboarded and thoroughly checked in the lab. Careful forethought and design will help minimize any unknown problems from showing up when the circuit is manufactured.

## SIMULATION SPEEDS THE DESIGN CYCLE

While simulation cannot replace breadboarding, the two can be used together to increase the efficiency of a design cycle. Simulation is very effective in the initial design phase to try out different ideas and circuit configurations. When a circuit topology has been decided upon and tested in SPICE, then a breadboard can be built. If the simulation was done carefully, the breadboard has good likelihood of working correctly without significant modifications. When the simulation and the actual results correlate, then the circuit can be easily altered in SPICE to perform many different types of analysis. For example, it is much easier to try to optimize the circuit in SPICE then it is to repeatedly modify the breadboard. Quick substitutions of the op amps and components can be made in SPICE and the results immediately viewed. Worst-case and sensitivity analysis can also be done in SPICE easier then on paper or on a breadboard. Using multiple SPICE runs, the sensitivity to a certain parameter can be determined.

## SPICE SAVES DESIGN TIME

- **Quickly Checks Circuit Ideas**
- **Eases Circuit Optimization**
- **Alter Component and Model Parameters for Worst Case Sensitivity Analysis**
- **Quickly Check Different Op Amps**

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Figure 13.29

There are many ways in which SPICE and the ADSpice macromodel make the design task easier. SPICE is a very effective design tool if it is used with forethought, understanding, and caution. The complete ADSpice library is available on a 1.2Mbit, 5-1/4" IBM PC compatible diskette. Contact your local sales office or the Analog Devices Literature Center for your free copy. The complete list of all 300 models on the "Release F, 4/92 version of the diskette is shown in Figure 13.30.

## ADSpice Release F, 4/92

AD624
AD624A
AD624B
AD624C
AD624S
AD630 *
AD630A *
AD630B *
AD630J *
AD630K *
AD630S *
AD645 *(N)
AD645A *(N)
AD645B *(N)
AD645J *(N)
AD645K *(N)
AD645S *(N)
AD704
AD704A
AD704B
AD704J
AD704K
AD704T
AD705
AD705A
AD705B
AD705J
AD705K
AD705T
AD706
AD706A
AD706B
AD706J
AD706K
AD706T
AD711
AD711A
AD711B
AD711C
AD711J
AD711K
AD711S
AD711T
AD712 *(N)
AD712A *(N)
AD712B *(N)
AD712C *(N)
AD712J *(N)
AD712K *(N)
AD712S *(N)
AD712T *(N)
AD713
AD713A
AD713B
AD713J
AD713K
AD713S
AD713T
AD734
AD734A *
AD734B *
AD734S *
AD743 *(N)
AD743A *(N)
AD743B *(N)
AD743J *(N)
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AD847A
AD847J
AD847S
AD848
AD848A
AD848J
AD848S
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AD9618
AD9630
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AMP02
MAT02
MAT03
MAT04
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OP160F
OP160G
OP177 (N)
OP177A (N)
OP177B (N)
OP177E (N)
OP177F (N)
OP177G (N)
OP200
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OP200E
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OP21G
OP21H
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OP220C
OP220E
OP220F
OP220G
OP221
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OP221B
OP221C
OP221E
OP221G
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OP249E
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OP249G
OP260
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OP497G
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OP64
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OP77E (N)
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OP77G (N)
OP90
OP90A
OP90E
OP90F
OP90G
OP97
OP97A *
OP97E *
OP97F *
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REF01A (N)
REF01C (N)
REF01E (N)
REF01H (N)
REF02 (N)
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REF05 (N)
REF05A (N)
REF05B (N)
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REF10B (N)
SSM2131
SSM2210
SSM2220

* Indicates new model since release E, 10/91
(N) Indicates noise model

Figure 13.30

# NOTES

[1] Boyle, Graeme et al, "Macromodelling of Integrated Circuit Operational Amplifiers," IEEE Journal of Solid State Circuits, Vol. sc-9, no. 6, December 1974