SC2200
Hardware Design Guide

UG6338; Rev 0; 9/16

Abstract
This document provides guidelines to enable designers to successfully integrated the SC2200 into their systems.

CONTENTS

List of Figures

List of Tables

1. Introduction

1.1. Purpose

This document provides guidelines and circuit optimization techniques to enable the designer to implement a successful SC2200 hardware integration. Following this document will ease the hardware integration task, using the same techniques as those employed for the SC2200 reference design board. It explains the SC2200 circuit topology, typical power levels, power supply considerations, and SPI hardware used to communicate with the IC.
Section **Error! Reference source not found.** provides an overview of the hardware design kit content while section 2 describes the SC2200 reference designs.
The remaining sections address all design/layout topics in order of priority. The designer should follow the flow described below to ensure optimum integration:

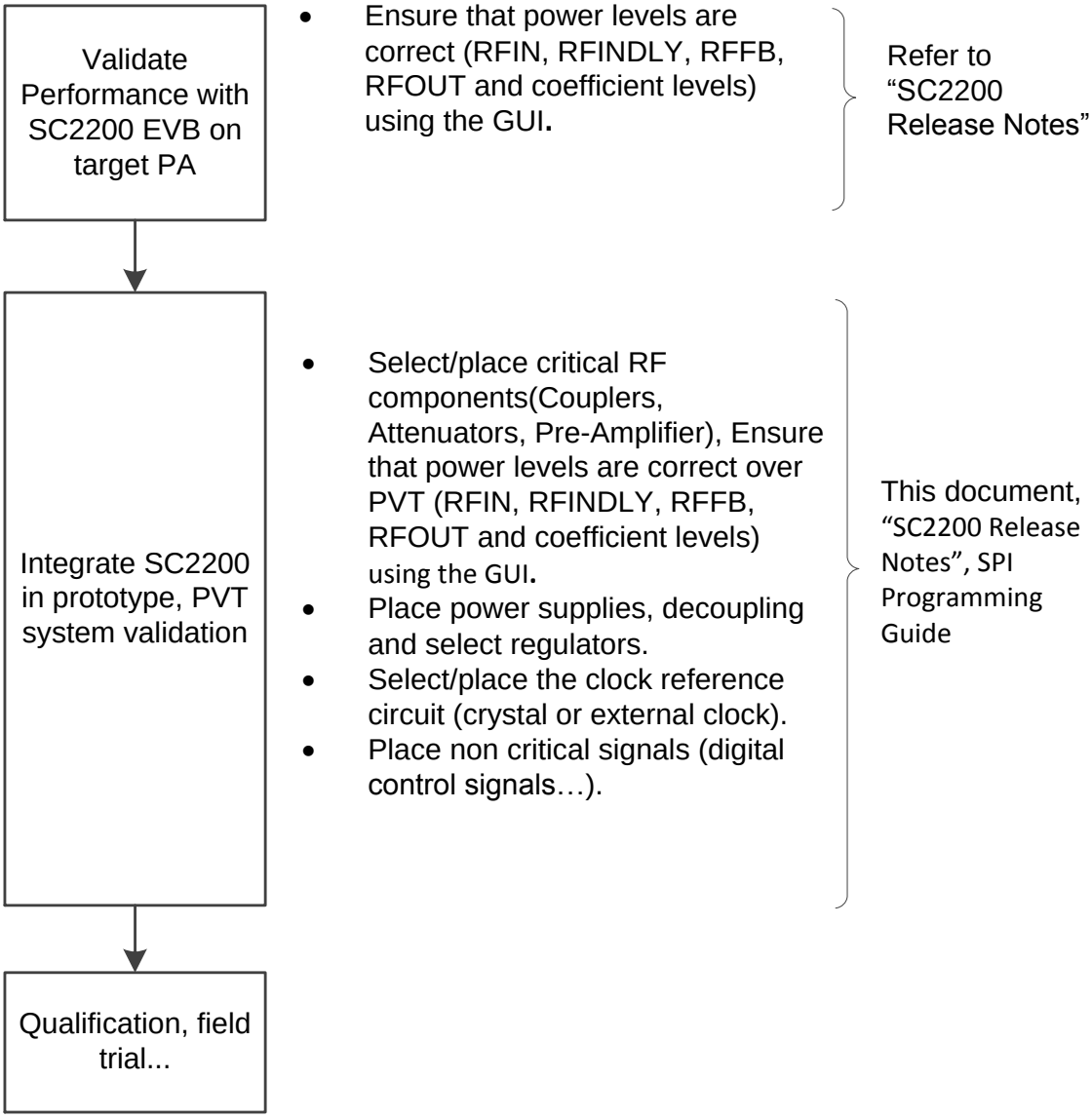


Figure 1: SC2200 Hardware Integration Flow

1.2. Revision History

Revision	Date	Description
0.5	August 2013	Original document
0.6	February 2013	Updated reference design layouts, added spur/noise section, information about usage of AIO and AIN pins
0.8	August 2014	Updated to include the PCB configuration option using the delay line.
1.0	April 2015	Production release
1.1	July 2015	Revised typical spurious signal values and added Reference Design board files.
1.2	June 2016	Fixed typos for DVDDIO range. Added RESETN section. Clarify power sequencing and troubleshooting section.
1.3	September 2016	General edits to remove requirement for NDA to access SC2200 collateral.

1.3. Acronyms

Acronyms	Description
ACPR	Adjacent Channel Power Ratio
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
CAL	FW State: Calibration
CW	Continuous Wave
DAC	Digital-to-Analog-Converter
EEPROM	Electrically Erasable, Programmable, Read-Only Memory
ESR	Equivalent Series Resistance
EVB	Evaluation Board
EVK	Evaluation Kit (Includes EVB, Layout, GUI, BOM)
GPIO	General Purpose Input/Output
GUI	Graphic User Interface (Software to operate RFPAL)
HDK	Hardware Design Kit
LO	Local Oscillator
NTC	Negative Temperature Compensation
PMU	Power Measurement Unit (accurate power detector)
PVT	Process, Voltage and Temperature
RFFB	RF Feedback
RFIN	RF Input
RFINDLY	Delayed RFIN input
RFOUT	RF Output
RFPAL	RF PA Linearizer
SPI	Serial Peripheral Interface
SSSN	SPI Slave Select Enable
XTAL	Crystal

1.4. Reference Documents

1. SC2200 Data Sheet
2. SC2200 Release Notes
3. SC2200 SPI Programming Guide
4. CAD and Layout Reference Design Files

2. SC2200 Reference Design

The SC2200 reference design contains all circuitry necessary for MIMO linearization, including power supply regulation from 5V DC. The PCB uses a single-side 4-layer FR4-06 dielectric design, ideally suited for cost and power consumption sensitive RF applications.

See Figure 2 for the SC2200 Reference Design block diagram for MIMO applications with two paths: path A and path B. In this configuration, the predistortion signal is combined with the input signal within the SC2200. Generally this yields a lower BoM cost, smaller PCB area, and accepts signal levels directly from the transceiver. In this configuration, the additional power consumption of the integral pre-amplifier trades-off directly against the power consumption savings from the eliminated external pre-amplifier.

The RF core layout floor plan is shown in Figure 3. For each Path (*= A or B), the RF input is split into two signals called RFIN* and RFINDLY*. The RFIN* signal is provided to the power detector input (PDET) through a splitter to generate the polynomial function of the RF signal envelope.

In the SC2200 reference design the splitter is realized with a 5dB 0805 sized SMT coupler. However, it can be implemented with SMT couplers or with resistive dividers as long as the data sheet power ranges are met with the PA levels set at the maximum operating power

The polynomial function is generated within the correction block (CORR). When added to the incoming input signal, this function synthesizes the inverse of the PA distortion. The delayed version of the RF input is fed to the RFINDLY* input. The RF delay line is optional for linearizing Class AB power amplifiers. For wide band signals and Doherty power amplifiers, a delay line may be required (Section 3.3). The RFINDLY* input is connected to the RF signal processor and the internal pre-amplifier.

The RFFB* signal is coupled from the PA output using the forward port of the directional coupler. The linearizer uses this signal to adaptively determine the nonlinear characteristics of the PA. This feedback signal is analyzed in the frequency domain to generate a metric used for the adaptation cost function.

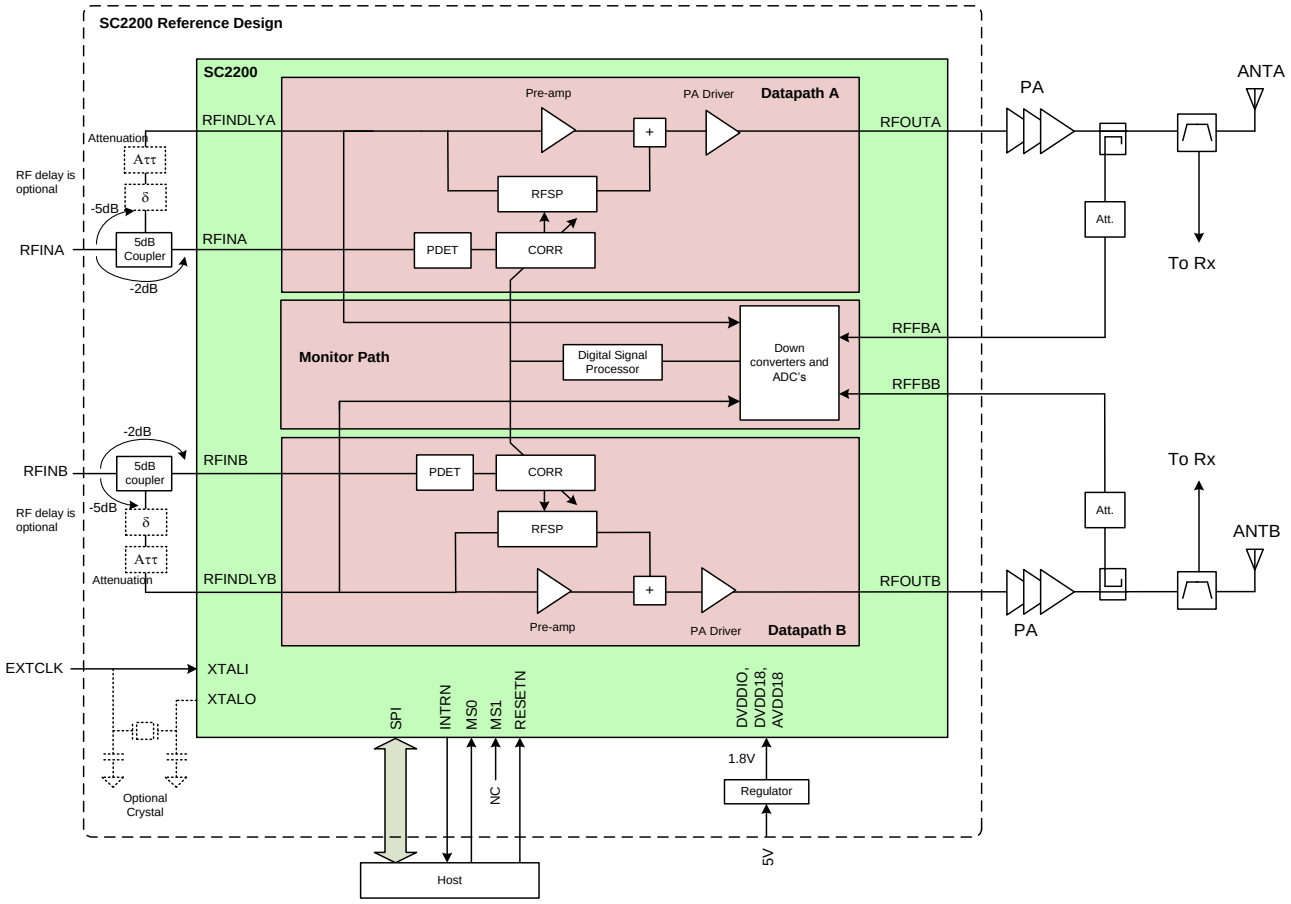


Figure 2: Simplified SC2200 Reference Design Block Diagram

This configuration has the advantage of requiring less input signal into the reference design than the previous generation linearizers. In addition, this configuration only requires one splitter/coupler per path.

2.1. Layout Floorplans

The reference design exhibits the following properties:

- SC2200 without delay line
  - 26 x 24mm, including RF components and decoupling
  - Single-side assembly
  - 4-layer FR4-06 PCB, where only the top layer is impedance controlled
- SC2200 with delay line
  - 26 x 53mm, including RF components, RF delay line and decoupling
  - Single-side assembly
  - 4-layer FR4-06 PCB, where only the top layer is impedance controlled

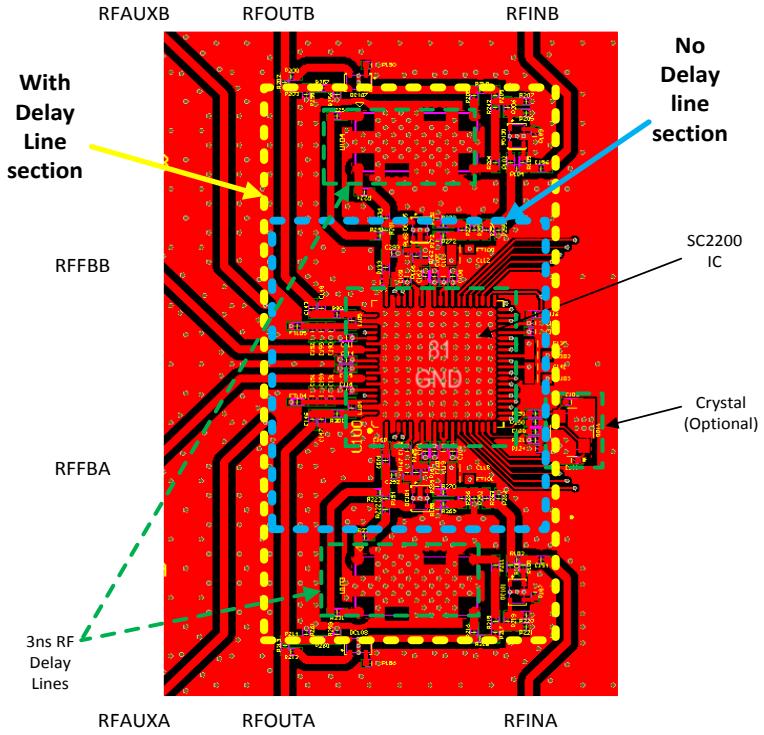


Figure 3: SC2200 Core Layout Floor Plan (with 3ns Delay Lines)

***IMPORTANT**: Although not represented in Figure 3, it is critical to implement a SPI interface connector or test points to allow firmware upgrades or operating parameter changes with the GUI during the system integration, bring up or production. The connector or test points must have the signals listed in section 8.5.*

3. RF Design with the SC2200

This section provides the information to optimize the SC2200 power levels, select the RF delay component (or not) and interface with the RF ports. Although the RF input ports have been designed to be close to 50Ω, matching may be required for some frequencies. The SC2200 RF ports' S parameters are provided as part of the HDK.

3.1. System Signal Power Optimization

This section provides the information to set the SC2200 power levels.

For RFPAL to function optimally, all power levels must be within a required range at all operating conditions when the PA operates at maximum power (temperature, supply voltage and batch-to-batch variations). This range is specified in the SC2200 data sheet . To meet these requirements components determining the power levels (coupler, attenuators, matching networks) must be chosen based on a systematic link budget analysis.

System designers are encouraged to consider temperature variation of each component over hot, cold and nominal conditions.

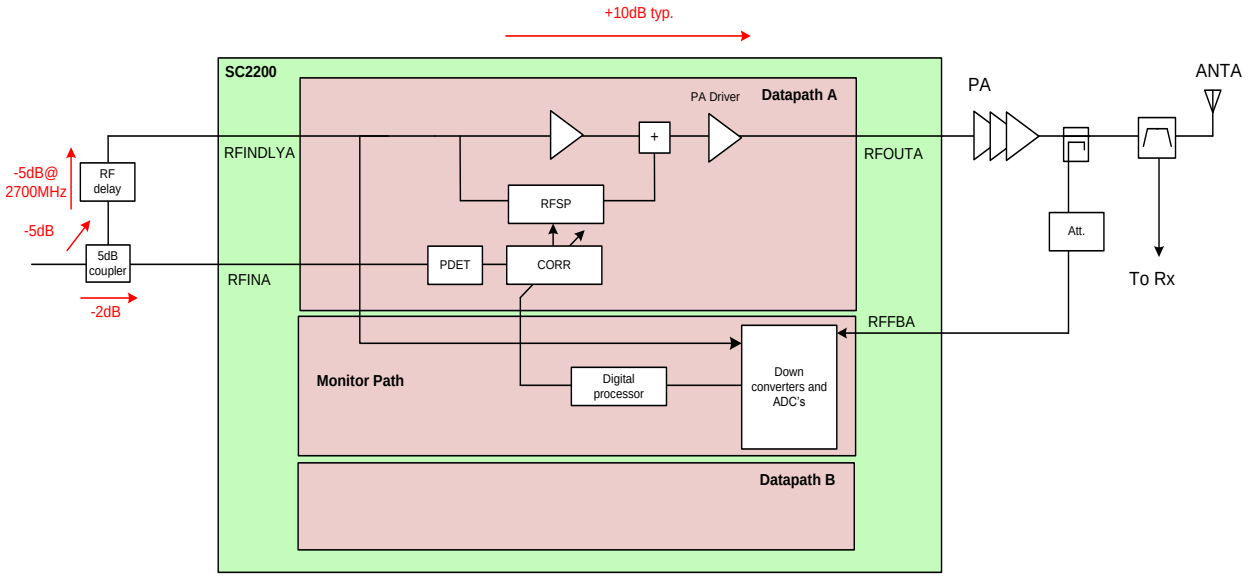


Figure 4: SC2200 with Delay Line RF Circuit Block Diagram

3.2. Temperature Dependent Attenuator Options

Due to temperature dependence of the power amplifier gain the RFOUT power, and therefore RF input power may also change with temperature. The RFOUT power must be kept within acceptable limits for optimum predistortion performance. One way to minimize variation of RFOUT level is to include an NTC (PTC) attenuator between the RFOUT output and the PA (Figure 5).

Layout provisions for resistive pi-attenuators should be included in the design to fine-tune the performance across the temperature range.

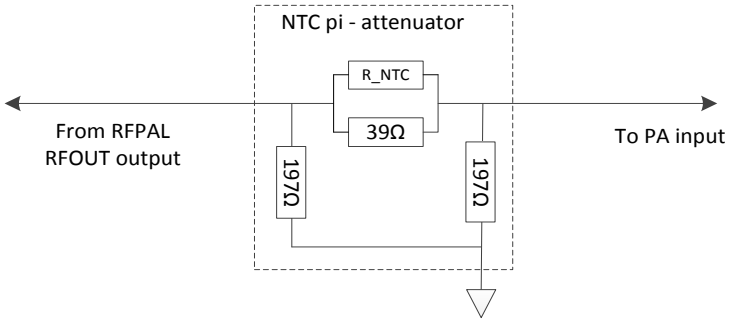


Figure 5: NTC Attenuator

***IMPORTANT**: As described above, it is critical to keep the PA gain variation (including NTC pi attenuator) below +/-1dB over temperature and frequency. Otherwise, the RFIN/RFINDLY data sheet power ranges may not be met.*

3.3. Delay Line Selection

The RF delay is used to align the SC2200 predistortion processing delay with the through path RF signal. The external delay must be close to the SC2200 memory polynomial average delay to fully take advantage of the integrated memory effect compensation.

For most Doherty PAs and wideband class AB PAs, the optimal delay is approximately 3ns; however, we encourage experimentation with this value for each new PA design and after any PA tuning. For class AB PAs amplifying more narrowband signals (BW ≤ 20MHz, typ), the delay line can be replaced by 4dB attenuation with acceptable performance.

The relative power levels between RFIN and RFINDLY shall be maintained at all frequencies:

***IMPORTANT**: If a delay line is not used in the design, place a 4dB attenuator in the RFINDLY RF path.*
The insertion loss of a delay line is not high enough at 900MHz. For designs in this frequency band, place a 2dB attenuator in the RFINDLY RF path. (The relative power levels between RFIN and RFINDLY shall be maintained.

We recommend the following delay lines that are available from RN2 and Anaren:

- XDL15-3-030S by Anaren (3ns): used on evaluation boards.
- DL3 by RN2 (3ns)

The SC2200 EVB's are loaded with the 3ns Anarendelay lines (XDL15-3-030S). Figure 6 and Figure 7 shows the insertion loss and delay versus frequency of XDL15-3-030S and DL3, respectively.

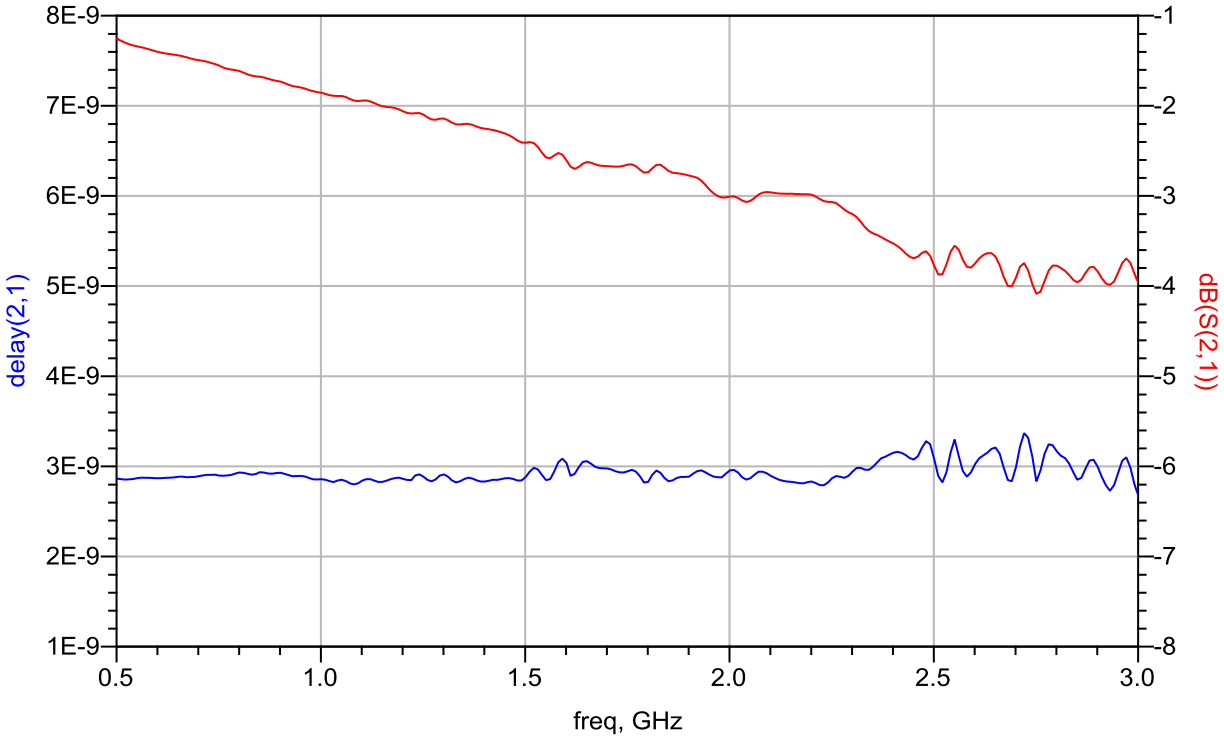


Figure 6: XDL15-3-030S Delay Line Insertion Loss (dB) and Delay (s)

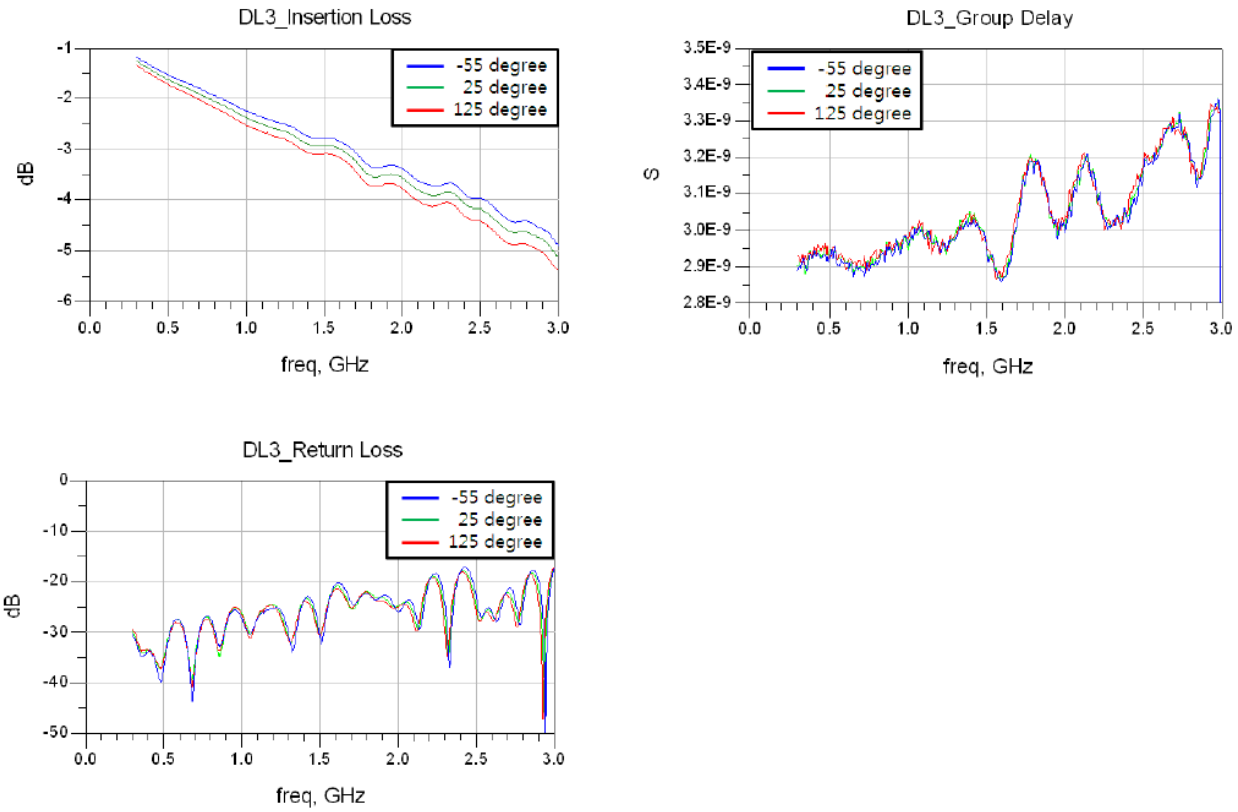


Figure 7: DL3 Delay Line Insertion Loss (dB), Delay (s) and Return Loss (dB)

3.4. RF Feedback Signal (RFFBA and RFFBB)

The SC2200 uses the RFFB ports to monitor the PA's output spectrum, power and linearity.
It is critical to keep a flat gain response between the PA output and the RFFB IC input (<1dB flatness over 3 times the signal bandwidth). This requirement does not apply to the PA output. It only applies to the path from the PA output to the SC2200 feedback input. The RFFB group delay and group delay variation are not critical.
In some systems, if the spurious/noise level outside the correction bandwidth is large, performance may be increased by adding a band pass filter at the RFFB input. The band pass filter bandwidth must be large enough to pass the PA non-linearities and meet the < 1dB flatness over 3 times the signal bandwidth. For example, PA's with large 2nd order harmonic (> -30dBc) can cause performance degradation. Low cost handset SAW filters are good candidates for this filter.

***IMPORTANT**: Spurious signals at the RFFB input may limit correction performance. Close-in (within 100MHz of the center frequency), the spurious/noise level due to external noisy circuits (i.e., not the SC2200) must be 10dB below the final correction. For example, if the ACLR requirement is -53dBc, the spurious level must be ≤-63dBc.*

3.5. RF Auxiliary Inputs (RFAUXA and RFAUXB)

The RF Auxiliary inputs are no longer supported.

3.6. RF Output (RFOUTA and RFOUTB)

The RFOUT pin contains different signals depending on the configurations:

- The RFOUT output carries the amplified RF input signal and the predistortion signal.

RFOUT is an open-drain output. An external choke provides a DC path to the AVDD18 power supply.

IMPORTANT

1. *The supply connection to the choke must be filtered to avoid supply noise leakage into the RFOUT port. We recommend using a ferrite bead in a π network configuration for optimum decoupling. It is especially important to filter out frequencies at the RFIN signal frequency.*
2. *When selecting the ferrite bead, beware of the DC resistance since an 80mA current (max) flows from the RFOUT pin. The DC voltage at the RFOUT pin must meet the data sheet AVDD18 supply limits. The ferrite bead must meet the DC current rating specification of 100mA.*
   For improved filtering, an inductor and capacitor in series to ground can be placed at the supply connection of the choke. The $L_{FILT}C_{FILT}$ combination should resonate at the center of the frequency band (f_{RF}). The values of L_{FILT} and C_{FILT} are given by:

$$f_{RF} = \frac{1}{2\pi\sqrt{L_{FILT} \times C_{FILT}}}$$

3.7. Matching Network Performance Requirements

Although the RF ports are close to 50Ω, different substrate material, layer stack and component choices may require circuit tuning in order to optimize the return loss and obtain optimum power transfer.
The table below summarizes matching performance requirements for the RF ports.

Table 1: RF Port Matching Network Characteristics

Port	Return Loss	Return Loss BW [1]	Insertion Loss	Group Delay Variation
Unit	**dB**	**MHz**	**dB**	**ns**
RFINA, RFINB	< -15	OBW	< -1.5	< 0.6[2]
RFINDLYA, RFINDLYB	< -15	OBW	< -1.5	< 0.6[3]
RFFBA, RFFBB	< -15	OBW + 6 x EBW	< -1.5	NA
RFAUXA, RFAUXB	< -15	OBW	< -1.5	NA
RFOUTA, RFOUTB	< -12	OBW + 6 x EBW	< -1.5	< 0.6[4]

[1] Example: OBW = Operating Bandwidth (i.e. 2100-2200MHz, or 100MHz). EBW = Envelope Bandwidth of the signal (i.e. for a 4-carrier WCDMA signal, 4x 5MHz, or ~20MHz). Total Required Return Loss Bandwidth: OBW+6 x EBW (i.e. 100MHz + 120MHz or 220MHz)
[2] Over a 200MHz Bandwidth and the Group Delay variation must be less than or equal to 10° at 3GHz.
[3] Over a 200MHz Bandwidth and the Group Delay variation must be less than or equal to 10° at 3GHz.
[4] Over a 200MHz Bandwidth and the Group Delay variation must be less than or equal to 10° at 3GHz.

4. Spurious and Noise

4.1. Spurious Performance

4.1.1. TRACK/FSA

The spurs in TRACK/FSA mode are described in Figure 8.

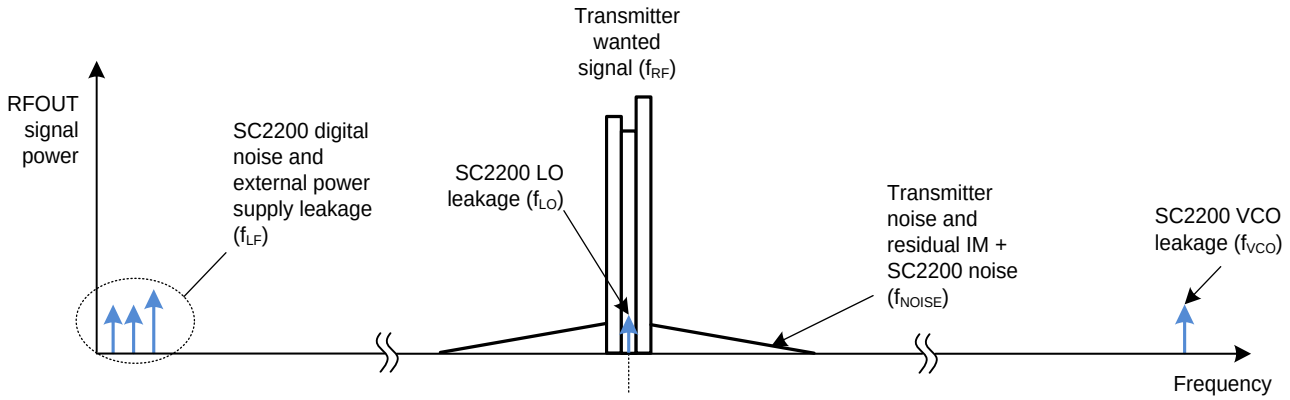


Figure 8: SC2200 Spurious Content (TRACK/FSA Mode)

Table 2: Spur List (TRACK/FSA State) Measured at RFOUT SMA Connector

Spur Type	Symbol	Frequency	Source(s)	Level[1]	Ways to Reduce Spurs/Noise Level
Low-frequency spurs[2]	f_{LF}	< 1000MHz	Direct digital noise leakage/coupling from SC2200 internal circuitry/supplies to RFOUT	< -55dBm	Decrease DVDD18 voltage (while meeting SC2200 data sheet limits) Optimize supply decoupling Some of these spurs can be moved in frequency
			Direct ADC clock leakage from SC2200 internal circuitry/supplies to RFOUT	< -65dBm	Decrease AVDD18 voltage (must meet SC2200 data sheet limits) Optimize supply decoupling network
			Switching regulator noise leakage	< -55dBm	Move switching regulator away from RFOUT output to reduce capacitive and electromagnetic (EM) coupling
LO leakage (due to SC2200)	$f_{LO} = f_{RF}$ ±0.5MHz	698–960MHz	SC2200 LO generation circuit coupling to RFOUT	< -80dBm	No fix, due to internal circuitry
		1800–2200MHz		< -65dBm	
		2300–2700MHz		< -65dBm	
Transmitter noise and residual IM	P_{NOISE}	f_{RF} = 2655MHz f_{Noise} = 2535MHz	SC2200 thermal noise and residual correction error	-135dBm/Hz	If necessary, use filtering at the PA input or output. 5x carrier BW required on PA input. Try band-pass filter on transceiver output (~1x carrier BW).

[1] *Measured at RFOUT SMA output*

[2] *Typically, low frequency spurs are not critical; they are filtered out by the PA DC blocking transfer function and other filtering elements at the PA output (diplexers…). Nonetheless, it is important to check that the low frequency spurs do not up-convert due to excessive second order distortion in the PA. To confirm this, it is recommended to apply a single CW tone at the RFIN input and measure the PA output spectral content around the wanted signal frequency.*

4.1.2. VCO Spurs in Track State

VCO spurs frequency and level depends on the frequency of the operation. These spurs are measured when RFPAL is in TRACK state. VCO spurs also exist in CAL state as shown in the next section. These spurs can be reduced with a filter in the RFOUT path. However, one should be careful not to disturb the correction signal.

Table 3: VCO Spurs at RFOUT Port

	Operation Freq (f_{RF})	f_{VCO}	Source	Level	How to Reduce VCO Spurs?
Internal VCO Leakage (RFIN Frequency Dependent)	698MHz –960MHz	f_{RF} * 4	SC2200 Internal VCO Coupling to RFOUT	< -60dBm	Use a bandpass or low-pass filter in the RFOUT-to-PA path. (Allow 5x carrier BW for the pass band)
	1800MHz –2200MHz	f_{RF} * 2		< -52dBm	
	2300MHz –2700MHz	f_{RF} * (4/3) & (2/3)		< -53dBm	

4.1.3. CAL Mode Scanning Spurs

During the CAL Mode, SC2200 searches for input signal by scanning the LO frequency through the band defined by the Min / Max scanning frequency limits (see SPI command documentation for setting the f_{MIN} and f_{MAX} values). During this mode, the internal LO circuit (f_{LO}) scans the f_{MIN} to f_{MAX} frequency range and leaks small amounts of signal to RFOUT. In addition, other LO generation circuit spurs are present at the RFOUT such as the VCO spur (f_{VCO}). The CAL mode spurs are described in Figure 9 and Table 4.

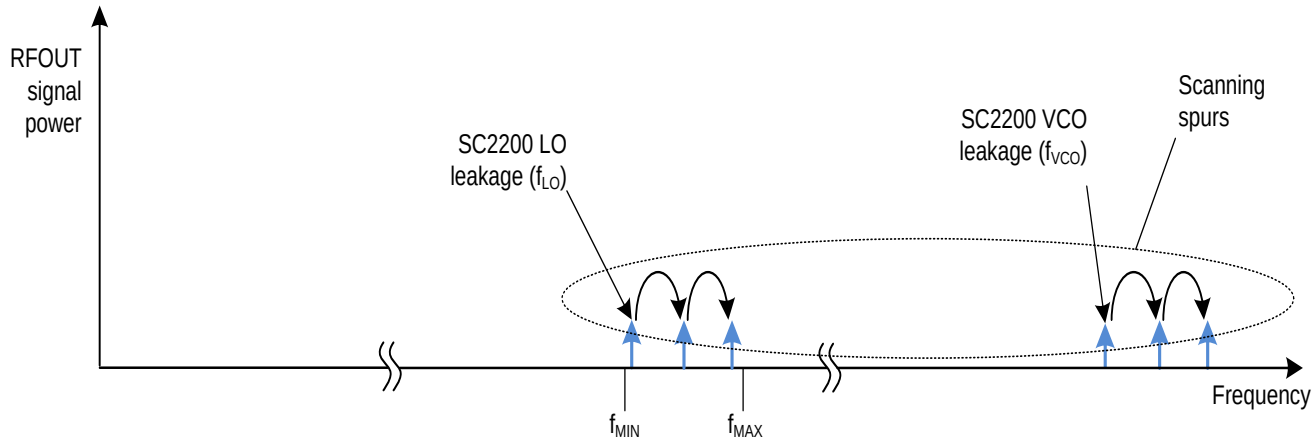


Figure 9: SC2200 Spurious Content (CAL Mode)

***IMPORTANT**: Restricting the f_{MIN} and f_{MAX} values to the band of interest is recommended to limit the Scanning spurs frequency range. For example, for the 2100 WCDMA band, f_{MIN} and f_{MAX} should be set to 2110 and 2170MHz, respectively.*

Table 4: Scanning Spurs List (CAL State)

Spur Type	Operation Frequency	Spur Frequency	Source(s)	Level[1]	Ways to Reduce Spurs/Noise Level
LO Leakage (f_{LO}) leakage (band dependent)	698MHz–960MHz	698 – 960MHz	SC2200 LO generation circuit coupling to RFOUT	< -80 dBm	
	1800–2200MHz	1800 – 2200 MHz		< -52dBm	
	2300MHz – 2700MHz	2300 – 2700MHz		< -55dBm	
VCO leakage f_{VCO} (band dependent)	698MHz – 960MHz	f_{RF} * 4	SC2200 VCO coupling to RFOUT	< -60dBm	Typically, these spurs are not an issue since they are far out of band and filtered out by the PA duplexer/filter. If one uses a band pass or low pass filter in the RFOUT-to-PA path. (Allow 5x carrier BW for the pass band)
	1800MHz–2200MHz	f_{RF} * 2		< -36dBm	
	2300MHz–2700MHz	f_{RF} * (2/3) & (4/3)		< -50dBm	

5. PCB Layout Considerations for SC2200

5.1. Floor Planning and Placement Priorities

Before laying out the board, it is important to create a good floor plan with optimum tradeoffs for best correction performance and lowest spurious emissions. Please follow the following guidelines in order of priority:

1. Priority 1: Select layer stack
2. Priority 2: Design RF traces, select/place critical RF components and optimize power levels (RFIN, RFINDLY, RFFB, RFOUT)
3. Priority 3: Place power supplies, decoupling and select regulators.
4. Priority 4: Select/place the clock reference circuit
5. Priority 5: Place non-critical signals (digital control and analog signals…)

5.1.1. SMT Component Size Selection

To support compact designs, the SC2200 was designed with a package lead pitch of 0.5mm. Use of 0402/0201 components are ideal for matching networks since they permit very compact and low parasitic implementations.

[1] Measured at RFOUT output

5.2. Layer Stack

The SC2200 reference board is built on a four layer, epoxy fiberglass, fabrication that is constructed with two cores each clad on both sides with 1oz Copper. Only the top layer (layer 1) must be impedance controlled. The layer stack up is shown in Figure 10:

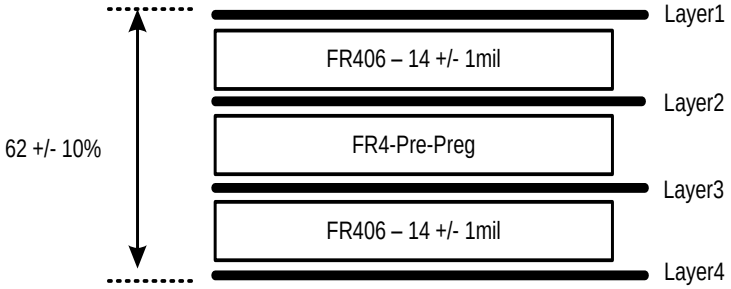


Figure 10: PCB Fabrication Layer Stack

***IMPORTANT**: It is NOT recommended to use a 2-layer PCB due to the complexity of connections and RF traces.*

5.2.1. Layer 1: RF and Signals

The top layer contains the RF, interface, power supply regulation and analog circuitry. All components are mounted on this layer. This layer is designed with an FR406 laminate that is 0.014 inches thick and has a nominal dielectric constant of 4.2. 50 Ohm trace width must be modified for a different dielectric material.

This dielectric and material thickness are well suited for RF design between 700MHz and 2700MHz since the 50Ω lines match the 0402 component landing pad size, hence avoiding discontinuities. Also, the dielectric thickness is large enough to have sufficient trace width to meet 50Ω line impedance, including typical PCB fabrication tolerances.

When possible, surround RF traces and matching networks by ground vias to control the RF return. All RF traces must have a continuous ground plane underneath for impedance control and noise immunity.

***IMPORTANT**: Care should be taken to ensure that no noisy return current paths are routed under or close to sensitive RF circuit blocks.*

Under the SC2200 ground paddle and the RF delay line, multiple vias ensure that the total parasitic inductance associated with the vias is minimized by several parallel connections. In addition, distributed vias ensure an even thermal distribution as described in section 5.3. Please refer to the Altium Layout and Gerber files.

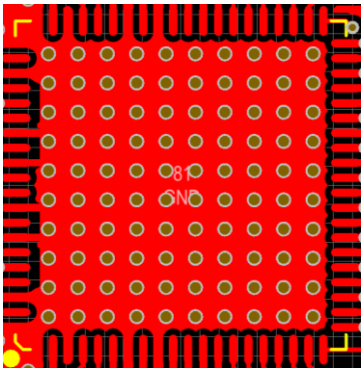


Figure 11: Via Array Under SC2200 Ground Paddle

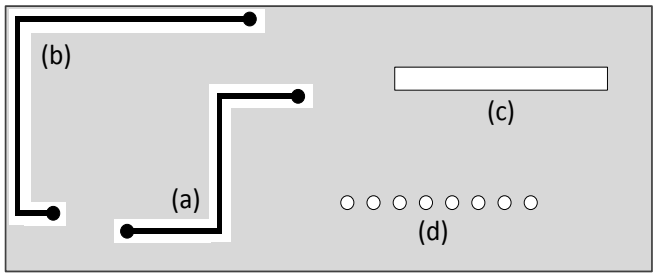
5.2.2. Layer 2: Ground Plane

The second layer is dedicated to the ground plane and fulfills the following functions:

- Provides a controlled impedance to RF signals
- Provides noise immunity to RF signals
- Provides a low impedance return path to all supplies, RF, digital and analog signals
- Enhances the thermal spreading of the PCB

Although this is not a hard rule, there are is no ground separation between the DC supply, RF and analog circuitry. This greatly simplifies the grounding and avoids unknown return paths due to complex grounding schemes. The following recommendation should be followed for the ground plane design:

- Pay attention to the holes and cutouts in the ground planes. They break up the plane and, therefore, cause increases in loop areas (see (a) and (b) in Figure 12).
- Avoid buried traces in the ground plane. If you have to use them, put them in the signal or power supply plane.
- Breaking up the plane with a row of holes is much better than having a long slot (see (c) and (d) in Figure 12).
- Connect directly components to the ground plane and avoid sharing vias.



(a) Poor: trace cuts ground plane and prevents direct returns
(b) Better: Perimeter trace avoids cutting ground plane. Best solution is not signal trace in ground plane
(c) Poor: slot cuts ground plane and prevents direct returns
(d) Better: via string maintains ground plane continuity

Figure 12: Ground Plane Recommendations

5.2.3. Layer 3: Power Supply Plane

Layer 3 is the power plane which distributes 1.8V and DVDDIO to the SC2200. Ground is placed under the RF delay area. Priority is given to the 1.8V supply since it provides power to the RF blocks and it consumes more DC power than the DVDDIO supply (Figure 13):

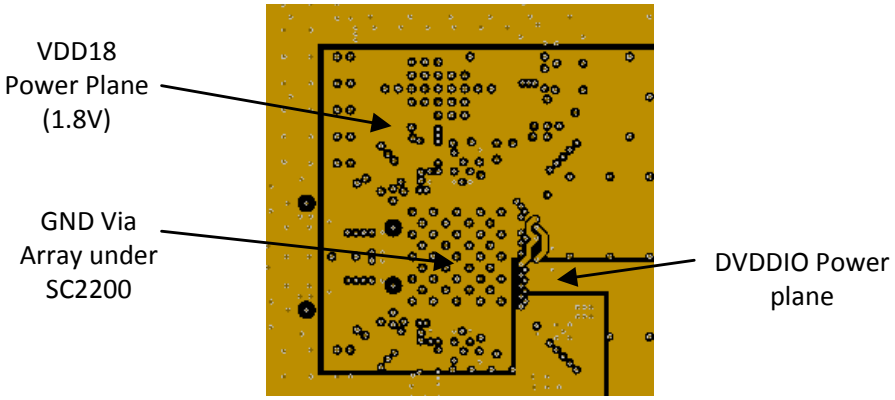


Figure 13: Layer 3, Power Supply Distribution

The dielectric between layer 2 and 3 is fabricated with an epoxy fiberglass material. Thickness of this dielectric material is not critical as this layer is primarily used for DC power distribution.

5.2.4. Layer 4: Ground Plane and signals

This layer is used to route non critical low frequency analog and digital signals. In addition to signal routing, a large portion of this layer is dedicated to grounding for thermal relief and low impedance grounding.

5.3. Thermal Considerations

The thermal relief pad under the SC2200 provides both thermal relief and a solid ground reference to the chip. This pad should be ideally connected to a component side ground connection which in turn is connected to the main ground plane layer by multiple vias. Figure 11 illustrates the multiple via (or “well stitched”) connections of the thermal relief pad to the main (inner) ground layer.
Filled vias and thick copper layers will further improve the thermal dissipation and ground connection.
The SC2200 is guaranteed to work up to 105˚C case temperature. Case temperature is the temperature at the ground paddle, as described in Figure 14:

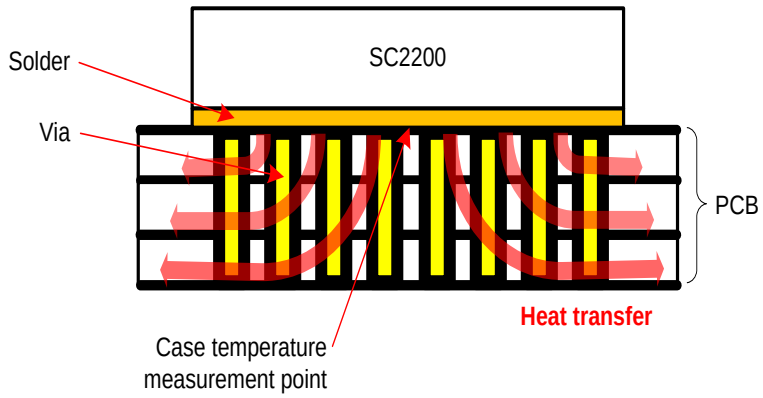


Figure 14: PCB Fabrication Layer Stack

Parameters for thermal simulations:

- QFN80 package Φ_{JC} = 0.8˚C/W
- Maximum SC2200 power consumption when PA driver is ON = 2.5W
- SC2200 junction temperature must not exceed 108˚C

5.4. PCB Parasitics

An area that is often overlooked during PCB layout is the electrical characteristics of the PCB material itself, component traces, and vias. The electrical characteristics of the PCB used to physically mount and connect the circuit components in a high frequency RF product can have a significant impact on the performance of that product.
An often overlooked PCB parasitic component is the via, used to connect one PCB layer to another. Typically, for a 1.6mm thickness PCB material, a single via can add 1.2nH of inductance and 0.5pF of capacitance, depending upon the via dimensions and PCB dielectric material.
All power supply decoupling capacitors must have ground vias very close to the capacitor ground connection.

6. Power Supplies

The SC2200 has been designed to support linear regulators as well as switching regulators. It is recommended to use switching regulators for better efficiency and reduce overall system power consumption.
This section describes how to:

- Properly size the regulators and supply feeds
- Design adequate supply noise/ripple
- Decouple the supply lines
- Sequence the power supplies

The DVDDIO pins supply the digital IO signals (DIO*) and the EEPROM.

6.1. Regulator Selection

The supply regulator must support the SC2200 peak current load (over voltage and temperature) as well as provide low ripple/noise. The typical SC2200 peak current per pin is provided in Table 7. The supply voltage tolerances are provided in the data sheet as well as the maximum SC2200 average and peak currents.

6.2. Power Supply Ripple

The power supply ripple must be less than:

- AVDD18: 30mV$_{PKPK}$ while meeting the SC2200 data sheet power supply DC voltage limits
- DVDD18: 50mV$_{PKPK}$ while meeting the SC2200 data sheet power supply DC voltage limits
- DVDDIO: 50mV$_{PKPK}$ while meeting the SC2200 data sheet power supply DC voltage limits

6.3. Supply Decoupling

Minimize current loops on PCB layouts by decoupling as close to the port being decoupled to ground as possible. Try and avoid capacitive coupling by ensuring that each circuit block or port has its own decoupling capacitor. Ensure that each decoupling capacitor has its own local via connection to ground. As a rule of thumb, components should not share vias.
All associated supply decoupling capacitors be mounted as close as possible to SC2200 power supply pins to:

- Provide efficient supply decoupling and reduce trace inductance
- Reduce the risk of polluting other circuits due to capacitive or electromagnetic coupling.

In addition to the decoupling capacitors, ferrite beads on selected supply lines are required. The ferrite beads are used to isolate digital noise generated by the SC2200. It is important to select a ferrite bead that will not introduce a large voltage drop. See the application circuit Bill of Materials for recommended ferrite bead part numbers.

6.4. Power Sequencing

The SC2200 contains a power-on-reset (POR) circuit connected to the DVDD18 power supply (which triggers between 1 and 1.3V).

IMPORTANT:

a. *The DVDDIO power supply must be within 90% of its final value at least 100□s before the DVDD18 power supply is turned on.*
b. *If this sequence cannot be implemented or DVDDIO and DVDD18 are connected together, then the RESETN pin must be asserted low for at least 1ms after the last supply is established.*

7. Reference Clock

Either a crystal resonator or external clock is required to generate an accurate reference. If a crystal oscillator is used, its frequency must be 20MHz. If an external clock is used, the system accepts various reference frequencies: 10, 13, 15.36, 19.2, 20, 26, and 30.72MHz.

IMPORTANT: *Reference Clock must be stable during SC2200 boot sequence.*

7.1. 20MHz Crystal Oscillator (Master Mode)

The crystal frequency must be 20MHz with the following characteristics:

- Tolerance < 250 ppm
- Drift < 100 ppm over temperature range and aging

When a crystal resonator is used, it should be connected across "XTALI" and "XTALO" with capacitors to ground. Reference the SC2200 reference circuit schematic for details.
To guarantee startup of oscillation a crystal with ESR < 50Ω and load capacitance to ground <12pF is required.

IMPORTANT*: Although the SC2200 is rated for -40°C to +105°C case temperature, many crystals are not routinely rated for an operating temperature range of -40°C to +105°C. Please ensure that the crystal is rated for -40°C to +105°C case temperature.*

7.2. 10–30.72MHz External Clock (Slave Mode)

In slave mode, the system accepts various reference frequencies: 10, 13, 15.36, 19.2, 20, 26, and 30.72MHz.

- Tolerance < 250 ppm
- Drift < 100 ppm over temperature range and aging

IMPORTANT: *Selecting an external reference clock frequency other than 20 MHz requires programming the SC2200 EEPROM through the SPI bus. See SC2200 SPI Programming Guide.*

For an external clock (sine and square wave are supported), the clock signal must be AC coupled (DC is set by the SC2200) to the "XTALI" pin. The amplitude must be between 0.5 and 1.5V_{PKPK} at the pin and phase noise must be better than -130dBc/Hz at 100kHz offset.
If only 3.3V logic levels are available in the system an appropriate level shifter must be utilized. We recommend an AC coupled voltage divider as shown in Figure 15. R1 and R2 values will need to be adjusted based on the clock source voltage level as described below:

$$V_{PKPK}\,(XTALI) = \frac{R2}{R1 + R2} \times V_{PKPK}\,(EXTALI)$$

Example: If the clock buffer has a 3.3V_{PKPK} output (EXTCLK), then if R1 = 1kΩ, R2 = 560Ω, V_{PKPK}(XTALI) ~ 1.2V_{PKPK}. C1 = 47pF. The clock buffer must have a low output impedance (or high current drive) so that Z_{OUT} < (R1 + R2)/10.

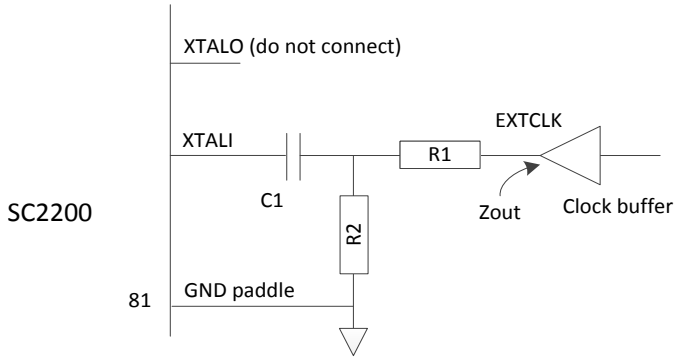


Figure 15: External Clock Diagram

IMPORTANT:

c. XTALO must not be connected when an external clock is utilized.
d. Ensure that the clock at XTALI has clean edges (no ringing or spurious transitions)
e. In case a square wave is used, the duty cycle must be between 45 and 55%

8. Digital IOs

One IBIS model is available to simulate the digital signal integrity for 1.8V DVDDIO supply level.

8.1. INTRN (Interrupt)

The INTRN pin is no longer supported. Internal pullup to DVDDIO.

8.2. RESETN

It is required that RESETN, pin 23, be connected to a host processor through a GPIO connection or use a 1uF capacitor connected between pin 23 and ground. The RESETN pin is internally pulled-up to DVDDIO through an integrated resistor. The RESETN (active low) signal must be kept low for at least 1us after the last supply is ramped to at least 90% of its final level. When this signal is LOW, the SC2200 will be in a reset mode. When the signal goes HIGH, the SC2200 will begin to boot-up and will complete this process in approximately 1 to 3 seconds (depending on firmware version). After the boot-up process, SC2200 will start adapting toward optimal linearization.

Implementing a GPIO connection to pin 23, RESETN, allows the Host Processor to remotely reset SC2200 if a re-initialization is required.

8.3. MS0 (EEPROM Load Enable)

The MS0 pin is used to upload firmware to the SC2200. This input is connected to an internal pull down resistor. It is recommended to connect the MS0 pin to the host controller GPIO. While this signal is ”low”, the SC2200 is in normal operation. When the MS0 signal is high, the SC2200 will be placed in a mode where the SPI Bus is directly connected to the internal EEPROM. Throughout programming, MS0 must be a logic level high and at the completion of the programming process the level must transition to a low logic level. After the programming has been completed, a hard reset should be initiated by commanding the RESETN input low for at least 1µs then toggled high.

8.4. SPI Slave Interface

The SPI slave bus is composed of 4 pins labeled: SSCLK, SSSN, SSDI, and SSDO. The SC2200 operates as a slave on this interface, can operate from 50 kHz up to 10 MHz, and can share the bus with other slave devices (including multiple SC2200’s) using distinct Slave Select signals from the host (SSN). The SPI Bus operates in Mode 0 (CPOL = 0 and CPHA = 0) which means that data is sampled on the rising edge and data is generated on the falling edge of SCLK. The signals use digital logic levels equal to the DVDDIO supply level and support the following functionality:

- SSCLK is an input which should receive a clock signal from the Bus Master during SPI transactions. The clock should have a 50% duty cycle and may operate from 50kHz up to 10MHz. Internally to the SC2200, the pin is connected to a resistor to ground.
- SSSN (Slave Select) is an active low input which functions as an active low Slave Select allowing the Host to act as the Bus Master to enable communications to the SC2200. Internally to the SC2200, the pin is pulled up with a resistor to DVDDIO.
- SSDI is an input which functions to receive addresses, messages/commands, and data values from the Host controller. This signal should be wired to the MOSI (master out / slave in) signal from the Bus Master. Internally to the SC2200, the pin is connected to a resistor to ground.
- SSDO is a tri-stated output when not in transaction. This signal should be wired to the host MISO signal (master in/slave out) signal. This pin does not have an internal pull-up or pull-down, and must be externally pulled-up by 10KΩ to DVDDIO. This pin is capable of driving 6mA. Listed below is the equation for determining the maximum load capacitance for the SSDO pin:
  - C_{MAX} (shunt) = 1.9e-4/f_{SPI} (in Farad), where f_{SPI} is the frequency of the SPI clock (SSCLK) in Hz.
  - For example: for f_{SPI} = 4MHz, the maximum load capacitance (C_{MAX}) to ground is 48pF. The SSDO pin capacitance is 2.8pF and must be taken into account when calculating C_{MAX}.
  - For values greater than C_{MAX}, a buffer is required.

The pull up/down input resistance varies with the DVDDIO supply. Please refer to the data sheet.

8.5. Digital Interface Connector

To upload new firmware and debug the operation of SC2200 PA linearizer, a digital connector shown in Figure 16 should be included in the final product. Refer to HDK for layout and part number for this connector.

***IMPORTANT**: ESD protection measures must be included around this connector to avoid any damage to digital pins of the IC.*

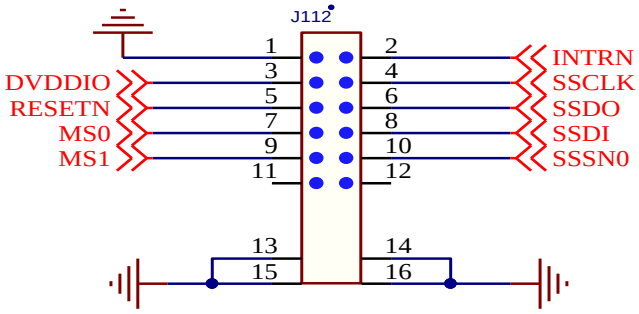


Figure 16: 12-pin Interface Connector for Firmware Upload and Development

Table 5: SPI Interface Pin Description

Pin	Description	Pin	Description
1	GND	9	MS1[2]
2	INTRN[2]	10	SSSN0
3	DVDDIO	11	DVDDIO[1]
4	SSCLK	12	GND[1]
5	RESETN	13[3]	GND
6	SSDO	14[3]	GND
7	MSO	15[3]	GND
8	SSDI	16[3]	GND

Note 1: Signal can be left unconnected
Note 2: Signal not used with SC2200 (can be left unconnected)
Note 3: Connections 13 to 16 are ground headers, not actual pins

IMPORTANT:

a. The SC2200 SSDO pin capacitance is 2.8pF and must be part of the C_{LOAD} calculation. See Section 7 for the maximum load capacitance calculation.
b. If this additional connector cannot be included because of layout restrictions at least test point pins should be included for debugging if necessary.
c. MS0 connection is required for FW upload to SC2200.
d. The INTRN and MS1 pins are no longer used by SC2200 firmware. These pin functions are not supported.

8.6. Digital Connections for Multi SC2200 Operation

SSDI, SSDO, and SCLK signals can be shared amongst several SC2200 (Figure 17). One SSN per SC2200 is needed. Special care must be taken when connecting long PCB traces at the SDO output since the capacitance (C_{LOAD}) will increase.

In addition to these SPI connections, RESETN, MS0, MS1 and INTRN signals are suggested to be included to the Host connection as in Figure 16.

The GUI can support only one chip. Therefore, for multi-chip applications, include layout provisions for a series 0 Ohm resistors in the SSN and SDO line of each RFPAL as shown in Figure 17 and connect this component only for the SC2200 being tested to avoid any conflict with the inactive SC2200 while working with the GUI.

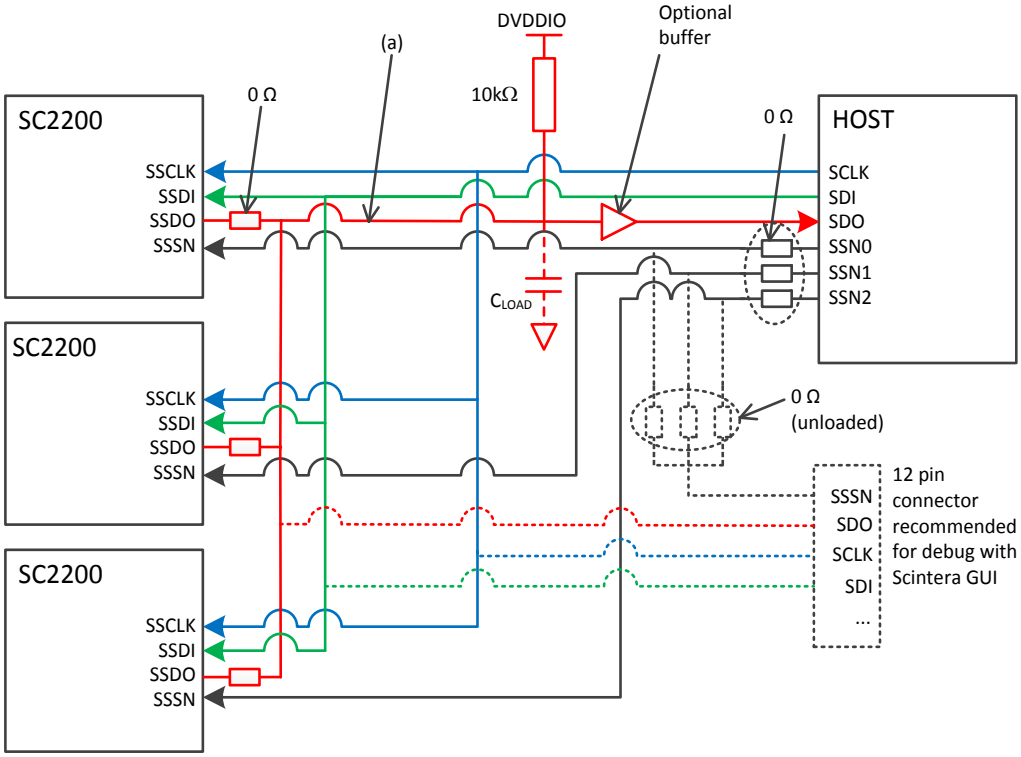


Figure 17: SPI Connections for Multi-SC2200 Applications

8.7. Miscellaneous Digital Pins

- DIO*: The DIO* are general-purpose digital input/outputs.

The DIO pins are not used by SC2200 firmware. These pin functions are not supported.*

9. Troubleshooting

If your system is not working correctly, reference the troubleshooting tips outlined in Table 6.

Table 6: Troubleshooting Tips

#	Symptom	Recommendations
1	No Correction	Verify 1.8V and DVDDIO are present at each of the supply pins and meet the data sheet limits and the ripple/noise requirements as described in section 2. If DVDDIO and 1.8V are connected together, make sure the RESETN pin is asserted low for at least 1μs after the last supply is established.
2	No correction but DVDDIO & 1.8V supplies are present at the IC pins	Verify that the supply currents are similar to those listed in Table 7 and that the pin voltages correspond to Table 8.
3	No correction but DVDDIO & 1.8V supplies are present at the IC pins	Verify the crystal is properly installed. A $1\pm0.3V_{PK-PK}$, sinusoid should be observed on pin XTALI. A low capacitance scope probe (<10pF) must be used to perform this measurement. If the software is not running, then 1.8V and DVDDIO current consumption is approximately 10mA for each supply.
4	No correction. Crystal/resonator is working properly. SC2200 remains in the CAL state (FW state can be determined through the GUI or based on current consumption). See section 6 for supplies typical current consumption	Verify that the RFIN splitters and matching components are installed and properly soldered to the PCB. Verify that the RFFB matching components are installed and properly soldered to the PCB.
5	RFIN power level displayed on GUI is much lower than expected	Verify that the input power to the coupler is within the recommended operating range (See SC2200 data sheet). Verify that the RFIN splitter and that the matching components are installed and properly soldered to the PCB
6	RFFB power level displayed on GUI is much lower than expected.	Verify input power level to RFFB is correct. Check that RFFB matching components are installed and properly soldered to the PCB. (See SC2200 data sheet)
7	RFIN and RFFB power level are correct, but there is no correction	Verify that all the RFOUT components are installed and properly soldered to the PCB.
8	If the board is correcting, but the GUI is not working	Verify that all SPI signals are present. Measure the SSCLK, SSSN, SSDI, SSDO signals and compare with information/diagrams described in section 8.4
9	If the board is correcting, but spurs are present.	Contact Maxim Integrated support. Please refer to section 4 for spur characterization.
10	No correction or worse correction performance at low and or high temperatures	Verify that RFIN and RFFB levels are within the recommended limits across the temperature range as specified in the SC2200 data sheet. Verify that crystal oscillator is still running with $600mV_{PP}$ across the temperature range
11	Correction is varying across the frequency	Verify that RFIN and RFFB levels are within the recommended limits across the frequency range as specified in the SC2200 data sheet
12	Firmware can't be uploaded	Verify that the crystal oscillator is running
13	RFPAL registers cannot be accessed by the host	Verify that the crystal oscillator is running

10. Appendix

10.1. SC2200 Supply Pin Current Consumption

Table 7: Typical SC2200 Supply Pins Current Consumption, FW5.0.x for AVDD18 = DVDD18 = DVDDIO = 1.8V

Pin	Name	Type	DC Current (pk)	DC Current (rms)	Unit	Comment
10	AVDD18	Supply		50	mA	Analog supply, switching noise (100MHz and harmonics)
11	AVDD18	Supply		55	mA	Analog supply, switching noise (100MHz and harmonics)
12	AVDD18	Supply		55	mA	Analog supply, switching noise (100MHz and harmonics)
13	AVDD18	Supply		50	mA	Analog supply, switching noise (100MHz and harmonics)
30	DVDDIO	Supply		~10mA per pad only during when DIO outputs are switching[8]	mA	Digital output IO supply (~10MHz and harmonics)
36	DVDDIO	Supply				
29	DVDD18	Supply	335	230[9]	mA	Digital core supply, digital noise (20, 100MHz and harmonics)
32	DVDD18	Supply				
37	DVDD18	Supply				
48	AVDD18	Supply		25	mA	Analog supply, switching noise (100MHz and harmonics)
49	AVDD18	Supply		55	mA	
50	AVDD18	Supply		55	mA	
51	AVDD18	Supply		55	mA	
55	AVDD18	Supply		15	mA	Analog supply
62	RFOUTB	Analog Out		80	mA	Output pulled to AVDD18 by external choke
64	AVDD18	Supply	65	40	mA	Analog supply, some RF content (700–2700MHz)
66	AVDD18	Supply		45	mA	Analog supply, some RF content (700–2700MHz)
70	AVDD18	Supply		40	mA	Analog supply, some RF content (700–2700MHz)
71	AVDD18	Supply		40	mA	Analog supply, some RF content (700–2700MHz)
75	AVDD18	Supply		45	mA	Analog supply, some RF content (700–2700MHz)
77	AVDD18	Supply	65	40	mA	Analog supply, some RF content (700–2700MHz)
79	RFOUTA	Analog Out		80	mA	Output pulled to AVDD18 by external choke
TOTAL				**1055[1]**	**mA**	

1. Refer to the SC2200 data sheet for maximum current.

[8] *Pins 30 and 36 are internally connected in the IC. Current consumption reflects the sum of all four pins.*
[9] *Pins 29, 32, and 37 are internally connected in the IC. Current consumption reflects the sum of all four pins.*

10.2. SC2200 Pin Voltages

Table 8: SC2200 Approximate Pin Voltages, AVDD18 = DVDD18 = 1.8V[10]

Pin	Name	Type	DC Voltage	Unit	Comment
1	GND	RF Shield	0	V	—
2	RFINDLYA	Analog In	0	V	50Ω connected to GND (Section 3)
3	GND	RF Shield	0	V	Ground for shield
4	AIN0A	Analog In	NA	V	Input
5	AIN1A	Analog In	NA	V	Input
6	AVDD18	Supply	1.8	V	Analog supply, some RF content (7002700MHz)
7	GND	RF Shield	0	V	—
8	RFINA	Analog In	0	V	50Ω connected to GND (Section 3)
9	GND	RF Shield	0	V	—
10	AVDD18	Supply	1.8	V	Analog supply, switching noise (100MHz and harmonics)
11	AVDD18	Supply	1.8	V	Analog supply, switching noise (100MHz and harmonics)
12	AVDD18	Supply	1.8	V	Analog supply, switching noise (100MHz and harmonics)
13	AVDD18	Supply	1.8	V	Analog supply, switching noise (100MHz and harmonics)
14	AIO0A	Analog In/Out	0-1.8	V	Configurable IO
15	AIO1A	Analog In/Out	0-1.8	V	Configurable IO
16	AIO2A	Analog In/Out	0-1.8	V	Configurable IO
17	AIO3A	Analog In/Out	0-1.8	V	Configurable IO
18	AIO4A	Analog In/Out	0-1.8	V	Configurable IO
19	XTALI	Analog In	~1	V	Section 7
20	XTALO	Analog Out	~1	V	Section 7
21	MS0	Digital In	NA	V	Input (Section 8.2)
22	MS1	Digital In	NA	V	Input
23	RESETN	Digital In	NA	V	Input (Section 8.5)
24	SSCLK	Digital In	NA	V	Input (Section 8.4)
25	SSSN	Digital In	NA	V	Input (Section 8.4)
26	SSDI	Digital In	NA	V	Input (Section 8.4)
27	SSDO	Digital Out	0-1.8	V	Digital Output (Section 8.4)
28	INTRN	Digital Out	0-1.8	V	Digital Output (Section 8.1)
29	DVDD18	Supply	1.8	V	Digital core supply, digital noise (20, 100MHz and harmonics)
30	DVDDIO	Supply	1.8	V	Digital output IO supply (~4MHz and harmonics)
30	DIO0	Digital In/Out	0-1.8	V	Configurable IO
32	DVDD18	Supply	1.8	V	Digital core supply, digital noise (20, 100MHz and harmonics)
33	DIO1	Digital In/Out	0-1.8	V	Configurable IO
34	DIO2	Digital In/Out	0-1.8	V	Configurable IO
35	DIO3	Digital In/Out	0-1.8	V	Configurable IO
36	DVDDIO	Supply	1.8	V	Digital output IO supply (~4MHz and harmonics)
37	DVDD18	Supply	1.8	V	Digital core supply, digital noise (20, 100MHz and harmonics)
38	DIO4	Digital In/Out	0-1.8	V	Configurable IO
39	DIO5	Digital In/Out	0-1.8	V	Configurable IO
40	DIO6	Digital In/Out	0-1.8	V	Configurable IO
41	DIO7	Digital In/Out	0-1.8	V	Configurable IO
42	DIO8	Digital In/Out	0-1.8	V	Configurable IO
43	AIO4B	Analog In/Out	0-1.8	V	Configurable Analog IO
44	AIO3B	Analog In/Out	0-1.8	V	Configurable Analog IO
45	AIO2B	Analog In/Out	0-1.8	V	Configurable Analog IO
46	AIO1B	Analog In/Out	0-1.8	V	Configurable Analog IO
47	AIO0B	Analog In/Out	0-1.8	V	Configurable Analog IO

[10] *Total power and current consumption are provided in the SC2200 data sheet.*

Pin	Name	Type	DC Voltage	Unit	Comment
48	AVDD18	Supply	1.8	V	Analog supply, switching noise (100MHz and harmonics)
49	AVDD18	Supply	1.8	V	Analog supply, switching noise (100MHz and harmonics)
50	AVDD18	Supply	1.8	V	Analog supply, switching noise (100MHz and harmonics)
51	AVDD18	Supply	1.8	V	Analog supply, switching noise (100MHz and harmonics)
52	GND	RF Shield	0	V	Ground for shield
53	RFINB	Analog In	0	V	RF single-ended Input Signal for Tx path “B” (Section 3)
54	GND	RF Shield	0	V	Ground for shield
55	AVDD18	Supply	1.8	V	Analog supply
56	AIN1B	Analog In	NA	V	Analog Input
57	AIN0B	Analog In	NA	V	Analog Input
58	GND	RF Shield	0	V	Ground for shield
59	RFINDLYB	Analog In	0	V	Delayed RF single-ended Input Signal for Tx path “B”. (Section 3)
60	GND	RF Shield	0	V	Ground for shield
61	GND	RF Shield	0	V	Ground for shield
62	RFOUTB	Analog Out	1.8	V	Output pulled to AVDD18 by external choke (Section 3)
63	GND	RF Shield	0	V	Ground for shield
64	AVDD18	Supply	1.8	V	Analog supply, some RF content (700–2700MHz)
65	RFAUXB	RF Input	0	V	50Ω connected to GND (Section 3.5)
66	AVDD18	Supply	1.8	V	Analog supply, some RF content (700–2700MHz)
67	GND	RF Shield	0	V	Ground for shield
68	RFFBB	Analog In	0	V	50Ω connected to GND (Section 3)
69	GND	RF Shield	0	V	Ground for shield
70	AVDD18	Supply	1.8	V	Analog supply, some RF content (700–2700MHz)
71	AVDD18	Supply	1.8	V	Analog supply, some RF content (700–2700MHz)
72	GND	RF Shield	0	V	Ground for shield
73	RFFBA	Analog In	0	V	50Ω connected to GND (Section 3)
74	GND	RF Shield	0	V	Ground for shield
75	AVDD18	Supply	1.8	V	Analog supply, some RF content (700–2700MHz)
76	RFAUXA	Analog Out	0	V	50Ω connected to GND (Section 3)
77	AVDD18	Supply	1.8	V	Analog supply, some RF content (700–2700MHz)
78	GND	RF Shield	0	V	Ground for shield
79	RFOUTA	Analog Out	1.8	V	Output pulled to AVDD18 by external choke (Section 3)
80	GND	RF Shield	0	V	Ground for shield
81	GND	Supply	0	V	Exposed paddle