Evaluation Board User Guide

EVAL-LTM4709-BZ

LTM4709

Single 9A, Ultralow Noise, High PSRR, Ultrafast µModule Linear Regulator with Configurable Output Array

General Description

The EVAL-LTM4709-BZ evaluation board features the LTM®4709, a triple 3A, ultralow noise, high power supply rejection ratio (PSRR), and ultrafast µModule® linear regulator with a configurable output array. The input voltage (V_{IN}) ranges from 0.6V to 5.5V. There are jumpers to set a 3-bit trilevel code that determines the output voltage (V_{OUT}) at preprogrammed levels that range from 0.5V to 4.2V. The maximum output current is 9A since the LTM4709 is configured as a single output. The EVAL-LTM4709-BZ requires an external BIAS voltage (V_{BIAS}) at least 1.2V higher than V_{OUT} and between 2.375V and 5.5V.

The LTM4709 of the EVAL-LTM4709-BZ requires few external components, therefore simplifying the circuit design and significantly reducing solution size. External component choice and careful PCB design help optimize noise, PSRR, load transient response, and V_{OUT} regulation performance. The LTM4709 only requires ceramic capacitors for the power input and the power output. The 22µF capacitor at the circuit output was chosen for high-frequency PSRR performance and to minimize V_{OUT} deviation during load transients.

The capacitor that bypasses the V_{IN} power for the LTM4709 and the corresponding V_{IN} PCB layout can affect PSRR (see the *Best PSRR Performance: PCB Layout for Input Traces* section for additional information). The EVAL-LTM4709-BZ decouples the V_{IN} power with a 4.7µF capacitor (see the LTM4709 data sheet for the minimum capacitor value required for V_{IN}). Note that an optional bulk 220µF tantalum polymer capacitor further reduces V_{IN} variation during load transients and reduces input voltage ringing that can be caused by inductive input power leads.

The LTM4709 has a precision current monitor that provides accurate current monitoring for the energy management system and current limit. An IMON*n* terminal is available for the current monitoring of each channel. The IMON*n* voltage is the product of the resistance that programs the current limit and the IMON*n* pin current, which is 1/3000 of the output current. By default, the EVAL-LTM4709-BZ has a 3.3A current limit per channel with IMONR*n* tied to GND. However, custom current limit levels can be programmed by floating IMONR*n* and connecting a resistor from IMON*n* to GND. The externally programmed current limit is triggered when the IMON*n* voltage is 1V.

An EN jumper (P17) is available on the EVAL-LTM4709-BZ to either connect the EN*n* pins to V_{BIAS} to turn the output on or to ground to disable the output. There is a PG*n* terminal for each channel that is pulled up to V_{BIAS} by a 100kΩ resistor when PGR*n* is connected to BIAS. PG*n* is pulled down by an open-drain, n-channel metal-oxide semiconductor (nMOS) output to indicate regulator output status and other fault modes. The voltage input-to-output control (VIOC1) terminal allows connections to automatically regulate the difference between the input voltage and output voltage of the LTM4709 to be a fixed value.

For applications that require multiple outputs, each channel of the LTM4709 can be standalone. The DC3211A board is an example of a triple 3A application for the LTM4709.

The LTM4709 data sheet must be read in conjunction with this demo manual before working on or modifying the EVAL-LTM4709-BZ.

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EVAL-LTM4709-BZ Board Files

FILE	DESCRIPTION
EVAL-LTM4709-BZ	Evaluation board design files.

***Ordering Information* appears at end of datasheet.**

One Analog Way, Wilmington, MA 01887-2356, U.S.A. | Tel: 781.329.4700

EVAL-LTM4709-BZ Board Photo

Part marking is either ink mark or laser mark.

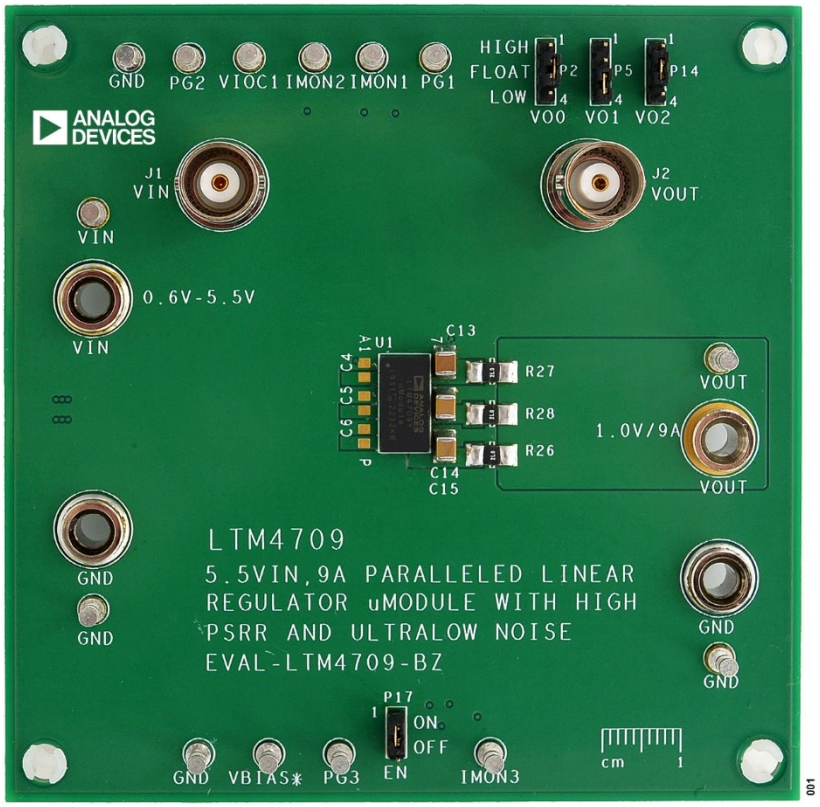

Figure 1. EVAL-LTM4709-BZ Board Photo

Performance Summary

(Specifications are at T_A = 25°C)

PARAMETER	CONDITIONS/NOTES	MIN	TYP	MAX	UNITS
Input voltage range		0.6		5.5	V
BIAS voltage range	$V_{BIAS} \geq V_{OUT}$ + 1.2V, $V_{BIAS} \geq V_{IN}$	2.375		5.5	V
Output voltage range Per channel	V_{OUT} = 0.5V, 10mA ≤ I_{OUT} ≤ 3A, 0.7V ≤ V_{IN} ≤ 0.9V	0.492	0.500	0.508	V
	V_{OUT} = 1.0V, 10mA ≤ I_{OUT} ≤ 3A, 1.2V ≤ V_{IN} ≤ 1.4V	0.988	1.000	1.012	V
	V_{OUT} = 1.2V, 10mA ≤ I_{OUT} ≤ 3A, 1.4V ≤ V_{IN} ≤ 1.6V	1.182	1.200	1.218	V
	V_{OUT} = 3.3V, 10mA ≤ I_{OUT} ≤ 3A, 3.5V ≤ V_{IN} ≤ 3.7V	3.250	3.300	3.350	V
	V_{OUT} = 4.2V, 10mA ≤ I_{OUT} ≤ 3A, 4.4V ≤ V_{IN} ≤ 4.6V	4.137	4.200	4.263	V
Output current	Per channel	10		3000	mA

Quick Start

Procedure

The EVAL-LTM4709-BZ evaluation board is an easy way to evaluate the performance of the LTM4709. See *Figure 2* for proper measurement equipment setup and follow the procedure below.

1. With the input supplies off and turned down, make all the connections shown in *Figure 2*. Ensure that the VO0, VO1, and VO2 jumpers to set V_{OUT} are in the proper positions for the desired output voltage according to the V_{OUT} selection matrix table in the LTM4709 data sheet. Also, ensure that the EN jumper (P17) is in the ON position.
2. Turn on the input and bias supplies. Increase the input supply so it is 300mV above the programmed output voltage. Adjust V_{BIAS} so it is between 2.375V and 5.5V and at least 1.2V higher than the V_{OUT} voltage for proper operation. Note that when setting the input and bias voltages, a V_{IN} or V_{BIAS} that is too close to the programmed V_{OUT} (too low) can cause dropout operation and a loss of V_{OUT} regulation. Also, a V_{IN} that is too high above the output can increase power dissipation to an unacceptable level.
3. Increase the load to the desired I_{OUT}. Readjust the input supply to be 300mV above the programmed output voltage. Verify that V_{OUT} is the expected voltage programmed by the jumpers. Note that for the most accurate measurements, measure the input and output voltages directly from the input and output capacitors. This will avoid any voltage drop from the vias or copper traces.
4. When the proper V_{OUT} is established, adjust the input voltages and load within the operating ranges and observe the V_{OUT} regulation, load transient response, and other parameters.
5. Refer to the Analog Devices application notes *AN83* and *AN159* for measuring output noise and PSRR. Note that J1 and J2 are BNC connectors that are used for noise and PSRR measurements for Channel 1.
6. Monitor power good at the PG*n* terminals and the output current at the IMON*n* terminals.
7. Refer to the LTM4709 data sheet for using the VIOC1 terminal.

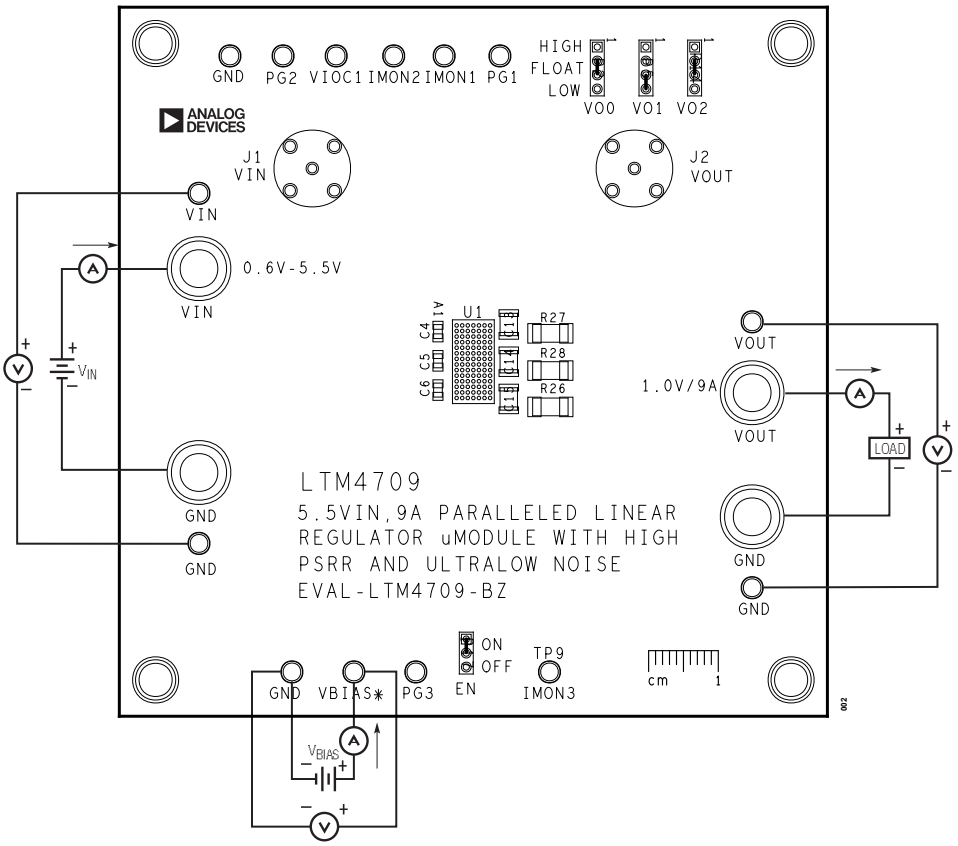

Figure 2. EVAL-LTM4709-BZ Measurement Setup

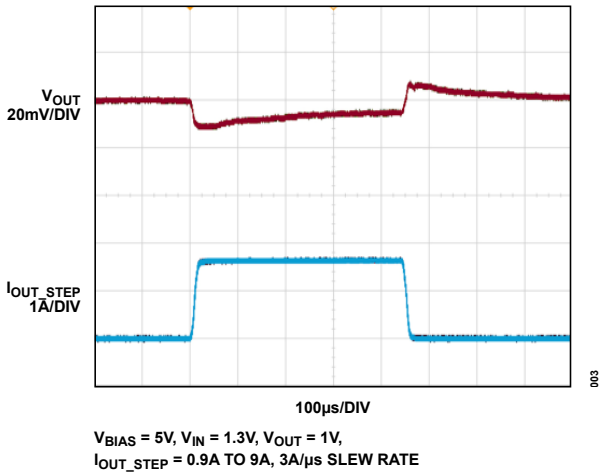

Figure 3. EVAL-LTM4709-BZ Load Step of LTM4709

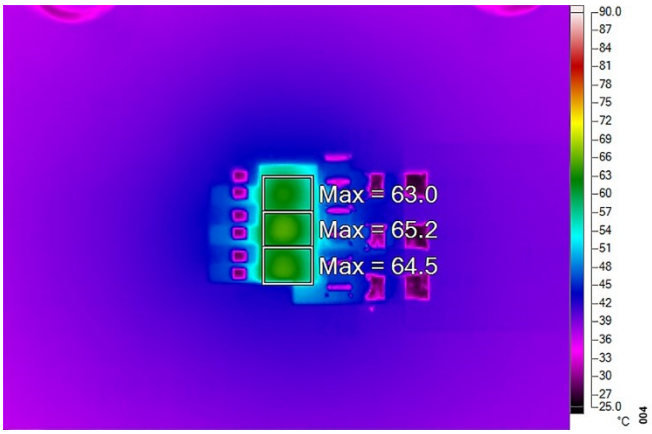

Figure 4. EVAL-LTM4709-BZ Thermal Image of LTM4709 V_{BIAS} = 5V, V_{IN} = 1.3V, V_{OUT} = 1V, I_{OUT} = 9A, No Airflow, T_A = 25°C

Printed Circuit Board (PCB) Layout

Best PSRR Performance: PCB Layout for Input Traces

For applications using the LTM4709 for post-regulating switching converters, placing a capacitor directly at the LTM4709 input results in AC current (at the switching frequency) flowing near the LTM4709. Without careful attention to the PCB layout, this relatively high-frequency switching current generates an electromagnetic field (EMF) that couples with the LTM4709 output, degrading its effective PSRR. Since the PSRR is highly dependent on the PCB, the switching preregulator, the input capacitor size, and other factors, the PSRR can easily degrade at high frequencies. This degradation is present even if the LTM4709 is desoldered from the board because it effectively degrades the PSRR of the PCB itself. While negligible for conventional low PSRR low dropout (LDO) regulators, the high PSRR of the LTM4709 requires careful attention to higher-order parasitics to realize the full performance offered by the regulator.

The EVAL-LTM4709-BZ alleviates this degradation in PSRR by using a specialized layout technique. On Layer 3, the input trace (V_{IN}) is highlighted in red (see *Figure 5*) with the return path (GND) highlighted on Layer 4, along with the input capacitors for each channel (see *Figure 6*). When an AC voltage is applied to the input of the EVAL-LTM4709-BZ, AC current flows on the path formed through the input capacitors by the input and ground traces. Without the proper PCB layout, the AC current that flows on this path can generate EMFs that do not completely cancel and coupled to the output capacitors and related traces, making the PSRR appear worse than it is. With the input trace directly above the return path, the EMFs are in opposite directions, and consequently, cancel each other out. Ensure that these traces exactly overlap each other to maximize the cancellation effect and thus provide the maximum PSRR offered by the regulator.

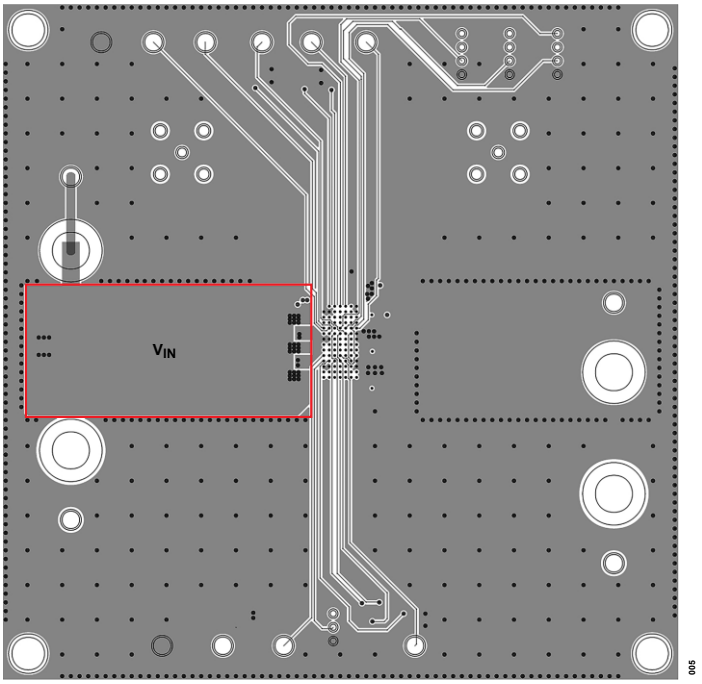

Figure 5. EVAL-LTM4709-BZ Layer 3

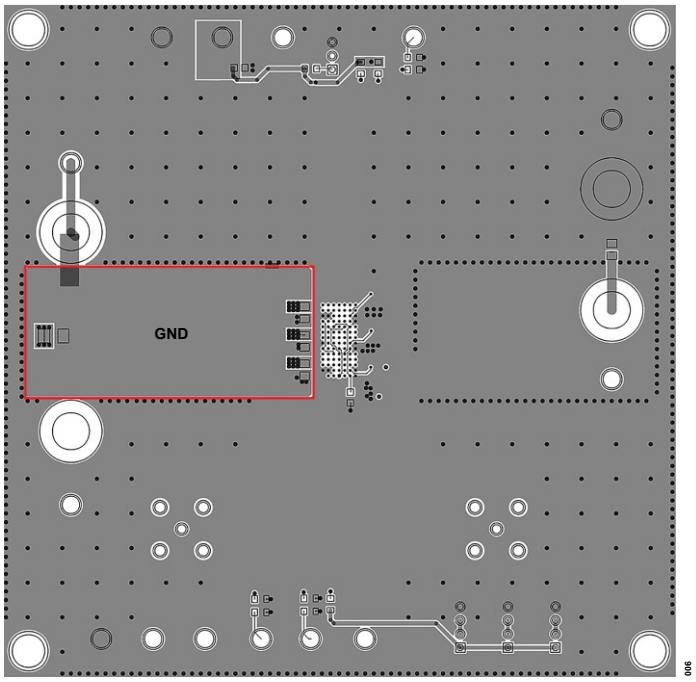

Figure 6. EVAL-LTM4709-BZ Layer 4

Ordering Information

PART NUMBER	DESCRIPTION
EVAL-LTM4709-BZ	The EVAL-LTM4709-BZ evaluation board features the LTM®4709, a triple 3A, ultralow noise, high PSRR, and ultrafast µModule® linear regulator with a configurable output array.

EVAL-LTM4709-BZ Evaluation Board Bill of Materials

SERIAL NUMBER	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	C1	CAP., 22µF, X7R, 10V, 10%, 1206	MURATA, GRM31CR71A226KE15L
2	3	C7-C9	CAP., 4.7µF, X5R, 16V, 20%, 0805	WURTH ELEKTRONIK, 885012107013
3	3	C13-C15	CAP., 22µF, X7R, 16V, 10%, 1210	MURATA, GCM32ER71C226KE19L
4	1	C19	CAP., 4.7µF, X5R, 16V, 10%, 0603	MURATA, GRM188R61C475KE11D
5	6	R2, R4, R6, R7, R19, R21	RES., 0Ω, 1/10W, 0603	VISHAY, CRCW06030000Z0EA
6	1	R8	RES., 100kΩ, 1%, 1/10W, 0603	VISHAY, CRCW0603100KFKEA
7	3	R26-R28	RES., 0.002Ω, 1%, 2W, 2010	VISHAY, WSLP20102L000FEA
8	1	U1	IC, ANALOG DEVICES ULTRALOW NOISE, HIGH PSRR, ULTRAFAST 50mV LOW DROPOUT LINEAR REGULATOR µModule WITH CONFIGURABLE TRIPLE 3A OUTPUT ARRAY	ANALOG DEVICES, LTM4709IY#PBF
Additional Demo Board Circuit Components				
1	0	C4-C6, C16	CAP., OPTION, 0805	
2	0	C10	CAP., OPTION, 0603	
3	0	R1, R3, R5	RES., OPTION, 0603	
Hardware: For Demo Board Only				
1	2	J1, J2	CONN., RF, BNC, RCPT, JACK, 5-PIN, ST, THT, 50Ω	AMPHENOL RF, 112404
2	3	P2, P5, P14	CONN., HDR., MALE, 1×4, 2mm, VERT, ST, THT	WURTH ELEKTRONIK, 62000411121
3	1	P17	CONN., HDR, MALE, 1×3, 2mm, VERT, ST, THT	WURTH ELEKTRONIK, 62000311121
4	14	TP1-TP4, TP6, TP9, TP12-TP17, TP22, TP23	CONN., TURRET, 0.094" MTG. HOLE, PCB 0.062" THK	MILL-MAX, 2501-2-00-80-00-00-07-0
5	4	TP10, TP11, TP32, TP33	CONN., BANANA JACK, FEMALE, THT, NON-INSULATED, SWAGE, 0.218"	KEYSTONE, 575-4
6	4		CONN., SHUNT, FEMALE, 2-POS, 2mm	WURTH ELEKTRONIK, 60800213421
7	4		STANDOFF, SELF-RETAINING SPACER, 12.7mm LENGTH	WURTH ELEKTRONIK, 702935000
8	1	PCB1	PCB, EVAL-LTM4709-BZ	ANALOG DEVICES APPROVED SUPPLIER, 08_068340b

EVAL-LTM4709-BZ Evaluation Board Schematic

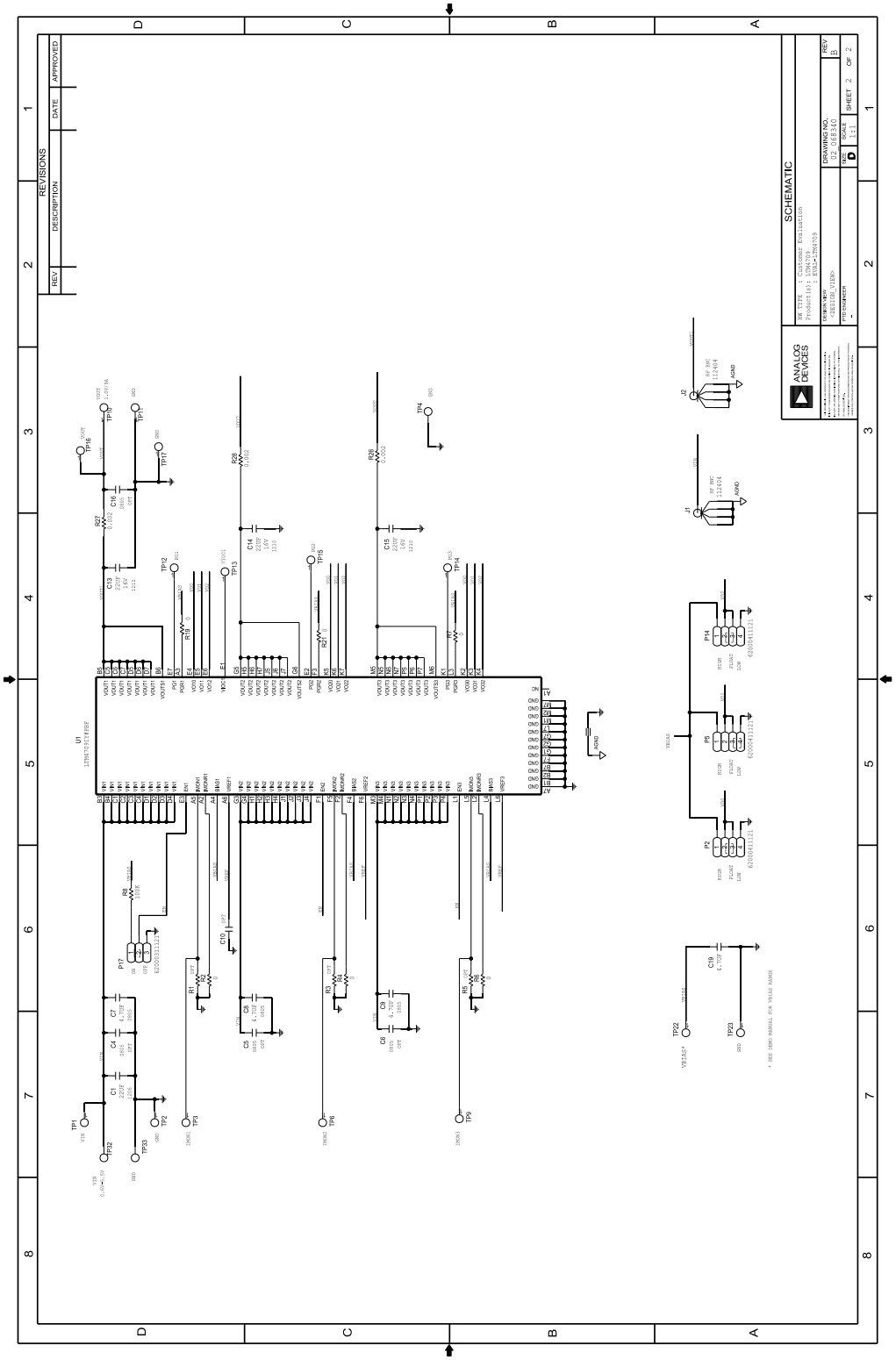

Figure 7. EVAL-LTM4709-BZ Schematic

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	02/24	Initial release	—

Notes