EV2HMC998APM5 Evaluation Board for GaAs, pHEMT, MMIC, Power Amplifier, DC to 22 GHz

FEATURES

- 2-layer Rogers 4350B evaluation board with heat spreader and wideband, surface-mount bias tee circuit
- End launch, 2.92 mm RF connectors
- Through calibration path

EVALUATION KIT CONTENTS

- EV2HMC998APM5 with heat spreader

EQUIPMENT NEEDED

- RF signal generator
- RF spectrum analyzer
- RF network analyzer
- 15 V, 0.8 A power supply
- −1.5 V, 100 mA power supply

GENERAL DESCRIPTION

The EV2HMC998APM5 consists of a 2-layer printed circuit board (PCB) fabricated from 10 mil thick, Rogers 4350B, copper clad, mounted to an aluminum heat spreader. The heat spreader assists in providing thermal relief to the device as well as mechanical support to the PCB. Mounting holes on the heat spreader allow it to be attached to a heat sink for improved thermal management. The RFIN and RFOUT ports are populated with 2.9 mm, female coaxial connectors, and their respective RF traces have a 50 Ω characteristic impedance.

The EV2HMC998APM5 differs from the EV1HMC998APM5 in one key respect. Whereas the EV1HMC998APM5 requires an external connectorized bias tee on its RFOUT port to operate (see the HMC998APM5E data sheet for additional details), the EV2HMC998APM5 contains an on-board, surface-mount bias tee circuit. This circuit allows the EV2HMC998APM5 to connect directly to RF test equipment, such as network analyzers and spectrum analyzers. This on-board, surface-mount bias tee circuit has an operating frequency up to approximately 22 GHz (see Figure 3).

The EV2HMC998APM5 is populated with components suitable for use over the entire operating temperature range of the HMC998APM5E. To calibrate out board trace losses, a through calibration path, THRU-CAL, is provided between the J5 and J6 connectors. J5 and J6 must be populated with 2.92 mm RF connectors to use the through calibration path. Refer to Figure 4 and Table 2 for the through calibration path performance. The power voltages, ground voltages, gate control voltages, and detector output voltages are accessed through two 4-pin headers, J3 and J4 (see Table 1).

The RF traces are 50 Ω, grounded, coplanar waveguide. The package ground leads and the exposed paddle connect directly to the ground plane. Multiple vias are used to connect the top and bottom ground planes, with particular focus on the area directly beneath the ground paddle, to provide adequate electrical and thermal conduction to the heat spreader.

The decoupling capacitors on the EV2HMC998APM5 represent the configuration used to measure the performance of the circuit, which is detailed in AN-2061. It is possible to reduce the number of capacitors connected to the ACG2, ACG3/ACG4, $V_{GG}1$, and $V_{GG}2$ pins, but this reduction varies from system to system. It is recommended to first remove the largest capacitors that are farthest from the HMC998APM5E when reducing the number of capacitors.

For full details on the HMC998APM5E, see the HMC998APM5E data sheet, which must be consulted in conjunction with this user guide when using the EV2HMC998APM5.

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REVISION HISTORY

12/2023—Revision 0: Initial Version

EV2HMC998APM5 EVALUATION BOARD PHOTOGRAPHS

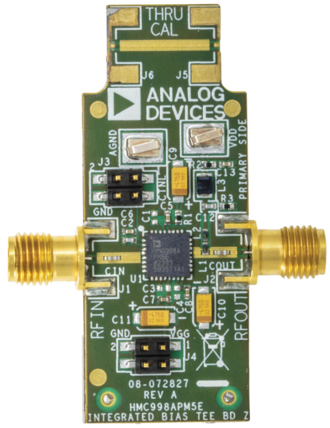

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Figure 1. Primary Side

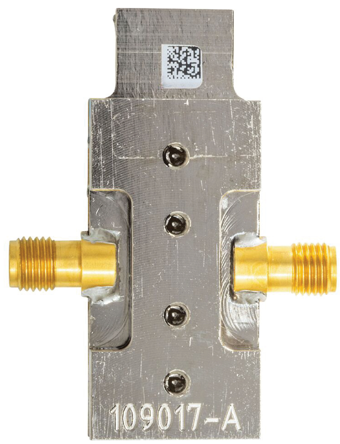

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Figure 2. Secondary Side

OPERATING THE EV2HMC998APM5

A 15 V, 0.8 A power supply is required to provide the main bias to the EV2HMC998APM5. Connect the 15 V power supply to the on-board, wideband, drain biasing network through the VDD clip lead. In addition, a −1.5 V, 100 mA power supply is required to provide the gate control voltage. Connect the −1.5 V power supply to the $V_{GG}1$ pin on the EV2HMC998APM5 through Pin 1 and Pin 3 of the J4 header.

DURING POWER-UP

The recommended bias sequence during power-up is as follows:

1. Connect GND to the RF and DC ground.
2. Initially set $V_{GG}1$ and V_{DD} to 0 V.
3. Set the $V_{GG}1$ voltage to −1.5 V.
4. Set V_{DD} to 15 V.
5. Increase the $V_{GG}1$ voltage to achieve a quiescent drain current of 500 mA.
6. Apply the RF input signal.

DURING POWER-DOWN

The recommended bias sequence during power-down is as follows:

1. Turn off the RF signal.
2. Decrease the $V_{GG}1$ voltage to −1.5 V to achieve supply current (I_{DQ}) = 0 mA (approximately).
3. Decrease V_{DD} to 0 V.
4. Increase $V_{GG}1$ to 0 V.

Table 1. Connections to the EV2HMC998APM5

Connector or Header Pin	Function Description
J1	Connects to the RFIN pin through the CIN AC coupling capacitor
J2	Connects to the RFOUT/V_{DD} pin through the COUT AC coupling capacitor
J3: Pin 1 and Pin 3	Connects to the $V_{GG}2$ pin
J3: Pin 2 and Pin 4	Ground
J4: Pin 1 and Pin 3	Connects to the $V_{GG}1$ pin
J4: Pin 2 and Pin 4	Ground
J5, J6	Connects to the RF through calibration path
VDD Clip Lead	Connects to the wideband bias tee network
AGND Clip Lead	Ground

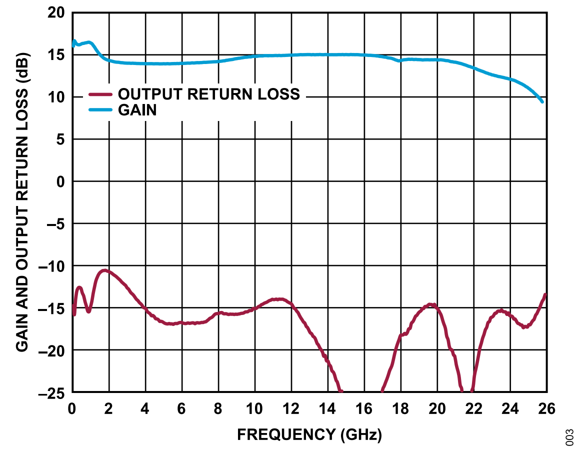

Figure 3. Gain and Output Return Loss of the EV2HMC998APM5

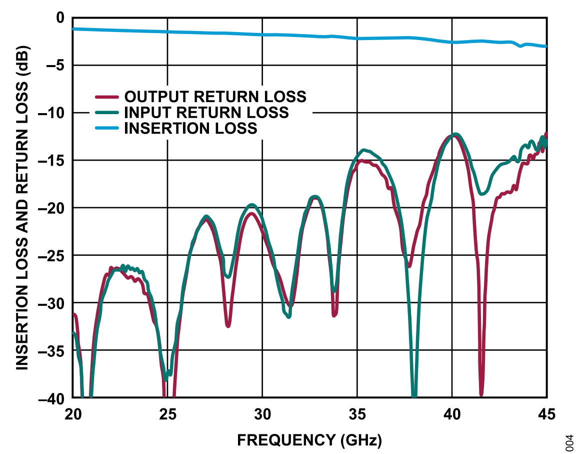

Figure 4. Insertion Loss and Return Loss of the Through Calibration Path

Table 2. Insertion Loss of the Through Calibration Path

Frequency (GHz)	Insertion Loss (dB)
0.01	0.037
0.1	0.059
1	0.265
5	0.566
10	0.709
15	0.916
20	1.142
22	1.355
25	1.48
30	1.671

EVALUATION BOARD SCHEMATIC AND ARTWORK

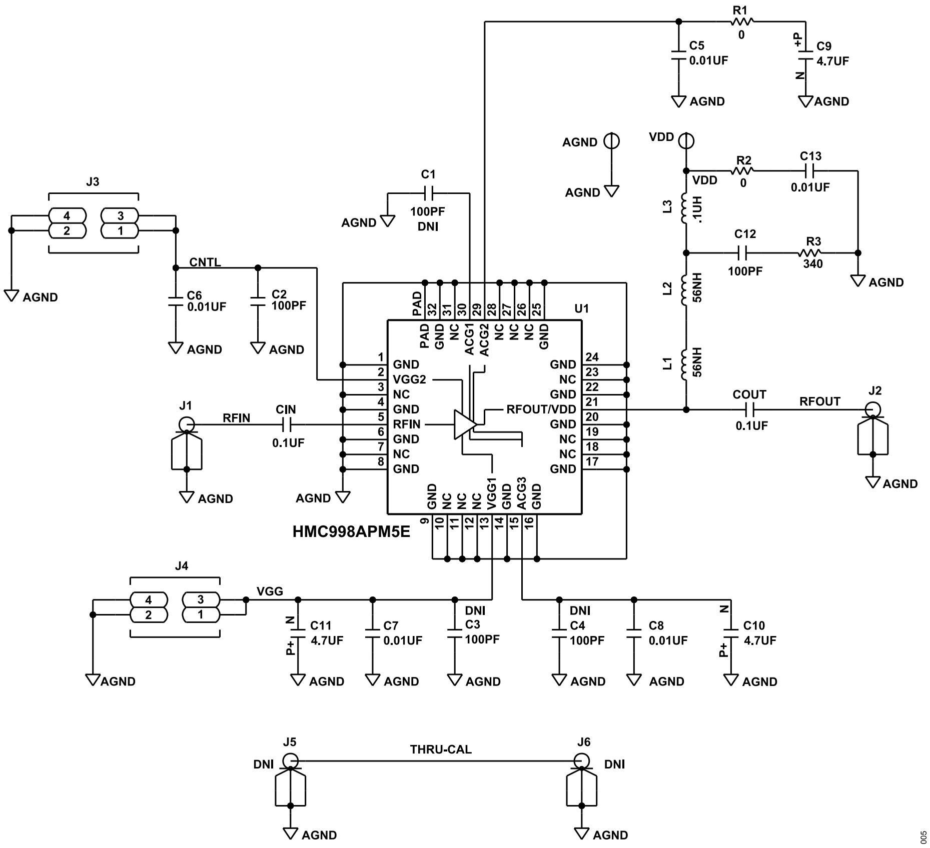

Figure 5. EV2HMC998APM5 Schematic

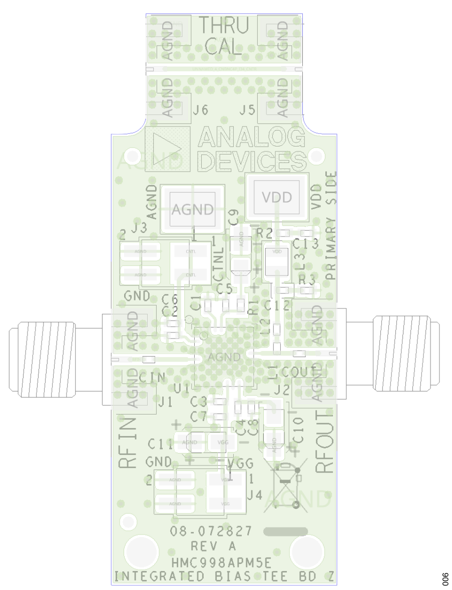

Figure 6. EV2HMC998APM5 Assembly Drawing

ORDERING INFORMATION

BILL OF MATERIALS

Table 3. EV2HMC998APM5 BOM

Reference Designator	Description	Value	Manufacturer	Part Number
C2	Capacitor, ceramic	100 pF	Johanson Dielectrics	500R07N101JV4T
C1 ,C3, C4	Capacitors, ceramic, C0G, do not install (DNI)	100 pF	Johanson Dielectrics	500R07N101JV4T
C5 to C8, C13	Capacitors, multilayer, ceramic, XR7	0.01 µF	TDK	C1005X7S2A103K050BB
C9, C10, C11	Capacitors, tantalum	4.7 µF	AVX	TAJA475K020RNJ
C12	Capacitor, ceramic, C0G	100 pF	Yageo	CC0402JRNPO9BN101
CIN, COUT	Capacitors, ceramic, 16 V + 20%, 0402	0.1 µF	ATC	ATC560L104YTT
J1, J2	Connectors, K jack edge	Not applicable	SRI Connector Gage Co.	25-146-1000-92
J5, J6	Connectors, K jack edge DNI	Not applicable	SRI Connector Gage Co.	25-146-1000-92
J3, J4	Connectors, PCB, 4-position, unshrouded, dual row header, 0.5 mm, 2 mm pitch, 3.8 mm post height	Not applicable	Molex	87759-0414
L1, L2	Chip inductors, 5%, 0.061 Ω, DC resistance (DCR), 1.2 A	56 nH	Coilcraft Inc.	0402DF-560XJR
L3	Inductor, 0805, 5%, 110 nH	0.11 µH	Coilcraft Inc.	0805LS-111XJLC
R1, R2	Resistors, thick film chip	0 Ω	Panasonic	ERJ-2GE0R00X
R3	Resistor, metal thin film chip, high reliability	340 Ω	Panasonic	ERA-2AEB3400X
U1	IC, gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC), power amplifier, DC to 22 GHz	Not applicable	Analog Devices, Inc.	HMC998APM5E
AGND, VDD	Connectors, PCB, surface-mount technology (SMT) test points	Not applicable	Keystone Electronics	5016
Not applicable	Aluminum heat spreader	Not applicable	Not applicable	M027558