

## Evaluating the ADuM4121 Single-/Dual-Supply, High-Voltage, Isolated SiC Gate Driver with Miller Clamp

# **FEATURES**

- Optimized for use with Wolfspeed SiC MOSFETs and power modules
- Compatible with Wolfspeed CIL test boards and half-bridge evaluation boards
- ▶ High-frequency, ultrafast switching operation
- ▶ Input and output side UVLO
- ► Shoot-through protection interlock
- Internal Miller clamp
- Differential inputs for increased noise immunity
- ▶ Isolated NTC thermistor measurement
- Onboard 2 W Isolated Power Supplies

## **EVALUATION KIT CONTENTS**

► EVAL-ADuM4121WHB1Z evaluation board

# **EQUIPMENT NEEDED**

- Wolfspeed SpeedVal Kit<sup>™</sup> modular evaluation platform
- ▶ Wolfspeed differential transceiver board (CGD12HB00D)
- ▶ For evaluating Wolfspeed half-bridge modules:
  - CAB011M12FM3 or CAB016M12FM3
  - ▶ Wolfspeed CIL board (KIT-CRD-CIL12N-FMA)
- ► For evaluating Wolfspeed six-pack modules:
  - ► CCB021M12FM3 or CCB032M12FM3
  - ▶ Wolfspeed CIL board (KIT-CRD-CIL12N-FMC)

## **DOCUMENTS NEEDED**

► ADuM4121 data sheet

#### **GENERAL DESCRIPTION**

The EVAL-ADuM4121WHB1Z is a half-bridge gate drive board that allows simple evaluation of the performance of the ADuM4121 when driving advanced Wolfspeed silicon carbide (SiC) metal-oxide semiconductor field-effect transistors (MOSFETs) and power modules. The EVAL-ADuM4121WHB1Z is intended to be used with the Wolfspeed SpeedVal Kit modular evaluation platform and Wolfspeed clamped inductive load (CIL) test boards or with the half-bridge evaluation boards and differential transceiver boards.

The EVAL-ADuM4121WHB1Z has an isolated return channel that is configured to read a negative temperature coefficient (NTC) thermistor and provide a variable frequency output corresponding to the resistance and temperature of the NTC.

The control and input interface for the EVAL-ADuM4121WHB1Z uses RS-422 signaling for improved noise and disturbance immunity and includes a 12 V power input for the EVAL-AD-uM4121WHB1Z.

For full details on the ADuM4121, see the ADuM4121 data sheet, which must be consulted when using the EVAL-ADuM4121WHB1Z.

# **EVALUATION BOARD PHOTOGRAPH**



Figure 1. EVAL-ADuM4121WHB1Z

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# **REVISION HISTORY**

7/2023—Revision 0: Initial Version

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# **EVALUATION BOARD HARDWARE**

#### LOGIC SIDE DIFFERENTIAL INTERFACE

The P2 logic side interface connector is a 16-position, 100 mil (2.54 mm) pitch, dual row header that is compatible with standard insulation displacement contact (IDC) connectors. The pinout for this interface is described in Table 1.

Table 1. Control Interface (P2) Pinout

Pin No.	Parameter <sup>1</sup>	Description
1	$V_{DC}$	12 V nominal power supply input.
2	Common	Common.
3	HS-P	Positive line of the 5 V differential, high- side, pulse-width-modulation (PWM) signal pair.
4	HS-N	Negative line of the 5 V differential, high-side, PWM signal pair.
5	LS-P	Positive line of the 5 V differential, low-side, PWM signal pair.
6	LS-N	Negative line of the 5 V differential, low-side, PWM signal pair.
7	No Connection	No Connection
8	No Connection	No Connection
9	RTD-P	Positive line of the 5 V differential, temperature dependent resistor, output signal pair.
10	RTD-N	Negative line of the 5 V differential, temperature dependent resistor, output signal pair.
11	No Connection	No connection.
12	Common	Common.
13	No Connection	No connection.
14	Common	Common.
15	No Connection	No connection.
16	Common	Common.

<sup>&</sup>lt;sup>1</sup> Pin 3 to Pin 10 are differential pairs.

## **OUTPUT CONNECTIONS TO POWER SWITCH**

The P7 and P8 output connectors connect to the power switch interface board using a 4-position header, 100 mil (2.54 mm) pitch, through-hole, gold plated connector (Samtec SSW-102-01-G-D).

The P4 and P5 output connectors provide Miller clamp connection to the power switch interface board using a 2-position header, 100 mil (2.54 mm) pitch, through-hole, gold plated connector (Samtec SSW-101-01-G-D).

# NTC THERMISTOR TEMPERATURE FEEDBACK

The EVAL-ADuM4121WHB1Z provides a varying frequency square wave on Pin 9 and Pin 10 of the P2 interface connector that is related to the resistance of an NTC thermistor. Note that one terminal of the thermistor is electrically connected to the low-side switch source.

The ADuM4190 isolated amplifier measures the voltage generated by the biased NTC thermistor and provides a scaled voltage that is galvanically isolated from the thermistor. The LTC6990 voltage-controlled oscillator (VCO) generates a varying frequency square wave based on this scaled voltage.

Table 2 shows the output frequency as a function of the NTC temperature when the EVAL-ADuM4121WHB1Z NTC input is connected to a Littelfuse SM502F1K NTC thermistor.

The temperature reported by the NTC differs largely from the junction temperature of the SiC MOSFETs. Therefore, it is not recommended to use the temperature reported by the NTC as an accurate junction temperature measurement.

Table 2. Temperature to Output Frequency

NTC Thermistor Temperature (°C)	NTC Thermistor Resistance ( $\Omega$ )	Output Frequency (kHz)
0	14,283	6.71
25	5,000	20.38
50	2,059	30.29
75	963	35.70
100	499	38.45
125	281	39.85
150	169	40.60
175	108	41.02

## **CONFIGURATION JUMPERS AND RESISTORS**

# Shoot-Through Protection Interlock

The shoot-through protection interlock feature of the ADuM4121 can be enabled or disabled based on the population of the R3 and R4 resistors (high-side) or R5 and R6 resistors (low-side). This interlock only allows one switch, high-side or low-side, to be on at the same time. Attempting to turn both switches on at the same time when the interlock is enabled results in both switches turning off.

Populating R4 or R6 with a 0603 package, 0  $\Omega$  resistor (and depopulating R3 or R5) disables the shoot-through protection interlock of the associated gate driver.

Populating R3 or R5 with a 0603 package, 0  $\Omega$  resistor (and depopulating R4 or R6) enables the shoot-through protection interlock of the associated gate driver.

The EVAL-ADuM4121WHB1Z by default has the shoot-through protection interlock enabled for both the high-side and low-side gate drivers.

## **TEST POINTS**

The EVAL-ADuM4121WHB1Z contains test points that allow the testing and monitoring of key signals on the gate drive board.

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# **EVALUATION BOARD HARDWARE**

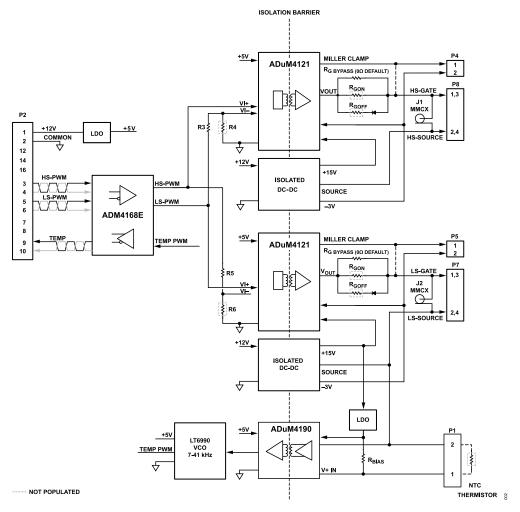


Figure 2. Block Diagram

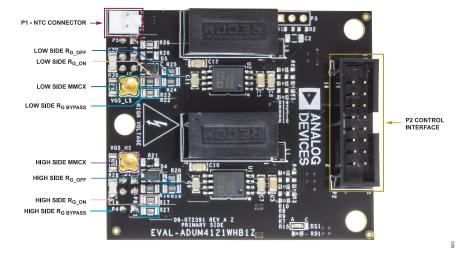


Figure 3. Top Side Feature Locations

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# **EVALUATION BOARD HARDWARE**

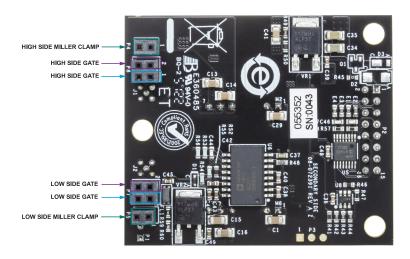


Figure 4. Bottom Side Feature Locations

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# **BOARD USE AND CONFIGURATION**

## **GATE DRIVE RESISTOR SELECTION**

The EVAL-ADuM4121WHB1Z provides two output paths for driving a switch. The benefit of this approach is that the user can select two different series resistances, one for the turn on and one for the turn off, which allow different turn-on and turn-off times. It is generally desired to have the turn off occur faster than the turn on.

To select the series resistance, choose the maximum allowed peak current ( $I_{PEAK}$ ) for the switch. Knowing the voltage swing on the gate, as well as the internal resistance of the gate driver, an external gate resistor ( $R_{G\ OFF}$  or  $R_{G\ ON}$ ) can be chosen.

$$I_{PEAK} = (V_{DD2} - V_{SS2}) / (R_{DSON N} + R_{G OFF})$$
 (1)

where  $R_{DSON\ N}$  is the pull-down n-channel metal-oxide semiconductor (nMOS) transistor on resistance.

Solve for  $R_{G\ OFF}$  using the following equation:

$$R_{G OFF} = ((V_{DD2} - V_{SS2}) - I_{PEAK} \times R_{DSON N}) / I_{PEAK}$$
 (2)

For example, if the turn-off peak current is 4 A with a nominal  $R_{DSON\_N}$  value of 0.6  $\Omega$  and a ( $V_{DD2}$  –  $V_{SS2}$ ) value of 18 V, the value is calculated as follows:

$$R_{G OFF} = (18 \text{ V} - 4 \text{ A} \times 0.6 \Omega) / 4 \text{ A} = 3.9 \Omega$$
 (3)

After  $R_{G\_OFF}$  is selected, a slightly larger  $R_{G\_ON}$  can be selected to arrive at a slower turn-on time.

If the selected switch has a nonzero internal gate resistance ( $R_G$ ), then this resistance must be subtracted from the calculated  $R_{G\_OFF}$  to arrive at the final  $R_{G\_OFF}$ .

The EVAL-ADuM4121WHB1Z is primarily intended to work with Wolfspeed SpeedVal Kit that already features an on-board  $R_G$ . For this reason, the default board configuration is with  $R_G$  bypassed (R17, R22 = 0  $\Omega$ ).

## **POWER DISSIPATION**

The power required by the gate driver is a function of the switch gate charge, switching frequency, and gate voltage swing. For one channel, the power dissipation is calculated using the following equation:

$$P_{SW} = Q_G \times F_{SW} \times (V_{DD2} - V_{SS2}) \tag{4}$$

where:

Q<sub>G</sub> is the switch gate charge.

 $F_{SW}$  is the switching frequency.

 $V_{DD2}$  and  $V_{SS2}$  are the isolated supply voltages.

For the EVAL-ADuM4121WHB1Z,  $V_{DD2} = 15 \text{ V}$  and  $V_{SS2} = -3 \text{ V}$ .

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# **EVALUATION BOARD SCHEMATIC**

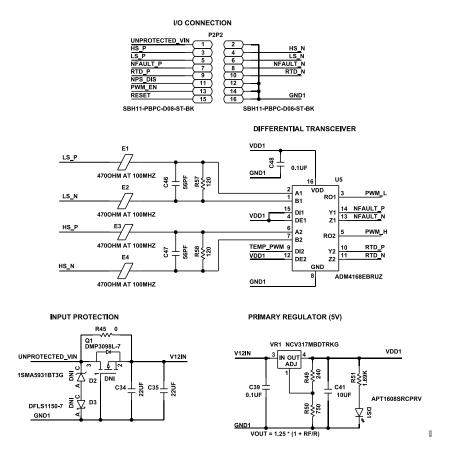


Figure 5. I/O Connection

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# **EVALUATION BOARD SCHEMATIC**

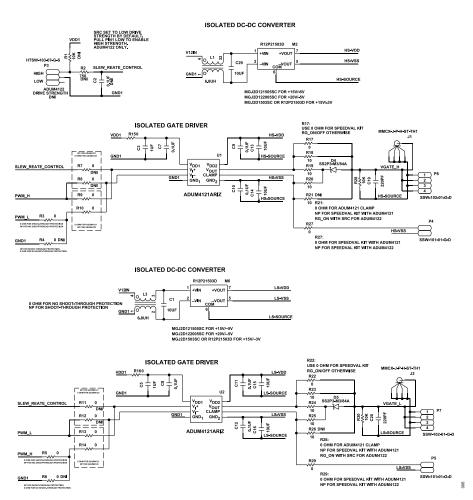


Figure 6. Isolated Gate-Drivers and Isolated Supply

#### ISOLATED TEMPERATURE MEASUREMENT

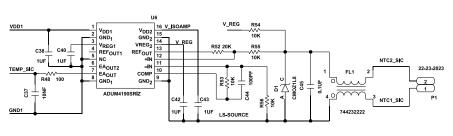




Figure 7. Isolated Temperature Measurement

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# **EVALUATION BOARD LAYOUT AND SILKSCREENS**

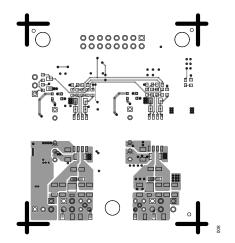


Figure 8. EVAL-ADuM4121WHB1Z Layout - L1 Top Layer

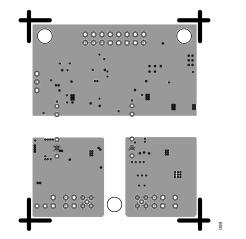


Figure 9. EVAL-ADuM4121WHB1Z Layout - L2 Second Layer

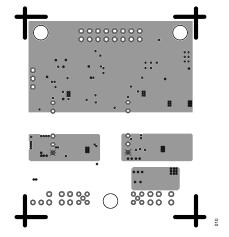


Figure 10. EVAL-ADuM4121WHB1Z Layout – L3 Third Layer

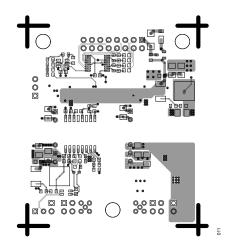


Figure 11. EVAL-ADuM4121WHB1Z Layout – L4 Bottom Layer

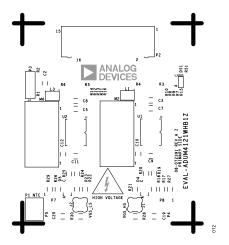


Figure 12. EVAL-ADuM4121WHB1Z Layout - Silkscreen Top

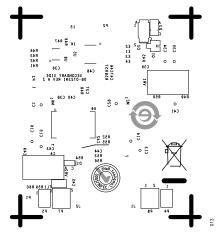


Figure 13. EVAL-ADuM4121WHB1Z Layout - Silkscreen Bottom

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# **ORDERING INFORMATION**

# **BILL OF MATERIALS**

LOCATION	DESCRIPTION	PART NUMBER	MANUFACTURER
C1, C13, C14, C15, C16, C29, C41	CAP CER, 10 μF, 50 V, 10% X7R 1206	CGA5L1X7R1H106K160AC	TDK
C7, C8, C9, C10, C11, C12	CAP CER, 0.1 µF, 50 V, 5% X7R 1206	12065C104JAT2A	AVX
C19, C20	CAP CER, 220 pF, 500 V, 5% C0G 1206	12067A221JAT2A	AVX
C3, C5	CAP CER, 1 µF, 25 V, 10% X7R 1206	C1206R105K3RAC7800	KEMET
C34, C35	CAP CER, 22 µF, 25 V, 20% X5R 1206	TMK316BBJ226ML-T	Taiyo Yuden
C36, C39, C45, C48, C49	CAP CER, 0.1 µF, 50 V, 10% X7R 0603	06035C104KAT2A	AVX
C37	CAP CER, 10 nF, 100 V, 10% X7R 0603	GCM188R72A103KA37J	Murata
C4, C38, C40, C42, C43	CAP CER, 1 µF, 35 V, 10% X7R 0603	C1608X7R1V105K080AC	TDK
C44	CAP CER, 100 pF, 50 V, 10% X7R 0603	C0603C101K5RAC	KEMET
C46, C47	CAP CER, 56 pF, 50 V, 5% C0G 0603	223886715569	Phycomp (Yageo)
D1	DIODE ZENER	CMOZ1L8 PBFREE	Central Semiconductor
D4, D5	DIODE SCHOTTKY BARRIER RECT	SS2P3-M3/84A	Vishay
DS1	LED 1.6 x 0.8 mm RED 640 nm	APT1608SRCPRV	Kingbright
E1, E2, E3, E4	IND FERRITE BEAD, 0.150 Ω direct conversion receiver (DCR), 1A	MPZ1608B471ATA00	TDK
FL1	Filter choke common-mode noise suppressor	744232222	Wurth Elektronik Group
J1, J2	CONN-PCB, 50 $\Omega$ , male micro-miniature coaxial (MMCX) connector straight through (ST) plug	MMCX-J-P-H-ST-TH1	Samtec Inc.
L1, L3	IND COUPLED CHIP, common-mode choke, 0.63 Ω, DCR 0.7A	PFD3215-682MEC	Coilcraft, Inc.
M2, M6	MOD DC-to-DC converters, 2 W, 12 V voltage input, +15 V to -3 V voltage output	R12P21503D	RECOM Power
P1	CONN-PCB, 2 point-of-sale (POS), male high dose rate (HDR) ST, 2.54 mm pitch, 3.68 mm solder tail	22-23-2023	Molex
P2	CONN-PCB, 16 POS, ST male header dual row, 2.54 mm pitch	SBH11-PBPC-D08-ST-BK	Sullins
P4, P5	CONN-PCB, 2 POS, female high dose rate (HDR) double row ST, 2.54 mm pitch	SSW-101-01-G-D	Samtec Inc.
P7, P8	CONN-PCB, 4 POS, female HDR double row ST, 2.54 mm pitch	SSW-102-01-G-D	Samtec Inc.
R3, R5, R9, R10, R13, R14, R15, R16, R45	RES SMD, 0 $\Omega$ , jumper, 1/10 W, 0603	RC0603JR-070RL	Yageo
R17, R22, R27, R29	RES SMD, 0 Ω, jumper, 1/4 W, 1206	ERJ-8GEY0R00V	Panasonic
R18, R19, R20, R23, R24, R25	RES SMD, 10 Ω, 1% 1/2 W, 1206	RCS120610R0FKEA	Vishay
R28, R30	RES SMD, 10 kΩ, 1% 1/4 W, 1206	ERJ-8ENF1002V	Panasonic
R41	RES SMD, 49.9 kΩ, 1% 1/10 W, 0603	ERJ-3EKF4992V	Panasonic
R42, R43, R44	RES SMD, 100 kΩ, 5% 1/10 W, 0603	RC0603JR-07100KL	Yageo
R46	RES SMD, 1 MΩ, 1% 1/10 W, 0603	CRCW06031M00FKEA	Vishay
R47	RES SMD, 390 kΩ, 1% 0.1 W, 0603	ERJ-S03F3903V	Panasonic
R48	RES SMD, 100 Ω, 0.1% 1/10 W, 0603	ERA-3AEB101V	Panasonic
R49, R59	RES SMD, 240 Ω, 1% 1/10 W, 0603	CRCW0603240RFKEA	Vishay
R50	RES SMD, 750 Ω, 1% 1/10 W, 0603	CRCW0603750RFKEA	Vishay
R51, R60	RES SMD, 1.69 kΩ, 1% 1/10 W, 0603	RC0603FR-071K69L	Yageo
R52	RES SMD, 20 kΩ, 1% 1/10 W, 0603	CRCW060320K0FKEA	Vishay
R53, R54, R55, R56	RES SMD, 10 kΩ, 1% 1/8 W, 0603	MCT06030C1002FP500	Vishay
R57, R58	RES SMD, 120 Ω, 1% 1/10 W, 0603	ERJ-3EKF1200V	Panasonic
U1, U2	IC-ADI, high-voltage isolated gate driver with Miller clamp	ADUM4121ARIZ	Analog Devices, Inc.
U5	IC-ADI, 15 kV, electrostatic discharge (ESD) protected, dual RS-422 transceiver	ADM4168EBRUZ	Analog Devices
U6	IC-ADI, high stability isolated error amplifier	ADUM4190SRIZ	Analog Devices
U8	IC-ADI, voltage-controlled silicon oscillator	LTC6990HS6#TRMPBF	Analog Devices

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#### ORDERING INFORMATION

LOCATION	DESCRIPTION	PART NUMBER	MANUFACTURER	
VR1, VR2	IC-LIN, 0.5 A, adjustable output, positive voltage regulator	NCV317MBDTRKG	onsemi	
C2	Not populated: CAP CER, 0.1 μF, 50 V, 5% X7R 1206	12065C104JAT2A	AVX	
D2	Not populated: DIODE ZENER, voltage regulators, 18 V, 1.5 W 5% Subminiature Version A (SMA)	1SMA5931BT3G	onsemi	
D3	Not populated: DIODE SCHOTTKY BARRIER RECT, 1A	DFLS1150-7	Diodes Incorporated	
P3	Not populated: CONN-PCB, 3 POS, male HDR unshrouded single row ST, 2.54 mm pitch	HTSW-103-07-G-S	Samtec Inc.	
Q1	Not populated: TRAN, Tp-channel enhancement mode metal oxide semiconductor field effect transistor (MOSFET)	DMP3098L-7	Diodes Incorporated	
R1	Not populated: RES SMD, 10 k $\Omega$ 1% 1/8 W, 0603	MCT06030C1002FP500	Vishay	
R4, R6, R7, R8, R11, R12	Not populated: RES SMD, 0 Ω, jumper, 1/10 W, 0603	RC0603JR-070RL	Yageo	
R2	Not populated: RES SMD, 750 Ω, 1% 1/10 W, 0603	CRCW0603750RFKEA	Vishay	
R21, R26	Not populated: RES SMD, 10 Ω, 1% 1/2 W, 1206	RCS120610R0FKEA	Vishay	



#### ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

#### **Legal Terms and Conditions**

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