ADRV904x Evaluation System User Guide

INTRODUCTION

The ADRV904x family evaluation system enables customers to evaluate an ADRV904x device without having to develop custom hardware or software. The system is comprised of an ADRV904x customer evaluation (CE) board and an ADS10-V1EBZ motherboard with accompanying wall adapter power supplies for both. The evaluation software uses the Analysis, Control, Evaluation (ACE) software developed by Analog Devices, Inc., extended by an ADRV904x specific board plugin. This plugin can be run with ACE on a Windows host PC communicating with the ADS10-V1EBZ motherboard using Ethernet. The ADS10-V1EBZ functions as a baseband processor running an application (ADRV904x command server) for controlling and communicating with the ADRV904x device.

This document also serves as a quick startup guide for the ADRV904x configurator, which is built into the ADRV9040 board plugin for ACE. The ADRV904x configurator allows the user to explore various configurations of an ADRV904x device to arrive at a desired use case configuration. The ADRV904x configurator also provides an overview of the frequency responses of the receiver (Rx), transmitter (Tx), and the observation receiver (ORx) datapaths for a chosen configuration.

This user guide details the steps required to install the ADRV904x evaluation software, program an existing use case, and evaluate the ADRV904x transmitter, receiver, and observation receiver datapaths. The configurator sections of this user guide enable the user to generate a new use case and view its corresponding datapath configurations and filter graphs for the ADRV904x. Note that this document updates as the configurator development progresses and as additional functionalities are added to the tool.

INITIAL SETUP

The ACE GUI is the graphical user interface (GUI) used to communicate with the evaluation platform. The GUI can run with or without evaluation hardware connected. When ACE runs without the hardware connected, the GUI can be fully configured for a particular operating mode. If the evaluation hardware is connected, the desired operating parameters can be setup with ACE and then the software can program the evaluation hardware. When the transceiver is configured, the evaluation software can be used to transmit waveforms generated from the internal numerically controlled oscillator (NCO) block or using custom waveform files as well as to observe signals received on one of the receiver or observation input ports.

PLEASE SEE THE LAST PAGE FOR AN IMPORTANT WARNING AND LEGAL TERMS AND CONDITIONS.

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REVISION HISTORY

6/2024—Revision 0: Initial Version

HARDWARE KIT

The ADRV904x evaluation system consists of the following hardware:

- One (1) ADRV904x CE board with a field programmable gate array mezzanine card (FMC) connector.
- One (1) 12 V, 3 A wall connector power supply cable for the CE board.
- One (1) ADS10-V1EBZ motherboard with an FMC connector.
- One (1) 12 V, 16.6 A power supply for powering the ADS10-V1EBZ.
- One (1) FMC adapter for ADS10-V1EBZ.
- Two (2) secure digital (SD) cards along with the evaluation kit.
  - ADS10-V1EBZ transmitter V1.0 SD card (used for booting Linux on ADS10-V1EBZ and running the ADRV904x command server application).
  - SD card type is 16 GB size, Class 10.

Note that the ADRV904x CE board can be any of the ADRV904X-MB/PCBZ, ADRV904X-HB/PCBZ, and ADRV904X-LB/PCBZ. The ADS10-V1 motherboard is not included in the ADRV904x evaluation board and must be purchased separately.

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SOFTWARE REQUIREMENTS

The host PC running the ACE evaluation software must meet the following requirements:

- The operating system on the controlling PC must be Windows 10 (x86 and x64).
- The PC must have a free Ethernet port to establish a dedicated connection over the following ports:
  - Port: 22—secure shell (SSH) protocol.
  - Port: 5000—for communicating with the command server on ADS10-V1EBZ.

  If the Ethernet port is occupied by another local area network (LAN) connection, a USB to Ethernet adapter can be used.
- ADRV904x customer software package—contact your Analog Devices representative to obtain access to this software.
- The user must have administrative privileges.
- The PC must have access to the internet to run automatic software updates.

  If internet access is restricted, a manual software update can be performed. Do not upgrade to newer ACE versions as this may cause issues.

HARDWARE SETUP

To setup the evaluation hardware, follow these steps in conjunction with Figure 1:

1. Insert the SD card that comes with the evaluation kit into the ADS10-V1EBZ MicroZED MicroSD card slot (J6).
2. Mount the FMC adapter on the ADS10-V1EBZ. This step is to protect the ADS10-V1EBZ FMC connector from multiple reinsertions.
3. Connect the ADRV904x customer evaluation board and the ADS10-V1EBZ motherboard together. Use the high pin count (HPC) FMC connector (P1001/P2), ensuring the connectors are properly aligned.
4. On the ADRV904x evaluation board, provide a reference clock source (122.88 MHz is the default, or use Reference A (REFA) frequency from AD9528 clock settings), at a +7 dBm power level to the J901 connector. This signal drives the reference clock into the AD9528 clock generation chip on the board. The REFA/REFA_N pins of the AD9528 generate the DEV_CLK for the device and REF_CLK for the FPGA on the ADS10-V1EBZ platform.
5. Connect the included 12 V, 16.6 A power supply to the ADS10-V1EBZ motherboard through the P2 header.
6. Connect the ADS10-V1EBZ to the host PC with an Ethernet cable (connect to P3). No driver installation required.

A USB to Ethernet adapter can be used if no Ethernet port is available on the host PC.

- On the Ethernet connection dedicated to the ADS10-V1EBZ platform, the user must manually configure the IP address (see Figure 2):
  - IPv4 address: 192.168.1.xyz, where xyz can be assigned such that no other device on the user local network uses the same IP address. Note that xyz must not be equal to 10 because 192.168.1.10 is used by the ADRV904x command server on the ADS10-V1EBZ.
  - IPv4 subnet mask: 255.255.255.0.
- The user must ensure that the following ports are not blocked by the host PC firewall:
  - Port: 22
  - Port: 5000
- Power up the CE board using the included 12 V, 3 A wall connector power supply.

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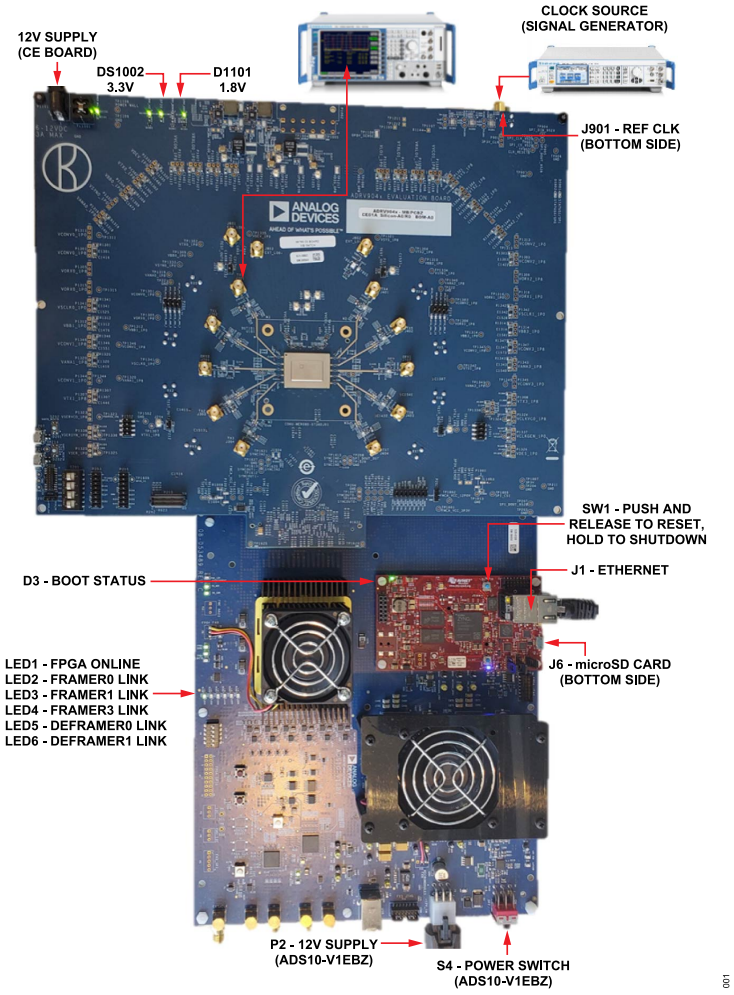

Figure 1. ADRV904x CE Board and ADS10-V1EBZ Motherboard with Instruments Required for Transmitter Testing

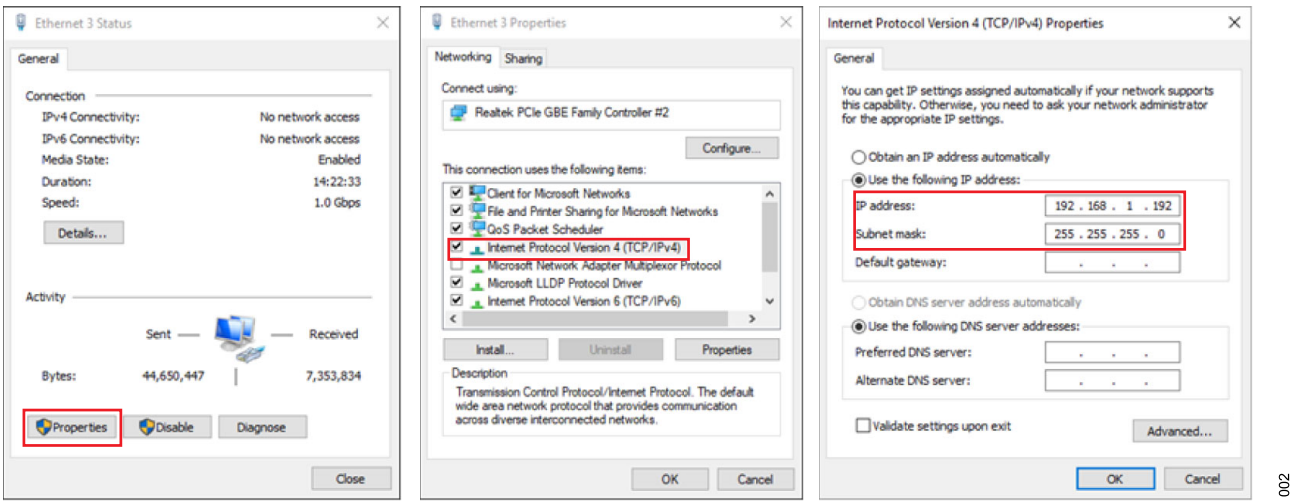

Figure 2. IP Settings for Ethernet Port Dedicated to ADS10-V1EBZ Motherboard. The Last Number in the IP Address Is Chosen by the User.

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SOFTWARE SETUP

The ADRV904x configurator uses the ACE software, which is a desktop application that allows the evaluation and control of various products from across the Analog Devices portfolio. ACE consists of a common framework (core) that can be extended by plugins for evaluating products such as the ADRV904x. ACE is designed to educate the user in the functional operation of a product and to enable access to the product evaluation system at a higher level of abstraction.

The ADRV904x evaluation software can be set up and updated to use the latest customer software package provided by Analog Devices. This update process requires the user to perform the following steps:

1. Install (or update) ACE on the host Windows PC.
2. Install (or update) the ADRV904x board plugin.
3. Update the ADS10-V1EBZ platform files. This step requires setting up a hardware connection.

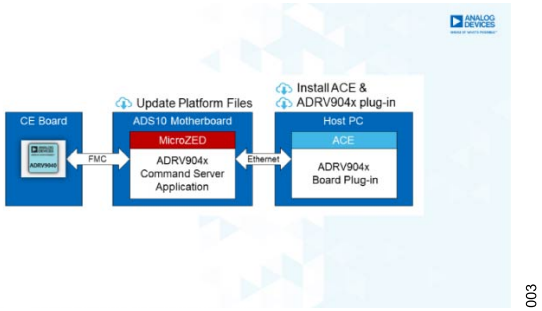

Figure 3. ADRV904x Evaluation Software Components

ACE CORE INSTALLATION

The ADRV904x evaluation software consists of an ACE core (shared framework) and an ACE plugin unique to the ADRV904x. The ACE core can be installed by running the ACE installer included in the customer software package provided by Analog Devices.

The installer consists of a single executable file with the ACE core version number included in the file name. The user can start ACE installation by double clicking on the installer and going through the recommended settings to install ACE. Administrator privileges are required for this installation.

If an older version of ACE was previously installed on the host PC, installing the included ACE version is strongly recommended to get the latest features and bug fixes. In case installation errors are seen, see the Uninstalling Older ACE section to start from a fresh install. Additional ACE documentation is available on wiki.analog.com/resources/tools-software/ace/user guide.

ADRV904X PLUGIN INSTALLATION

The ADRV904x ACE plugin is also included with the customer software package as a **Board.ADRV9040.acezip** file.

Once ACE is installed, the ADRV904x plugin can be installed by double clicking on the included **.acezip** file. This launches ACE with the ADRV904x plugin listed in the **Explore Without Hardware** section as **ADRV9040 Board** (see Figure 4). The plugin may take a moment to load on ACE first launch. Alternatively, ACE plugin manager can be used for installing the plugin as described in the Installing the ADRV904x Plugin Using the Plugin Manager section. The uninstallation process for plugins is also described in the Appendix section.

With the ADRV904x plugin installed, the search bar on ACE **Start** page can be used to navigate to the plugin with the ID **ADRV9040 Board**. The user can then verify that the installed plugin version number matches the version in the **.acezip** file name. Once the desired ADRV904x plugin version is installed in ACE, it can be run either:

- Without hardware. Double click on the ADRV904x plugin row under **Explore Without Hardware** or select the plugin row and click on **Add Selected Subsystem(s)** to start as shown in Figure 4.
- With hardware. Configure a hardware connection between ACE and the ADRV904x command server running on the ADS10-V1EBZ motherboard and update platform files, then double click the **ADRV9040 Board** icon.

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Important: if the host PC already has an ADRV903x board plugin installed, the user may need to uninstall this ARDV903x plugin before the ADRV904x plugin can be run (see the Appendix section). This issue will be resolved in upcoming releases such that ADRV903x and ADRV904x plugins can coexist within ACE as needed.

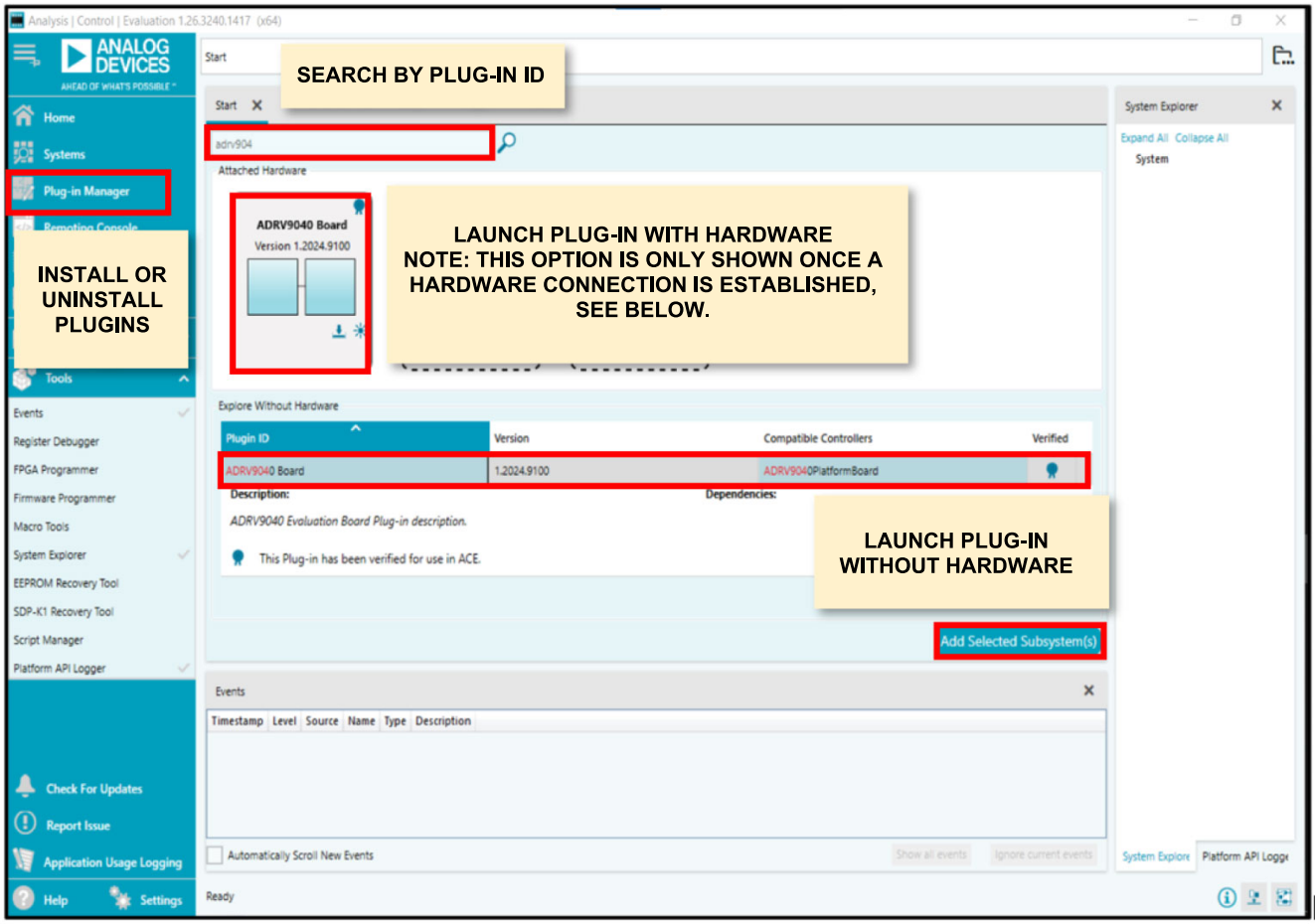

Figure 4. ACE Startup Screen Showing the Installed ADRV904x Plugin Which can be Double Clicked to Start the Configurator Without Hardware

HARDWARE CONNECTION

The ADRV904x plugin can be used standalone (without hardware) as a use case configurator for the ADRV904x family. See the ADRV904x Configurator section to explore the plugin without connecting to ADS10-V1EBZ/CE board evaluation hardware.

If the user is evaluating with hardware, ACE must first be configured to connect to the ADRV904x command server application running on the ADS10-V1EBZ motherboard. By default, the ADRV904x command server listens for incoming connections from the host PC on the IP address 192.168.1.10 and port 5000. The same IP address and port information can be provided to ACE by taking the following steps:

1. Open ACE **Settings** and navigate to the **Ethernet Boards** tab.
2. Click on **+** to make a new server connection.
3. Enter server settings as shown in Figure 5. **ADRV904x Platform** must be selected for platform.
4. Click **OK** to connect ACE to the ADRV904x server running on ADS10-V1EBZ.

Setting up this connection allows ACE to update the ADRV904x command server running on ADS10-V1EBZ. This process can take a moment, and the user must monitor events associated with updating and starting the ADRV904x command server by displaying the **Events** panel from **Tools** then **Events** on the left panel of ACE.

Once the command server has been started successfully, the **Start** page updates to list the **ADRV9040 Board** under **Attached Hardware** (Figure 6). In case the **ADRV9040 Board** does not show under **Attached Hardware**, refer to the Hardware Setup section to ensure that the

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hardware is powered properly. Verify the command server IP address configured under **ACE Settings** > **Ethernet Boards** and ensure that no other software application (or ACE instance) is accessing the IP address 192.168.1.10:5000.

The Appendix section additionally covers disconnecting from and reconnecting ACE back to the command server application running on ADS10-V1EBZ.

ADS10-V1EBZ PLATFORM FILES UPDATE

The ADS10-V1EBZ platform files must be updated to use the platform files included with the ADRV904x plugin The user may then click the **Update Platform Files** button on the **ADRV9040 Board** icon to update the ADS10-V1EBZ to use the platform files included with the plugin. A loading screen is shown while the update is in progress. This process takes about a minute.

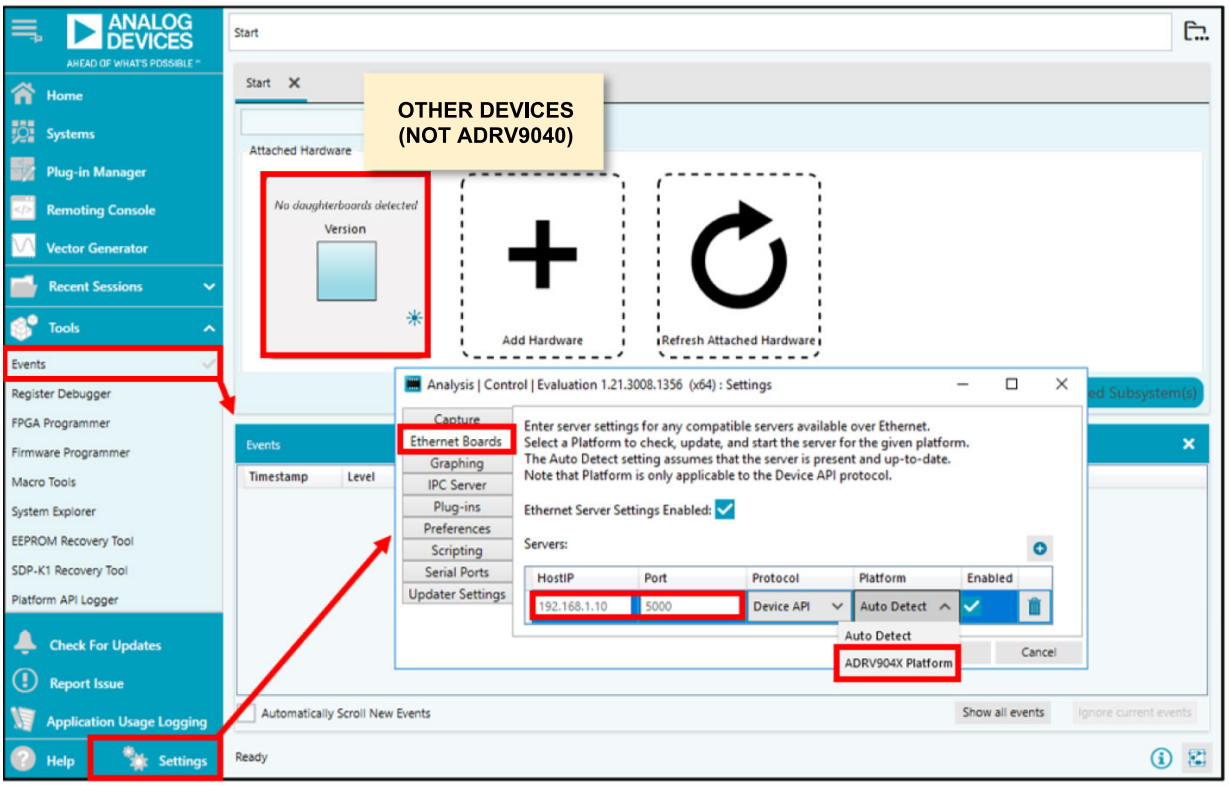

Figure 5. Providing ADRV904x Command Server Application IP Address, Port, and Platform Type to ACE

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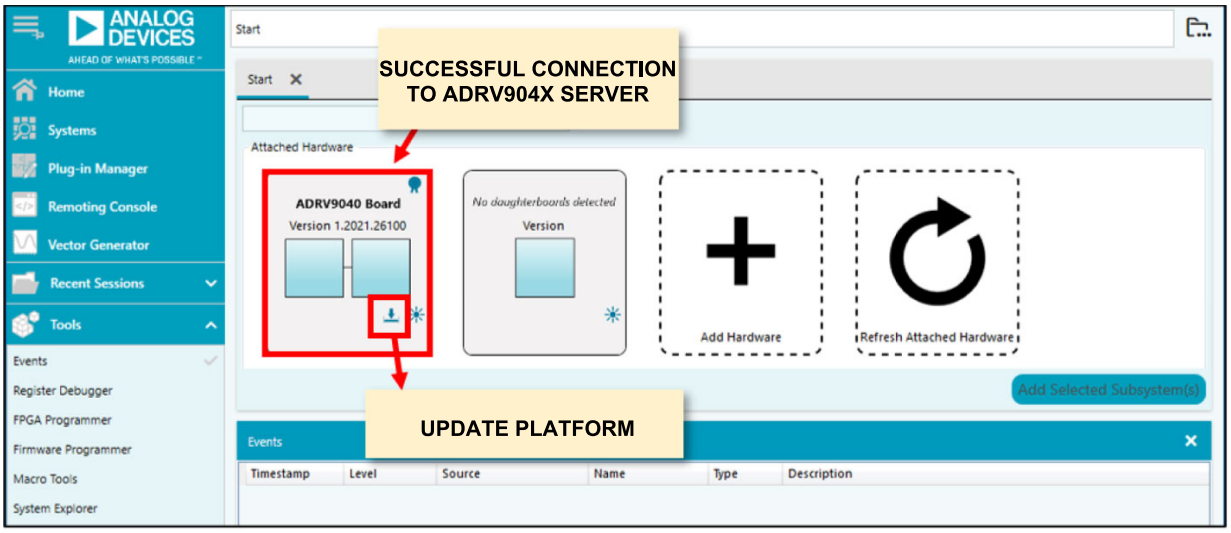

Figure 6. ADRV9040 Board Gets Populated Under Attached Hardware When ACE Successfully Interfaces to ADS10-V1EBZ

If the loading screen is not seen, the user can attempt to update the platform files again. In case issues persist, the user may navigate to **Tools** > **System Explorer** > **Debug**, and read back FPGA Address 0x43000000 to compare against a good setup.

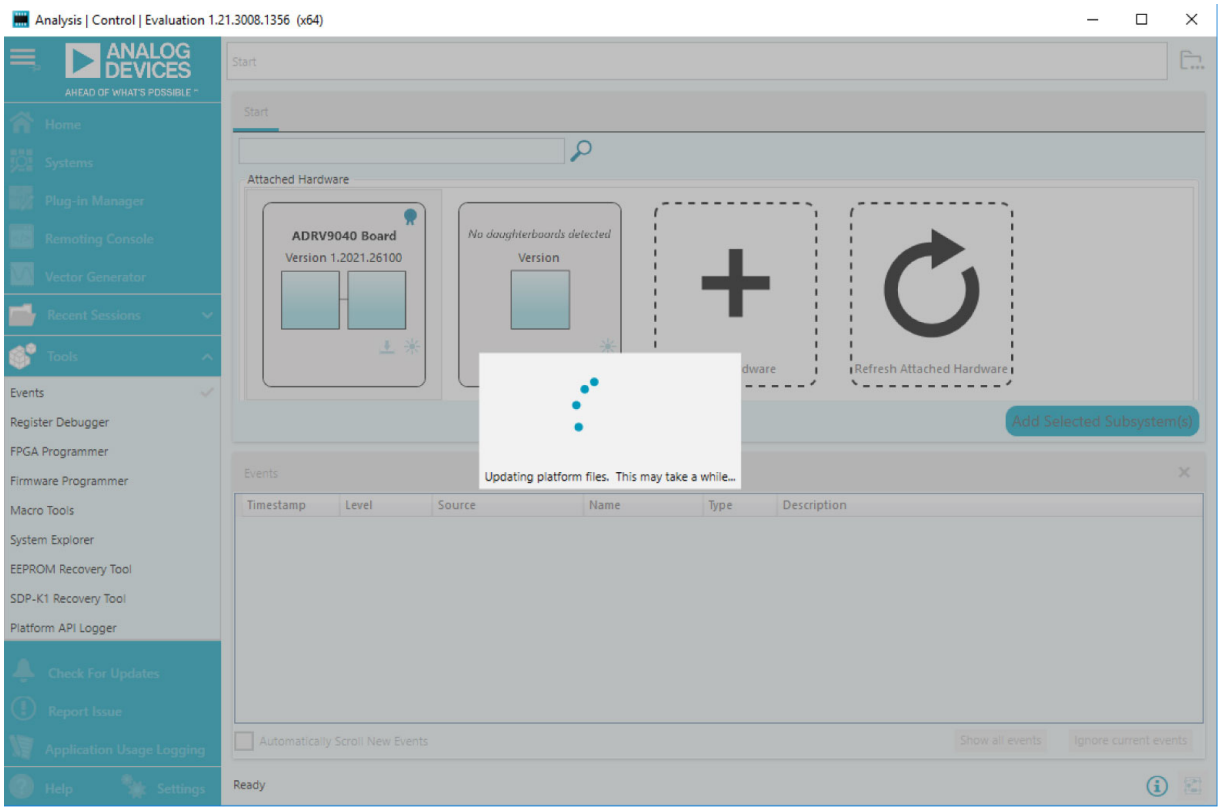

Figure 7. Loading Screen While Updating Platform Files

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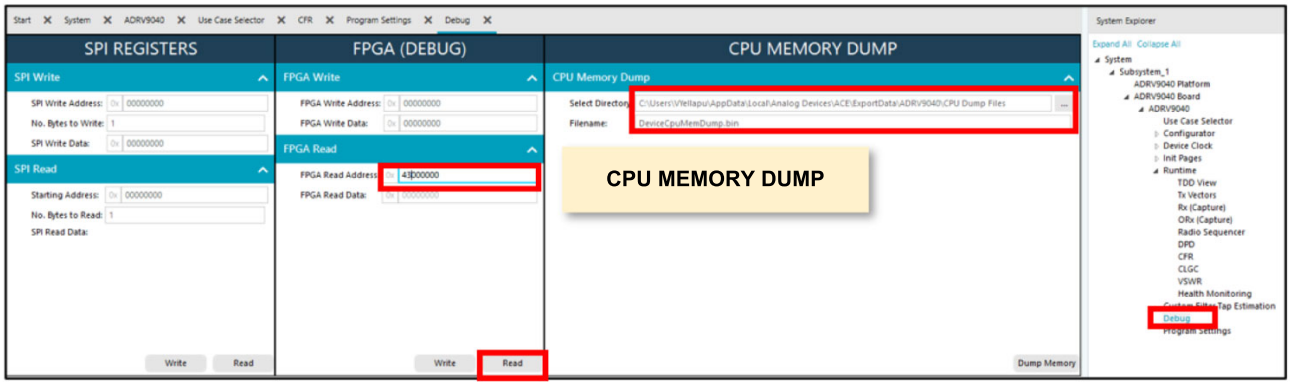


Figure 8. Platform Files Version Can Be Verified by Reading Back FPGA Address 0x43000000 from the Debug Page

CPU memory dump can be taken for analysis as shown in Figure 8. Browse to the directory. Once the directory is selected, the memory dump automatically gets saved.

ADRV904X PLUGIN OVERVIEW

The ADRV904x plugin can be launched with a hardware connection from the **Start** page by double clicking the **ADRV9040 Board** icon under **Attached Hardware**. It can also be run in configurator only mode, without hardware, to explore various ADRV904x configurations. The plugin looks and feels the same when launched with or without hardware, but a hardware connection is essential for programming the ADRV904x device and evaluating performance through runtime pages.

The **Tools** menu on the ACE panel can be used to display **System Explorer** for navigating the different pages included with the ADRV904x plugin. These pages are briefly described, and can be navigated as follows:

- **Configurator** pages: create, modify, program, and export ADRV904x use cases by setting up the following:
  - **Top Level Config** (see Figure 10): maps various **Tx/Rx Profile Assignment** and **ORx Profile Assignment** channels to profiles, export the current state of the configurator as a JSON use case, view the device **Open Help File**, and access the **Configurator** pages.
  - Subsequent **Configurator** pages can be used to configure the local oscillator (LO), carrier digital up conversion (DUC), transmitter, carrier digital down conversion (DDC), receiver, observation receiver, and JESD settings to arrive at and validate a desired ADRV904x use case.
  - **Power Analysis**: estimate power consumption in time division duplex (TDD) and frequency division duplex (FDD) modes for a configured use case.
- **Use Case Selector**: load and program a previously generated ADRV904x use case. This page allows the following:
  - Loading the **Configurator** pages above with an existing use case as a starting point, and then the user modifies settings as needed to derive a new use case.
  - Bypassing the **Configurator** pages and programming an existing use case as is.
- **AD9528 Clock Settings**: generate the desired ADRV904x device clock using the AD9528 clock chip on the CE board.
- **Init Pages**: set ADRV904x initialization parameters including the following:
  - **Tx Init** and **Rx Init** settings, calibrations, post multichip synchronization (MCS) init TRX_CTRL pin assignments, and transmitter to observation receiver mappings.
- Program the ADRV904x (if connected with hardware) from the following:
  - **Use Case Selector**: if running the selected use case default settings, refer to Figure 11. If running a modified use case, use a ADRV904x configurator at the top level as shown in Figure 11.
  - Track the ADRV904x device programming phases though the ACE **Events** window, as shown in Figure 11.
- **Program Settings**: enable exporting software resource files for the chosen configuration and init parameters. These files can then be integrated into the user application code.
- **Runtime**: evaluate the ADRV904x device performance through the following:
  - Transmitting JESD data or NCO tones using the **Tx Vectors** page.
  - Capturing receiver data using either on-chip random access memory (RAM) or JESD through the **Rx (Capture)** page.
  - Capturing observation receiver data using on-chip RAMs or JESD through the **ORx (Capture)** page.

ADRV904X PLUGIN OVERVIEW

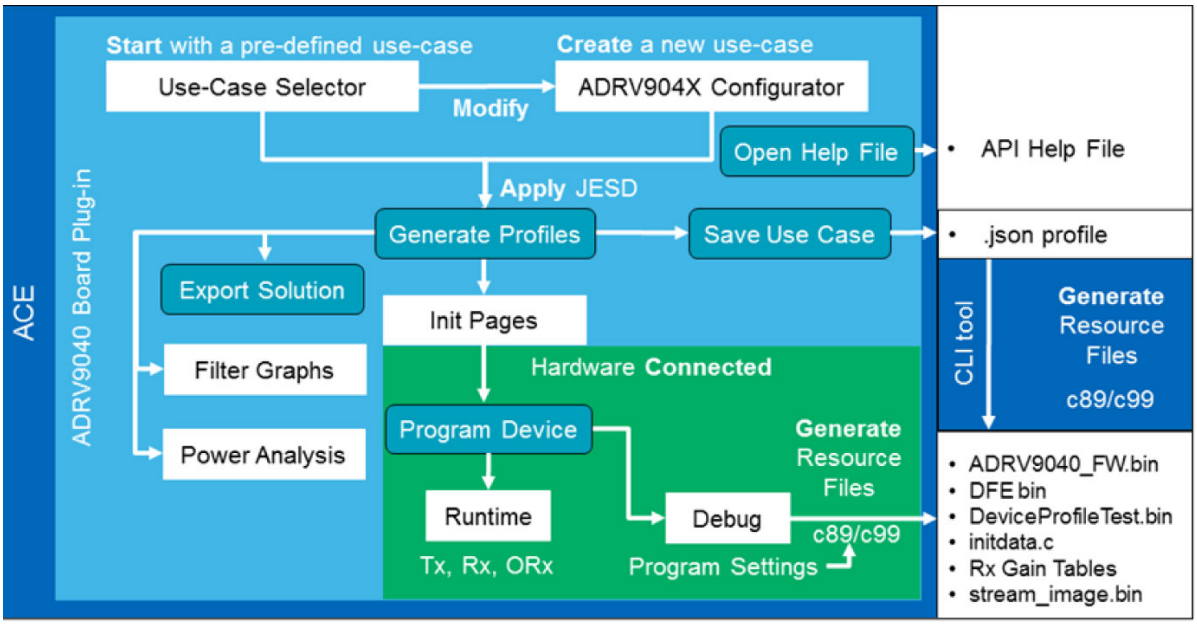


Figure 9. A Typical ADRV904x Programming Flow Where the User Programs a Use Case and Generates Software Resource Files

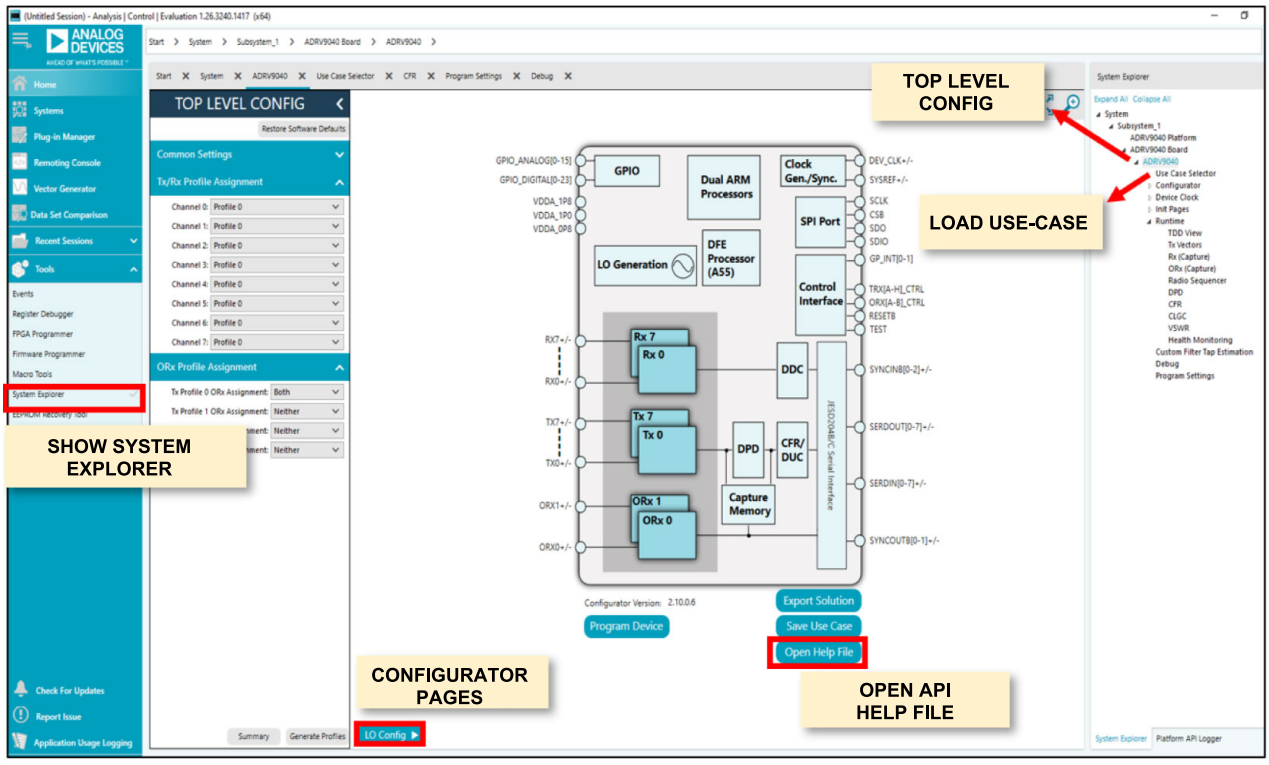


Figure 10. Launching the ADRV904x Plugin Opens the ADRV904x Configurator Top Level Config Page

USE CASE SELECTOR

This page allows the user to load the ADRV904x configurator with a predefined use case by taking the following steps:

1. Select the desired use case from **Use Case Selector** as shown in Figure 11.
2. Click **Generate Profiles** to load the selected use case settings into the ADRV904x configurator pages, or

ADRV904X PLUGIN OVERVIEW

3. Click **Program** to program the ADRV904x device using the default settings from the selected use case. Clicking **Program** automatically runs **Generate Profiles**, overriding any previous user inputs to the **Configurator** pages.

New use cases can also be added to the **Use Case Selector** page by either providing a directory to load multiple JSON files from or by providing direct paths to each JSON file to be added. To add new use cases, take the following steps:

1. Navigate to **System Explorer** > **Use Case Selector**.
2. Click **Add Use Case Source** to add a new directory to the use case list. This directory is then displayed as a new tab.
3. Alternatively, the user can add one JSON file at a time by selecting **Load Use Case**. This creates a new **Misc. Files** tab and multiple use cases can be added to this tab as well.

Once the **Configurator** pages are loaded by generating profiles, the user must then modify the selected use case default settings as shown in Figure 11. Such a modified use case must be programmed from the ADRV9040 **Top Level Config** page as previously shown in the ADRV904x Plugin Overview section. The modified use case can also be exported as a .json file from the ADRV9040 **Top Level Config** page.

Important: the ADRV904x device can be programmed from two different pages within the plugin. Programming behavior changes between these two buttons, and care must be taken to retain and program any configuration changes intended by the user. The two different pages are as follows:

- **Use Case Selector** page > **Program**
  - Click the **Program** button to program the ADRV904x with the default configuration for a selected use case.
  - Clicking this button reloads the **Configurator** pages, which overrides any changes made by the user.
- ADRV904x **Top Level Config** page > **Program** device
  - Click the **Program** button to program the current state of the **Configurator** pages (as modified by the user).

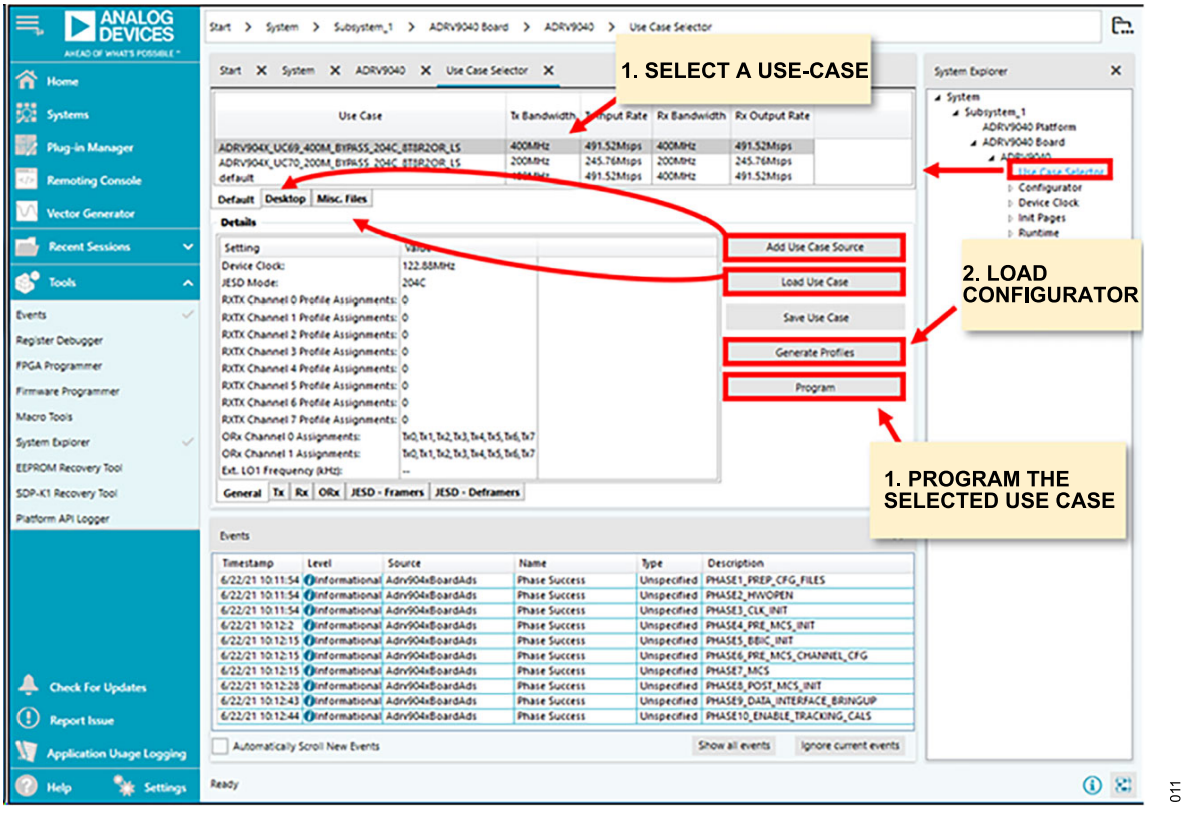


Figure 11. Loading a Predefined Use Case from Use Case Selector Page

ADRV904X PLUGIN OVERVIEW

DEVICE PROGRAMMING

Clicking either of the **Program** button from the **Top Level Config** page or the **Use Case Selector** page, which executes the 10 programming phases tabulated in Table 1.

Table 1. Description of ADRV904x Programming Phases and Order of Execution

Phase	Description
PHASE1_PREP_CFG_FILES	This phase generates stream, central processing unit (CPU), digital front end (DFE), and profile binaries. This phase also copies resource files to a location available to the application processor interface (API) for the remainder of the program sequence.
PHASE2_HWOPEN	This phase calls open on the available devices on the board.
PHASE3_CLK_INIT	This phase sets up and initializes the AD9528 clock chip on the board.
PHASE4_PRE_MCS_INIT	This phase calls the ADRVGen6 PreMcsInit broadcast API function. This includes loading the CPU, stream, and profile binaries, along with the Rx gain tables.
PHASE5_BBIC_INIT	This phase sets up and initializes the available baseband processor (ADS10-V1EBZ FPGA).
PHASE6_PRE_MCS_CHANNEL_CFG	This phase calls the ADRVGen6 PreMcsInit non broadcast API function.
PHASE7_MCS	This phase calls the ADRVGen6 Multi-Chip Sync (MCS) API sequence.
PHASE8_POST_MCS_INIT	This phase calls the ADRVGen6 PostMcsInit API function and initializes calibrations.
PHASE9_DATA_INTERFACE_BRINGUP	This phase initializes the data interface on the board (JESD204B/C).
PHASE10_ENABLE_TRACKING_CALS	This phase enables tracking calibrations after full initialization and post data interface bring up.

PROGRAMMING ERRORS

Setup issues with the evaluation system, such as the CE board missing a power or clock input can cause the ADRV904x device programming to error out. ACE **Tools** > **Events** window allows the user to monitor programming progress across multiple phases and identify a phase that may have triggered an error event as shown in Figure 12. Detailed error messages can be accessed from ACE **AppTrace.log** file: **C:\Users\%USERPROFILE%\AppData\Local\Analog Devices\ACE\AppTrace.log**.

Note that this log gets overwritten every time the user restarts ACE. Occasionally, multiple **AppTrace.log** files may be generated, and the most recently modified log file contains error information from the last programming attempt.

ACE **Report Issue** can be used for accessing **AppTrace.log** and reporting any unclear errors to Analog Devices for support.

Table 2. Common Programming Errors and Error Resolution

Programming Error	Resolution
There was a problem programming the device (Phase: PHASE3_CLK_INIT). See the trace log for more information.	Check the REFA clock input to AD9528. Also verify that the REFA input from the clock source matches the REFA clock frequency set on the AD9528 clock settings page.
There was a problem programming the device (Phase: PHASE5_BBIC_INIT). See the trace log for more information.	Verify that platform files are up to date, see the ADS10-V1EBZ Platform Files Update section.
There was a problem programming the device (Phase: PHASE6_PRE_MCS_CHANNEL_CFG). See the trace log for more information.	Ensure that the CE board is powered up.

ADRV904X PLUGIN OVERVIEW

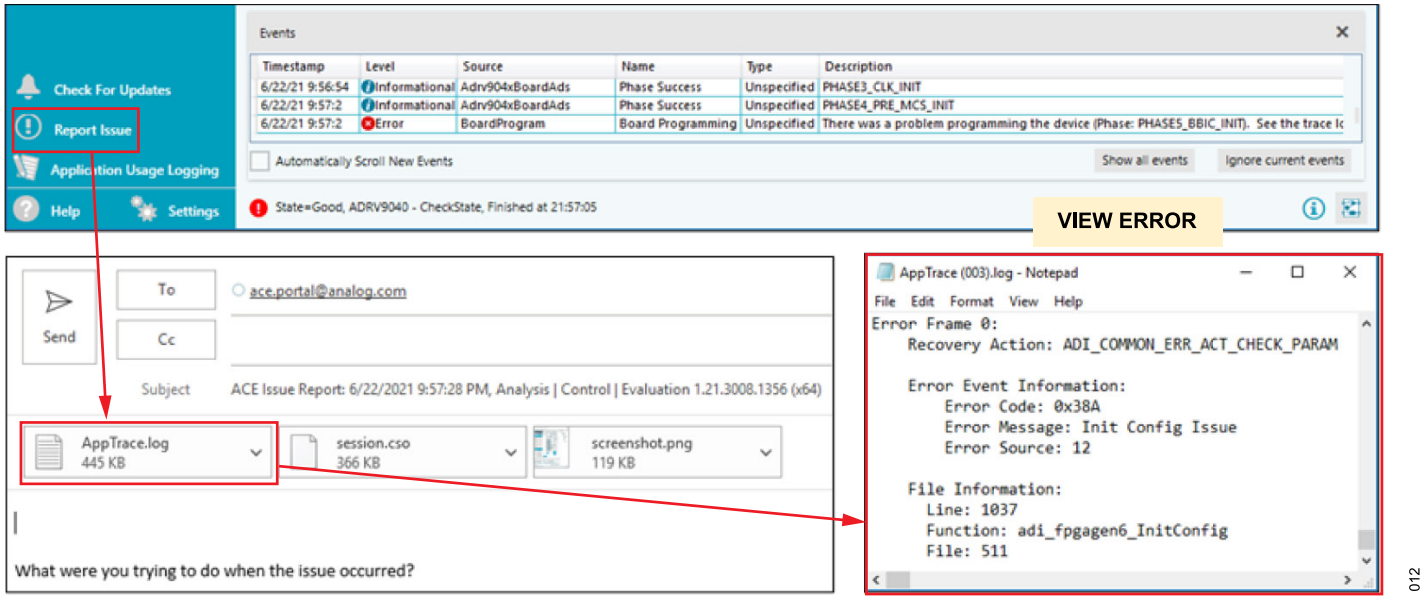


Figure 12. Procedure for Viewing Error Messages from ACE AppTrace.log File

ADRV904X CONFIGURATOR

The ADRV904x **Configurator** pages enable the user to arrive at a desired use case configuration by exploring different options available for configuring various subsystems of the ADRV904x, including the following:

- Setup of the CDUC, transmitter, CDDC, receiver, and observation receiver datapaths.
- Preview of the frequency graphs (analog, digital, and composite) for the receiver, transmitter, and observation receiver.
- JESD data interface parameters for the framers and deframers.
- LO settings.

The user must start from a known state by loading a use case from the **Use Case Selector** page and clicking on **Generate Profiles** to load the ADRV904x **Configurator** pages with a desired configuration. This function generates the transmitter, receiver, and observation receiver datapath configurations along with their corresponding filter responses for each enabled profile, as described in the following sections. Alternatively, the user can start from the default state of the **Configurator** pages (as preloaded when the ADRV904x plugin is launched) and then provide inputs to the various **Configurator** pages.

TOP LEVEL CONFIGURATION

On the **Top Level Config** page, the user can assign profiles for each of the transmitter, receiver, and observation receiver channels as shown in Figure 13. The configurator pairs receiver and transmitter channels together for profile assignment. For example, the user can assign Tx0/Rx0 to one profile and Tx1/Rx1 to a different profile. However, each ORx channel can be assigned separate profiles as needed. This grouping of channels for profile assignment is not a hardware constraint but it is a consequence of the current configurator format. Profile assignment flexibility allows an 8T8R ADRV904x device configuration to be split in various ways, such as two 4T4R configurations.

Note that the term profile is not the same as a use case. A use case refers to an ADRV904x device configuration, which consists of one or more profiles, where profiles are a set of configuration parameters applied to a group of transmitter/receiver/observation receiver datapaths. This grouping by profile minimizes the time needed to set up a use case as each datapath is not configured individually.

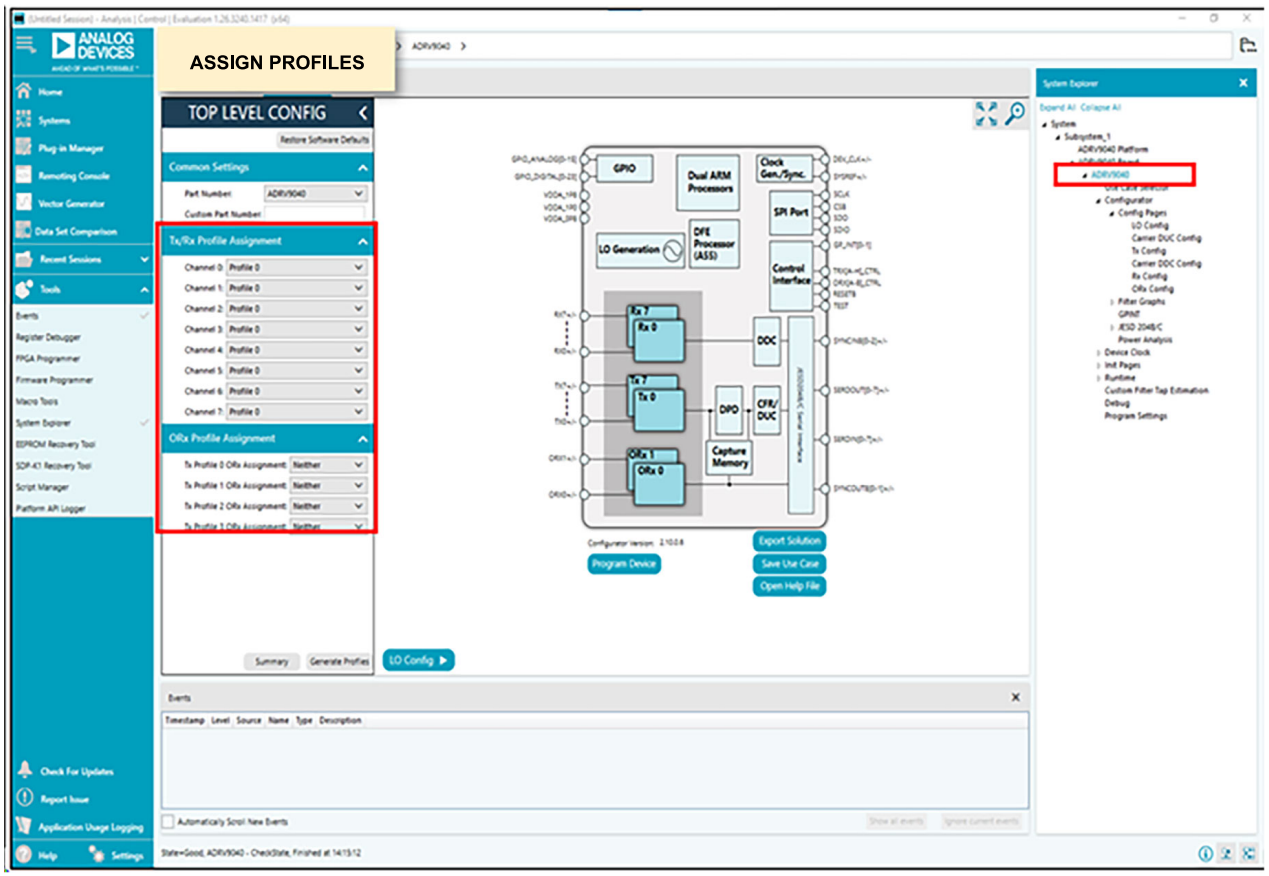


Figure 13. Top Level Config Page Showing All Tx/Rx/ORx Assigned to Profile 0

ADRV904X CONFIGURATOR

LO CONFIGURATION

After setting the desired profile mappings on the **Top Level Config** page, the user can navigate to the **LO Config** page. Click on the **LO Config** button at the bottom of the **Top Level Config** page as shown in Figure 14.

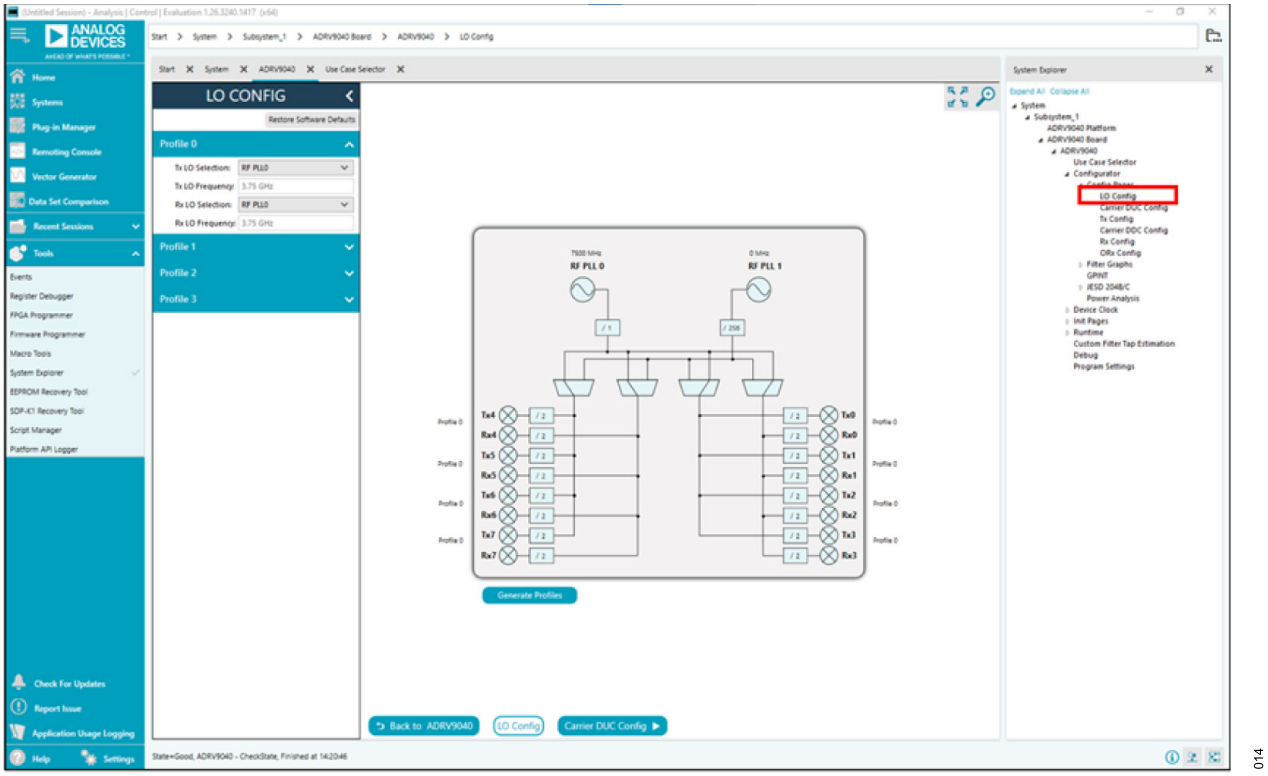


Figure 14. LO Config Page Showing ADRV904x LO Generation Setup for Given LO Frequency

On the **LO Config** page, the user can set the LO frequency for each of the receiver and transmitter channels per profile, as assigned on the **Top Level Config** page. The **LO Selection** dropdown box allows the user to select between **RF PLL0** and **RF PLL1** as the source of each LO. The accompanying block diagram is then updated when the user clicks on **Generate Profiles**.

Note that profile generation requires all the **Configurator** pages to be set up correctly, otherwise errors might occur. An error is also displayed if the user selects an out of range or invalid setting for any of the available parameters. These error messages can be accessed from the left panel of the ACE under **Tools** > **Events**. If at any point the configurator is put into a bad state, the user can click on **Restore Software Defaults** to return to a known good state as shown in Figure 14.

Once profiles are generated without error, the LO diagram updates to show a high level view of the LO generation setup inside the ADRV904x device for all assigned profiles, which includes the mux connections, radio frequency (RF) phase locked loop (PLL) voltage controlled oscillator (VCO) frequencies, and dividers used per receiver and transmitter channels. Figure 14 shows the **LO Config** page with the LO set to **3.75 GHz**.

LO Frequency Change Steps

The following steps describe the LO frequency change and other procedures associated with configuration changes:

1. Select the desired use case from **Use Case Selector** and **Generate Profiles** as shown in Figure 15.

ADRV904X CONFIGURATOR

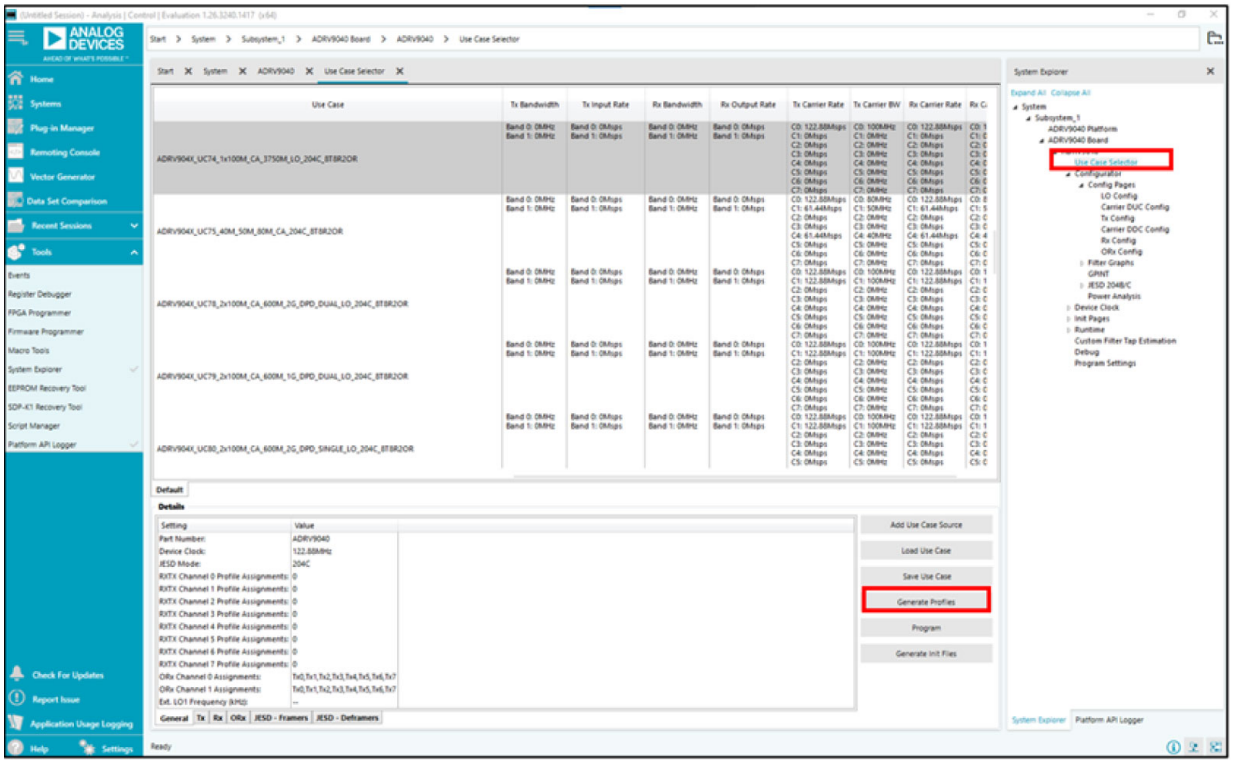


Figure 15. Generate Profiles

2. Update the RF PLL frequencies under **LO Config** as shown in Figure 16.

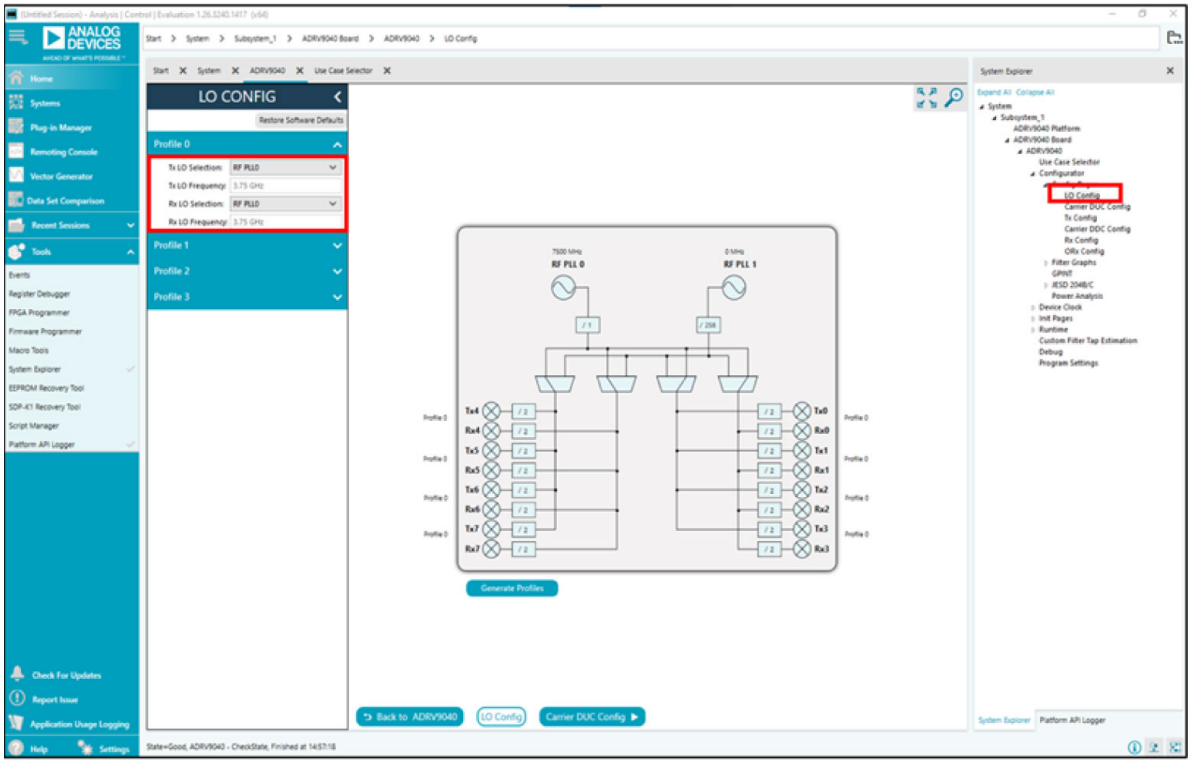
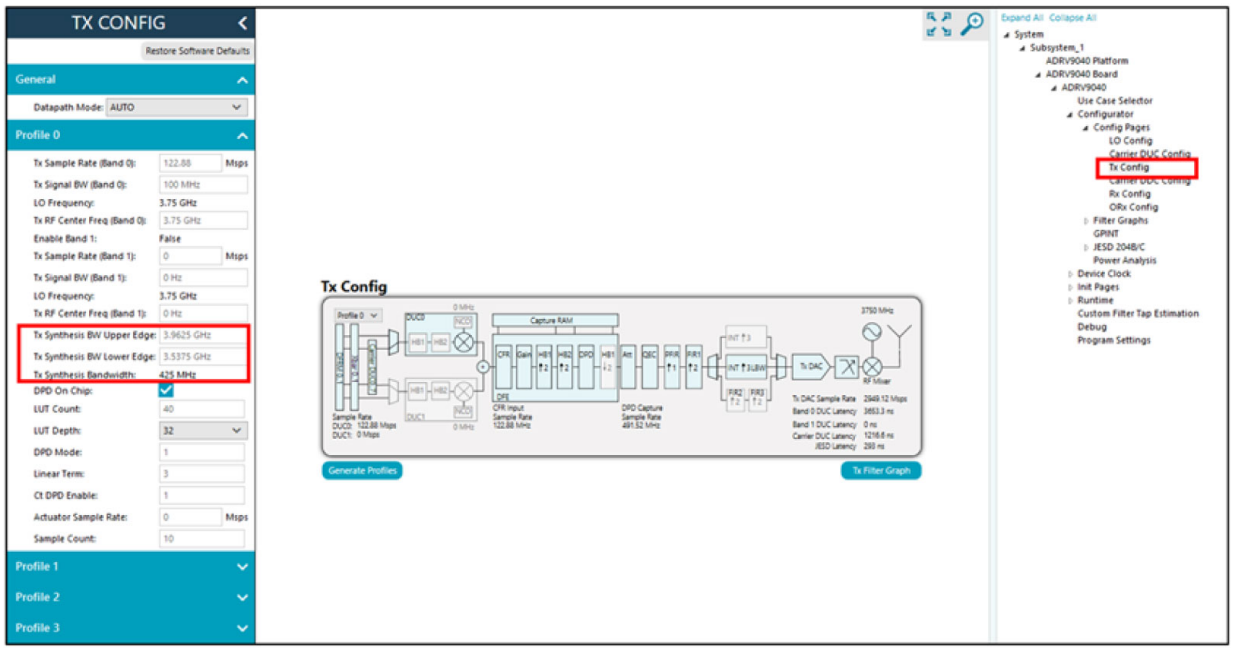


Figure 16. LO Config Page

3. Update **Tx Synthesis BW Upper Edge** and **Tx Synthesis BW Lower Edge** from the **Tx Config** as shown in Figure 17.

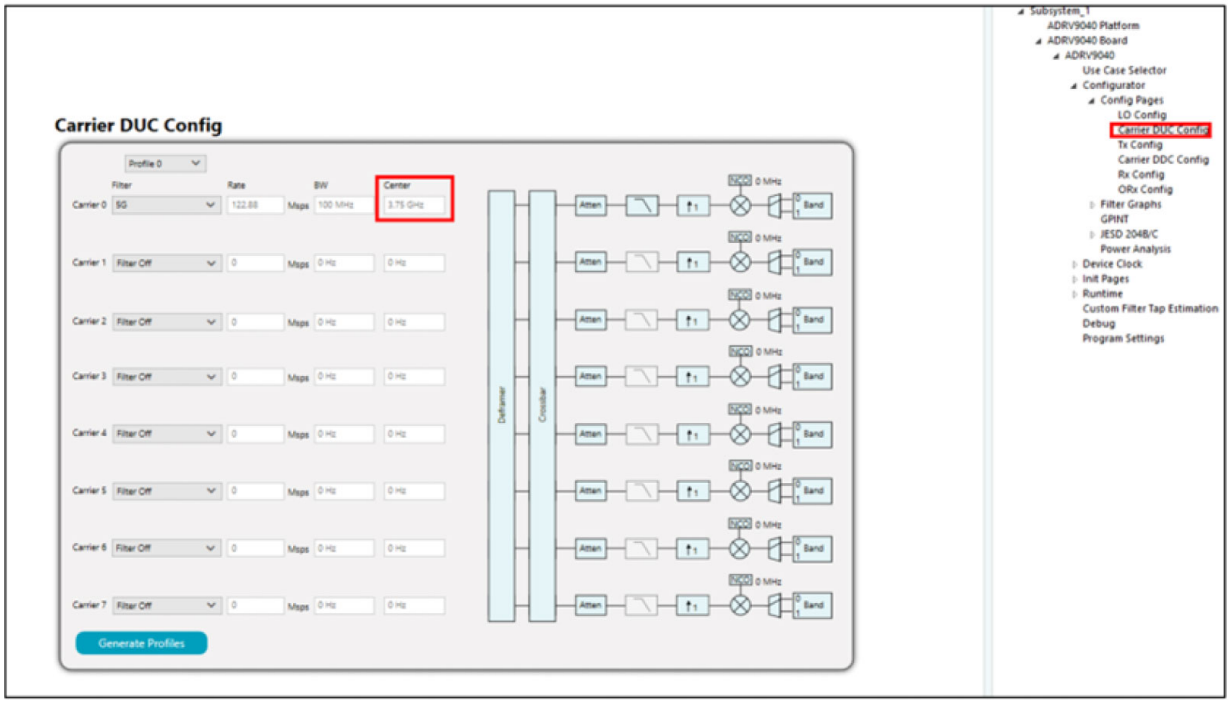
ADRV904X CONFIGURATOR



017

Figure 17. Tx Config Page

4. This step is optional for profiles with CDUC/CDDC enabled only. Go to **Carrier DUC Config** as shown in Figure 18 and **Carrier DDC Config** as shown in Figure 19, and update carrier NCO frequencies.



018

Figure 18. Carrier DUC Config Page

ADRV904X CONFIGURATOR

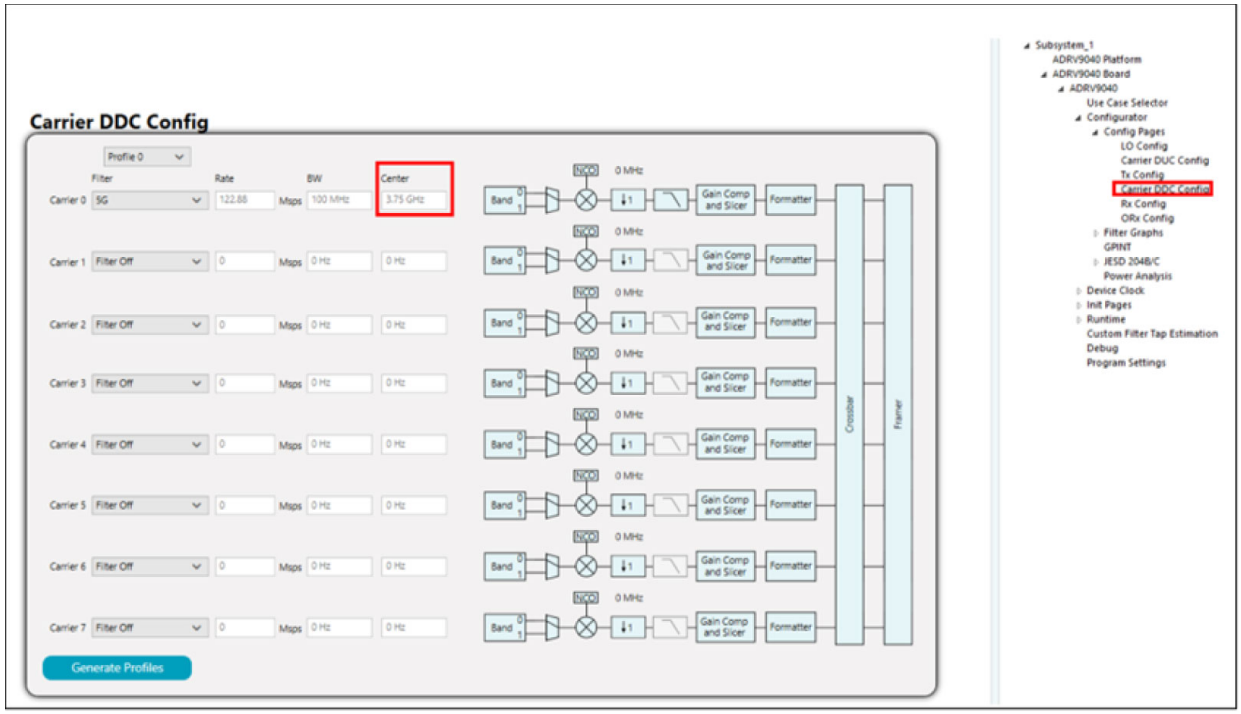


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Figure 19. Carrier DDC Config Page

5. Click on **Program Device** as shown in Figure 20. Once the part is programmed successfully, the updated LO frequency is ready to use.

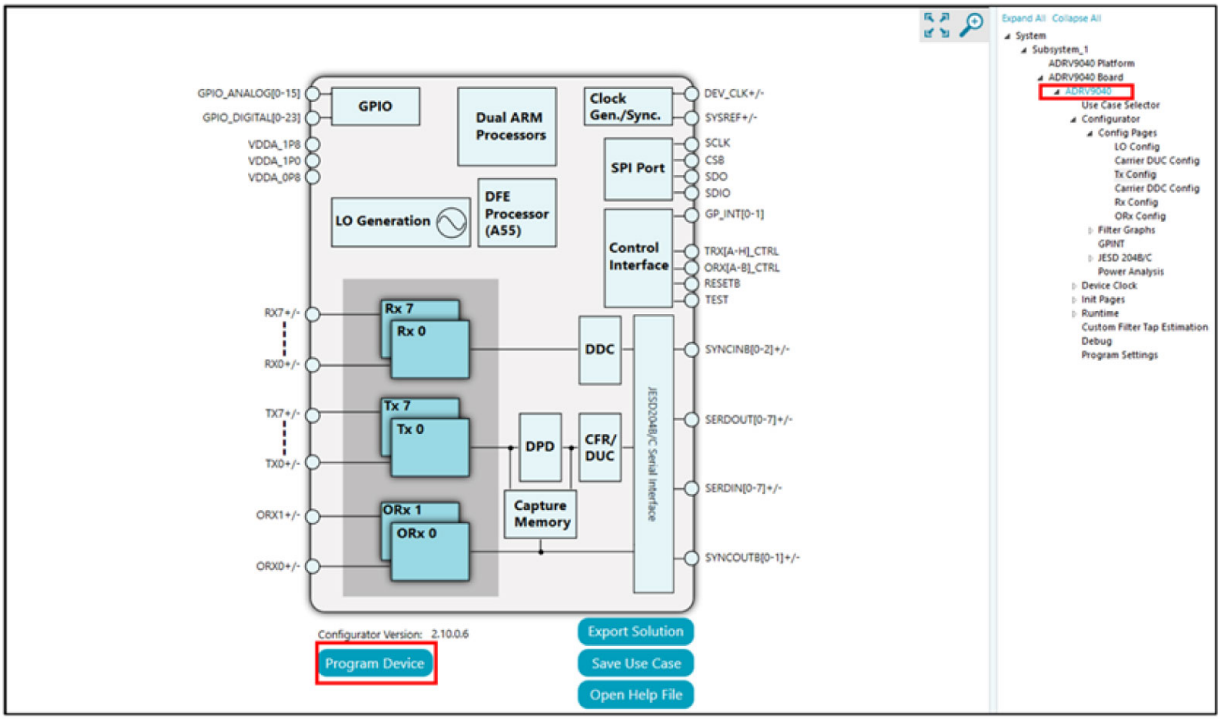

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Figure 20. Top Level Program Page

ADRV904X CONFIGURATOR

TRANSMITTER CONFIGURATION

CDUC Configuration

The CDUC is a part of the ADRV904x DFE on the transmit path and performs the function of filtering and up converting the baseband signal centered on DC to a higher sample rate. The CDUC has five half-band filters that support up to 32× interpolation. A maximum of eight carriers are supported by the CDUC. The output of the CDUC is passed to one of the two band digital upconverters (BDUC) to combine the composite carriers into a passband signal.

The CDUC configurator helps reduce the implementation time by compiling the most efficient CDUC configuration for a given set of carrier requirements. The ADRV904x CDUC supports the LTE and new radio (NR) air interface standards. To access the **Carrier DUC Config** page, navigate to ADRV9040 > **Configurator** > **Config Pages** > **Carrier DUC Config** in the system explorer window as shown in Figure 21.

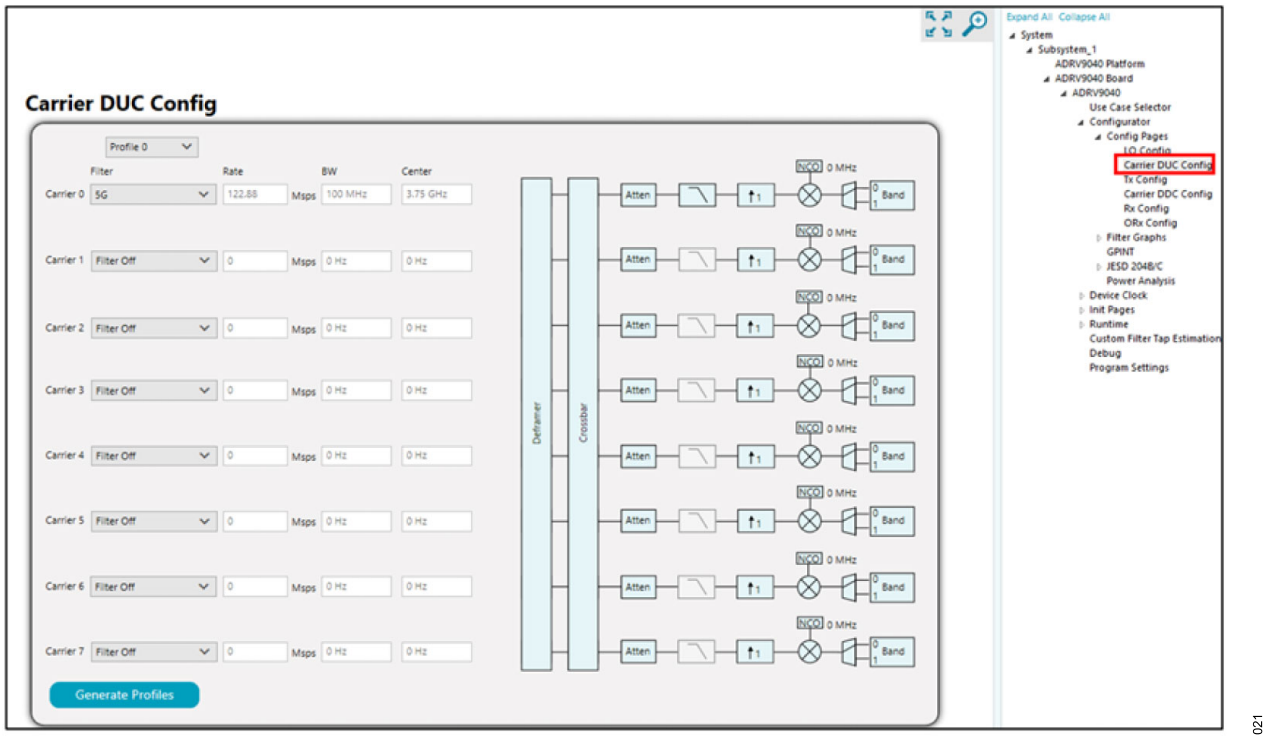

Figure 21. CDUC Configurator Page

Unless the user has loaded an existing use case with carriers enabled, the **Carrier DUC Config** page launches in carrier DUC bypassed mode. The user can configure the carriers by following the compilation flow below (refer to Figure 22):

1. Select one of the four profiles for which to apply the CDUC settings.
2. Select the channel filtering option appropriate for the carrier as described in Table 3.
3. Configure the carrier settings including the sample rate for the carrier as described in Table 3, which indicates the bandwidth of the carrier and the RF center frequency of the carrier. Note that the carriers must be arranged in descending order of sample rates with Carrier 0 assigned to the carrier with the highest sample rate, and Carrier 7 assigned to the carrier with the lowest sample rate.
4. Once the carrier settings are entered, click on **Generate Profiles** to ensure that the carrier settings for the use case entered are valid. The **Tx Config**, **ORx Config**, and JESD pages must also be updated before this step can be completed successfully, as described below:
   - The CDUC configurator automatically resolves the interpolation rate from the carrier configuration entered by the user in Step 3.
   - The CDUC configurator automatically resolves the carrier NCO shift and the band assignment (Band 0 or Band 1) based on the separation between the carriers and to minimize the net bandwidth per band.

Note that additional parameters must be updated while compiling and generating the profiles in the **Carrier DUC Config** page settings, including the following:

ADRV904X CONFIGURATOR

- The digital predistortion (DPD) analysis bandwidth (transmitter synthesis bandwidth) and internal DPD enable must be entered on the **Tx Config** page as shown in Figure 23.
- The ORx sample rate for the ORx, which is mapped to the transmitter that corresponds to the CDUC being configured (see the Observation Receiver Configuration section).
- The JESD settings and sample crossbar assignments (see the JESD Configuration section).

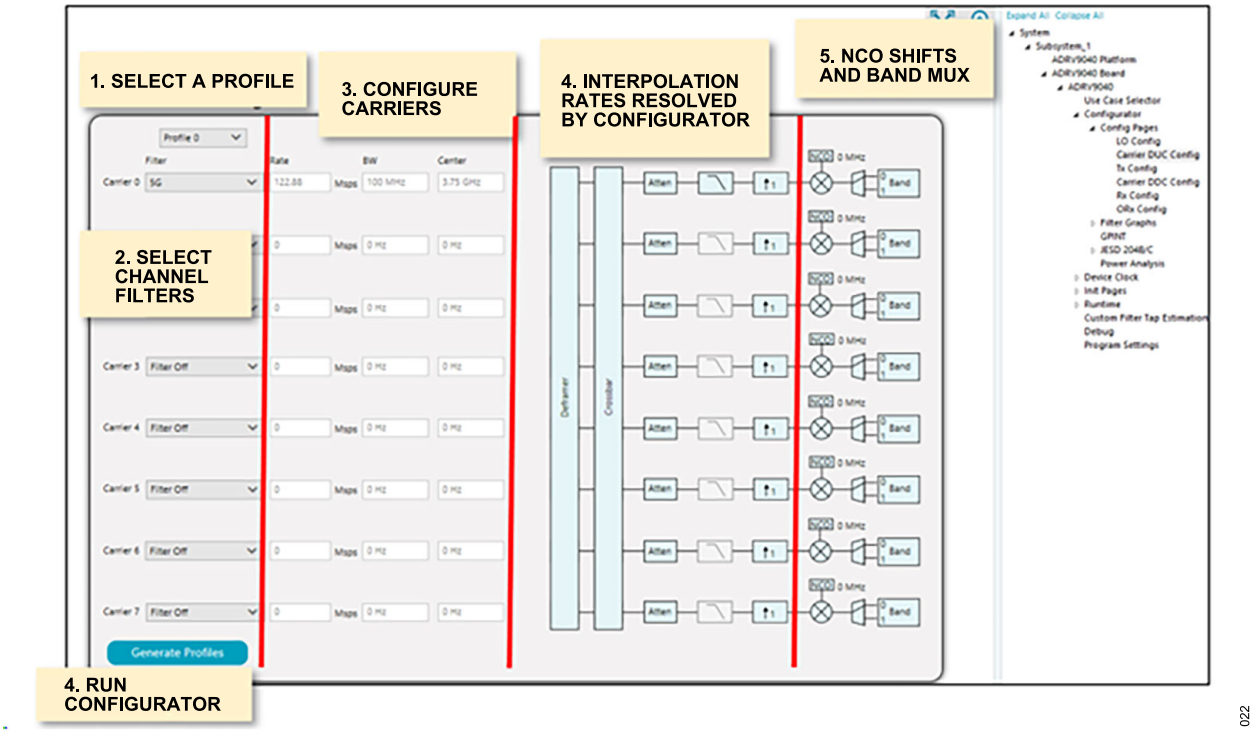

Figure 22. Compilation Flow of CDUC Settings

Table 3. Channel Filtering and Sample Rate Options Supported by ADRV904x CDUC Configurator

Filter Option	Carrier Bandwidth (MHz)	Recommended Carrier JESD Sample Rate (MSPS)	Comments
LTE	5	7.68	
	10	15.36	
	20	30.72	
5G NR	15, 20, 25	30.72	
	30, 40, 50	61.44	
	60, 70, 80, 90, 100	122.88	
High Bandwidth 5G NR	100	122.88	Recommended when there are more than two NR100 carriers
Filter Off (Carrier En)	N/A	N/A	Offers NCO shift only without any channel filtering
Filter Off	N/A	N/A	Disables CDUC (bypass mode)

The ADRV904x transceiver supports a maximum of 800 MHz synthesis bandwidth for DPD analysis. The transmitter synthesis upper and lower edges must be configured in the **Tx Config** page to generate profiles successfully in the **Carrier DUC Config** page.

Refer to the example shown in Figure 24 where the passband consists of 3× NR100 carriers centered at 3.4 GHz, 3.6 GHz, and 3.7 GHz, respectively. The gray shaded region shown in Figure 24 represents the 800 MHz synthesis bandwidth spanning from 3.1 GHz (transmitter synthesis BW lower edge) to 3.9 GHz (transmitter synthesis BW upper edge). For this example, configure the transmitter synthesis BW upper edge as 3.9 GHz and the transmitter synthesis BW lower edge as 3.1 GHz on the **Tx Config** page as shown in Figure 23.

ADRV904X CONFIGURATOR

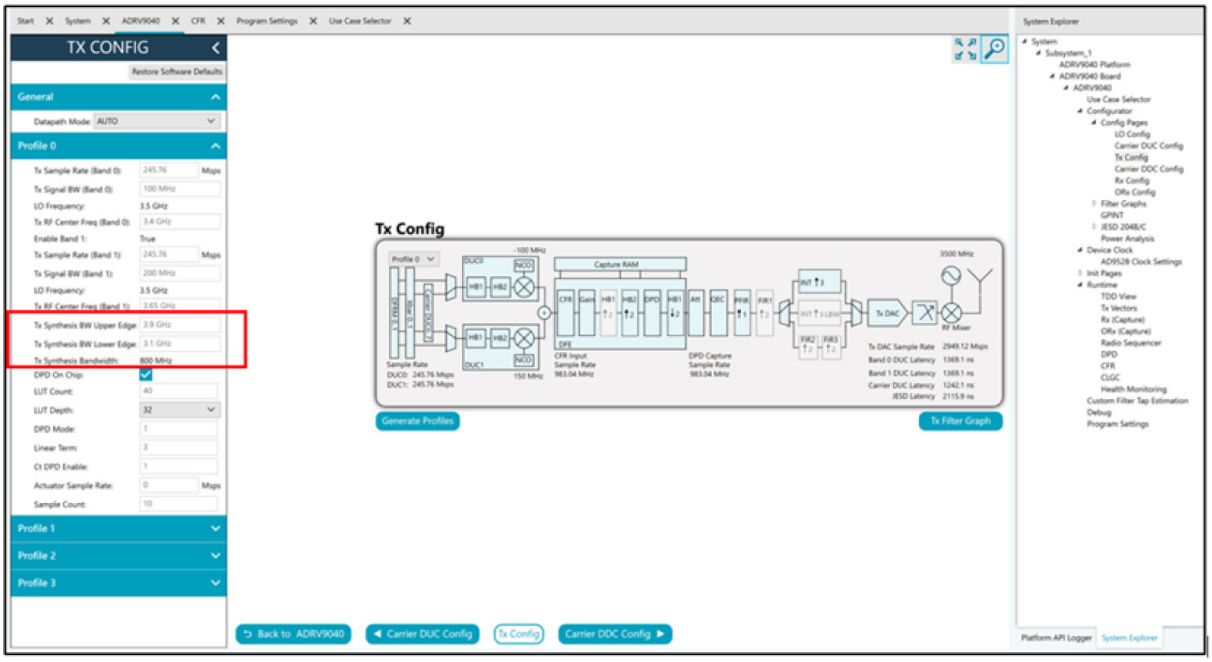

Figure 23. Tx Synthesis BW Configuration

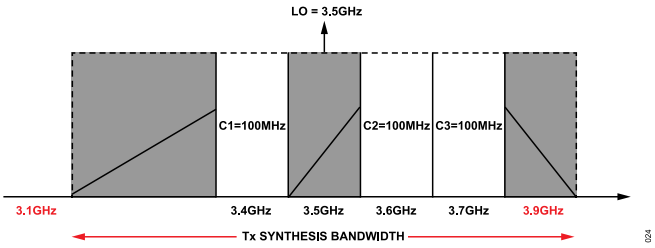

Figure 24. Tx Synthesis Bandwidth Configurator for CDUC Configurator

Transmitter Datapath Configuration

After configuring the **Carrier DUC Config** page as desired, click on the **Tx Config** to navigate to the **Tx Config** wizard as shown in Figure 25. **Tx Config** can also be accessed from under **Config Pages** in system explorer.

On the **Tx Config** page, the user can assign the following parameters for different profiles as mapped to transmitter channels on the top level configuration page as follows:

- Datapath mode to set the data path interpolation rate, effectively selecting the transmitter DAC rate.
- Transmitter synthesis bandwidth. DPD correction BW as specified by the upper and lower edge user inputs.
- Enable on-chip DPD.

The transmitter sample rates, RF center frequencies, signal bandwidths, and Band 1 enable are solved by the configurator based on the user inputs to the **Carrier DUC Config** page. The configurator solved outputs populate correctly only after all the configurator pages have been setup and the user clicks on **Generate Profiles**, which is accessible from various pages. Once generated, the **Tx Config** figure updates to show the transmitter data path configuration for the profile selected as shown in Figure 25. Blocks colored blue are enabled and blocks that remain opaque are bypassed. Calculated datapath latencies are also shown.

Note that the Tx sample rates displayed in the **Tx Config** wizard on the left panel are different from the DUC0/DUC1 sample rates displayed in the **Tx Config** figure. The wizard sample rates are the input rates to the carrier DUC, and the figure sample rates are calculated based on the interpolation ratios resolved on the **Carrier DUC Config** page as shown in Figure 22. This is visualized and summarized in Table 4.

ADRV904X CONFIGURATOR

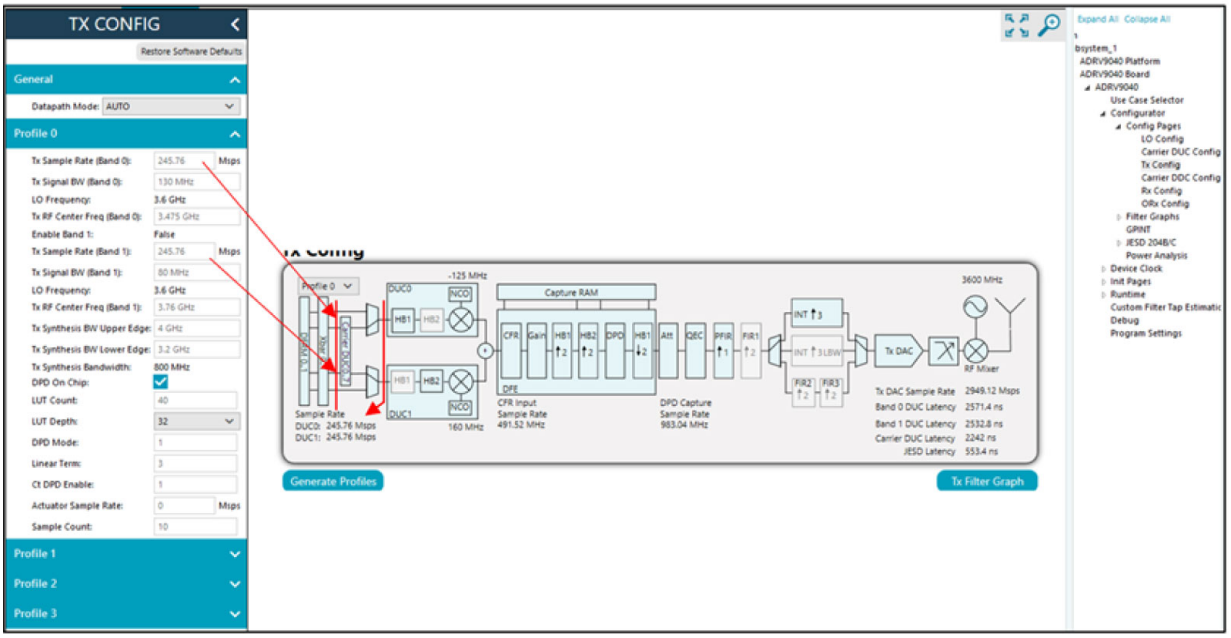

Figure 25. Transmitter Configuration Setup Diagram

Table 4. Comparison of Tx Sample Rates Displayed in the Tx Config Wizard and the Tx Datapath Figure

Location	Parameter	Description
Tx Config Panel	Tx sample rate (Band 0) and Tx sample rate (Band 1)	This is the carrier DUC input sample rate
Tx Config Figure	DUC0 sample rate and DUC1 sample rate	This is the carrier DUC output sample rate, and the band DUC input rate

Transmitter Filter Graph

Corresponding transmitter filter graphs for the profile selected on the **Tx Config** page can be viewed by clicking on the **Tx Filter Graph** button. This helps the user understand the frequency response of the selected transmitter profile. An example is shown in Figure 26.

The transmitter filter graph includes the band and carrier digital composite responses, the programmable finite impulse response (PFIR) to RF response, the analog composite response (including the transmitter DAC), and the full composite response. The user can change the profile selection on the **Tx Config** page to display the filter graphs corresponding to the selected profile.

ADRV904X CONFIGURATOR

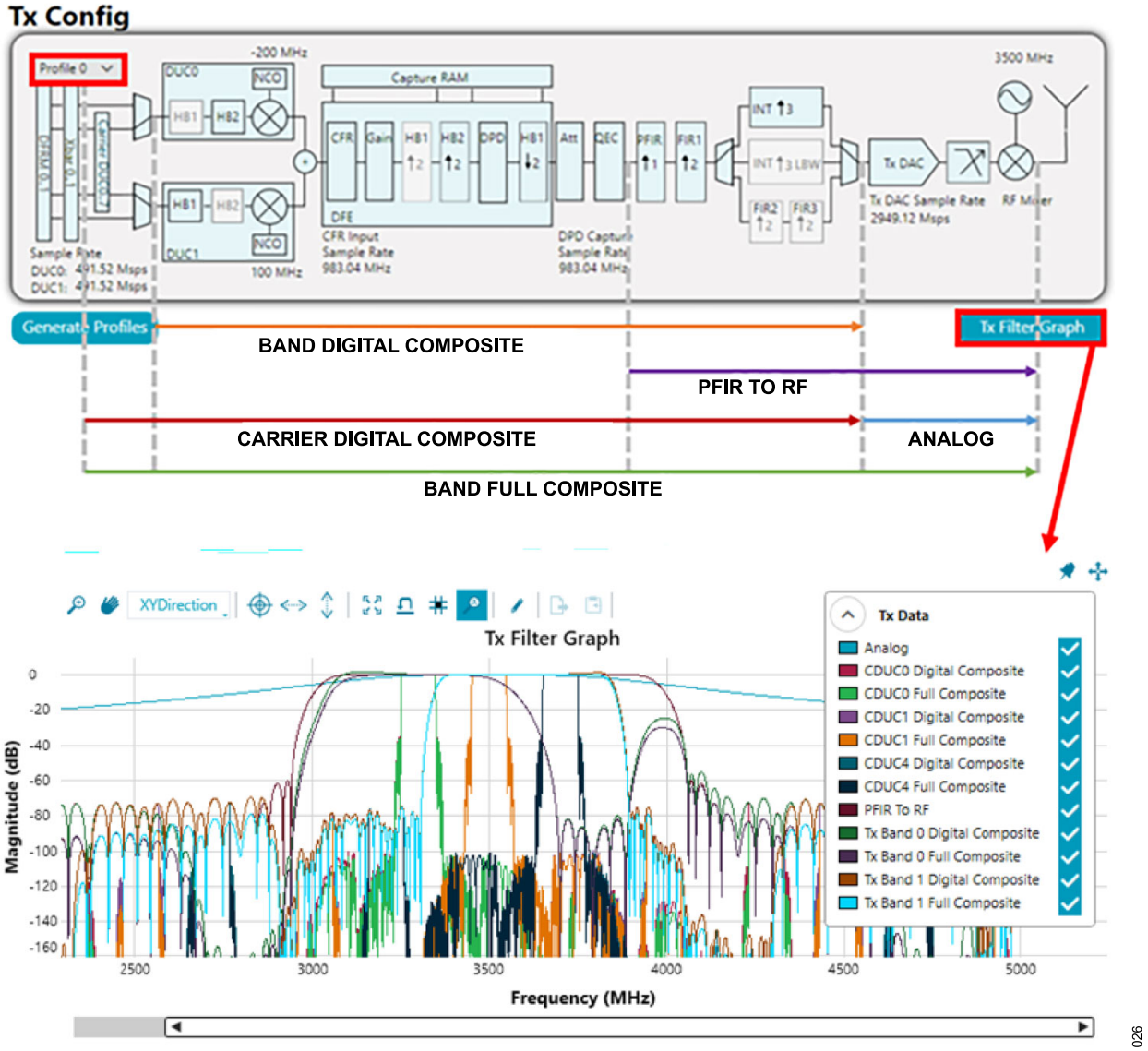

Figure 26. Transmitter Datapath Filter Graphs

RECEIVER CONFIGURATION

CDDC Configuration

The CDDC on the ADRV904x DFE offers the capability to convert a receiver passband signal into composite carriers centered at DC. The ADRV904x CDDC supports LTE and NR air interface standards, and a maximum of eight carriers. Similar to the CDUC, there are five half-band filters per carrier that support a maximum decimation rate of 32×.

To access the **Carrier DDC Config** page, navigate to ADRV9040 > **Configurator** > **Config Pages** > **Carrier DDC Config** in the system explorer window as shown in Figure 28.

ADRV904X CONFIGURATOR

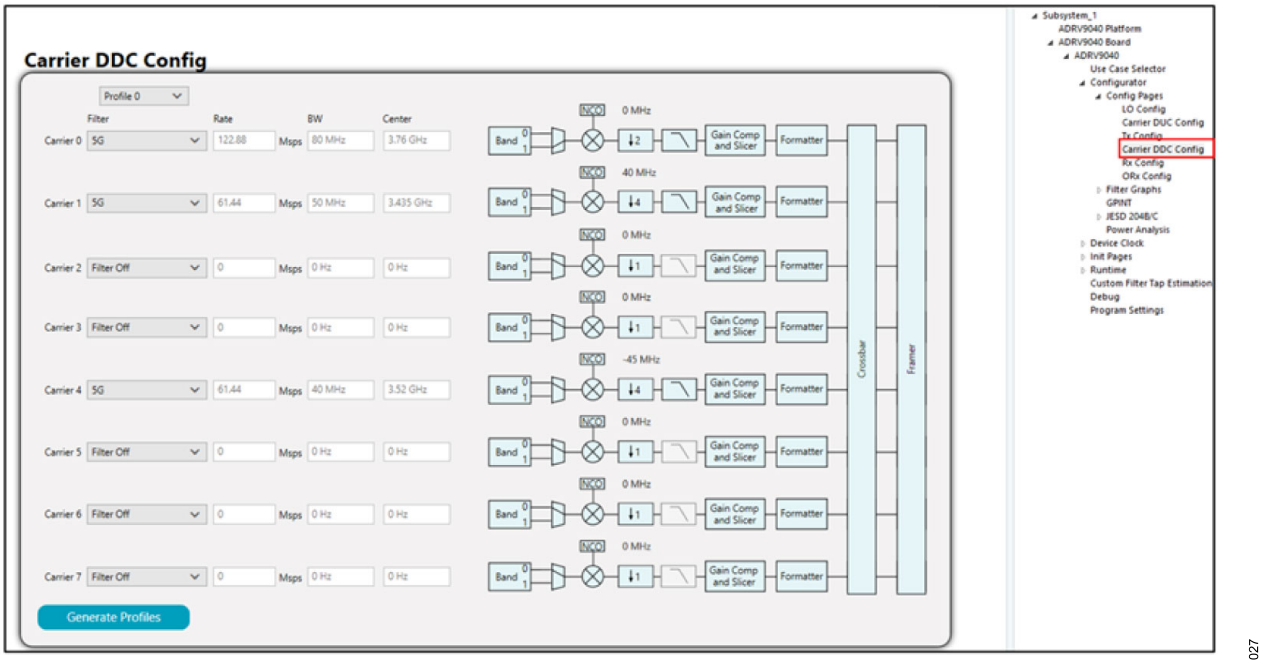

Figure 27. CDDC Configuration in the ADRV904x Configurator GUI

Unless the user loads an existing use case with carriers enabled, the **Carrier DDC Config** page launches in carrier DDC bypassed mode. The user can then configure the carriers by following the compilation flow as shown in Figure 29 or taking the following steps:

1. Select one of four profiles for which to apply the CDDC settings.
2. Select the channel filtering option appropriate for the carrier as described in Table 3.
3. Configure the carrier settings including the sample rate for the carrier as described in Table 3, the bandwidth of the carrier, and the RF center frequency of the carrier. Note that the carriers must be arranged in descending order of sample rates with Carrier 0 assigned to the carrier with the highest sample rate and Carrier 7 assigned to the carrier with the lowest sample rate.
4. Once the carrier settings are entered, click on **Generate Profiles** to ensure that the carrier settings for the use case entered are valid. Note that the JESD configuration must be updated, which include sample crossbar assignments, in parallel with updating the carrier settings to arrive at a valid configuration.
5. The CDDC configurator automatically resolves the decimation rates, carrier NCO shifts, and band assignments from the carrier configuration entered by the user in Step 3.

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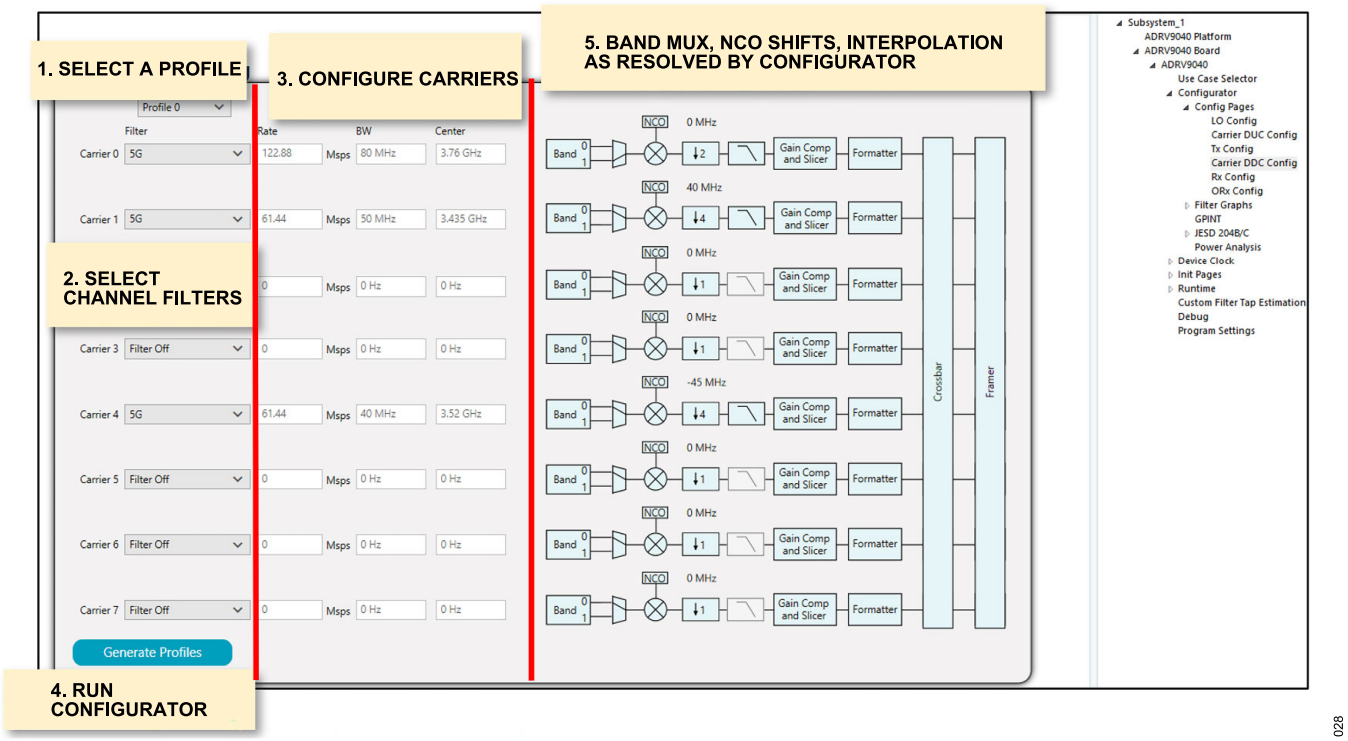

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Figure 28. CDDC Configuration Flow for the ADRV904x Transceiver

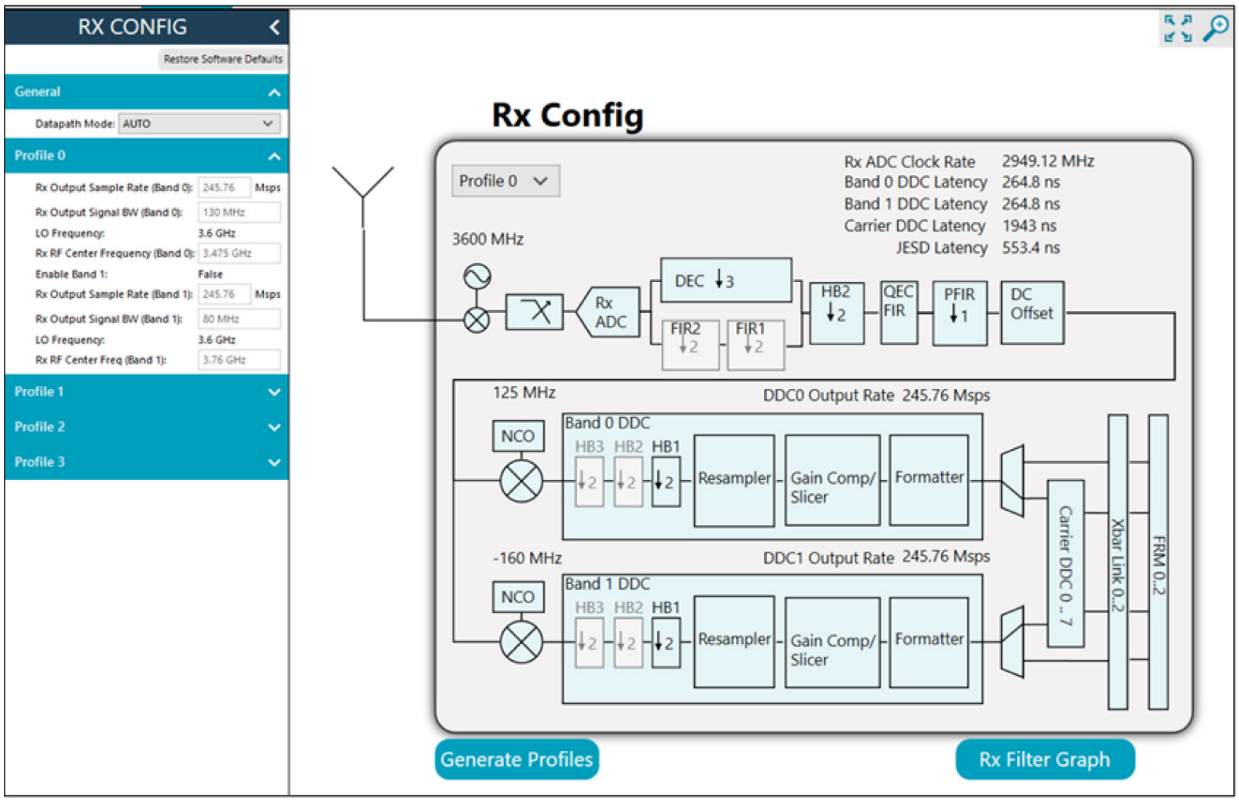

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Figure 29. Receiver Configuration Wizard and Datapath Diagram Updated After Generating Profiles

ADRV904X CONFIGURATOR

Receiver Datapath Configuration

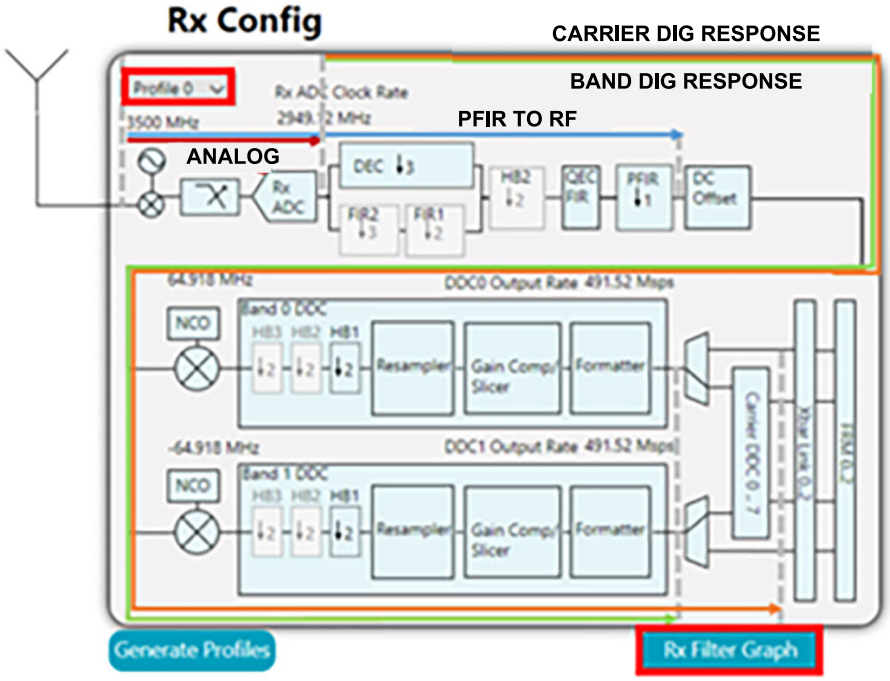
The user can navigate to the **Rx Config** page found under the **Carrier DDC Config** page or by using the ACE system explorer. The **Rx Config** page allows the user to change the Rx datapath decimation to select a different ADC rate through the datapath mode drop down menu.

Once the carrier DDC is resolved and profiles are generated, the **Rx Config** page updates to show the receiver datapath configuration and latencies as shown in Figure 29. Note that the profiles can only be generated successfully after all configurator pages have been setup. A dropdown box on the top left corner of the **Rx Config** page allows the user to view configurator solutions for different profiles as defined from the Top Level Configuration section. Blocks that are colored blue are enabled and blocks that remain opaque are bypassed.

Receiver Filter Graph

A corresponding receiver filter graph of the profile can be viewed via the **Rx Filter Graph** button. This helps the user understand the frequency response of the selected receiver profile. An example is shown in Figure 30. The Rx filter graph includes the digital composite response, Rx ADC response, and the analog composite response. The user can change the profile selection on the **Rx Config** page to see the corresponding filter response for the selected profile.

ADRV904X CONFIGURATOR



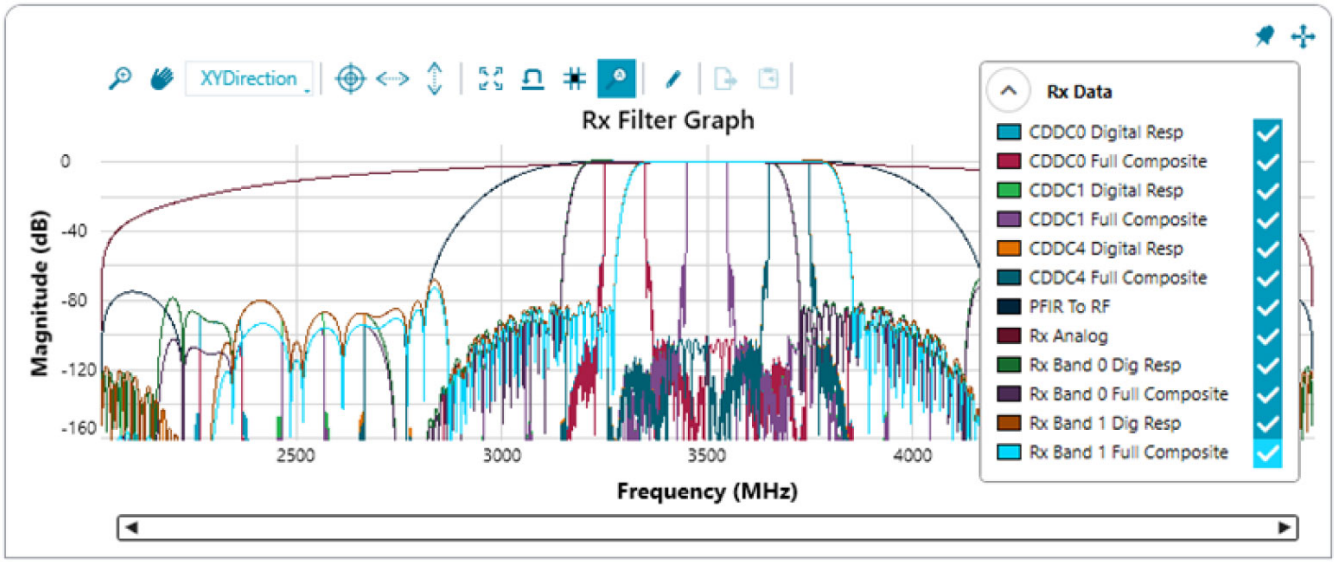


Figure 30. Receiver Datapath Filter Graphs

OBSERVATION RECEIVER CONFIGURATION

Observation Receiver Datapath

On the **ORx Config** page, the user can set the following:

- Observation receiver ADC CLK rate mode to switch between ADC rates.
- Observation receiver enables for ORx0/ORx1.
- Output sample rates for the enabled ORx channels.

ADRV904X CONFIGURATOR

Figure 31 shows the **ORx Config** input fields on the left panel. After configuring the remaining configurator pages and clicking **Generate Profiles**, which can be accessed from multiple **Configurator** pages, the observation receiver datapath figure is updated. Switch the displayed parameters of the figure between different profiles and ORx configurations via the drop down boxes at the top left corner of the datapath figure. Blocks that are colored blue are enabled and blocks that remain opaque are bypassed.

Note that once the **Carrier DUC** page is populated, the **ORx Config** page sample rates must be updated to allow the configurator to solve for an appropriate transmitter DPD rate. In case the configurator is unable to resolve the DPD rate, Figure 32 shows the error message. The user must then try alternative carrier DUC rates or modify the observation receiver sample rates.

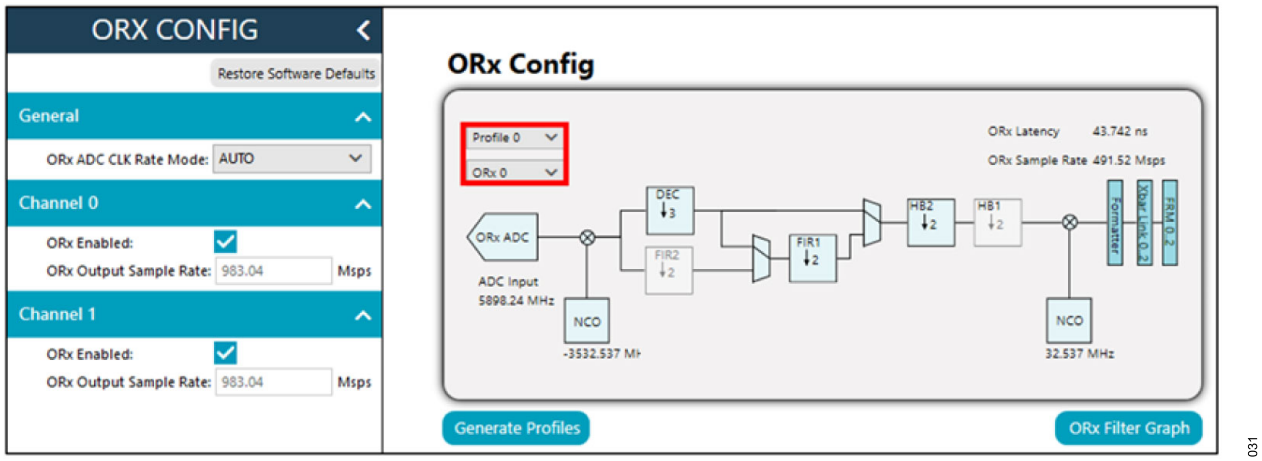


Figure 31. Observation Receiver Configuration Setup Diagram

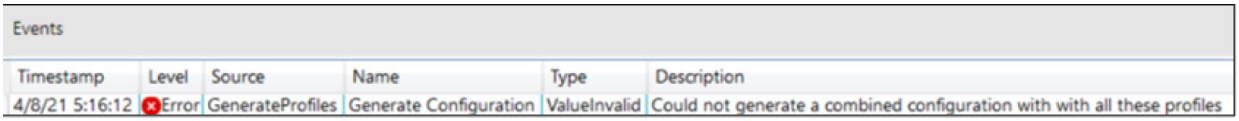


Figure 32. One Possible Error if the Configurator is Unable to Resolve the Tx DPD Rate

Observation Receiver Filter Graph

A corresponding observation receiver filter graph of the profile can be viewed via the **ORx Filter Graph** button. This helps the user understand the frequency response of the selected observation receiver profile. An example is shown in Figure 33.

In the current configurator version, only the digital composite response of the observation receiver datapath is displayed, but analog filter contributions are not included. The user can change the profile selection on the **ORx Config** page to see the corresponding filter response for a selected profile.

ADRV904X CONFIGURATOR

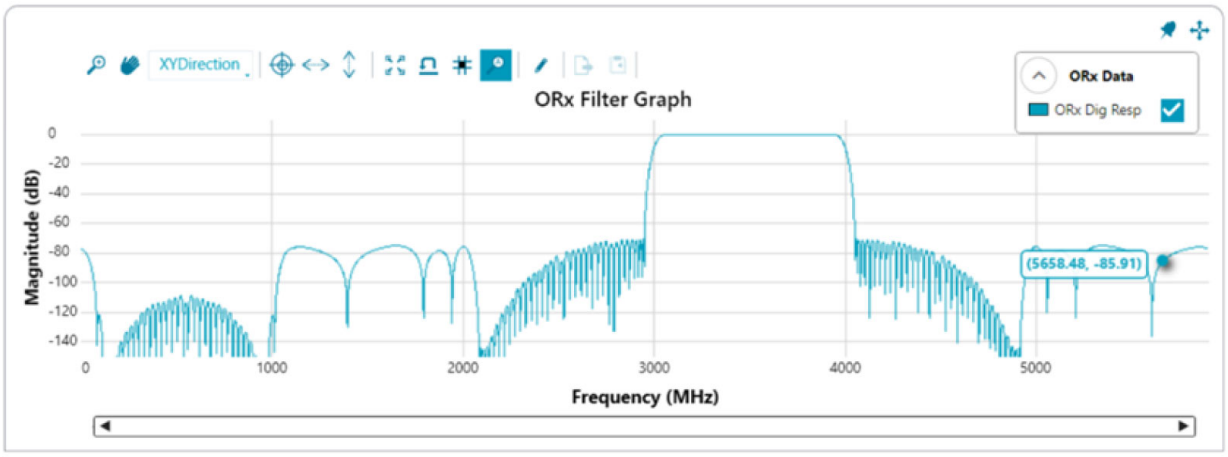


Figure 33. Observation Receiver Digital Filter Composite Frequency Response

JESD CONFIGURATION

The ADRV904x transceiver supports JESD interface standards for the serializer/deserializer (SERDES) link between the baseband unit and the transceiver to facilitate high-speed high bandwidth data transfer. The JESD interface on the ADRV904x transceiver supports JESD 204B and JESD 204C standards, and SERDES lane rates of up to 24.3 Gbps over eight serial lanes.

The JESD configuration pages can be accessed by expanding the menu under ADRV9040 > **Configurator** > **JESD 204B/C** in the system explorer window. The user can start with the basic JESD page as shown in Figure 34, and navigate to the appropriate sample crossbar settings page depending on whether the CDUC or CDDC is enabled, as described in Table 6 and Table 7. The JESD configuration inputs required from the user are listed in Table 6 and Table 7.

Table 5. Overview of JESD Configuration Pages

JESD Configuration Page	Description
Basic JESD	JESD 204B/C mode selection Framer/deframer NP and L assignments Framer/deframer lane crossbar assignments Framer/deframer selections for Rx/Tx/ORx sample crossbar auto assignment
Component Carrier Sample Crossbar	Converter sample crossbar settings for enabled deframer(s) when CDUC is enabled Converter sample crossbar settings for enabled framer(s) when CDDC is enabled
General Sample Crossbar	Converter sample crossbar settings for enabled deframer(s) when CDUC is bypassed Converter sample crossbar settings for enabled framer(s) when CDDC is bypassed

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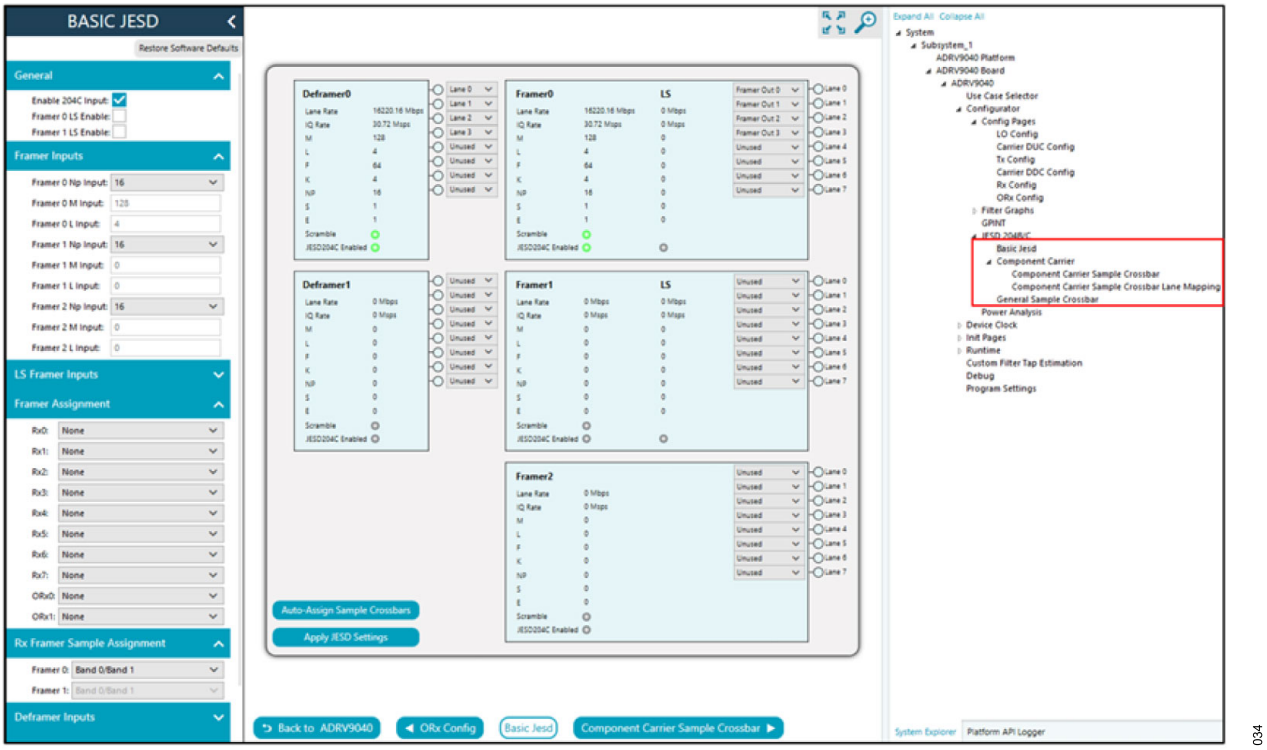

Figure 34. Basic JESD Configuration Page

Table 6. ADRV904x JESD Deframer Configuration Parameters

JESD Deframer (Tx Side) Configuration	
Parameters	**Description**
Deframer Lane Crossbar	Lane crossbar settings between the deserializer and the deframer in the Tx path.
DAC Sample Crossbar	Sample crossbar settings between the deframer output and the DAC input.
M	Number of virtual digital to analog converters on the transmitter side. Each carrier is mapped to a virtual pair of 30.72 MSPS DAC converters. For example, if each transmitter is transmitting three carriers at 30.72 MSPS, then the total number of virtual converters = 8 channels × 3 carriers per channel × 2 converters for I and Q per carrier = 48 virtual converters. To consider another example, if each transmitter is transmitting three carriers at 61.44 MSPS, then the total no. of virtual converters = 8 channels × 3 carriers per channel × 2 converters for I and Q per carrier × 2 = 96 virtual converters, where the last factor of two is sample rate (61.44 MSPS) ÷ virtual converter rate (30.72 MSPS).
NP	DAC sample bit-width.
L	Number of input lanes at the ADRV904x deserializer input.
F	Number of DAC bytes per frame of data.

Table 7. ADRV904x JESD Framer Configuration Parameters

JESD Framer (Rx Side) Configuration	
Parameters	**Description**
Framer Lane Crossbar	Lane crossbars settings between the framer and the serializer in the Rx path.
ADC Sample Crossbar	Sample crossbar settings between the ADC output and framer input.
M	Number of virtual analog to digital converters on the receiver side. Each carrier is mapped to a virtual pair of ADC converters. For example, if each receiver is transmitting three carriers, then the total number of virtual converters = 8 channels × 3 carriers per channel × 2 converters per carrier = 48 virtual converters.
NP	ADC sample bit width.
L	Number of output lanes at the ADRV904x serializer output.
F	Number of ADC bytes per frame of data.

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Basic JESD

The user can select between JESD 204B and JESD 204C under **General** settings. Additionally, the user can configure **NP** and **L** under **Framer Inputs** or **Deframer Inputs**, and assign serial lanes to selected framers/deframers on the figure itself. Note that the JESD parameters displayed in Figure 36 are calculated and updated once the configurator runs successfully and generates the desired profiles. Profiles can be generated from the basic JESD page via **Apply JESD Settings**, but the sample crossbar settings must be updated before profiles can be generated without error.

To simplify the JESD configuration process, the **Basic JESD** page supports automatic assignment of sample crossbar settings, which means that the user can select assignments for framers and deframers for the receiver, observation receiver, and transmitter samples. Additional flexibility is provided where the user can select either Rx Band 0, Rx Band 1, or both Rx Band 0/Rx Band 1 samples to be assigned to a given framer under **Rx Framer Sample Assignment**. ORx samples can be assigned to any framer(s) or left unassigned as desired. **Sample Assignment** dropdowns are only enabled for framers with valid NP and receiver assignments.

In the example shown in Figure 35, all Rx channels are mapped to Framer 0 such that both Band 0 and Band 1 samples are assigned to Framer 0. This way, the user can autoassign each receiver band to separate framers, or leave one or both bands unassigned. Alternatively, observation receiver samples are left unassigned such that observation receiver data are not sent over JESD. If desired, observation receiver samples can be assigned to a framer under **Framer Assignment**. However, band sample selections do not apply to the observation receiver. Therefore, the **Rx Framer Sample Assignment** section only needs to reflect the desired receiver band sample assignments.

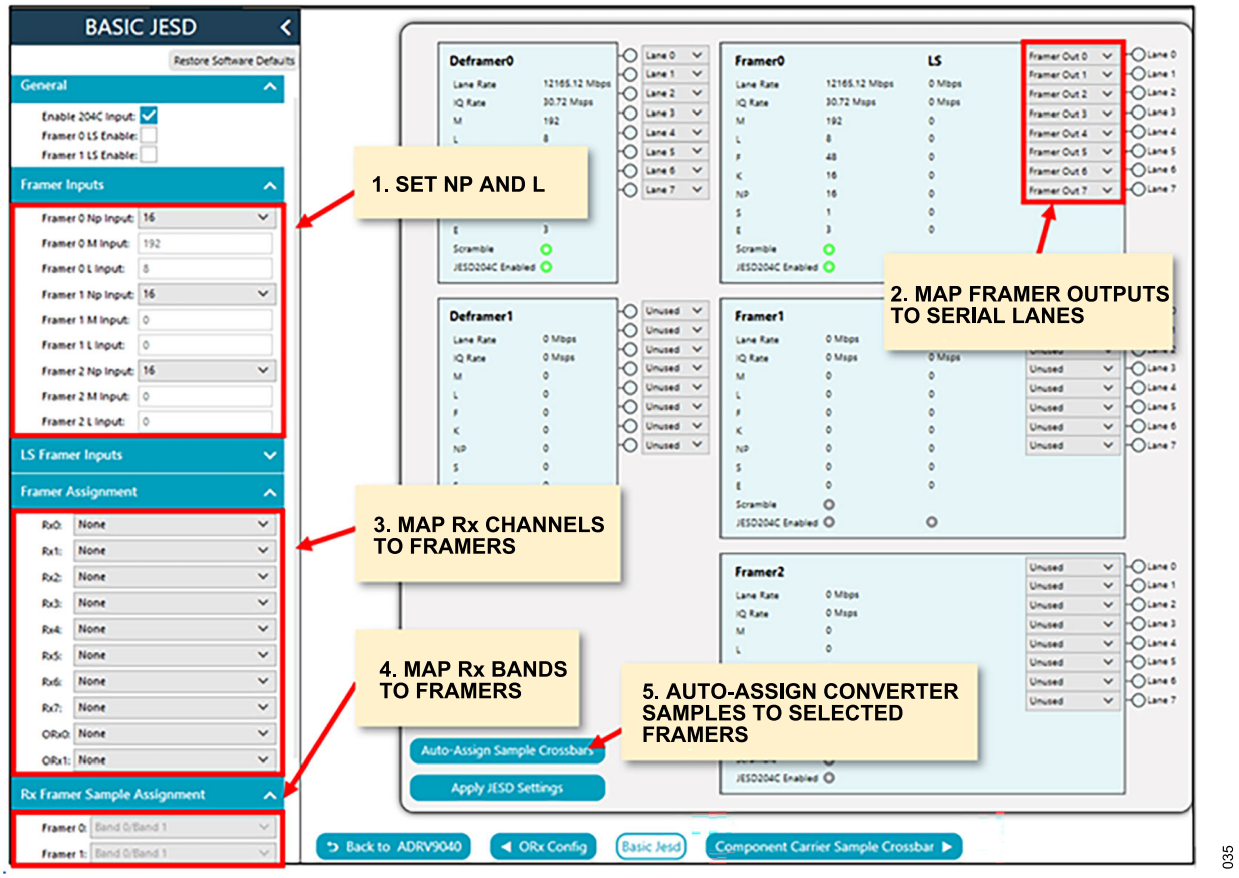


Figure 35. Steps to Configure JESD Framers and Specify User Preferences for Sample Crossbar Auto Assignment

On the transmitter side, the user can configure the deframer NP and L settings and assign serial lanes to deframer inputs. The user can also map transmitter channels and bands to either deframer for setting up sample crossbar auto assignment. Sample assignment dropdowns are only enabled for deframers with valid NP and transmitter assignments. In the example shown in Figure 36, all transmitter channels Band 0 and Band 1 samples are mapped to Deframer 0.

ADRV904X CONFIGURATOR

Once framer/deframer assignments and band selections are made, the user can click on **Auto-Assign Sample Crossbars** to automatically populate the sample crossbar pages. Clicking **Apply JESD Settings** runs the configurator, and the framer/deframer figures are updated to display the JESD parameters solved by the configurator.

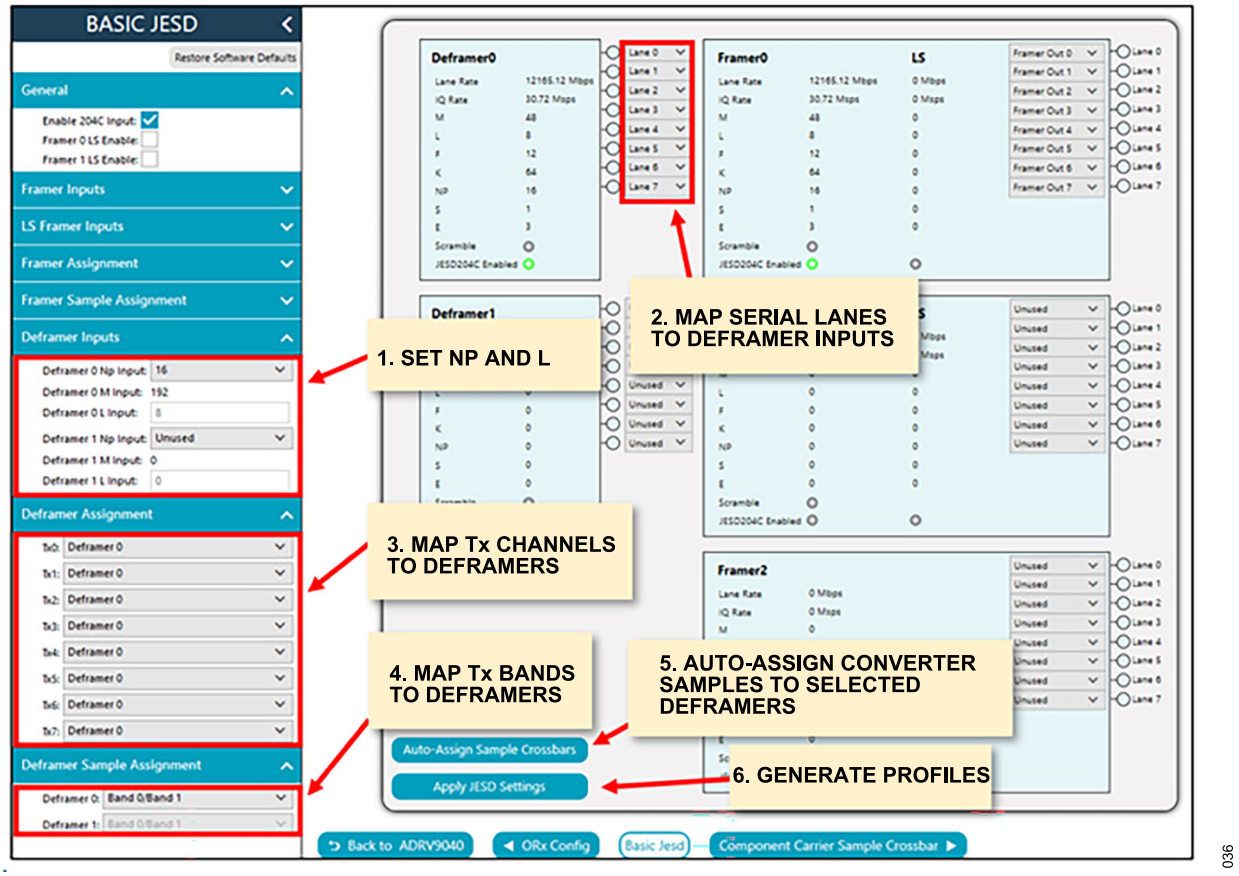


Figure 36. ADRV904x JESD Deframer Configuration

Note that if the carrier configuration is updated at any time through either the **Carrier DUC** or **Carrier DDC** pages, the user can rerun **Auto-Assign Sample Crossbars** to eliminate any configurator errors associated with stale sample crossbar assignments (from a previous carrier configuration).

Important: the current implementation of the **Basic JESD** page does not expose observation receivers deinterleaving parameters. This will be addressed in upcoming releases.

Component Carrier Sample Crossbar

The sample crossbar page is used to assign CDUC/CDDC samples to enabled deframers/framers. The sample crossbar assignments can be auto populated as described in the Basic JESD section. Auto assignment can serve as a starting point, and the sample assignments can be modified manually as desired.

The user can navigate between different deframers and framers through the drop down menus at the bottom of the figure. Note that deframer/framer Entry 0 through Entry 191 are split across six assignment pages, which can also be switched from the dropdown menus at the bottom. Each entry can be assigned to the desired component carrier sample by selecting a channel and a corresponding carrier sample on each row as shown in Figure 37.

Once the sample crossbar is configured as desired, the user can click on **Apply JESD Settings** to generate profiles.

ADRV904X CONFIGURATOR

Figure 37. Component Carrier Sample Crossbar Showing Auto Assigned Samples

General Sample Crossbar

This sample crossbar page is used to assign DAC/ADC samples to enabled deframers/framers when CDUC/CDDC is bypassed. The sample crossbar assignments can be auto populated as described in the Basic JESD section. Auto assignment can serve as a starting point, and the sample assignments can be modified manually as desired.

The user can navigate between different deframers and framers through the drop down menus at the bottom of the figure. Note that framer Entry 0 through Entry 63 are split across two assignment pages, which can also be switched from the drop down menu underneath the framer selection. Each entry can be assigned to the desired converter sample by selecting a sample on each row as shown in Figure 38.

Once the sample crossbar is configured as desired, the user can click on **Apply JESD Settings** to generate profiles.

ADRV904X CONFIGURATOR

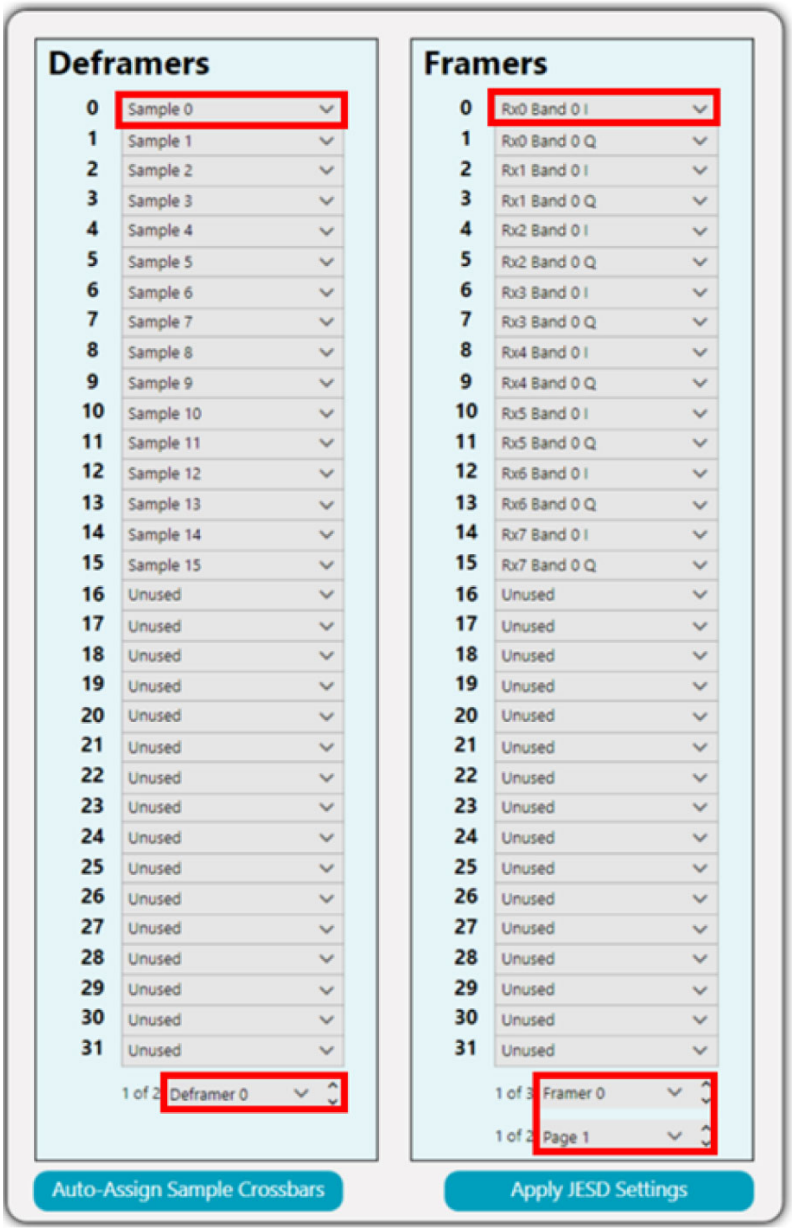


Figure 38. General Sample Crossbar Page Showing Auto Assigned Samples

POWER ANALYSIS

A separate **Power Analysis** page provides power estimates for the ADRV904x configuration set using the preceding configurator pages. The user can navigate to this page from the **Power Analysis** button underneath the **General Sample Crossbar** or by using the ACE system explorer.

Figure 39 shows a snapshot of the **Power Analysis** page.

The **Power Analysis** page displays the current draw and power consumed per voltage supply rail, as split between the transmitter, receiver, observation receiver, and common blocks. The common block shows the combined power consumed by the VCOs, dividers, JESD blocks, general purpose input/output (GPIO) blocks, and certain digital blocks.

On the left panel, the user can switch between configuration options to compare the associated power consumption as follows:

ADRV904X CONFIGURATOR

- **Datapath Mode** sets transmitter/receiver datapath interpolation/decimation rations to select different transmitter DAC and receiver ADC rates.
- **ORx ADC CLK Rate Mode** selects between observation receiver ADC clock rates.
- **Tx Attenuation** sets transmitter attenuation per channel, or copy Channel 0 attenuation setting to all channels by ticking the **Use Shared Tx Attenuation Value** checkbox. **Tx Attenuation** is set to 6 dB by default.
- **DPD** parameters input resource utilization for a desired DPD model. Two examples are shown in Figure 40.

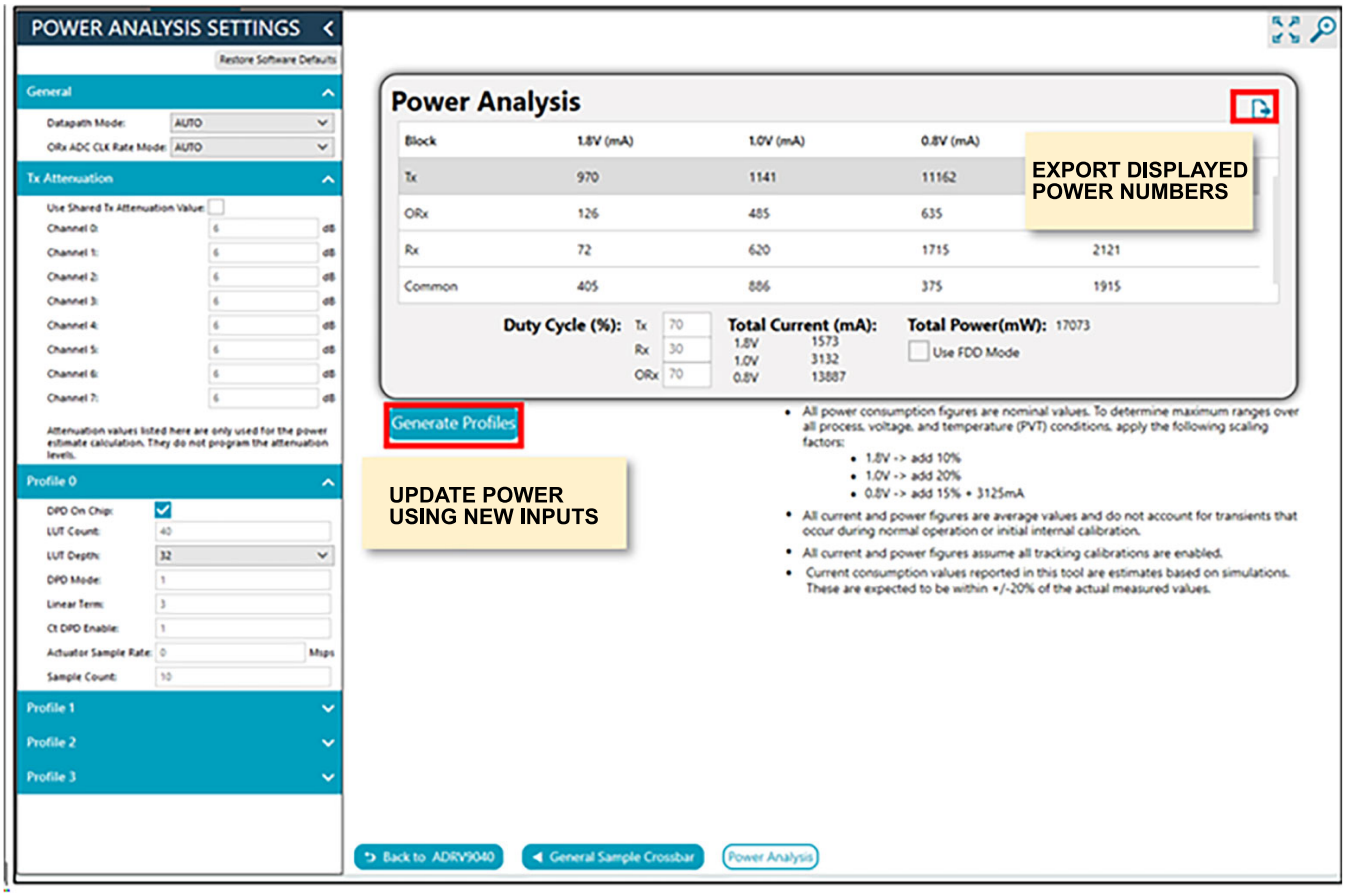


Figure 39. Power Analysis Settings and Estimates

Typical 200MHz DPD Resources		Maximum DPD Resources	
DPD On Chip:	☑	DPD On Chip:	☑
LUT Count:	26	LUT Count:	50
LUT Depth:	64	LUT Depth:	64
Complex Multiplier Count:	6	Complex Multiplier Count:	29
Sample Count:	8	Sample Count:	15

140

Figure 40. Example DPD Model Parameters for Power Analysis

On **Power Analysis**, the user can enter the TDD duty cycle for the transmitter, receiver, and observation receiver channels to get an estimate of the power consumed in TDD mode. The **Use FDD Mode** button allows the user to get the total power consumed when all transmitter, receiver, and observation receiver channels are enabled, which essentially sets the duty cycle to 100% for receiver/transmitter and observation receiver modes. The user must click on **Generate Profiles** to update the power numbers.

ADRV904X CONFIGURATOR

A typical usage of the **Power Analysis** is to get an estimate of the power consumed in different states of the ADRV904x as shown in Figure 41 to Figure 45. The displayed power numbers can also be exported to a CSV file by using the export button to the top left of the **Power Analysis** diagram.

Standby Mode

This mode represents the total standby current consumed when all transmitter, receiver, and observation receiver channels are in the off state.

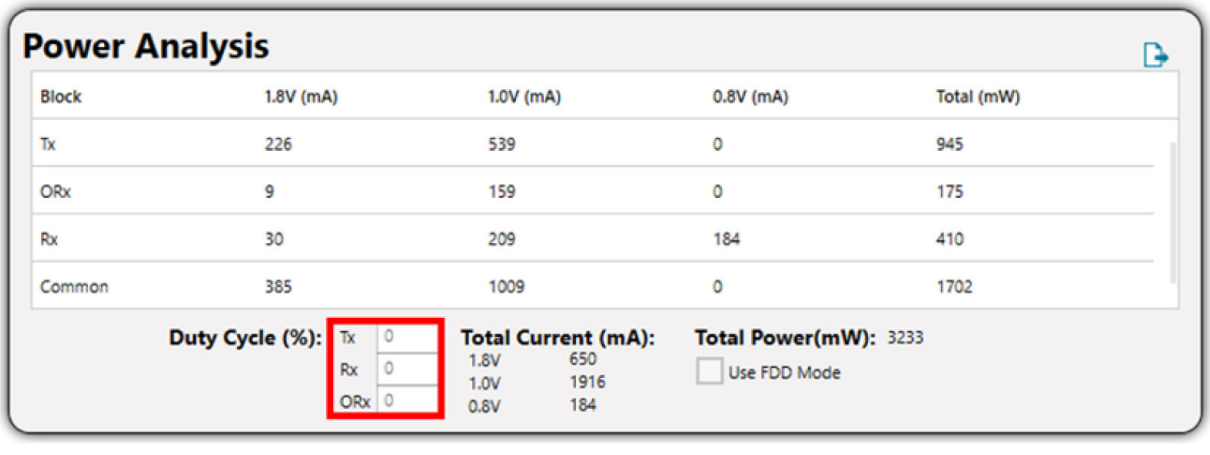


Figure 41. Example of Current Consumed in Standby Mode

Transmitter Only Mode

Transmitter only mode represents the total current consumed when only the transmit channels are enabled. All receiver and observation receive channels are in the off state.

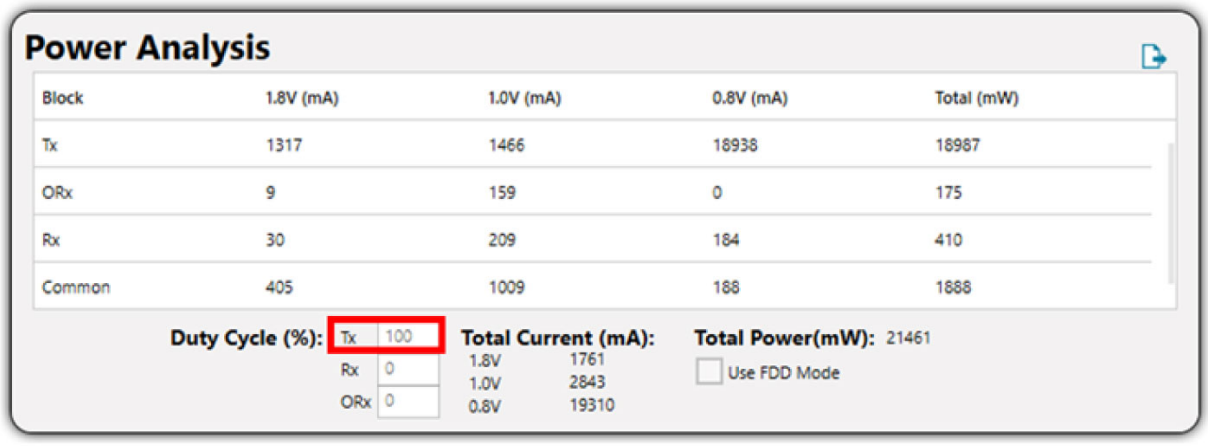


Figure 42. Example of Current Consumed in Tx Only Mode

Observation Receiver Only Mode

Observation receiver only mode represents the total current consumed when only observation receive channel/s are enabled. All transmit and receive channels are in the off state.

ADRV904X CONFIGURATOR

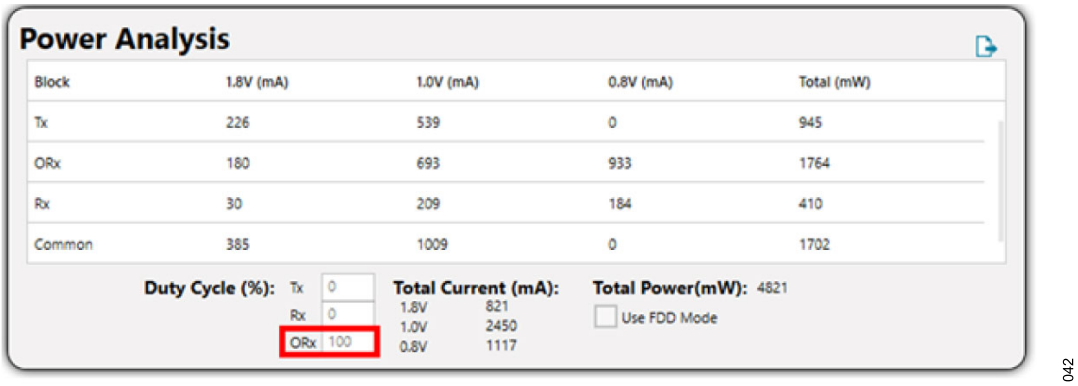


Figure 43. Current Consumed in ORx Only Mode

Transmitter + Observation Receiver Only Mode

Transmitter + observation receiver only mode represents the total current consumed when only the transmit channel and observation receive channel/s are enabled. All receive channels are in the off state.

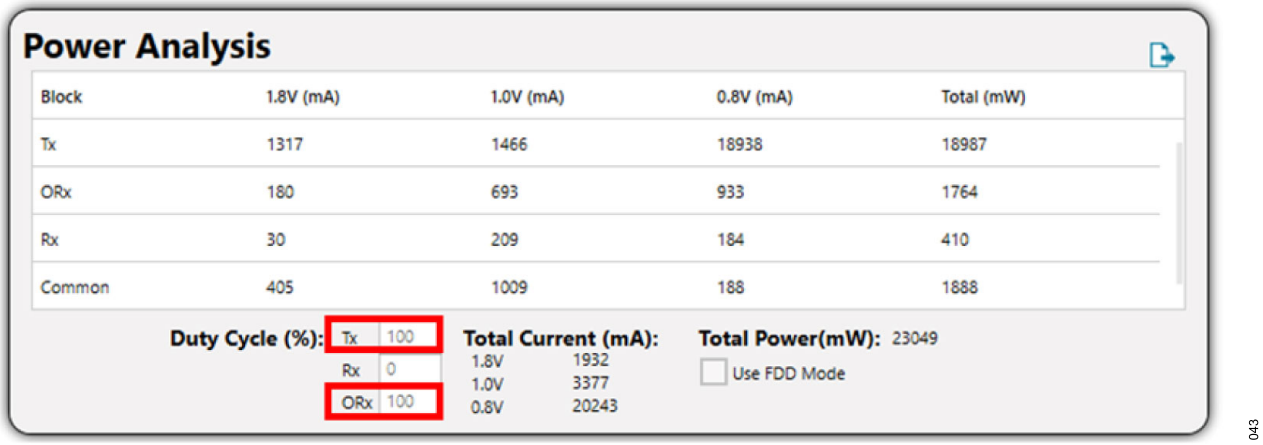


Figure 44. Current Consumed in Tx + ORx Only Mode

Receiver Only Mode

Receiver only mode represents the total current consumed when only receive channels are enabled. All transmit and observation receive channels are in the off state.

ADRV904X CONFIGURATOR

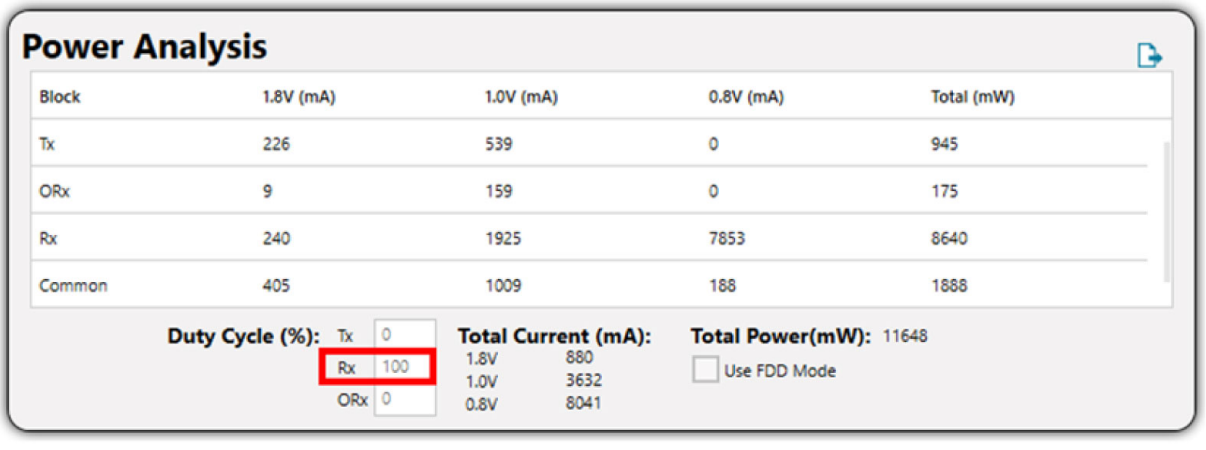


Figure 45. Current Consumed in Rx ONLY Mode

It is recommended that the user must estimate the TDD power by configuring ACE into the transmitter + observation receiver only mode as shown in Figure 44 and record the total power. Then the user can configure ACE in receiver only mode as shown in Figure 45 and record the total power. Finally, the user can take a weighted average of the two to get to the correct TDD power consumed for different receiver/transmitter/observation receiver duty cycles.

Note that the values reported here are steady state current and power numbers. These numbers do not account for the transients that occur during calibration.

It is also important to note that the power numbers reported here are only an estimate. Analog Devices does not run exhaustive testing to cover for all cases that can be set up using the configurator. The user must contact Analog Devices for any issues with the power consumption numbers reported by the tool.

INIT PAGES

The **Init Pages** can be used to set initialization parameters for ADRV904x device datapaths.

POST MCS INIT

If using pin mode, the **Post MCS Init** page can be used to assign TRX_CTRL pins as enables for various ADRV904x transmitter and receiver channels through user specified channel masks as shown in Figure 46. Refer to the following steps:

1. Set **Pin Select** bit mask to 1 for each TRX_CTRL pin to be configured as an enable. For instance, setting **Pin Select** to 0x3 selects TRXA_CTRL and TRXB_CTRL to be used as channel enables.
2. Set **Config Select** bits to select whether pin controls are updated for transmitter, transmitter alt, receiver, and receiver alt settings.
3. If configuring transmitter enables, map the transmitter channel mask to be enabled per TRX_CTRL pin. For example, mapping 0xFF to TRXA_CTRL allows all eight transmitter channels to be enabled by TRXA_CTRL.
4. If configuring receiver enables, map the receiver channel mask to be enabled per TRX_CTRL pin. For example, mapping 0xFF to TRXC_CTRL allows all eight receiver channels to be enabled by TRXC_CTRL.
5. Transmitter alt and receiver alt pin mappings can be assigned in the same way.
6. The user can program these TRX_CTRL mappings by clicking on program device from the **Top Level Config** page. Alternatively, clicking on **Configure Mappings** applies the pin mappings after initialization.

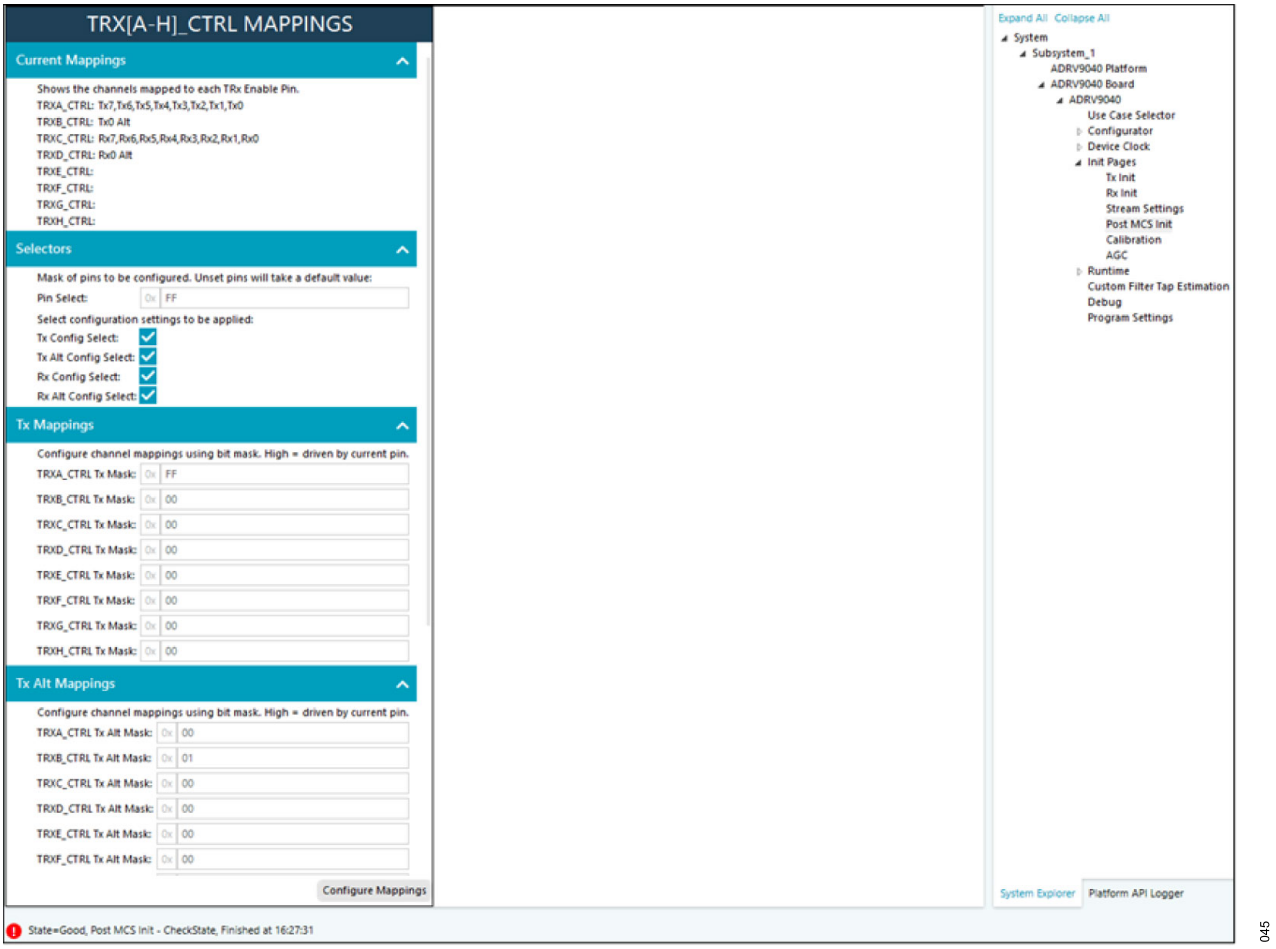


Figure 46. TRXA_CTRL to TRXH_CTRL Pins Mapped as Tx/Rx Datapath Enables on Post MCS Init Page

CALIBRATION

Device calibrations to be run during ADRV904x initialization can be enabled/disabled from **Init Pages** > **Calibration**. Refer to the release notes accompanying a given customer software package for more information regarding supported calibrations.

INIT PAGES

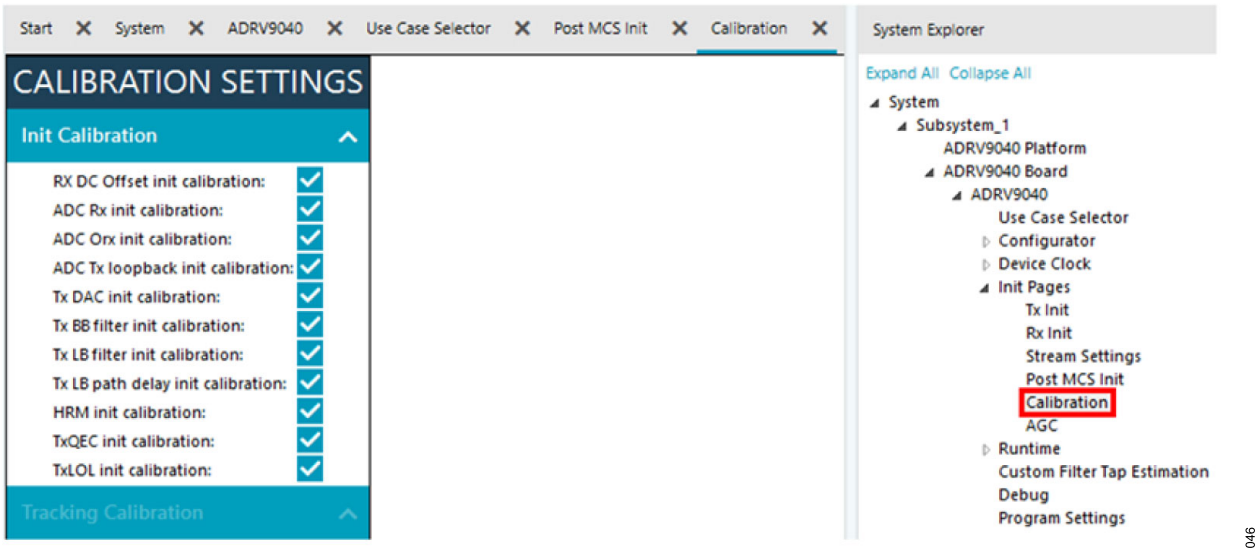


Figure 47. Calibration Page is Used to Update the Init Calibration Mask Run During Initialization

AD9528 CLOCK SETTINGS

The CE board comes with an AD9528 clock generator that takes a **Ref A Clock** input and generates the ADRV904x device clock and the FPGA device clock as outputs. The CE board includes a crystal oscillator running at 122.88 MHz voltage-controlled crystal oscillator (VCXO).

The AD9528 page can be used to program the ADRV904x using a clock input different from the default. After configuring this page, the user must program the ADRV904x from the **Top Level Config** page, the ADRV9040.

INIT PAGES

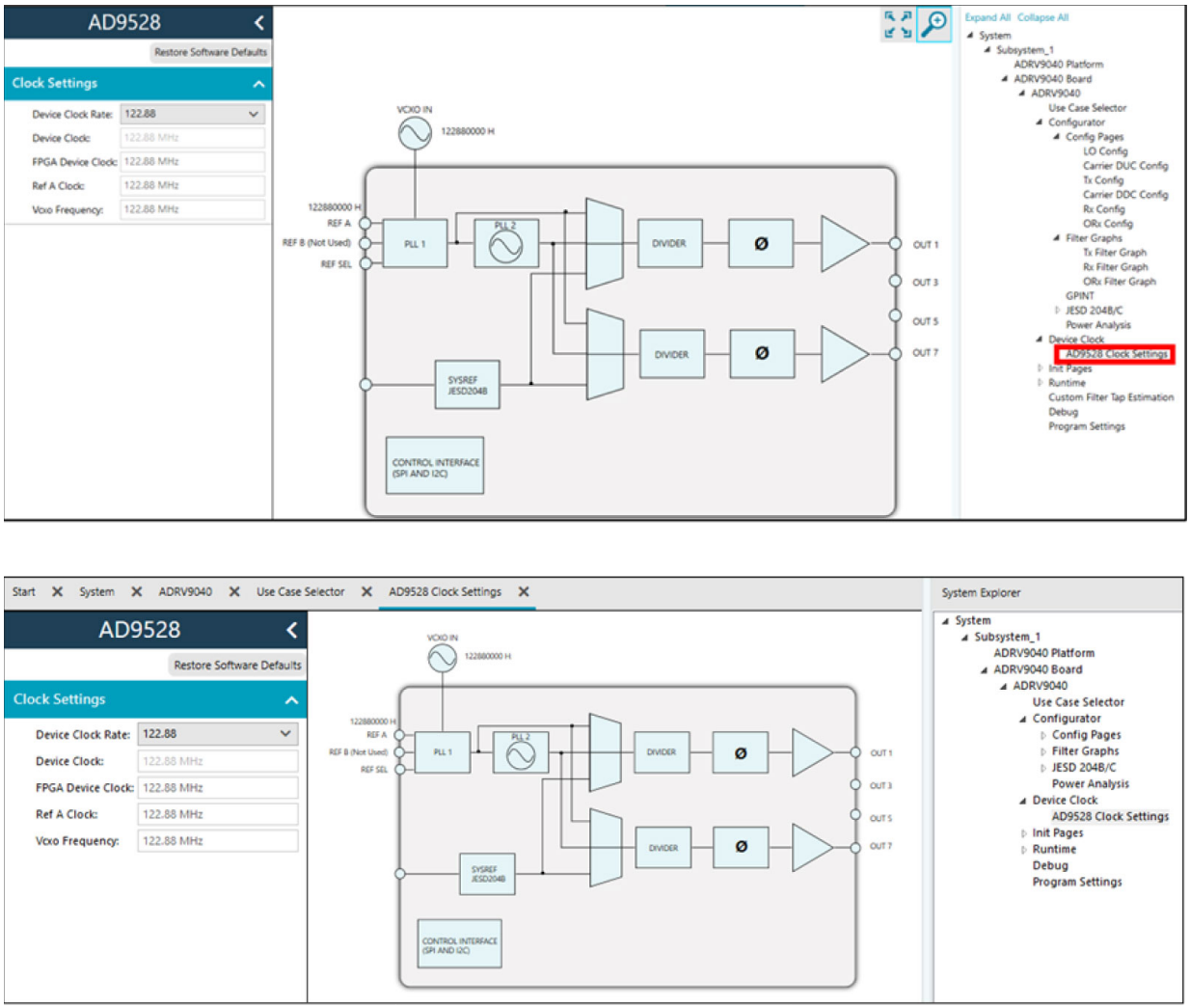


Figure 48. AD9528 Page for Changing Clock Generator Settings

RUNTIME

Once programmed, the runtime pages can be used for testing the performance of different ADRV904x datapaths. These runtime pages provide data sourcing capability for the transmitters, and capturing functionality for the receivers and observation receivers.

TRANSMITTER VECTORS

Transmitter performance can be evaluated by sending data over the JESD link, or by generating test tones using ADRV904x on-chip NCO in each baseband of a transmitter datapath. The vector generator of ACE can be used for creating new data vectors or importing vectors from existing data files, and can also be used to change attenuation settings for each enabled transmitter.

Generating JESD Data Vectors

For illustration, a single tone vector can be generated using the following steps:

1. Launch **Tx Vectors** from **System Explorer** > **Runtime** > **Tx Vectors** as shown in Figure 49.
2. Click on **Vectors** to open the vector generator of ACE.
3. Create a new single tone vector by clicking on **+** besides the **Single Tone Vector** under common waveforms as shown in Figure 50.
4. Set the vector's data rate to match the transmitter sample rate (as configured in the Use Case Selector section or LO Frequency Change Steps section).
   - Data rate must match the carrier sample rate for CDUC/CDDC profiles.
   - For FDD, the play length (time) must be equal for each carrier. For example, the record length of a 122.88 MHz carrier should be four times the record length of a 30.72 MHz carrier.
   - Change the record length of the vector as per the sample rate.
5. Set the desired baseband frequency of the tone.
6. Select **Generate Complex Data** to generate a data vector containing I and Q samples.
7. Preview the vector to verify parameters. If needed, this vector can be exported to a text file by clicking on **Export**.
8. Switch back to the **Tx Vectors** page. However, do not close the **Vector Generator** tab completely by pressing **x**. The **Vector Generator** must remain open as a background tab for the vectors to be selectable on the **Tx Vectors** page.
9. Enable the desired transmitter channel(s) and transmitter observability from the **Tx Vectors** page.
10. Configure each transmitter channel data input to the intended vector, as named and defined on the **Vector Generator**.
    - For profiles with CDUC/CDDC enabled: user can map a specific vector to each carrier as shown in Figure 52.
11. Update **Tx Attenuation** (dB) field as needed.
12. Enable the QEC and LOL tracking calibrations.
13. **Play** transmitter data continuously over JESD as shown in Figure 51. This updates the waveform and fast Fourier transform (FFT) plots to preview the loaded vectors. The transmitter RF output can then be captured using a spectrum analyzer as shown in Figure 52.
14. **Stop** halts the data transmission.

RUNTIME

Figure 49. Tx Vectors Page is Used to Enable Tx Channels, Map Vectors to Each Enabled Tx, and Plot the Baseband Vectors

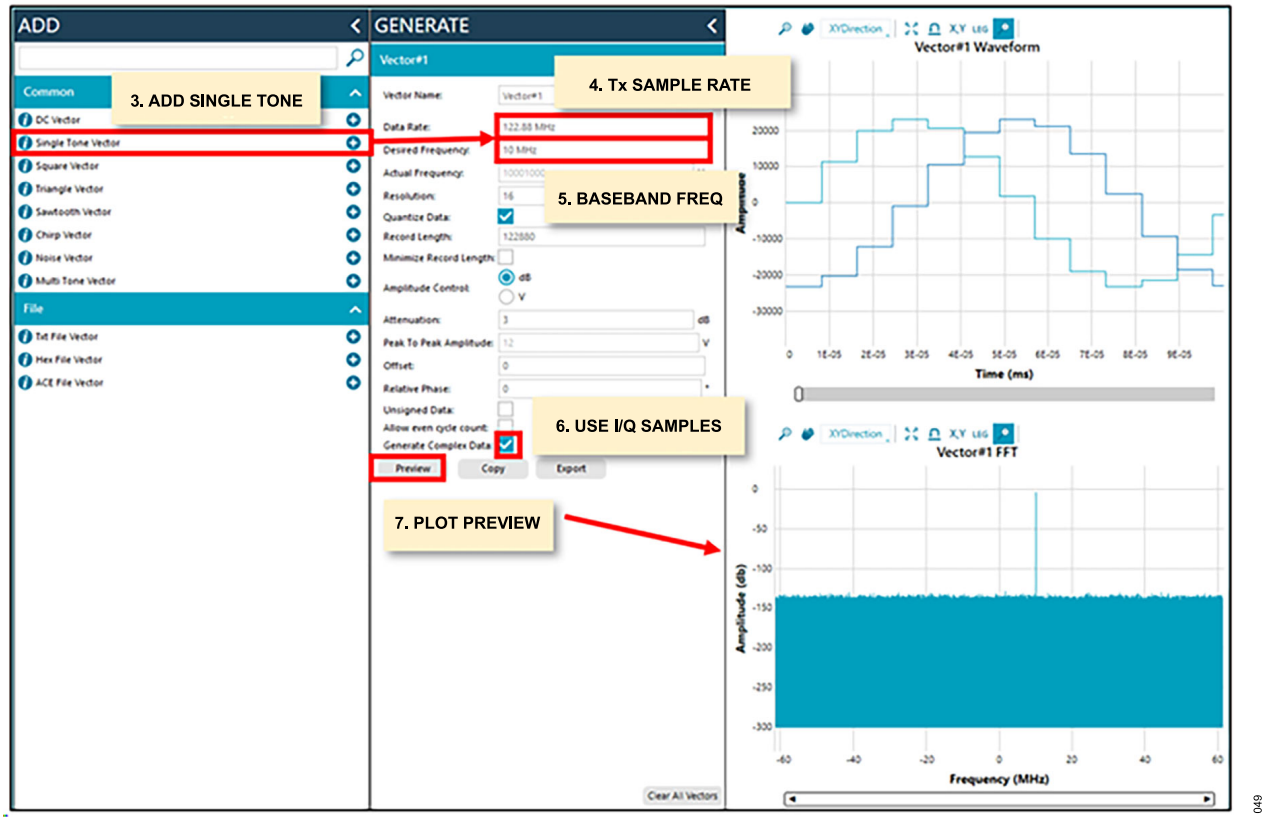


Figure 50. Steps for Generating a Complex Single Tone Vector Using ACE Vector Generator

RUNTIME

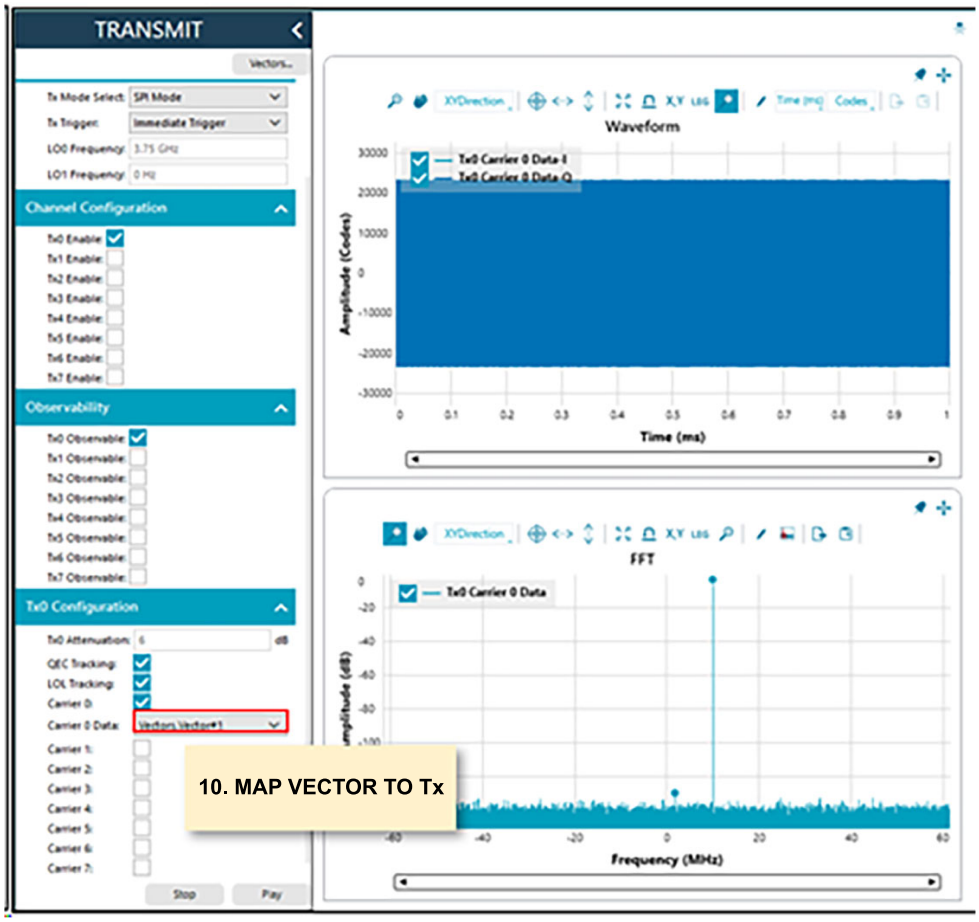


Figure 51. Tx Vector Mapping to Each Carrier

RUNTIME

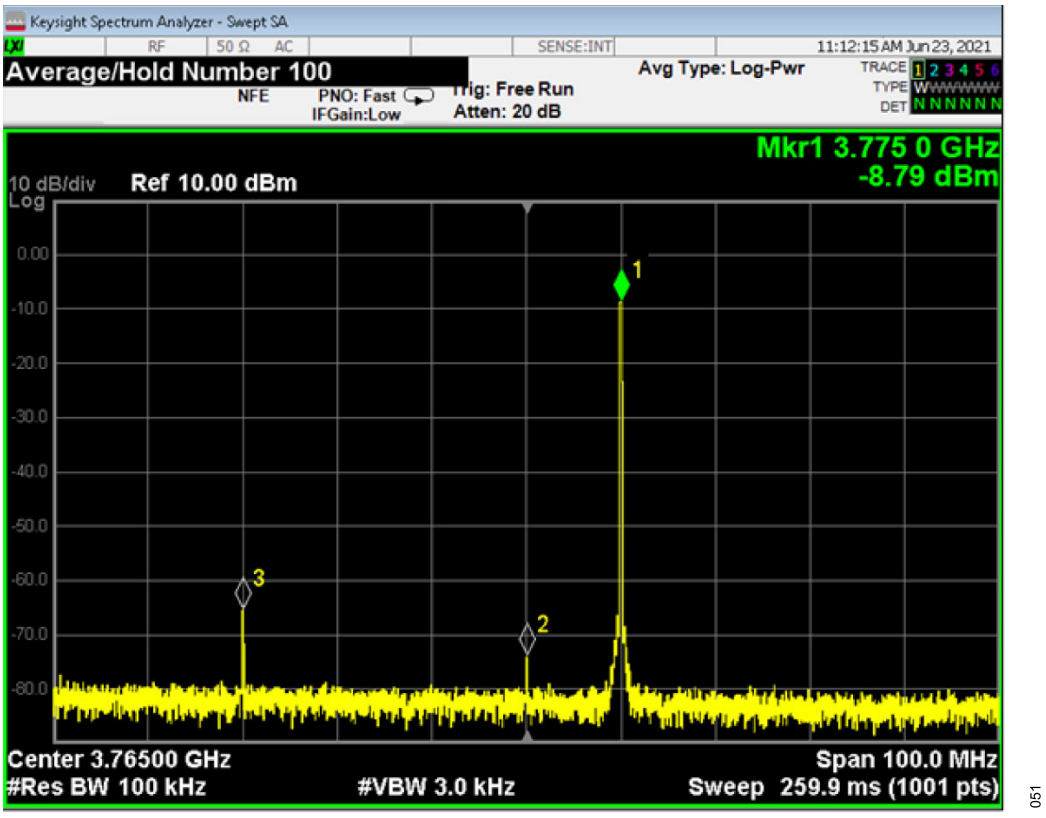


Figure 52. Tx0 Single Tone Spectrum as Captured by a Spectrum Analyzer

Exporting and Importing JESD Data Vectors

The **Vector Generator** page also allows exporting and importing of vectors. The user can export a vector from **Vector Generator** by clicking on **Export** from the **Generate** panel as shown in Figure 53. This writes the vector out to a .txt file in the ACE export data directory **C:\Users\%USERPROFILE%\AppData\Local\Analog Devices\ACE\ExportData**.

This vector can be imported back into the **Vector Generator** as follows:

1. Click **+** to add a .txt file vector.
2. Select **Complex – Interleaved**. ACE generated .txt vectors are a single column with I- and Q-samples interleaved.
3. Match data rate to the transmitter sample rate (as configured by in the Use Case Selector section or LO Frequency Change Steps section).
4. Click on **Preview** to confirm the vector parameters.

RUNTIME

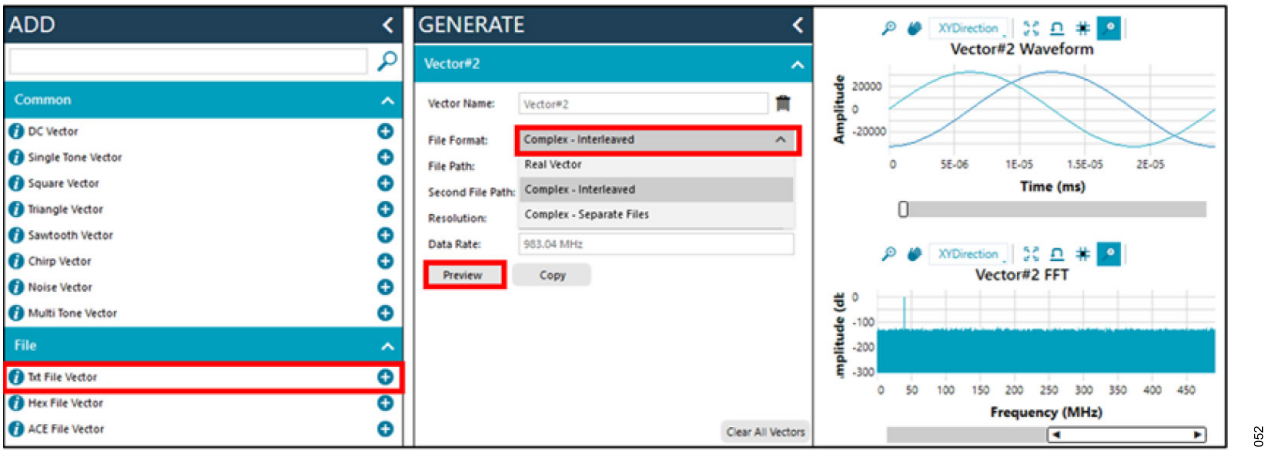


Figure 53. Importing a .txt File Vector into a Vector Generator

Setting Transmitter Attenuation

Transmitter attenuation can be set in dB for each enabled transmitter channel individually.

Note that transmitter attenuation changes are only applied when the user clicks **Play**.

RX (CAPTURE)

Receiver data can be captured over JESD and analyzed using the **Rx (Capture)** page as shown in Figure 54. The user must do the following:

1. Navigate to **System Explorer** > **Runtime** > **Rx (Capture)**.
2. Confirm that the desired receiver channels are enabled. If using a link sharing profile, ensure that no observation receiver channels are enabled at this time. Observation receiver channels can be disabled from the **System Explorer** > **Runtime** > **ORx (Capture)** page.
3. Click **Run Once** or **Run Continuously** to capture data.
4. For profiles with CDDC enabled, the user can specify each carrier to monitor as shown in Figure 55.

Other than capturing data over JESD, the user can also capture data internally using ADRV904x RAMs. However, this method limits the data capture size and takes longer to execute. To use the internal RAM, the user must only have one receiver channel enabled on the **Rx Capture** page (and all obsrevation receivers disabled on the **ORx Capture** page). Then, the user can select DDC0/DDC1 output as **Capture Mode** and run the capture. Enabled DDC paths can be viewed from the **Rx Configuration** page.

RUNTIME

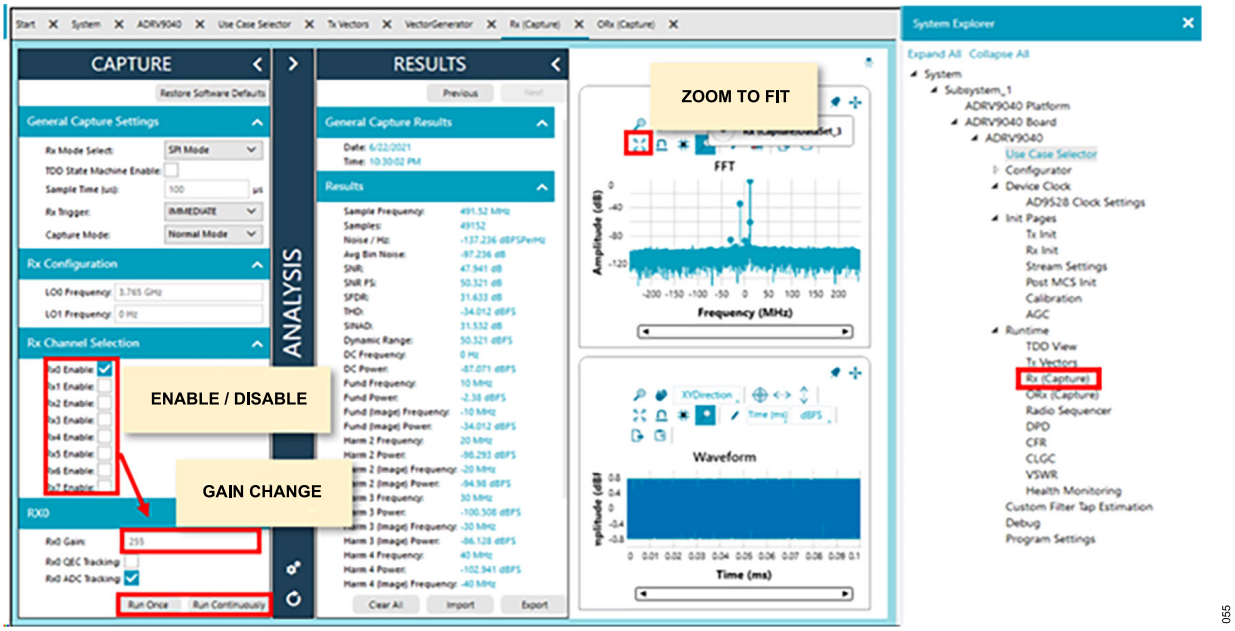


Figure 54. Rx (Capture) is Used to Capture and Analyze Receiver Outputs over JESD

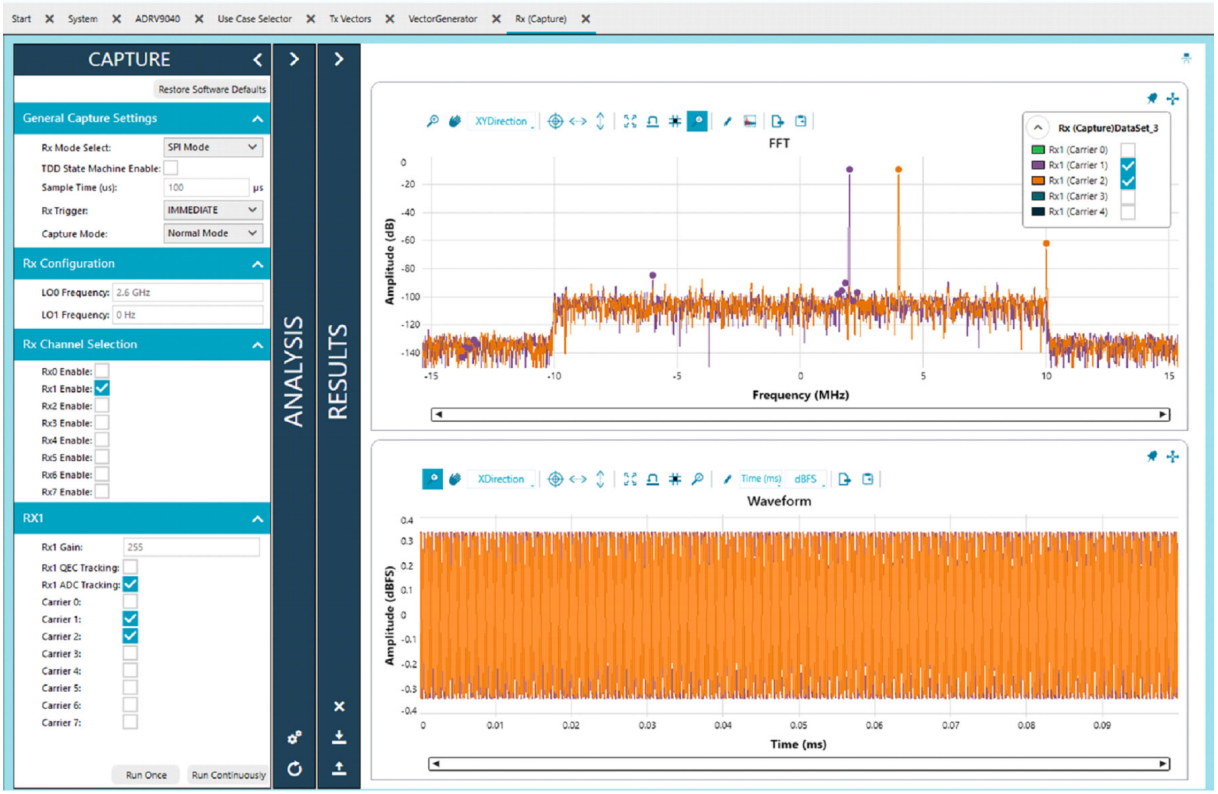


Figure 55. Rx Capture with Carriers Selection

Setting Receiver Gain

The gain index for any enabled receiver channel can be changed by either entering a new gain index or by using the arrowheads to increment/decrement the gain index in steps of one. Gain changes are applied to the ADRV904x as soon as the values are updated, regardless of the data capture state whether halted or running continuously.

RUNTIME

Enabling Receiver QEC Tracking

The user can additionally enable quadrature error correction (receiver QEC tracking) calibration for each enabled receiver as shown in Figure 56.

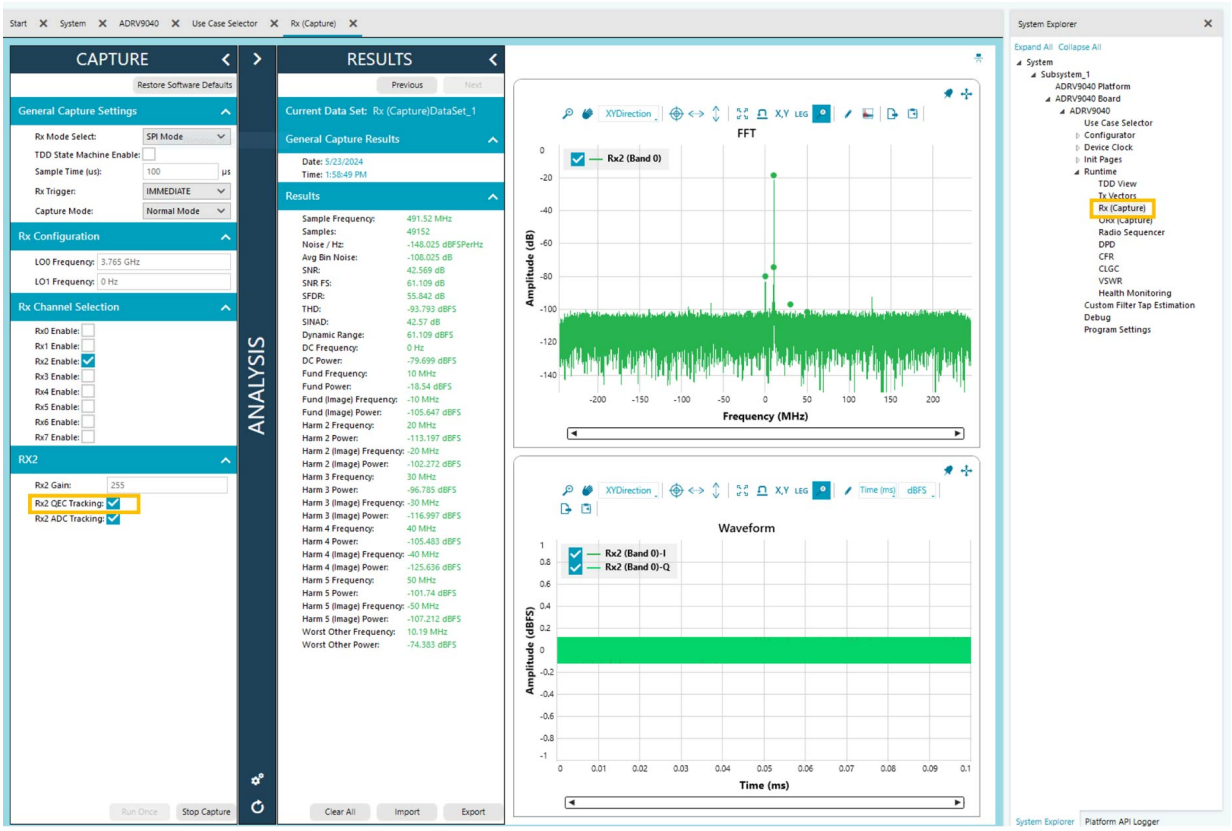


Figure 56. Rx Capture Performed after Enabling Rx QEC Tracking for Rx0

It is important to take note of the following if using a link sharing profile:

- Only receiver channels must be enabled when attempting to capture receiver data.
- Currently the user must disable any additionally enabled observation receiver channels from the **ORx (Capture)** page before receiver data can be captured over the shared JESD link.
- The user can click on **Zoom to Fit** to correctly rescale the FFT plot when switching between receiver and observation receiver.

ORX (CAPTURE)

The process for capturing observation receiver data is similar to the **Rx (Capture)** process as shown in Figure 57. The process is as follows:

1. Navigate to **System Explore** > **Runtime** > **ORx (Capture)**.
2. Confirm that the desired observation receiver channels are enabled. Not that when using a link sharing profile, ensure that no receiver channels are enabled at this time. Receiver channels can be disabled from the **System Explore** > **Runtime** > **Rx (Capture)** as shown in Figure 57.
3. Under **Capture Mode**, select **Normal Mode**, which captures observation receiver data over the JESD link.
4. Click on **Run Once** or **Run Continuously** to capture data.

RUNTIME

Figure 57. ORx0 and ORx1 Data Captured over JESD Link, with Tx LO + 10MHz Input Tone Applied to ORx0

Setting Observation Receiver Attenuation

Observation receiver attenuation can be entered in dB for each observation receiver channel. Attenuation changes are applied to the ADRV904x as soon as the user clicks on **Enter** in data capture state (halted or running continuously).

Setting ORx1 attenuation through the **ORx (Capture)** page might not work as expected. This is expected to be addressed in the upcoming releases of the ADRV904x plugin.

RADIO SEQUENCER

The ADRV904x features an internal timing generator called a **Radio Sequencer**. It defines the timing of the internal signals that control Tx, Rx, and ORx enable. It also creates any output timing signal required through any of the GPIO or Analog_GPIO available in the ADRV904x. This configuration can be applied after the part is programed and overwritten as many times as needed, but the signals that the radio sequencer can take control over have to be configured in the use case JSON file.

Settings

The **Settings** tab contains the following inputs:

- **Enable**, which needs to be set to enable the radio sequencer.
- **Settings**, which is the path for the configuration file (JSON) for the radio sequencer.
- **Numerology**, which is the subcarrier spacing that the radio sequencer will use to generate the timings. All 4G and 5G numerology timings are supported.
- **Sync Mode**, wherein two options are available:
  - **Internal**: SSB_sync is generated internally. The timing depends on the configuration done during initialization.
  - **External**: Every SSB_sync from external source is used to track and shift the internal SSB_sync to ensure the skew across ADRV904x is maintained without intervention of baseband processor (BBP).
- **SSB Period**, which indicates the period of the SSB_sync signal.
- **GPIO**, which is used to input the SSB_sync external signal.
- **Generate Image**, which generates the binary file than can later be loaded to the ADRV904x.
- **Generate Profiles**, which loads changes to the profile if needed.

RUNTIME

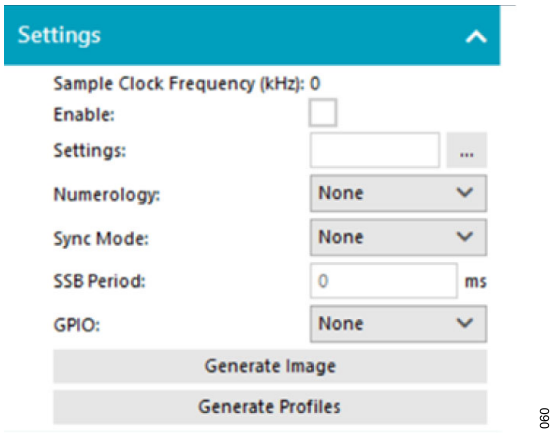


Figure 58. Radio Sequencer Settings

Table 8 provides the details of the numerology selection in Figure 58, which includes symbols per slot and number of frames.

Table 8. Numerology vs. Slots

μ	N^{slot}_{symb}	$N^{frame,\mu}_{slot}$	$N^{subframe,\mu}_{slot}$
0	14	10	1
1	14	20	2
2	14	40	4
3	14	80	8
4	14	160	16

Sequencer

This section explains the creation of the radio sequencer timing configuration. The configuration is created as a JSON file format that defines the different signals that the radio sequencer controls and its timings. Figure 59 shows an example of the radio sequencer timing configuration and JSON update.

The different levels that can be programmed are as follows:

- Patterns. Multiple patterns can be defined to enable multiple configurations to be loaded. The pattern played by the **Radio Sequencer** can be selected at runtime using API. The selected pattern repeats every SSB_sync period.
- Sequences. The total duration of the pattern can be divided in sequences.
- Timing definitions. The timing behavior of the signals. Each sequence can contain multiple timing definitions.

RUNTIME

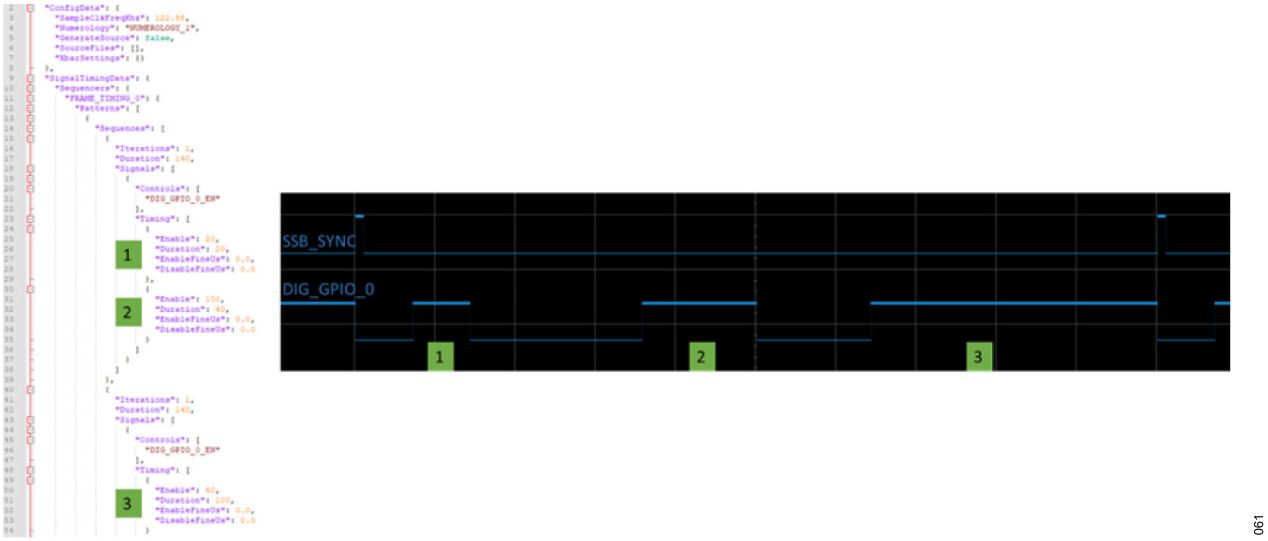


Figure 59. Example of Radio Sequencer Timing Configuration

To create a timing definition, the procedure is as follows as shown in Figure 61:

1. In the **Sequencer Select** dropdown menu, select the sequencer to which the configuration is applied.
2. In the **Number of Sequences** and **Number of Patterns** dropdown menus, select the number of sequences and patterns for the configuration.
3. In the **Sequencer Pattern** and **Pattern Sequence** dropdown menus, select the sequence and pattern index to which the inputs apply.
4. In the **Select Timing Definitions** dropdown menu, select the number of timing definitions that is created for that pattern.
5. Add the desired timing definition values into the input boxes as shown in Figure 60.
    a. Timing enable. Select the symbol index at which the signal enable starts.
    b. Timing duration. Select how many symbols the enable signal lasts.
    c. Timing enable fine. Delay in µs to apply before the signal is enabled after the starting symbol.
    d. Timing disable fine. Delay in µs to apply before the signal is disabled after the last symbol.
6. Select the signals that are controlled by the selected sequencer in the **Signals** section as shown in Figure 60.
7. Apply the current configuration by selecting **Apply Sequencer Settings**. This updates the view in the **Settings Preview** screen with the new configuration.

RUNTIME

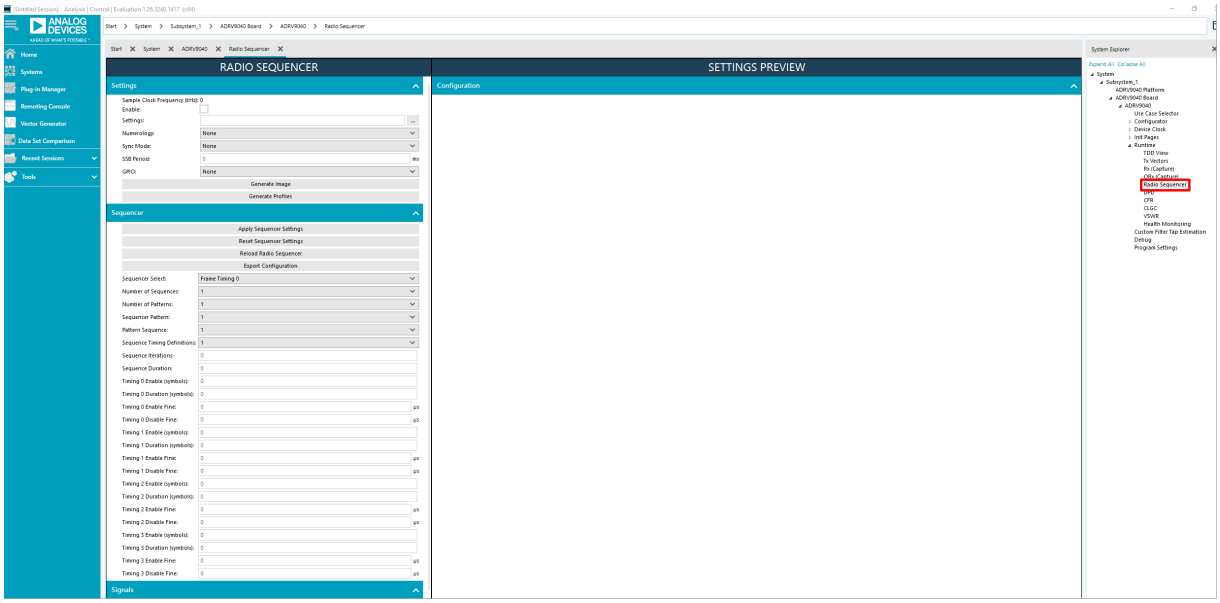


Figure 60. Radio Sequencer Timing Settings

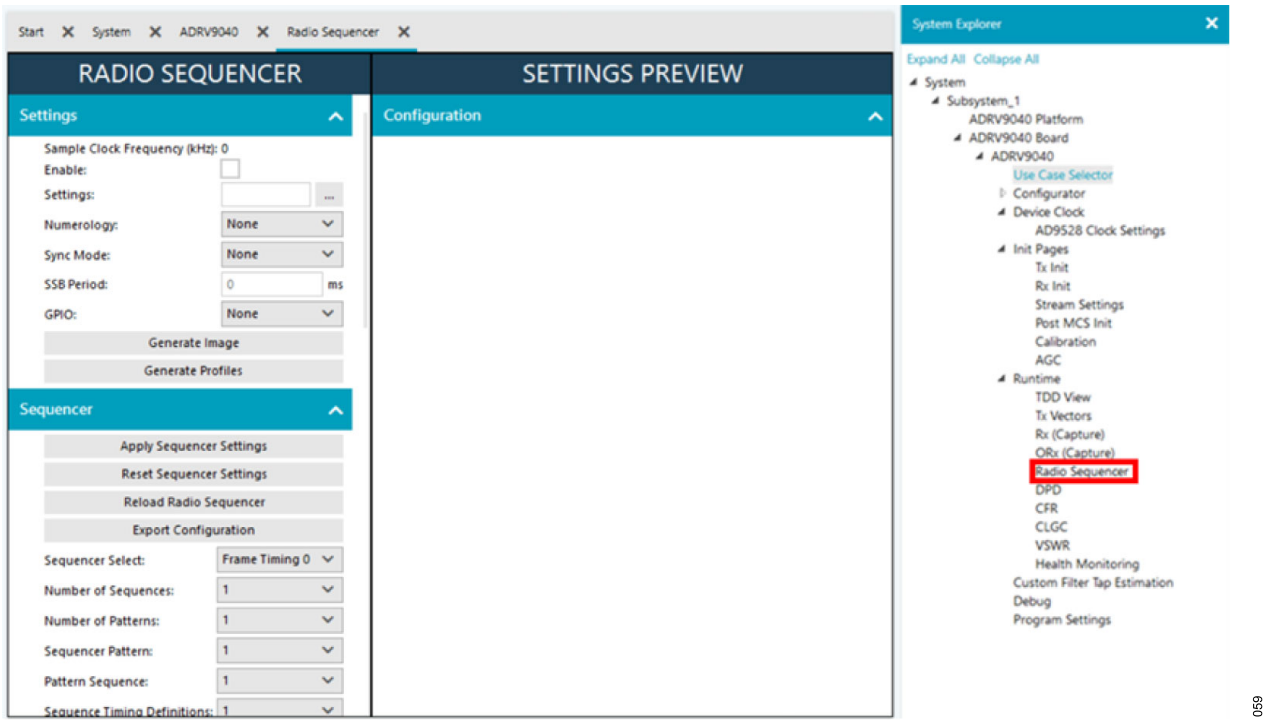


Figure 61. Radio Sequencer Tab

A new pattern or sequencer can be selected to create a new configuration. After clicking on the **Apply Sequencer Settings**, the new configuration is merged with the previous configuration, which allows the creation of multiple sequencers and patterns in sequence. The current configuration can be deleted and restarted by clicking on **Reset Sequencer Settings**.

Once the configuration is created, if the ADRV904x is already programmed with a user case, the **Radio Sequencer** can be loaded by first selecting **Generate Image** to create the binary file and then selecting **Reload Radio Sequencer** to load the same binary.

Export Configuration is used to store the configuration in a file, and review and load at initialization by selecting it in **Settings** before programming the part.

RUNTIME

TDD VIEW

This section explains the setup TDD timings for each TRX_CTRL pin configured during post MCS init. The procedure is as follows:

1. Enter start and stop times to specify a time range for driving each TRX_CTRL pin. Four start and stop time ranges can be specified per pin. LTE presets can also be applied to each CTRL pin from under **LTE Presets**. Figure 62 applies **4G LTE 0 (Tx)** preset to **TRXA_CTRL LTE** and **4G LTE 0 (Rx)** preset to **TRXB_CTRL LTE**.
2. Click **Apply** to plot the TDD timings for review. This only updates the plot, but it does not enable TDD.
3. Click **Configure** to configure the TDD state machine using the specified timings. This enables the TDD state machine (the **Enable TDD FSM** checkbox). To perform data sourcing and capture in TDD mode, the user must additionally modify capture settings on the **Runtime** pages, as illustrated in Figure 63 .

Delay Settings on the **TDD View** page can be used to add delays per JESD link between the enable inputs and data outputs.

Miscellaneous settings can be used to loop the TDD frame timings continuously.

TDD can be disabled by unselecting the **Enable TDD FSM** checckbox. Note that clicking **Configure** is not required for disabling TDD FSM as **Configure** reselects the **Enable TDD FSM** checkbox.

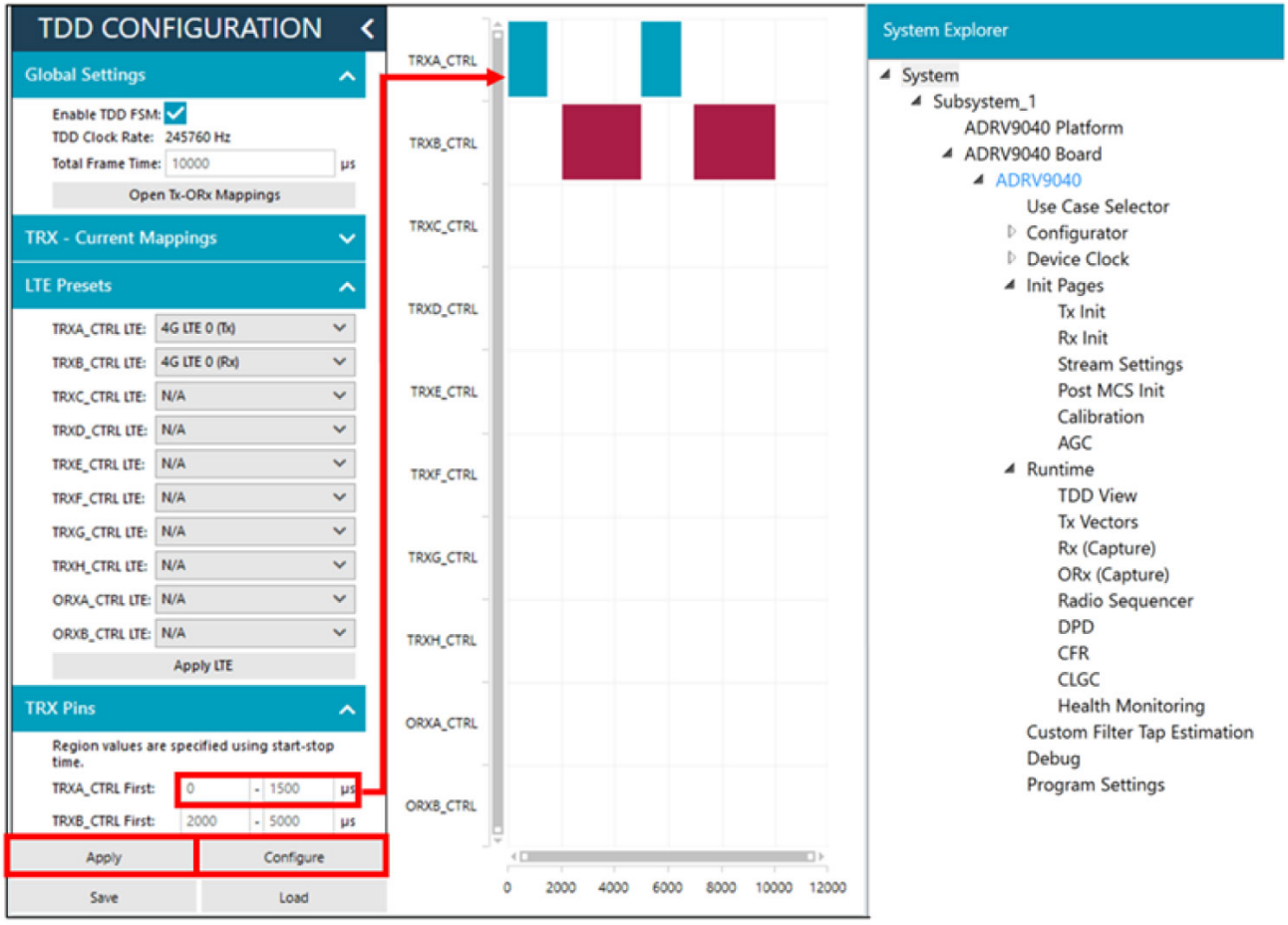


Figure 62. TDD Configuration Page Used to Specify Enable Timings for Each CTRL Pin and Configure the TDD State Machine

RUNTIME

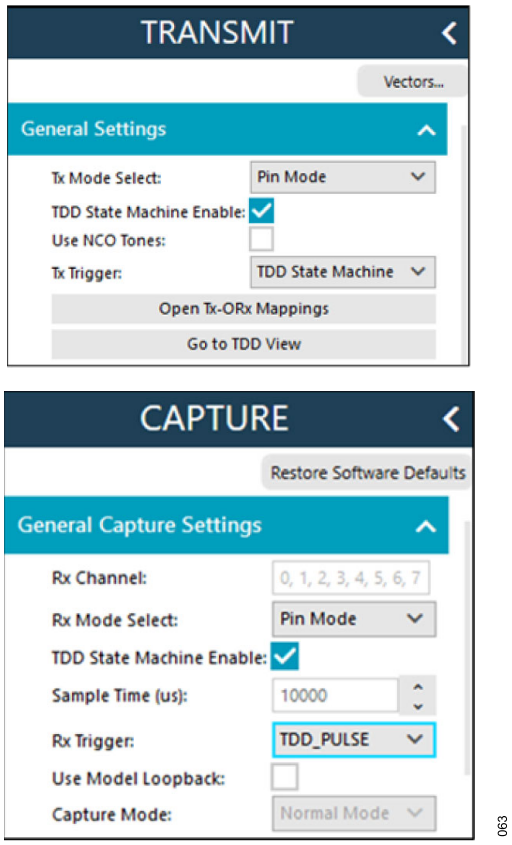


Figure 63. Runtime Pages Updated to Trigger Data Source and Capture Using the TDD State Machine for Rx

FFT ANALYSIS

On the **Rx (Capture)** and **ORx (Capture)** pages (see Figure 56 and Figure 57), each provides data analysis tab that allows the user to manipulate the FFT calculations to best fit their requirements. The user can configure FFT analysis settings, manipulate FFT durations, and perform simple spur analysis. On both **Rx (Capture)** and **ORx (Capture)** pages, the **Analysis** tab provides information about the received signal. This tab is directly related to the **Results** tab, such that the selections determine the information presented to the user.

Analysis Settings

The user can select the preference of how results of the FFT analysis is generated, and determine what is presented on the **Results** tab. The following are the key options available to the user:

- Select preference tones power measurements in dBc or dBFS.
- Selection specifies a 1- or 2-tone analysis for information on harmonics or intermodulation.
- Options for strategy used to find the fundamental tones, such as the following:
  - Highest bin.
  - Mirror image.
  - Fixed.
- Selection for type of windowing used in FFT spectrum generation, such as the following:
  - Blackman Harris 4 (default).
  - Blackman Harris 7.
  - Blackman Harris 7 scaled.
  - Hann.
  - None.

RUNTIME

- Specify number of harmonics reported, such as the following:
  - Harmonics. Single tone analysis.
  - Intermodulations. Two tone analysis.
- Specify number of bins used during the FFT analysis power calculations for the following:
  - Fundamental tones.
  - DC component.
  - Worst other (spurs).

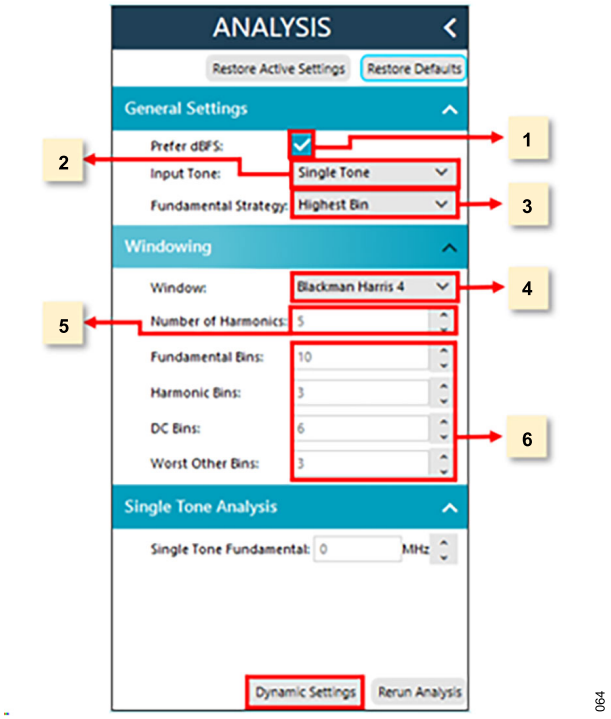


Figure 64. Analysis Tab with Default Parameters

FFT Ranges

For some operations, the user does not need the FTT analysis to cover the full capture duration, especially during TDD operations where the duration of capture is much larger than the duration of the desired signal. The rest of this section explains how to use this feature through the framework of a TDD operation outlined in Figure 65. For this example, the Tx0 and Tx4 outputs tones of 10 MHz and 30 MHz delta from LO, respectively. The two transmitters are then combined using a splitter and the resulting signal is sent into another splitter, which is then fed to ORx0 and Rx1.

RUNTIME

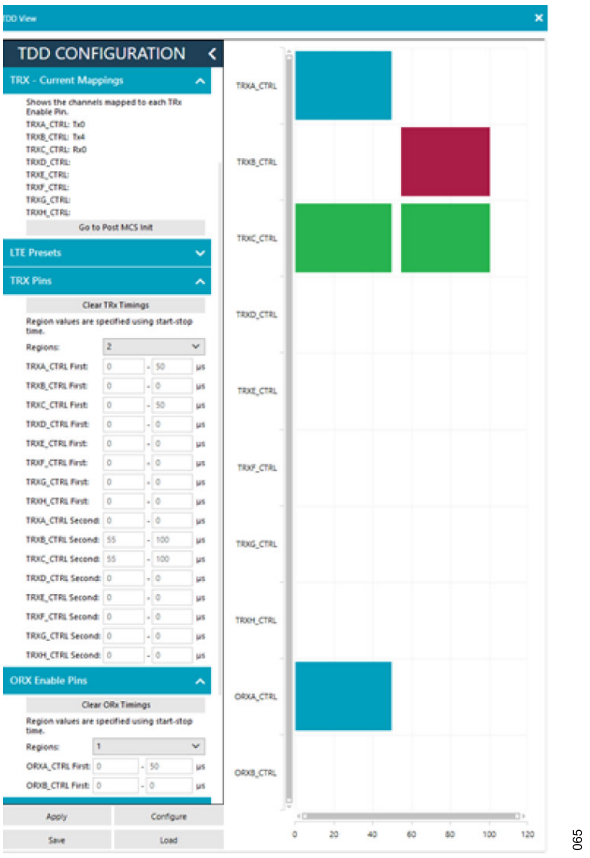


Figure 65. Example TDD Configuration to Demonstrate Dynamic FFT Duration Feature

Adding an FFT Range

On the **ORx (Capture)** page with a capture period equal to the TDD frame of 100 µs, a regular capture does not produce a true FFT representation of the signal received during the slot seen in Figure 66. Therefore, it is essential to use the FFT duration feature available though the **Dynamic Settings** available on the **Analysis** tab as shown in Figure 64.

Upon clicking the **Dynamic Settings**, a pop-up window, as shown in Figure 67, appears. To add an FFT range, take the following steps:

1. Click on **+** to create an instance of the FFT range.
2. Select the appropriate channel.
3. Set the starting sample index in reference to the capture period.
4. Set the number of samples used for analysis.

Take note of the following:

- All numerical inputs involved with adding an FFT range is in terms of samples.
- The start index and max sample count define the range of the FFT analysis.
- For each channel, only one FFT range is allowed.
- Each FFT range addition or update must be followed by clicking on **Rerun Analysis** on the **Analysis** tab.

RUNTIME

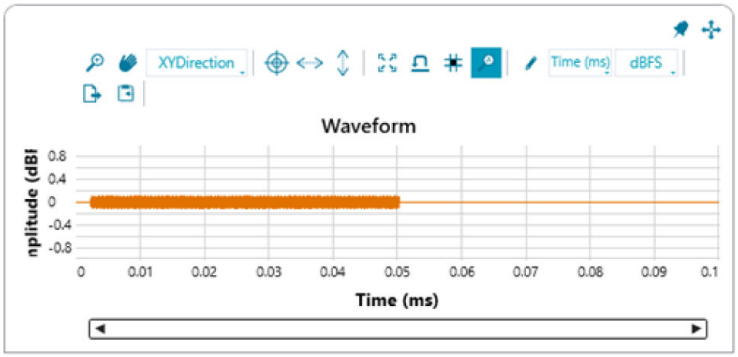


Figure 66. ORx Capture for FFT Duration Example

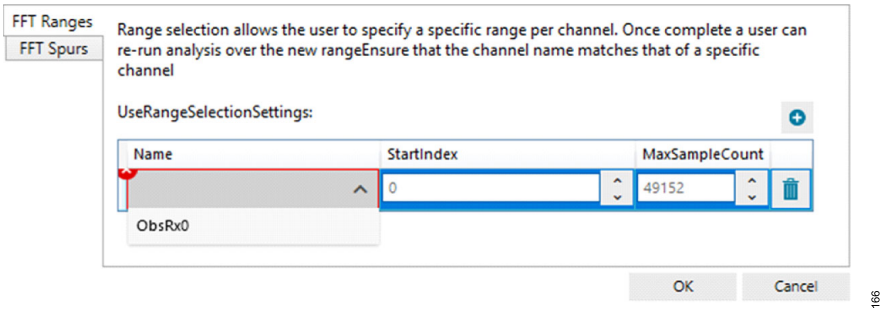


Figure 67. FFT Range Settings Window

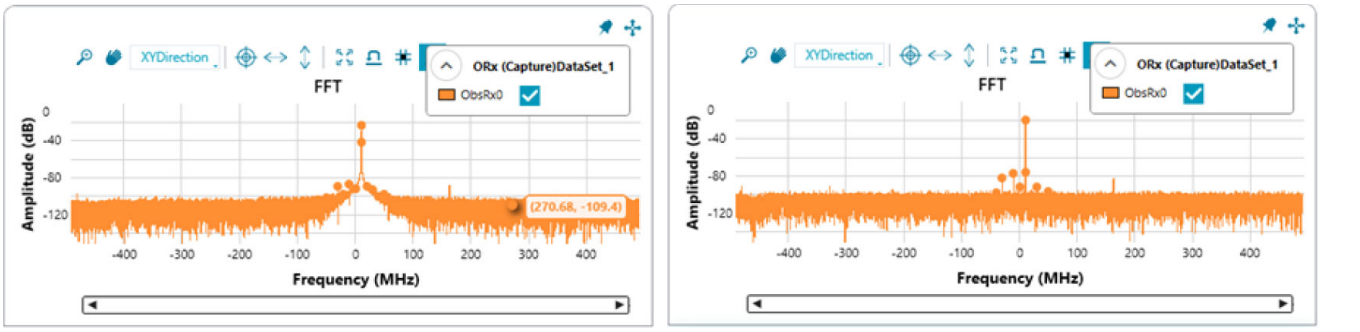


Figure 68. ORx Capture FFT Plot Before and After Applying FFT Range

Inserting Spur

The user can perform simple spur analysis by inserting spurs to track the power measurements of a specific spur. This feature can be accessed through the **Dynamic Settings** as shown in Figure 64. The following outlines the use of this feature.

For this demonstration, the ORx is used to capture a 20 MHz tone. Because of the direct conversion from the RF, there is a significant spur at approximately 153 MHz. The following steps are recommended for adding a spur:

1. Upon clicking the **Dynamic Settings**, a pop-up window appears.
2. Navigate to the **FFT Spurs** tab. From there, a window as shown in Figure 69 appears.
3. Set the following parameters:
    a. Prove a **Name** for administrative purposes.
    b. Set **Frequency** in MHz.
    c. Set spur **SingleSideBand** (SSB).

RUNTIME

d. Select **Units** of SSB.
e. Specify whether spur is considered in noise calculations.
f. Enable or disable spur.

4. Click **OK** followed by clicking **Rerun Analysis** on the **Analysis** tab.

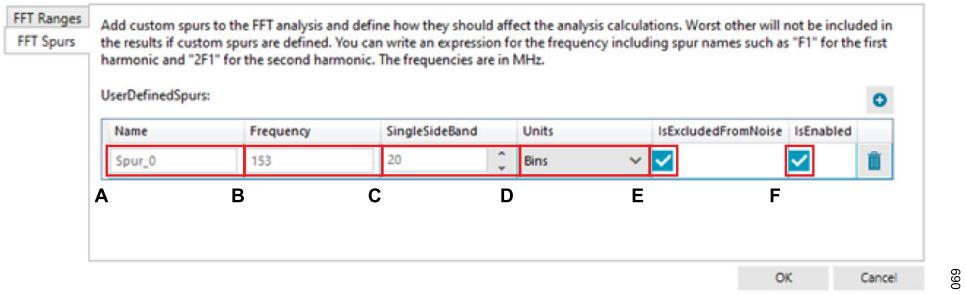
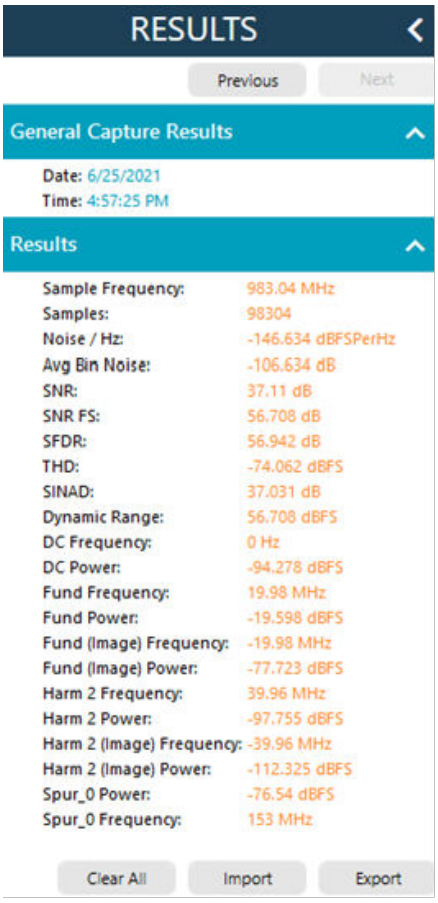
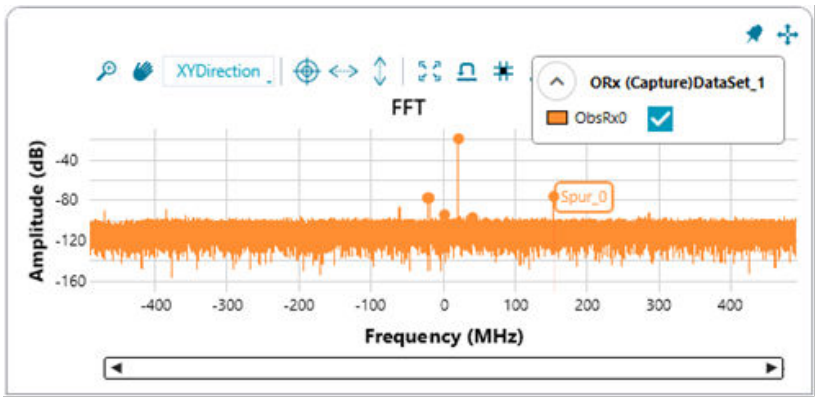


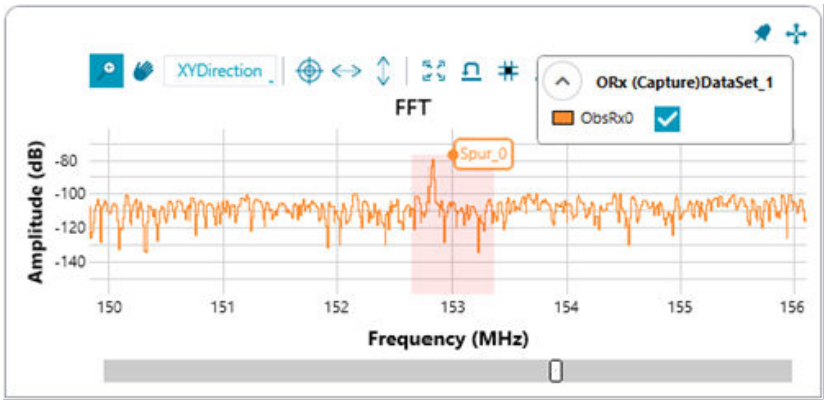
Figure 69. FFT Spur Configuration Window



(A) RESULTS TAB WITH INSERTED SPUR



(B) FFT PLOT WITH INSERTED SPUR



(C) FFT PLOT ZOOMED ONTO INSERTED SPUR

070

Figure 70. Results and FFT Plot After Spur Inserted at 153 MHz

Exporting Captured Data

This section seeks to explain the feature of exporting captured data. The user can perform non native measurements or operations on the received signal. Found on both the **Rx (Capture)** and **ORx (Capture)** pages, the **Results** tab provides the ability to export data via the **Export** button as shown in Figure 71. The process is as follows:

RUNTIME

1. Upon clicking **Export**, a pop-up window prompts the user to the save an XML file.
   - Note that the name of the file is the base name of the generated files in CSV format.
   - Default naming convention is [CapturePage]DataSet_#_DDMonthYYY_HH_MM_SS.
   - Default path follows as **C:\Users\$UserFolder$\AppData\Local\Analog Devices\ACE\ExportData\ADRV9040**.
2. The total number of additional files generated depends on the number active channels during the capture.
   - Key files and brief descriptions.
     - FFT. File with FFT plot data with additional summary information.
     - Raw sample. Raw data in an interleaving format of I and Q samples. Each column corresponds to a different channel. This file is used for importing data to the **Results** tab.
     - Waveform. File with waveform plot data with additional summary data.
       - Samples are interleaved by I and Q samples.
       - Multiple waveform files are generated depending on number of active channels during capture.
       - File name follows as [CapturePage]DataSet_#_waveform_[Channel]_ DDMonthYYY_HH_MM_SS.

Figure 71. ORx (Capture) Page Results Tab with Plots

DPD

Hardware Prerequisites

To evaluate DPD, ensure that a gain line up is connected to the transceiver similar to Figure 72. Tune the power levels appropriately to ensure that the observation receiver is not saturating. Once the gain line up is connected, proceed to transmit data in TDD/FDD mode as described in the Transmitter Vectors section and verify the output on a spectrum analyzer.

For an FDD use case, the TDD flag needs to be set to false from the profile/use case and it must be true in case of TDD.

Ensure that the power amplifier (PA) is turned off while programming the device to avoid damages from high-power tones transmitted by ADRV904x calculations.

RUNTIME

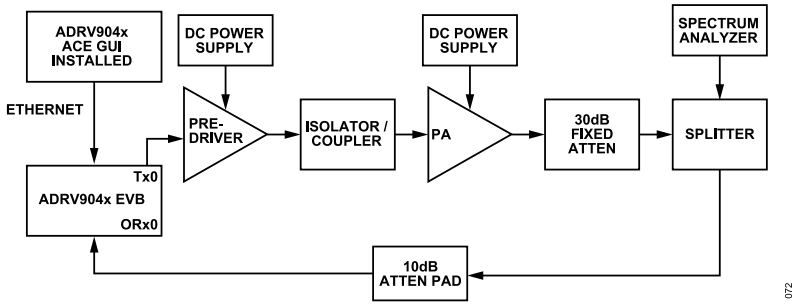


Figure 72. Hardware Connections for Evaluating DPD

Once the transmit data is verified, proceed to check that the ORx data is correct following the instructions described in the ORx (Capture) section.

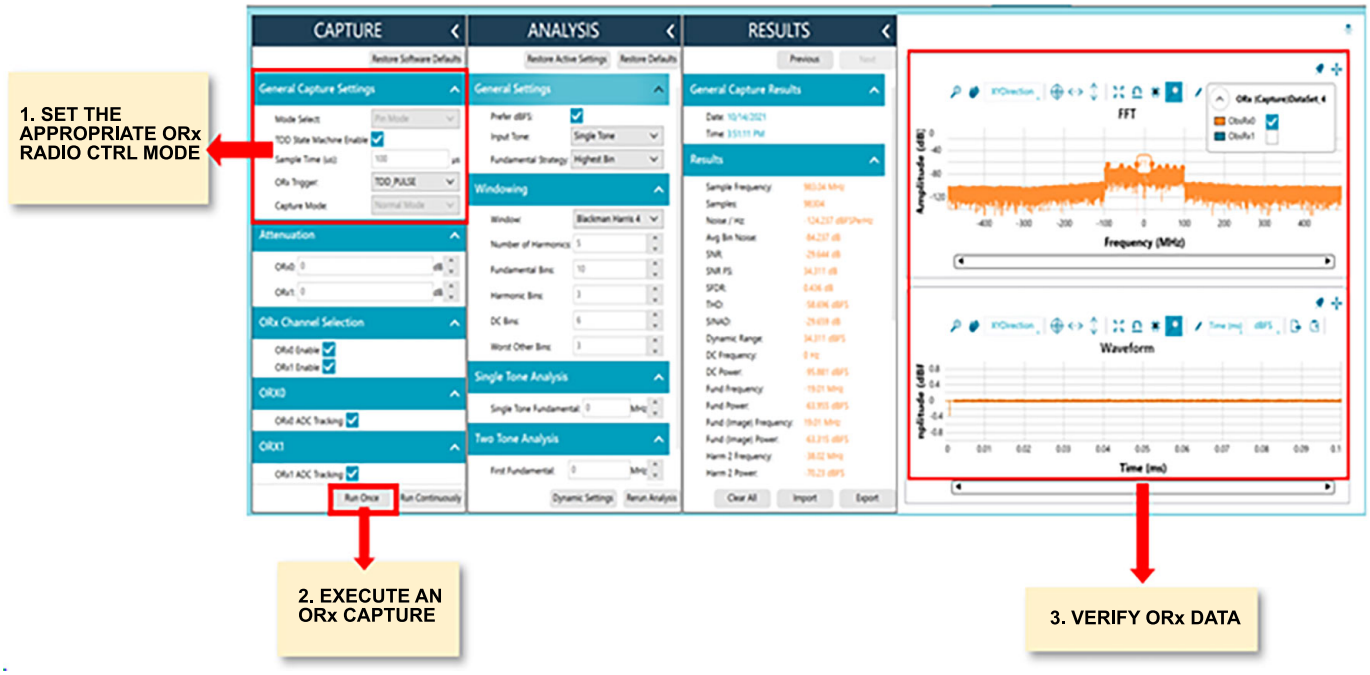


Figure 73. Verify the ORx Data for DPD

Following successful verification of the ORx data, proceed to DPD configuration and enable DPD tracking in the **DPD** window under the **Runtime** page as shown in Figure 74.

RUNTIME

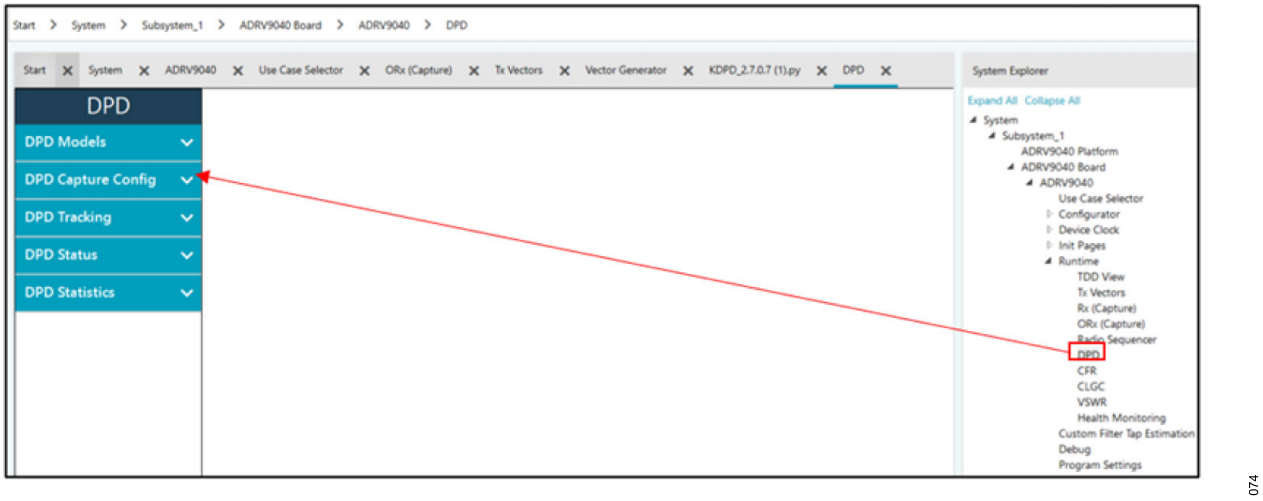


Figure 74. DPD Configuration Window

Proceed to load the DPD model as shown in Figure 75. The DPD model configuration is included as a metadata at the top of the DPD model file. The DPD model library is part of the software package.

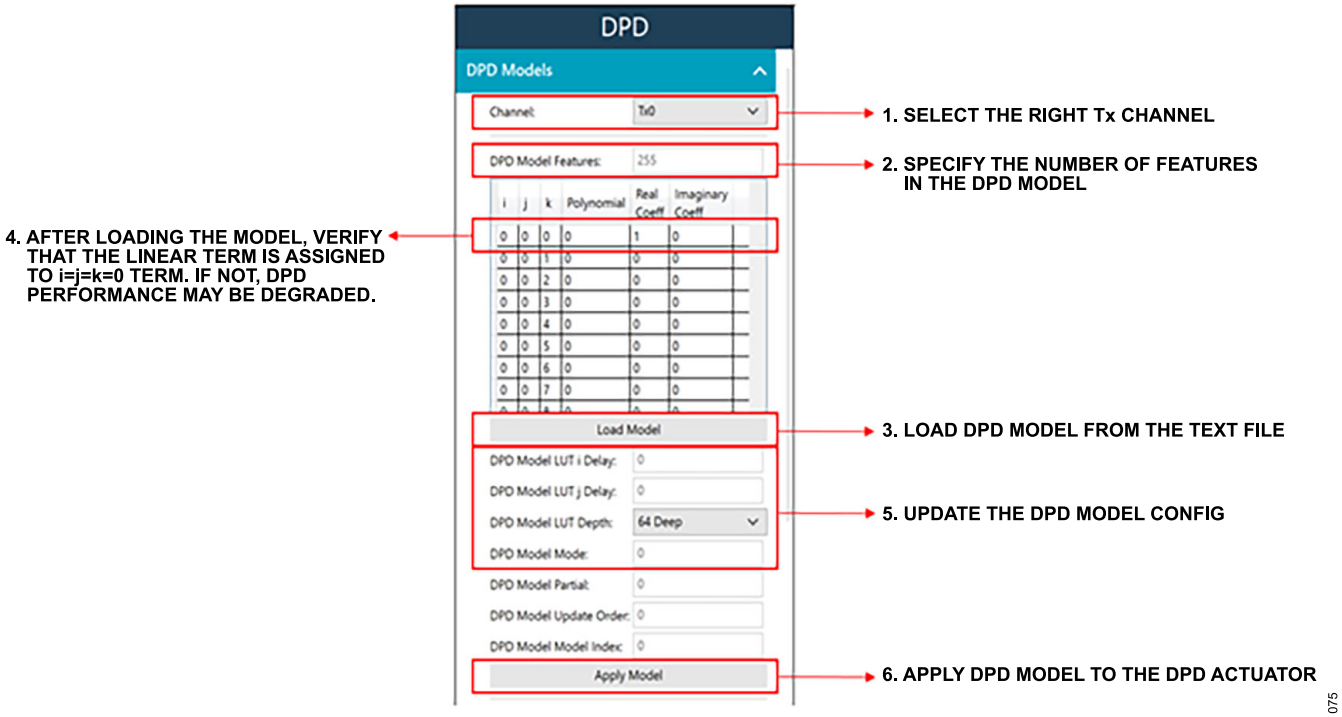


Figure 75. DPD Model Loading User Interface

Select the DPD capture configuration as shown in Figure 76.

RUNTIME

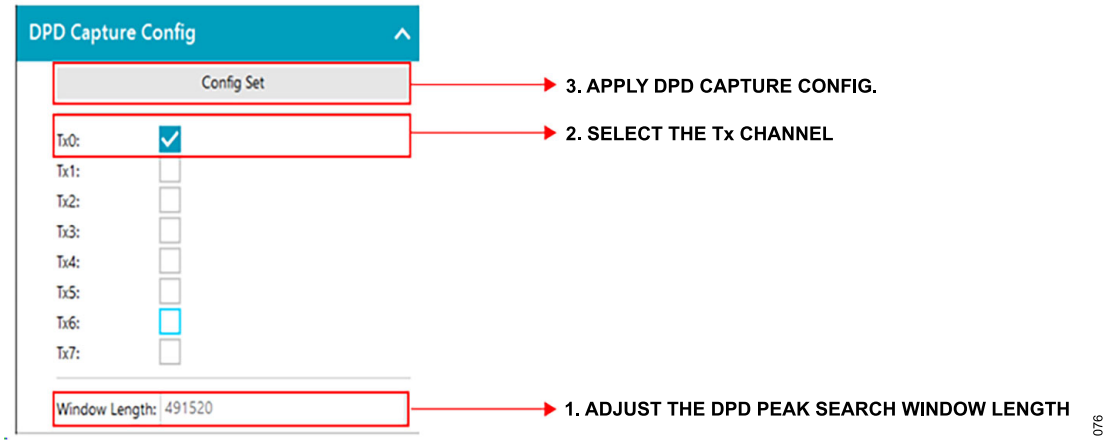


Figure 76. DPD Capture Configuration User Interface

Adjust the DPD tracking configuration and enable the DPD tracking calibration on the appropriate Tx channel.

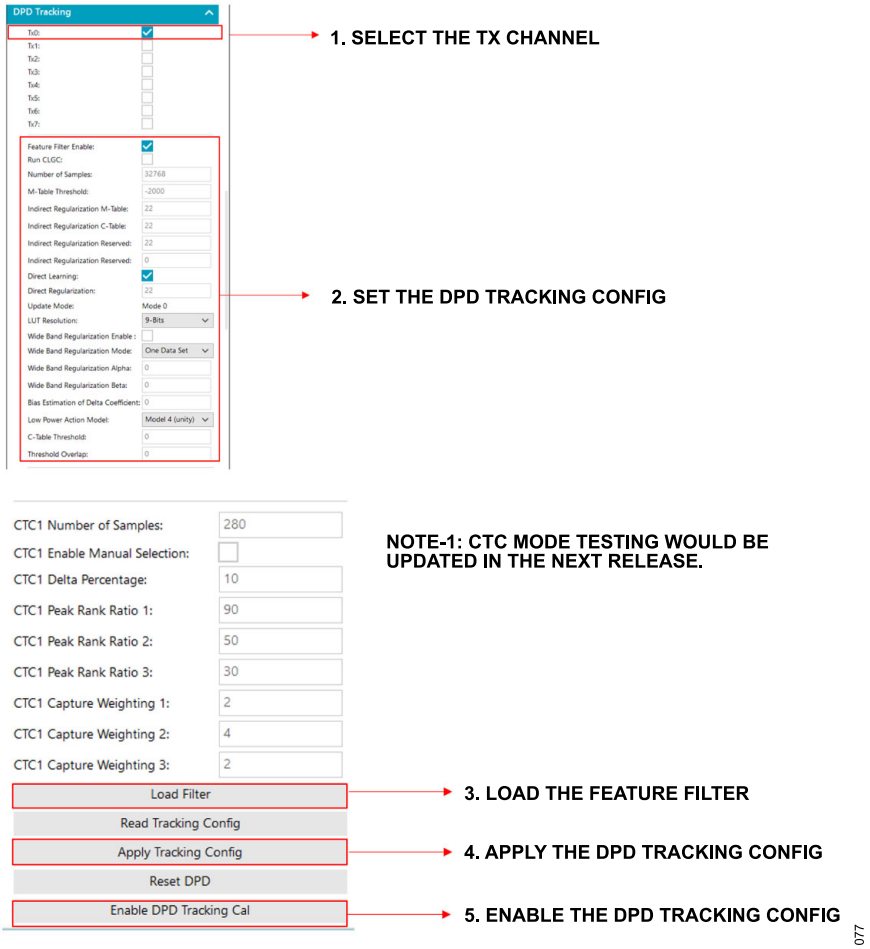


Figure 77. DPD Tracking Configuration User Interface

After the DPD tracking calibration is enabled, verify the adjacent channel leakage ratio (ACLR) correction on the spectrum analyzer. Monitor the DPD status to ensure that the DPD update counts are incrementing and that there is no error as shown in Figure 78.

RUNTIME

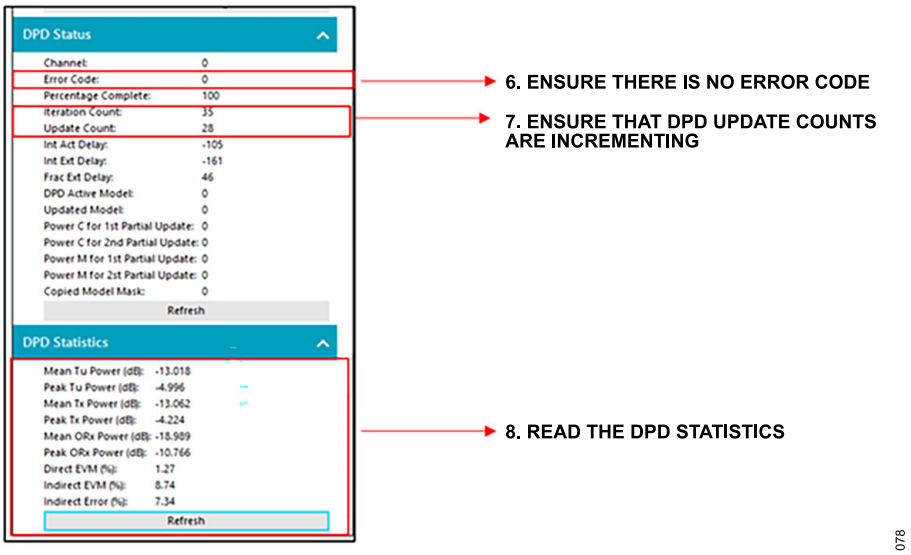


Figure 78. DPD Status User Interface

Support for DPD charge trap correction (CTC) mode is in an upcoming software release.

CFR

CFR Block on the Runtime: Step 0

The **CFR** block is under **Runtime**. When clicked, **CFR Configuration**, **Channel Configuration**, and **CFR Statistics** are displayed as shown in Figure 79.

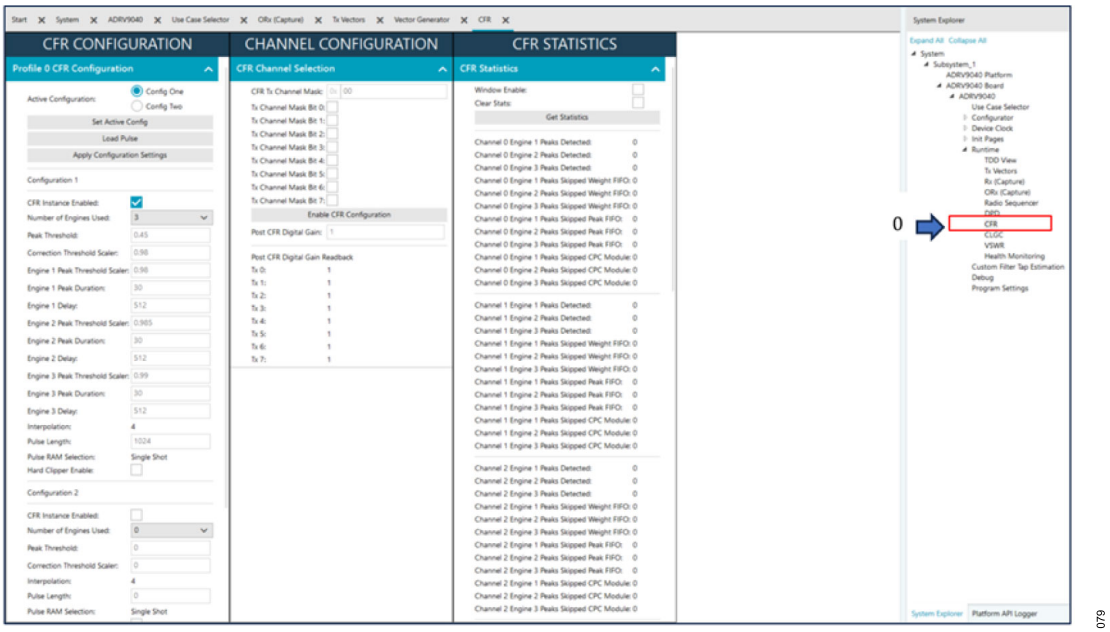


Figure 79. CFR Block in Runtime

Transmitter Channel Configuration: Step 1

First, the transmitter channel needs to be selected so that the CFR function is added to the selected transmitter channel. In Figure 80, one channel, **Tx Channel Mask Bit 0**, is selected.

RUNTIME

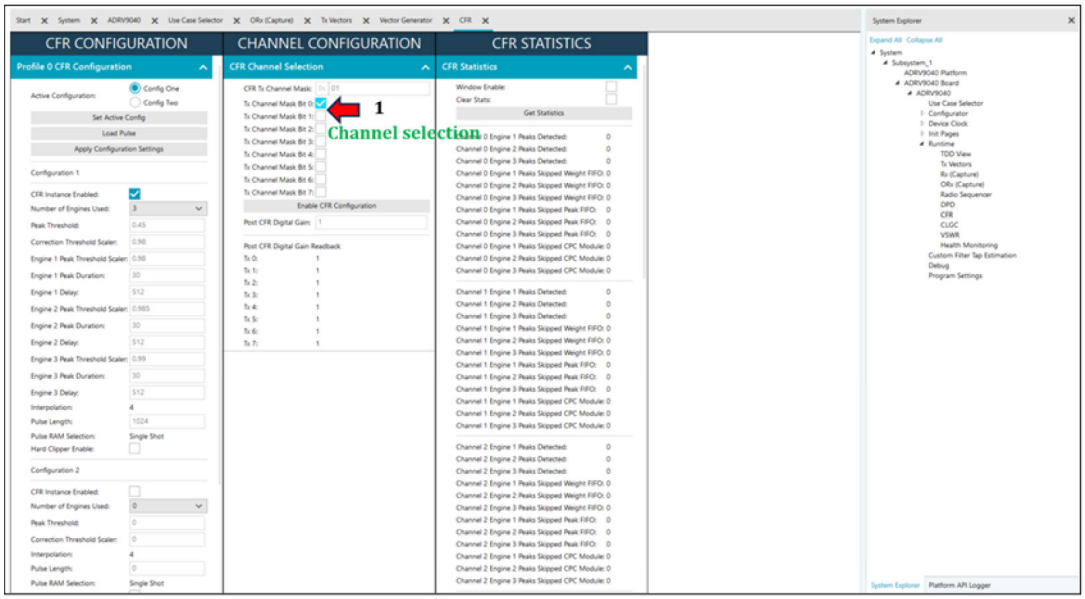


Figure 80. Tx Channel Selection for Adding CFR Block

Inactive Configuration 1 and Active Configuration 2: Step 2 and Step 3

To set **Config One**, set it to inactive for it not to impair the transmitter channel when the CFR correction pulse and parameters are loaded to the inactive **Configuration 1**.

Once **Config Two** is active, the configuration is ready to be updated with the CFR correction pulse and CFR parameters as shown in Figure 81 and Figure 82.

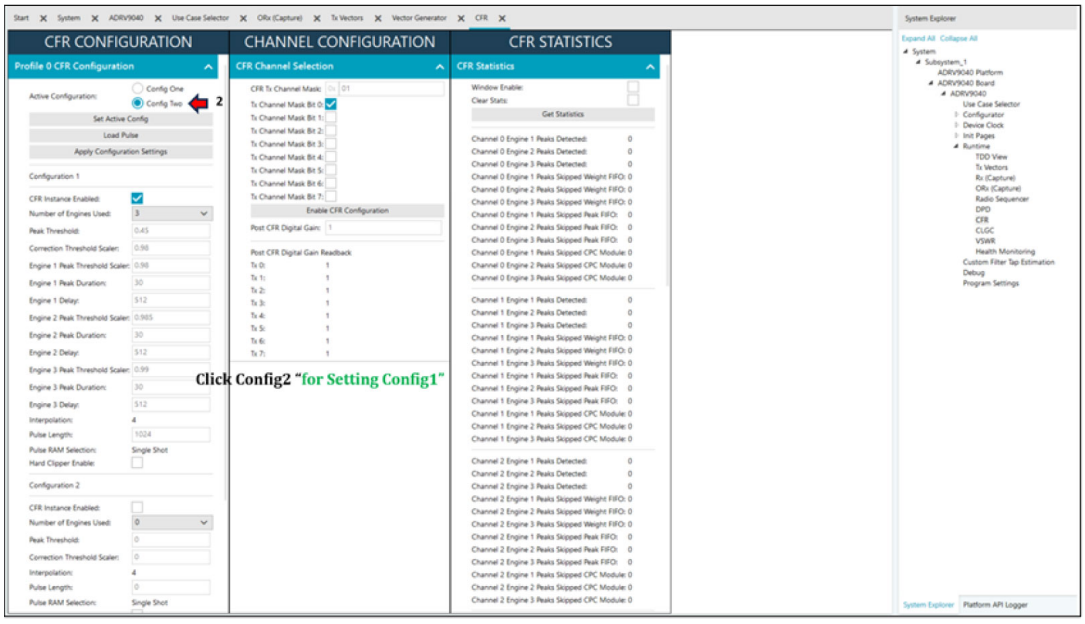


Figure 81. Inactive Config One, Active Config Two: Step 2

RUNTIME

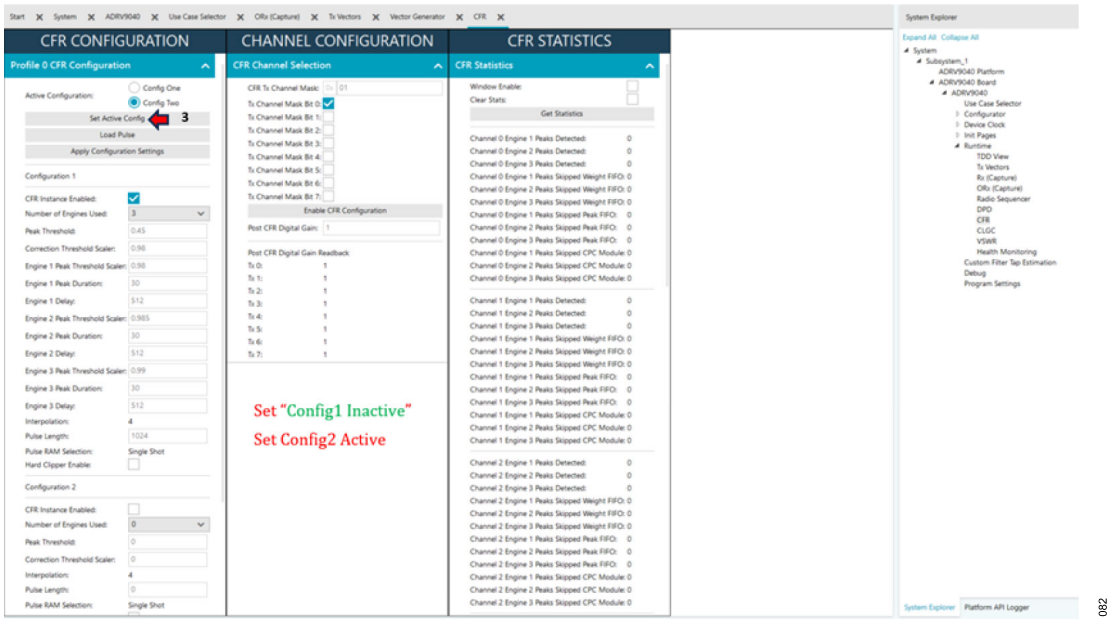


Figure 82. Inactive Config One, Activate Config Two: Step 3

Loading CFR Correction Pulse: Step 4

To upload the CFR correction pulse, click on the **Load Pulse** button as shown in Figure 83.

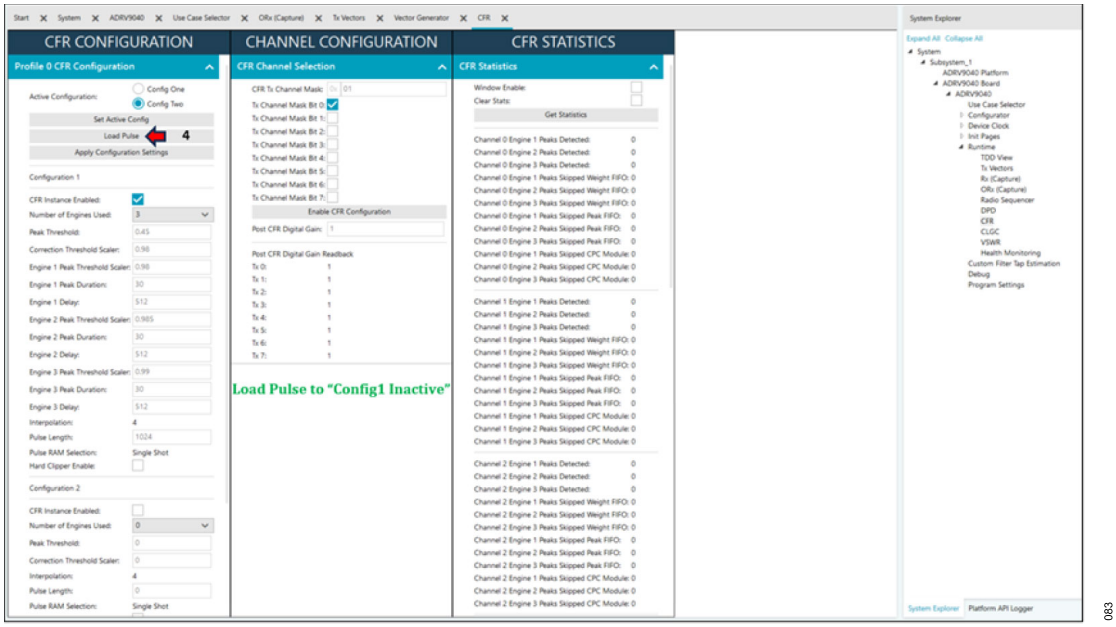


Figure 83. Loading CFR Correction Pulse of Configuration 1: Step 4

Once selected, the directory and CFR correction pulse location are shown as in Figure 84, assuming the CFR correction pulse exists.

RUNTIME

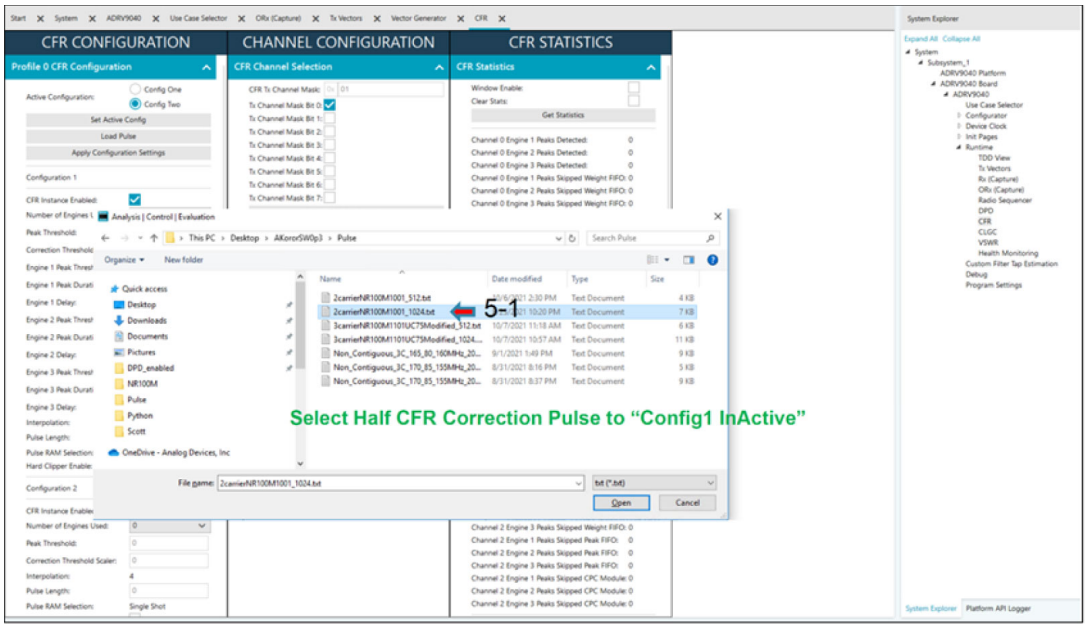


Figure 84. Loading CFR Correction Pulse of Configuration 1: Step 5-1

Once the CFR correction pulse is loaded correctly, a message displays as shown in Figure 85

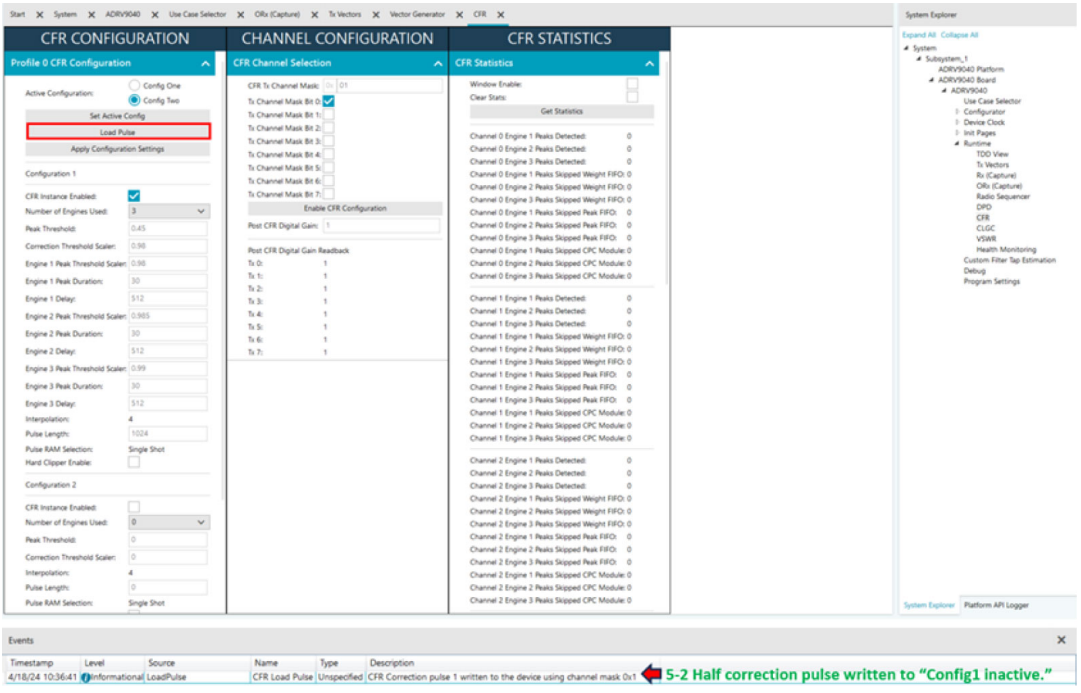


Figure 85. Loading CFR Correction Pulse of Configuration 1: Step 5-2

Setting CFR Parameters

All CFR parameters can be placed, which depend on the target peak to average ratio (PAR) and the RMS crest factor reduction (CFR) input power. The current **Peak Threshold** 0.3814 is calculated based on the two inputs, namely PAR at 8.0 dB and CFR input at −16.3 dBFS.

RUNTIME

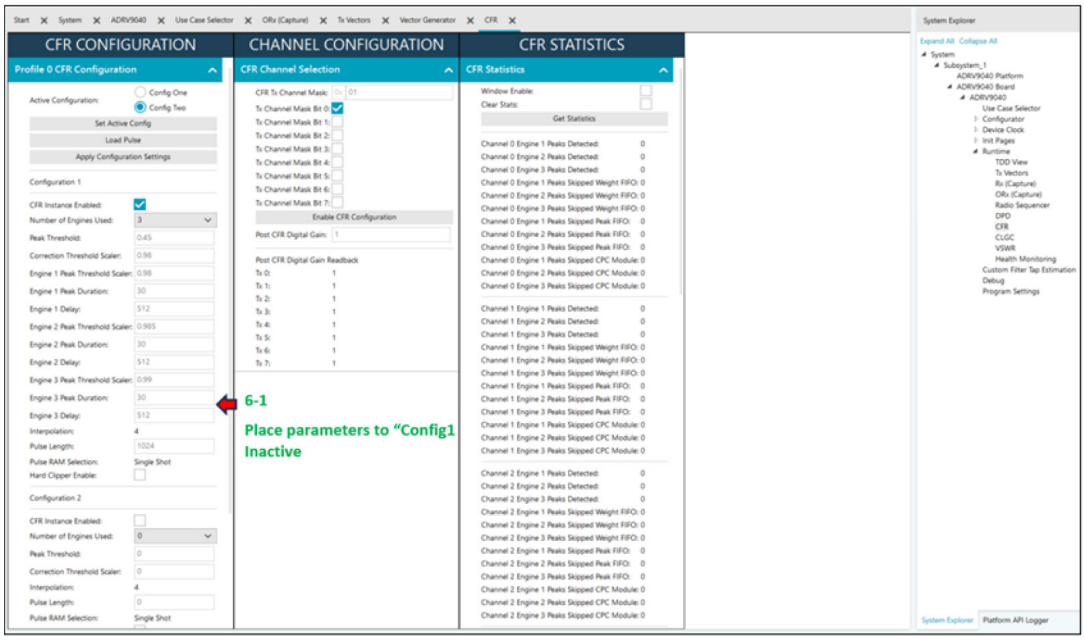


Figure 86. Setting CFR Parameters of Configuration 1, Step 6-1

Once all required parameters are set, click on **Apply Configuration Settings** as shown in Figure 87. Once the parameters are loaded to the inactive **Configuration 1**, the event message is shown as in Figure 87.

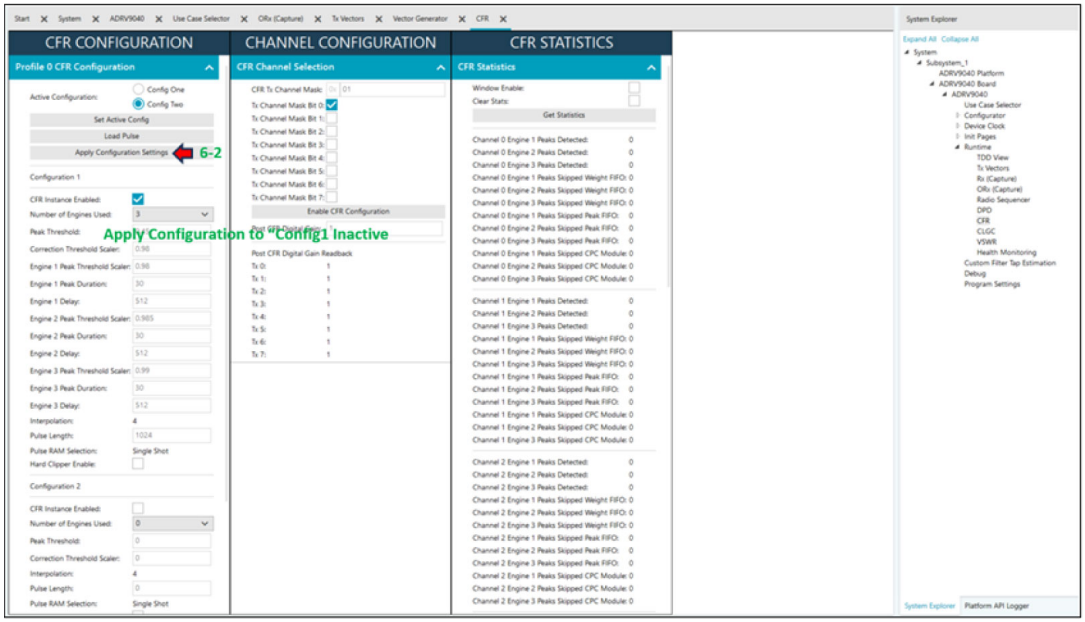


Figure 87. Apply Configuration 1 Settings: Step 6-2 and Step 6-3

Next, both CFR correction pulse and CFR configuration parameter of **Configuration 1** must be enabled by clicking on **Enable CFR Configuration**. The event message as shown in Figure 88 confirms that **Configuration 1** (inactive) is loaded.

RUNTIME

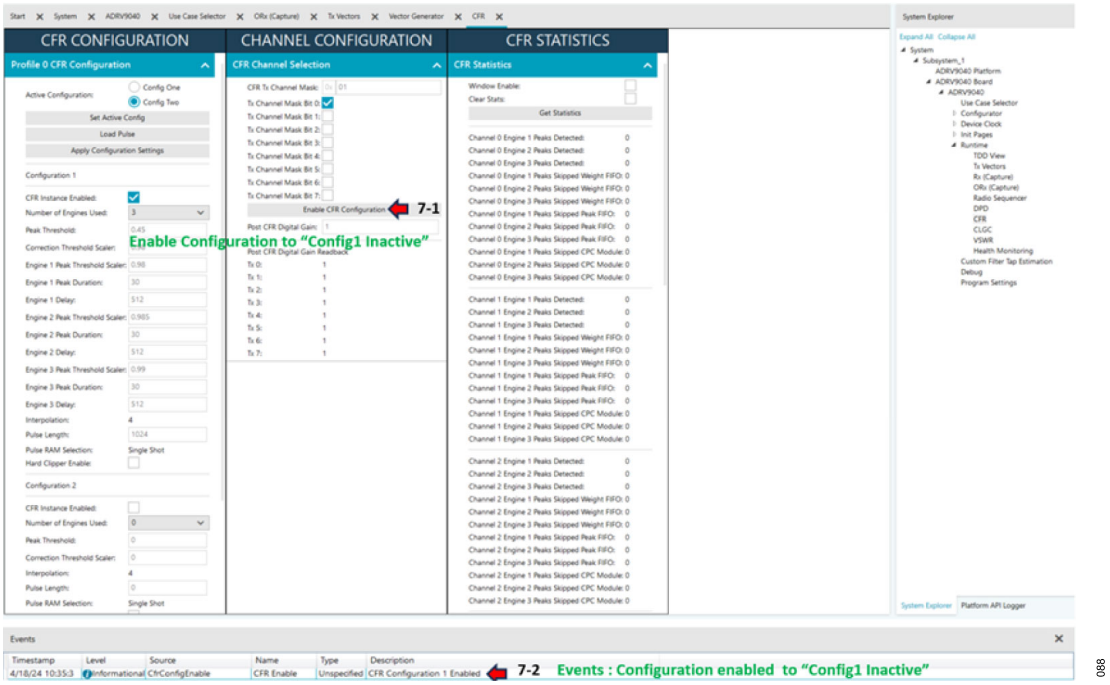


Figure 88. Enable CFR Configuration 1: Step 7-1 and Step 7-2

Lastly, click on **Config One** and then **Set Active Config** as shown in Figure 89.

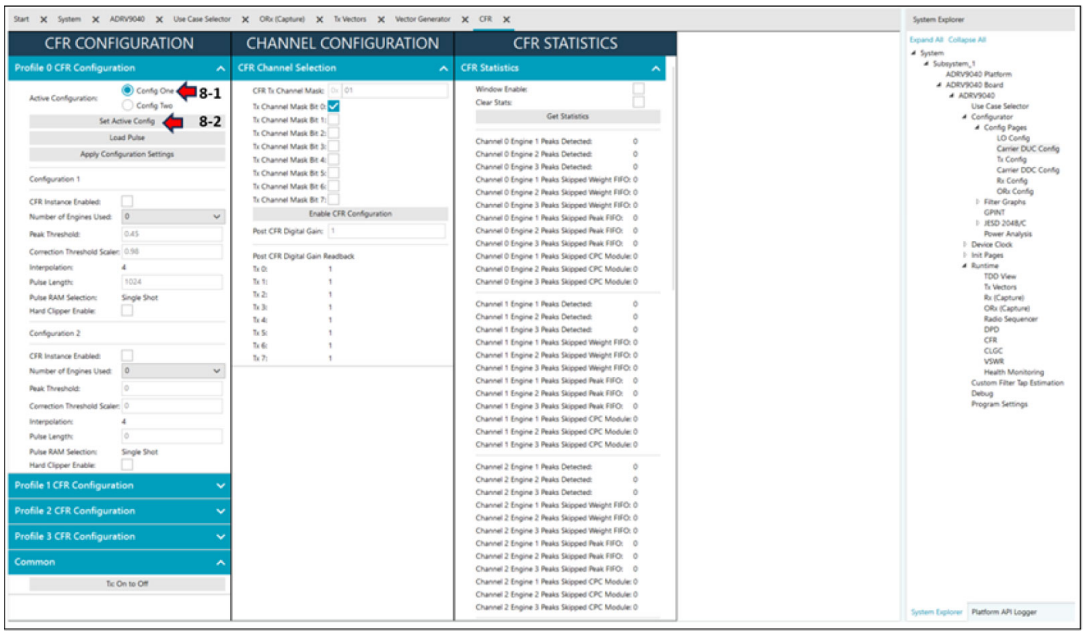


Figure 89. Activate CFR Configuration 1: Step 8-1 and Step 8-2

Before **Config One** is enabled, check that the original ACLR and Gaussian complementary cumulative distribution function (CCDF) of spectrum analyzer are confirmed. After CFR **Config One** is enabled, it is observed that ACLR is by 0.1 dB degraded and PAR is reduced to 8.10 dB at 0.01% from 9.65 dB at 0.01% as shown in Figure 91.

RUNTIME

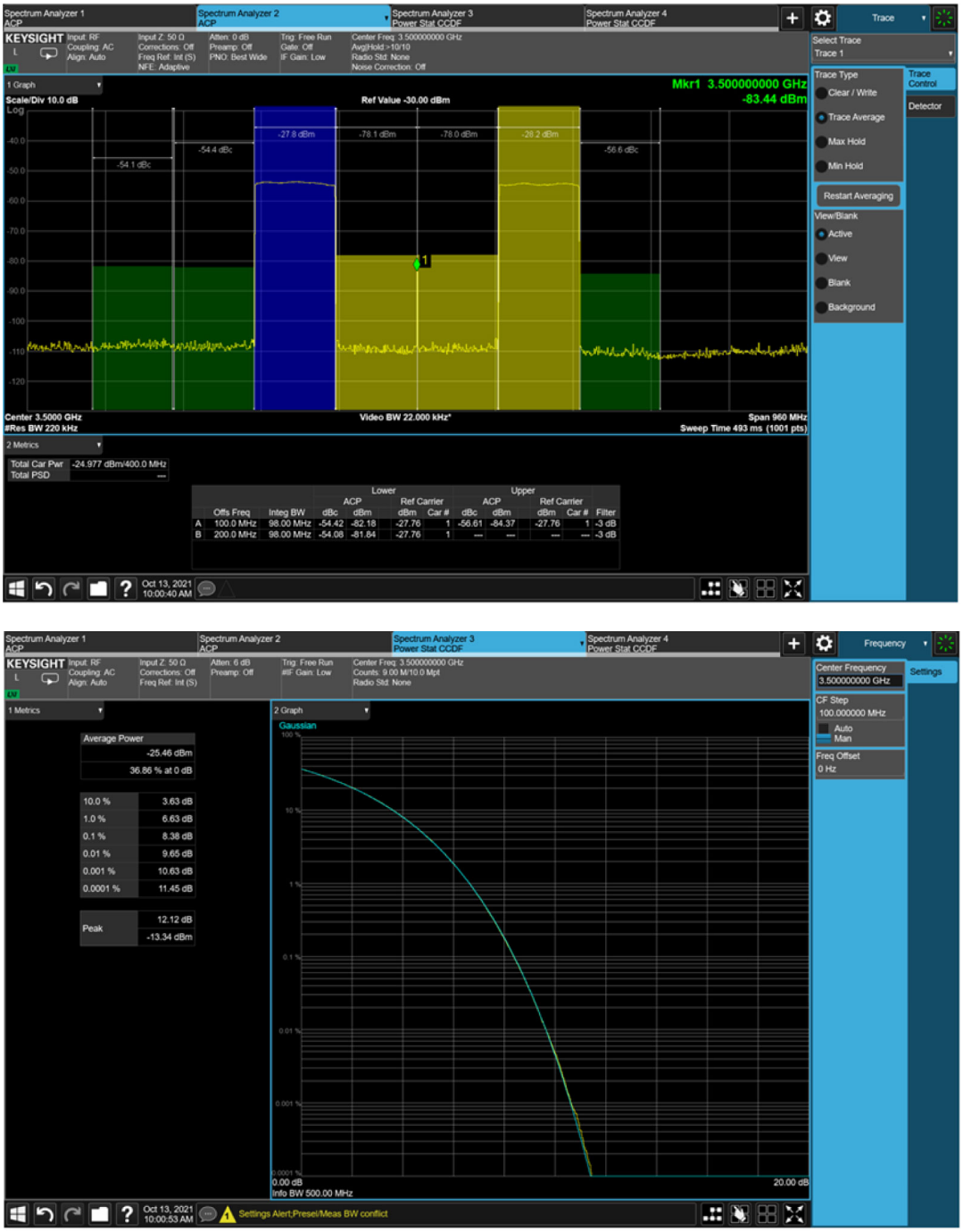


Figure 90. Initial CFR Configuration 1: ACPR and CCDF

RUNTIME

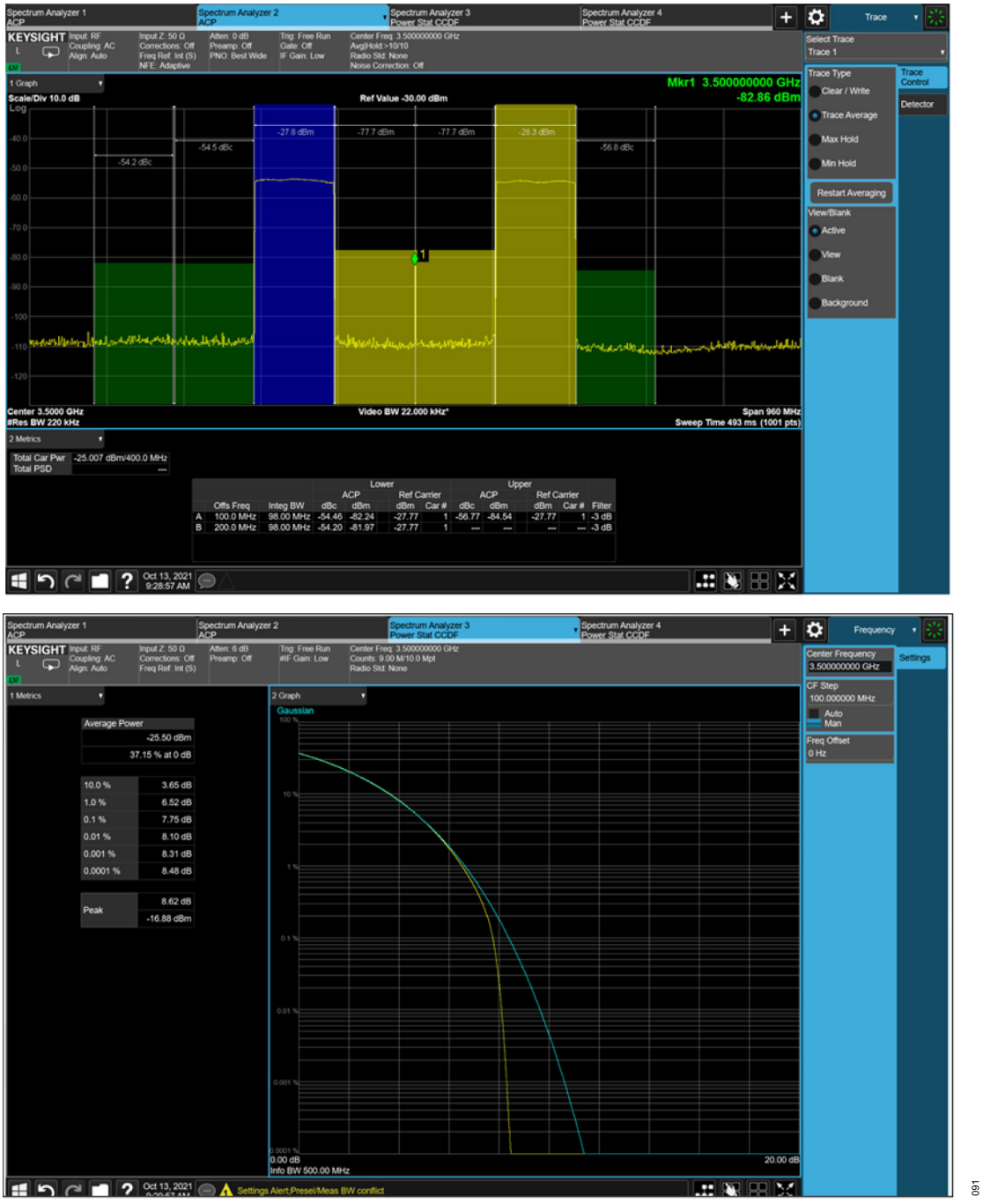


Figure 91. After Enabling Set CFR Configuration 1: ACPR and CCDF

Using statistics in the GUI, check that there is no peak skipping with **Configuration 1**. Before clicking on **Get Statistics**, **Window Size** needs to be filled with the range 15 as shown in Figure 92. It can be executed by clicking on **Get Statistics** to get the CFR statistics. As shown in Figure 93, the peaks of signals over the three engines are detected but no peak skipping is observed.

RUNTIME

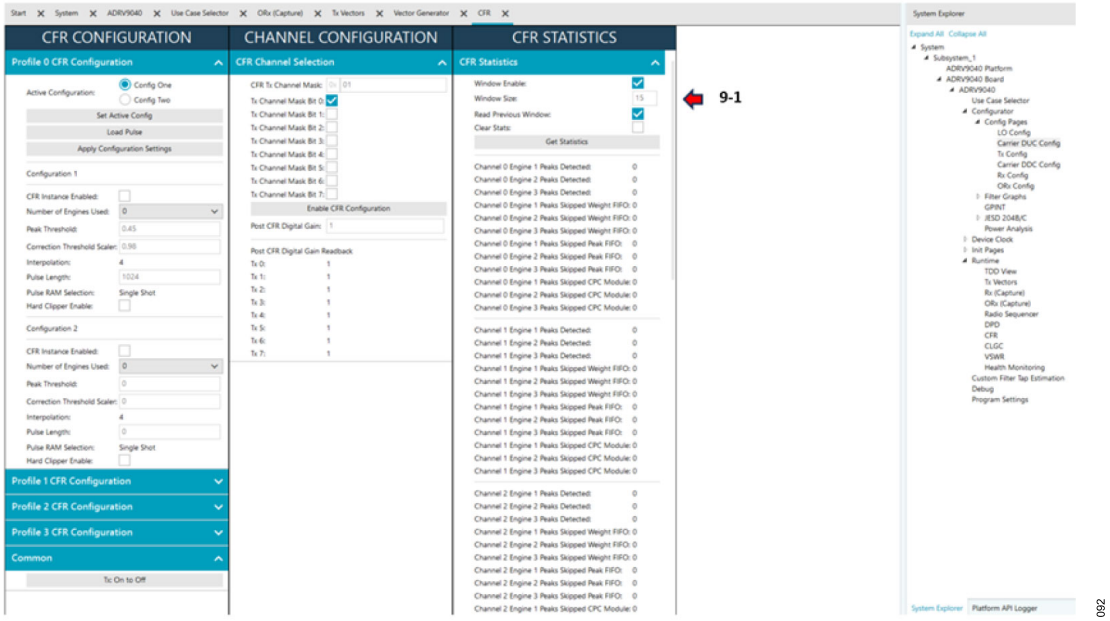


Figure 92. Get Statistics of Configuration 1: Window Size

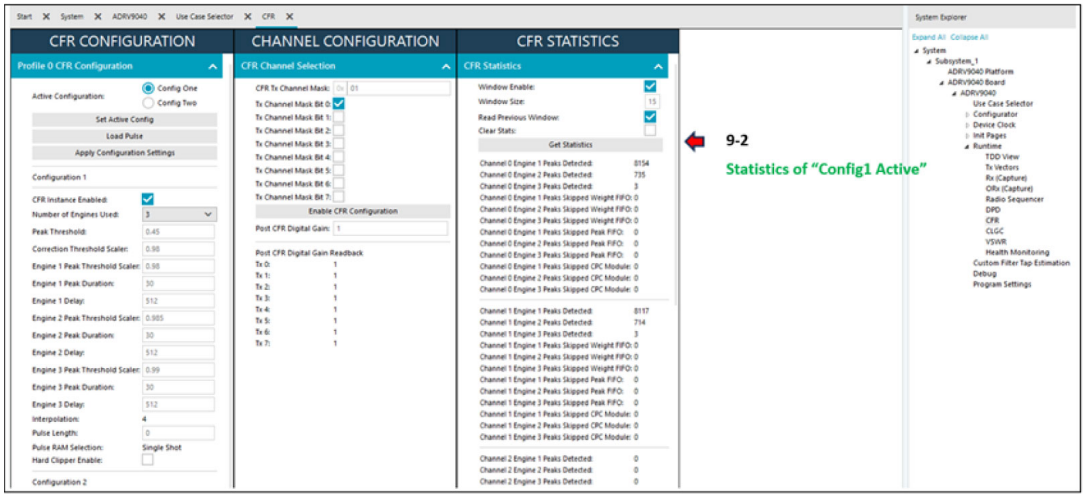


Figure 93. Get Statistics of Configuration 1

Configuration 2

The sequence of **Configuration 2** is the same as that of **Configuration 1**. Therefore, only figures without an auxiliary explanation are added to enable **Configuration 2**.

Activate Configuration 1 and Inactive Configuration 2: Step 10 and Step 11

To set **Configuration 2**, it must be inactive to not impair the Tx channel when the CFR correction pulse and parameters are loaded to the inactive **Configuration 2**.

RUNTIME

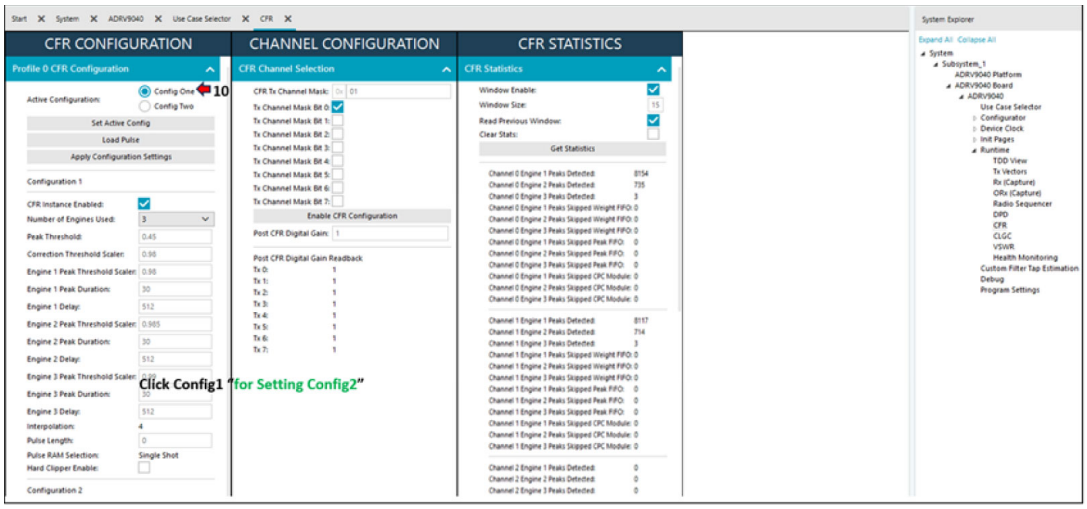


Figure 94. Activate Configuration 1 and Inactive Configuration 2: Step 10

Once selected, **Configuration 1** is active and configuration is ready to be updated with the CFR correction pulse and CFR parameters in Figure 94 and Figure 95.

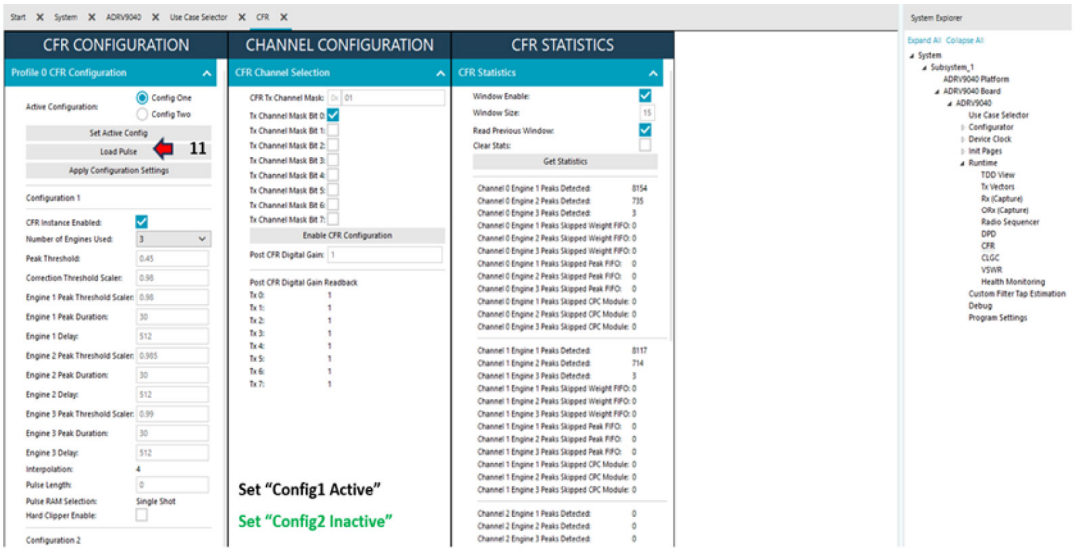


Figure 95. Activate Configuration 1 and Inactive Configuration 2: Step 11

Loading CFR Correction Pulse: Step 4 for Config Two

To upload the CFR correction pulse, click on **Load Pulse** as shown in Figure 96.

RUNTIME

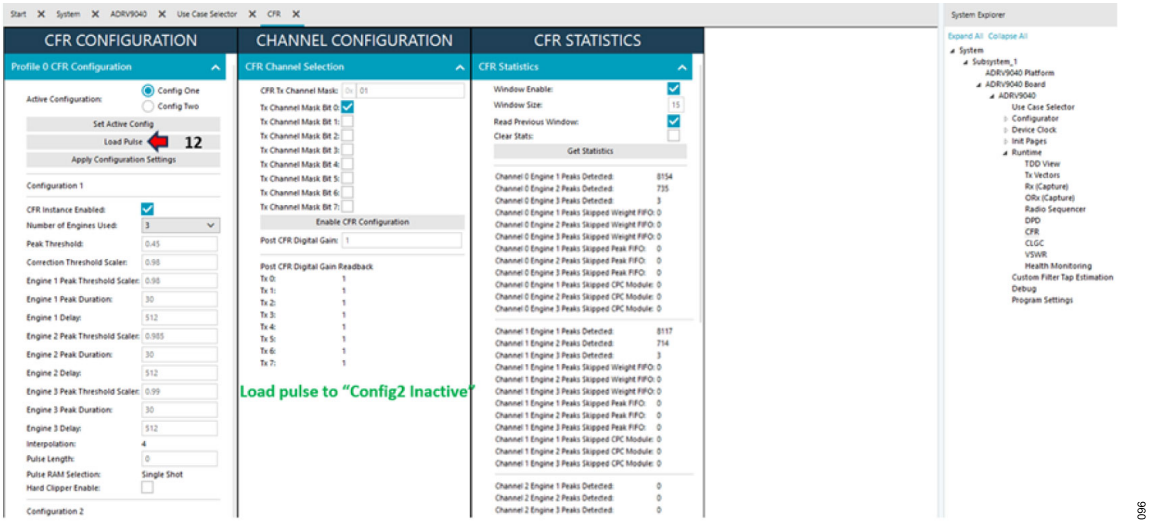


Figure 96. Loading CFR Correction Pulse of Configuration 2: Step 12

Once clicked, the directory and the CFR correction pulse can be located in Figure 97, assuming that the CFR correction pulse exists.

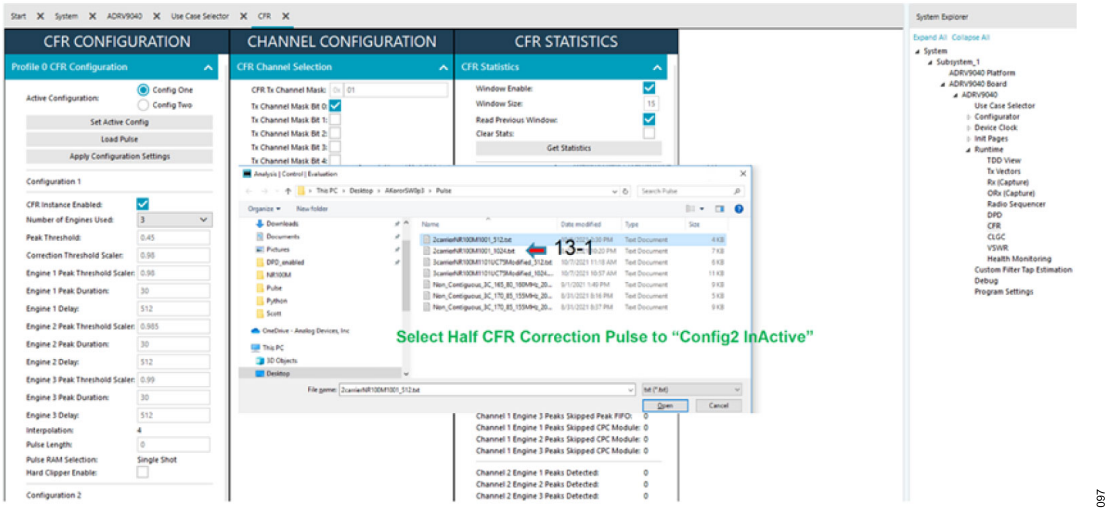


Figure 97. Loading CFR Correction Pulse of Configuration 2: Step 13-1

Once loaded correctly, the message is displayed as shown in Figure 98.

RUNTIME

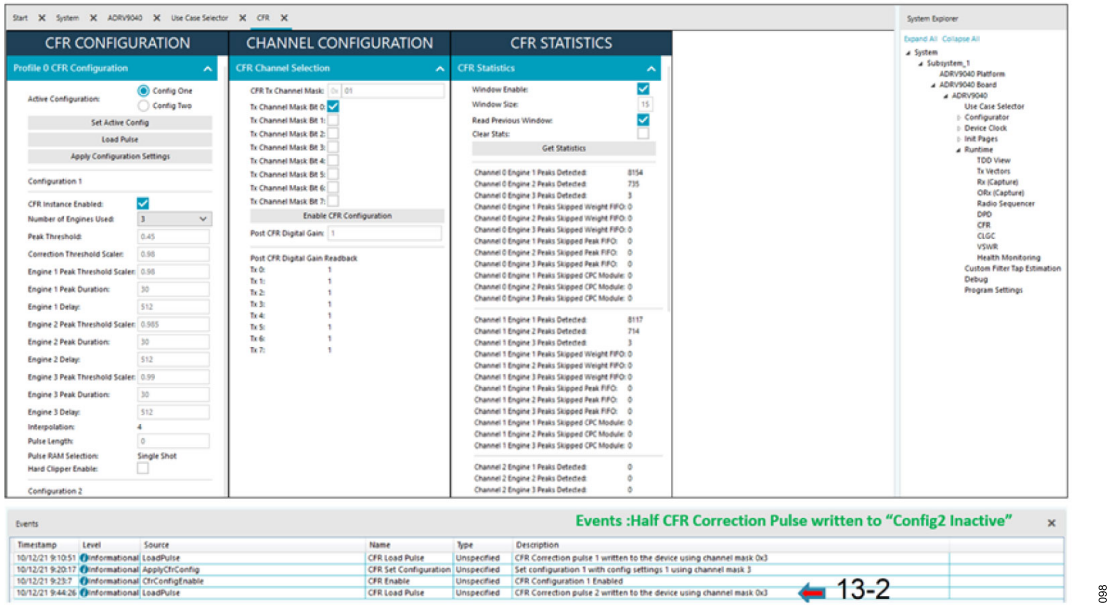


Figure 98. Loading CFR Correction Pulse of Configuration 1: Step 13-2

Setting CFR Parameters for Configuration 2

All CFR parameters can be placed, which depend on the target PAR and the RMS CFR input power. The current **Peak Threshold** 0.3814 is calculated based on the two inputs, namely PAR at 8.0 dB and CFR input at −16.3 dBFS.

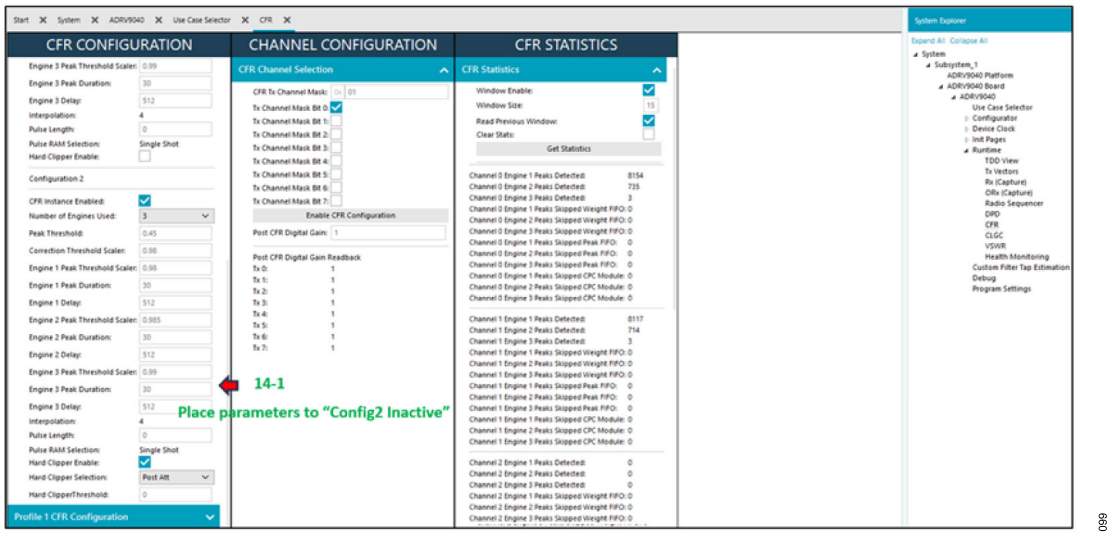


Figure 99. Setting CFR Parameters of Configuration 1: Step 14-1

Once all required parameters are set, click on **Apply Configuration Settings** as shown in Figure 100. Once the parameters are loaded to the inactive **Configuration 2**, the event message is shown as in Figure 100.

RUNTIME

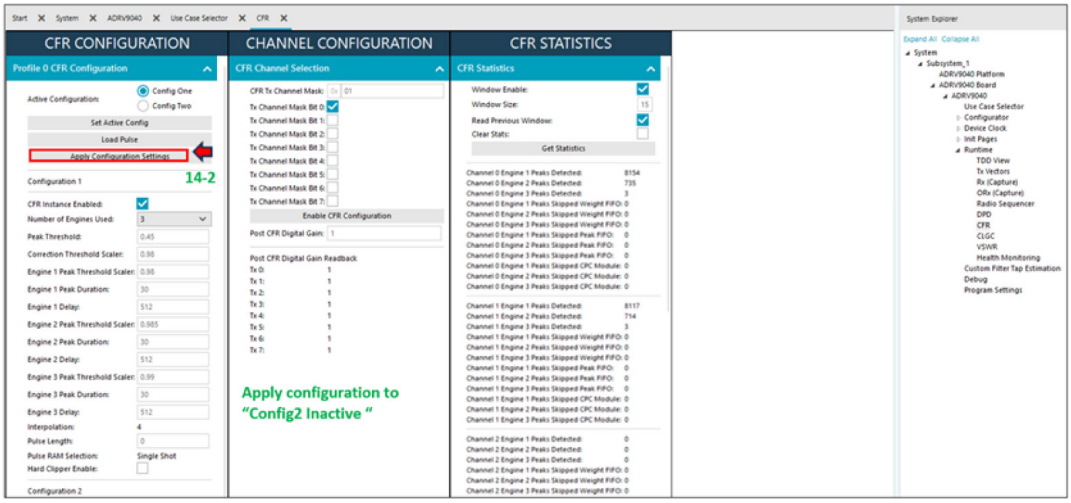


Figure 100. Apply Configuration 1 Settings: Step 14-2 and Step 14-3

Next, both CFR correction pulse and CFR configuration parameter of **Configuration 2** must be enabled by clicking on **Enable CFR Configuration**. The event message as shown in Figure 101 confirms that **Configuration 2** (inactive) is loaded.

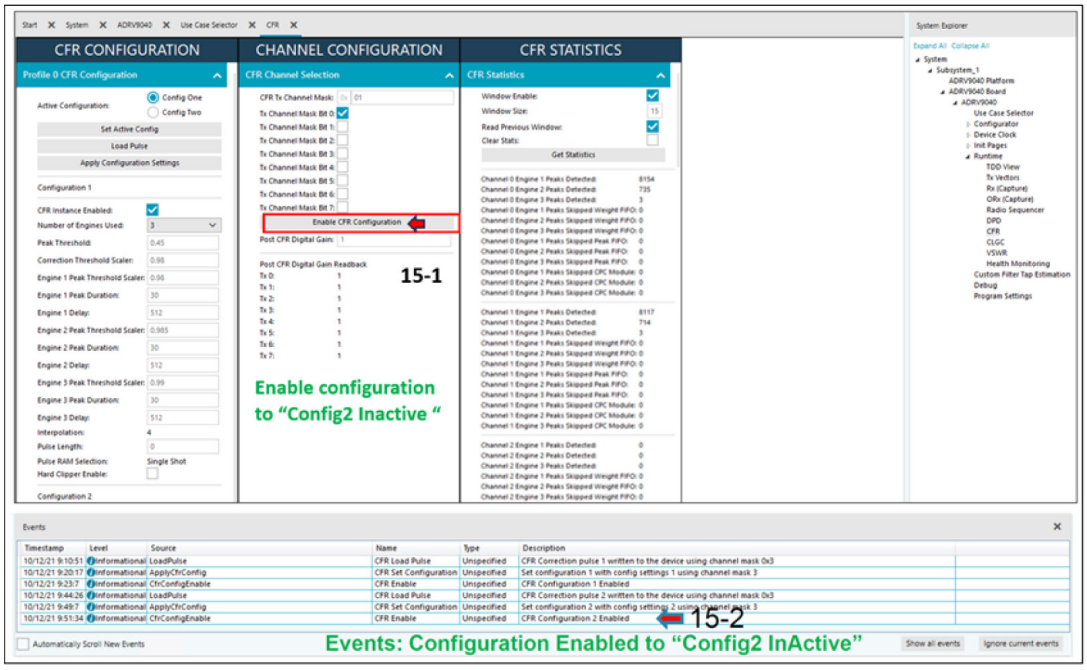


Figure 101. Enable CFR configuration 1: Step 15-1 and Step 15-2

Lastly, click on **Config Two** and then **Set Active Config** as shown in Figure 102.

RUNTIME

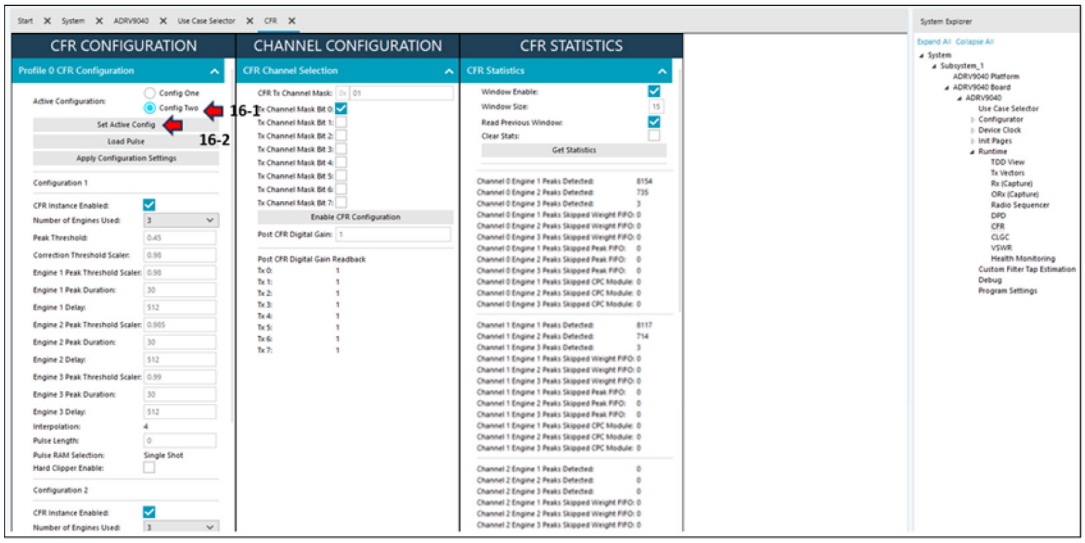


Figure 102. Activate CFR Configuration 1: Step 16-1 and Step 16-2

Before **Config Two** is enabled, check that the original ACLR and Gaussian CCDF of spectrum analyzer are confirmed. After CFR **Config Two** is enabled, it is observed that ACLR is by 0.1 dB degraded and PAR is reduced to 8.10 dB at 0.01% from 9.65 dB at 0.01% as shown in Figure 104.

RUNTIME

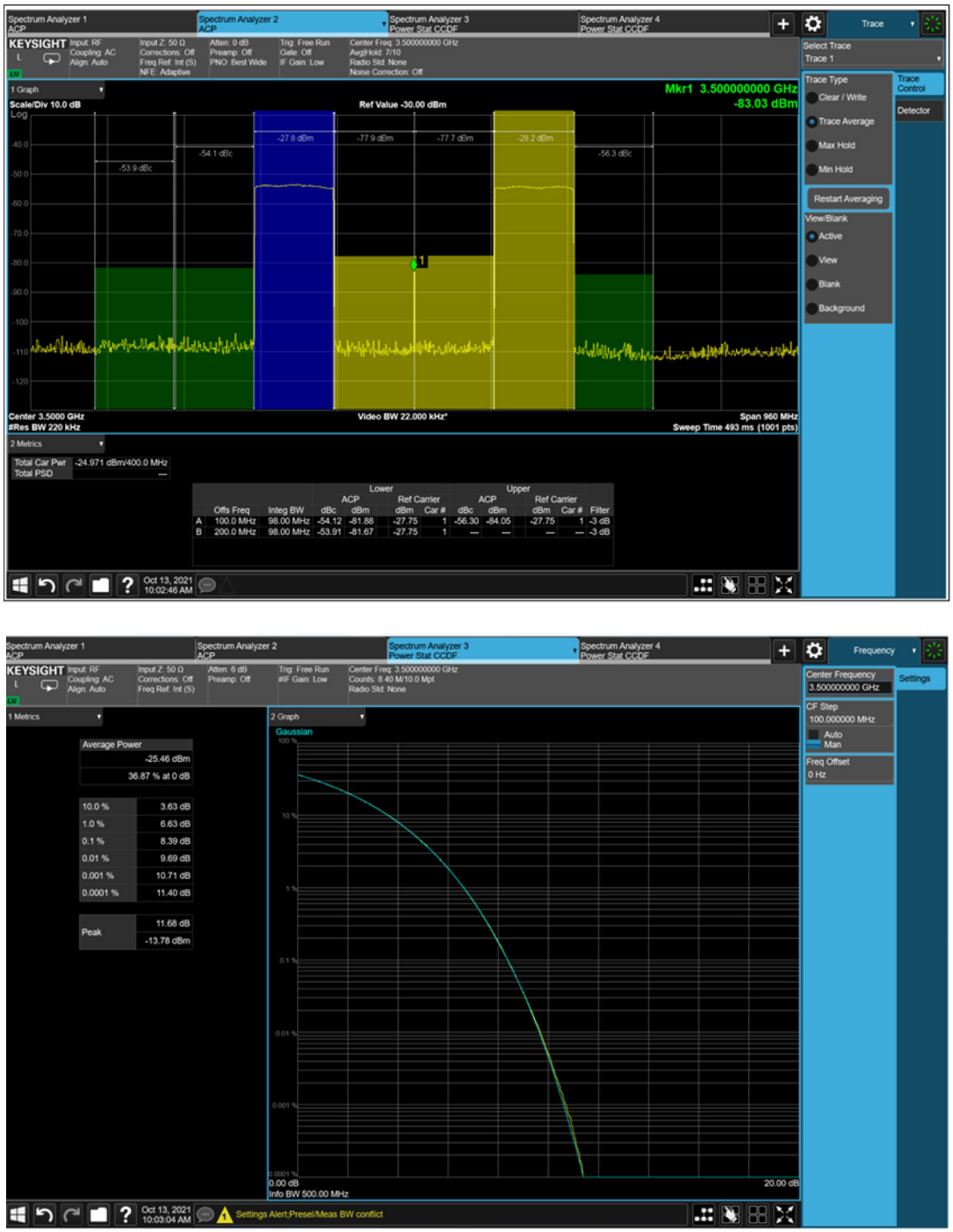


Figure 103. Initial CFR Configuration 2: ACP and CCDF

RUNTIME

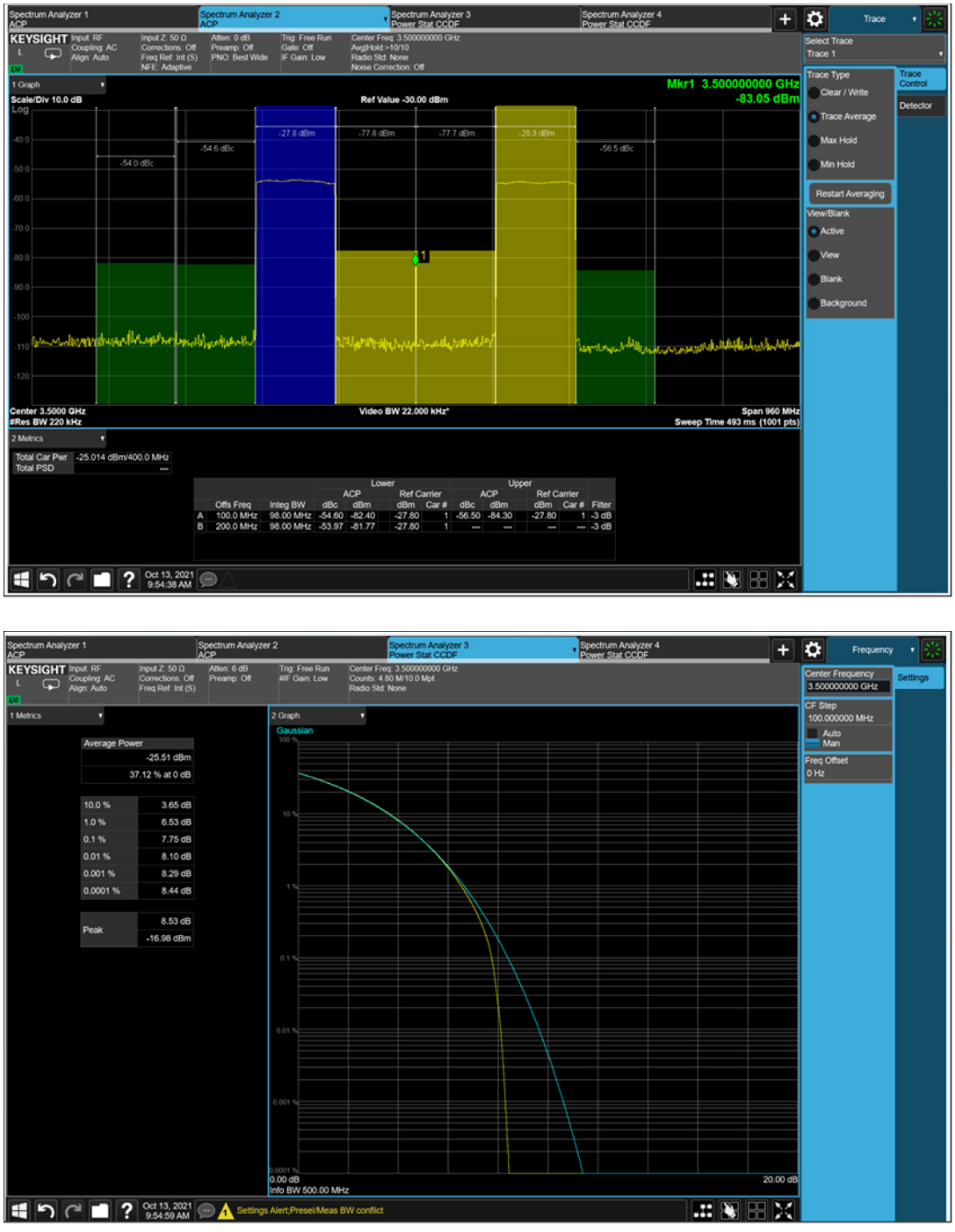


Figure 104. After Enabling Set CFR Configuration 2: ACP and CCDF

Using statistics in the GUI, check that there is no peak skipping with the **Configuration 2**. Before clicking on **Get Statistics**, **Window Size** needs to be filled with the range 15 as shown in Figure 105. It can be executed by clicking on **Get Statistics** to get the CFR statistics. As shown in Figure 106, the peaks of signals over the three engines are detected but no peak skipping is observed.

RUNTIME

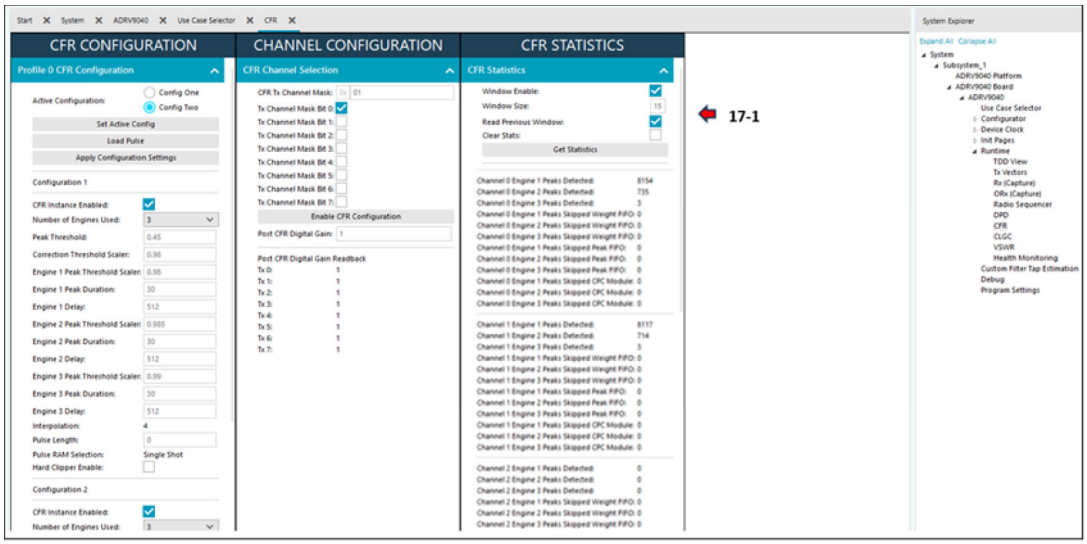


Figure 105. Get Statistics of Configuration 2: Window Size

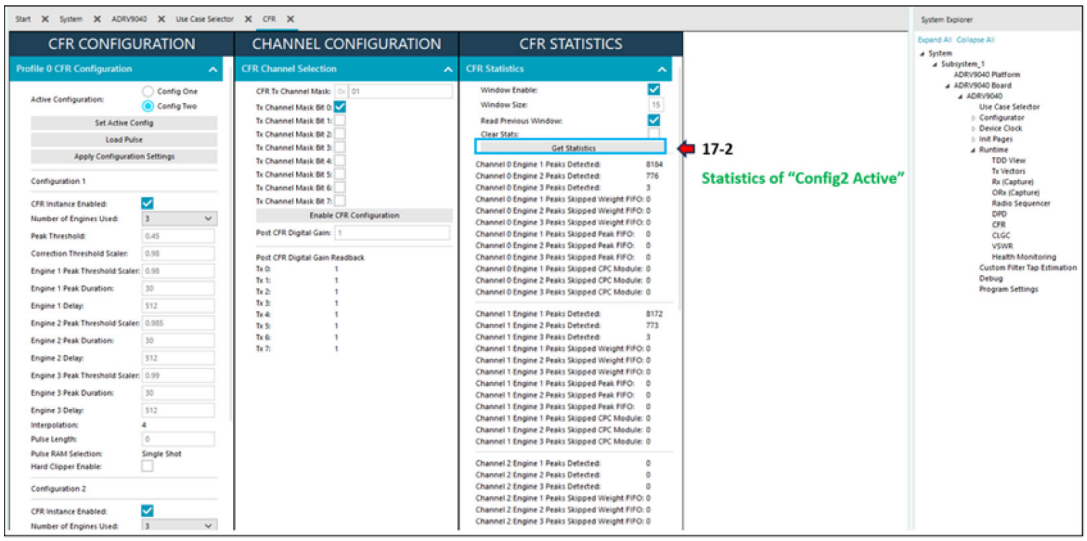


Figure 106. Get Statistics of Configuration 2

CLGC (CLOSED LOOP GAIN CONTROL)

Hardware Prerequisites

To evaluate CLGC, ensure that a gain line up is connected to the transceiver as shown in Figure 72, and ensure that the transmitter path is connected back to the feedback/observation receiver channel as per the transceiver configuration. Tune the power levels to ensure that the observation receiver is not saturating.

Ensure that there is a sufficient headroom for the transmitter attenuation to adjust it as part of the CLGC tracking. Note that DPD is a prerequisite for the CLGC to run. The summary of the minimum sequence to enable CLGC is as follows:

1. Program the desired profile, then transmit the carriers.
2. Setup transmitter to observation receiver mapping.
3. Load the DPD model.
4. Reset DPD.
5. Reset CLGC tracking.

RUNTIME

6. Set up DPD tracking configuration.
7. Set up DPD capture configuration.
8. Set up CLGC capture configuration.
9. Set up CLGC tracking configuration.
10. Enable DPD tracking.
11. Run CLGC.

It is assumed that the user has already configured DPD (not enabled) following the steps mentioned in the DPD section. Note that DPD must be disabled to proceed with the CLGC configuration. The additional steps to configure/enable CLGC are as follows:

1. Select the **CLGC** option from **Runtime** under **System Explorer**.

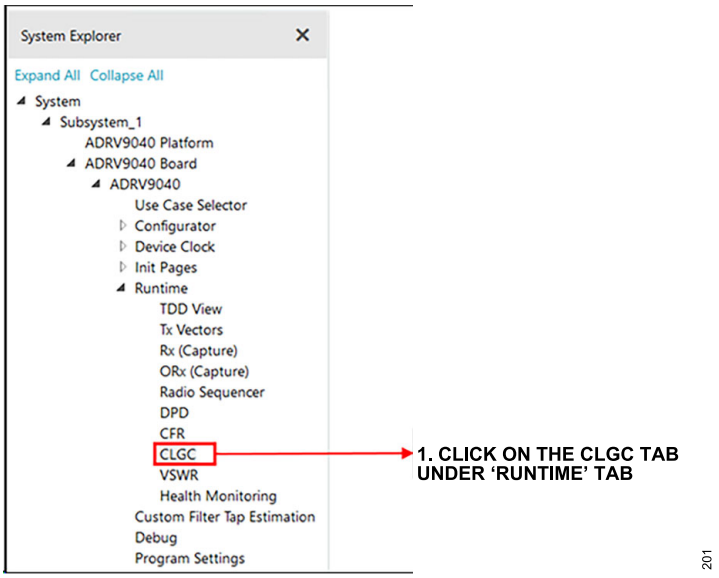


Figure 107. CLGC Tab Under Runtime

2. Enable the channel from **Channel Selection** as shown in Figure 108.
3. Set the desired **Capture Config**. There are two modes for capturing the signal. One is transmitter signal strength indicator (TSSI) and the other is peak detect mode.
4. Set the desired **CLGC Tracking Config**, which consists of **Min Tx Atten Limit (dB)** and **Max Tx Atten Limit (dB)** expected loop gain (if known already) that is to be tracked by the CLGC calibration.
5. In the **DPD** tab, ensure that DPD is configured and click the box beside **Run CLGC**, then click **Apply Tracking Config** and **Enable DPD Tracking Cal**.
6. Set the **Tracking Enable** option as follows:
   a. As shown in Figure 109, to estimate the current open loop gain, unselect the box next to **Tracking Enable**.
   b. Enter the estimated loop gain in **Current Loop Gain (dB)** under **CLGC Tracking Config**.
   c. Select the box next to **Tracking Enable**. The same loop gain is maintained by the CLGC calculation by adjusting the Tx attenuation. To track the loop gain, select the box next to **Tracking Enable**.
7. From the CLGC status, the user can observe that the expected loop gain is maintained, and it also shows the current Tx attenuation. If the CLGC is running, CLGC iteration count and update count must be incrementing.

RUNTIME

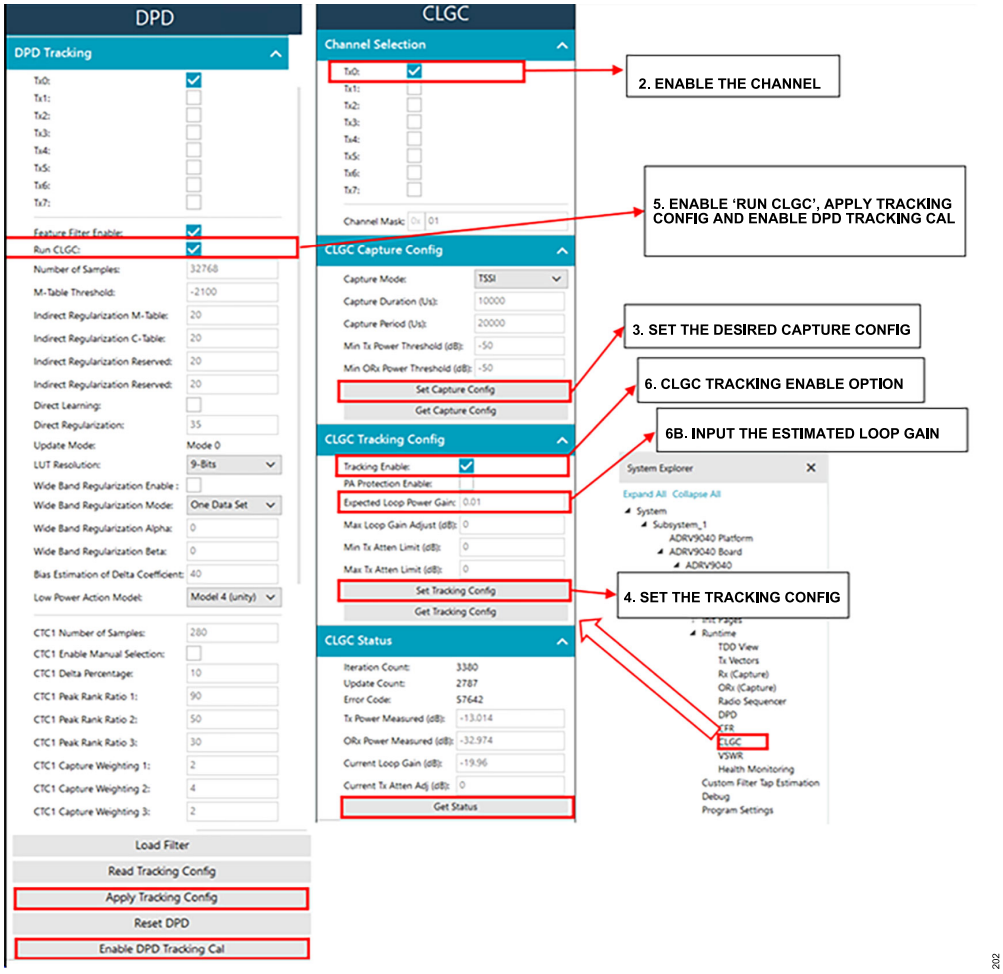


Figure 108. Enabling CLGC: Step 2 to Step 6

RUNTIME

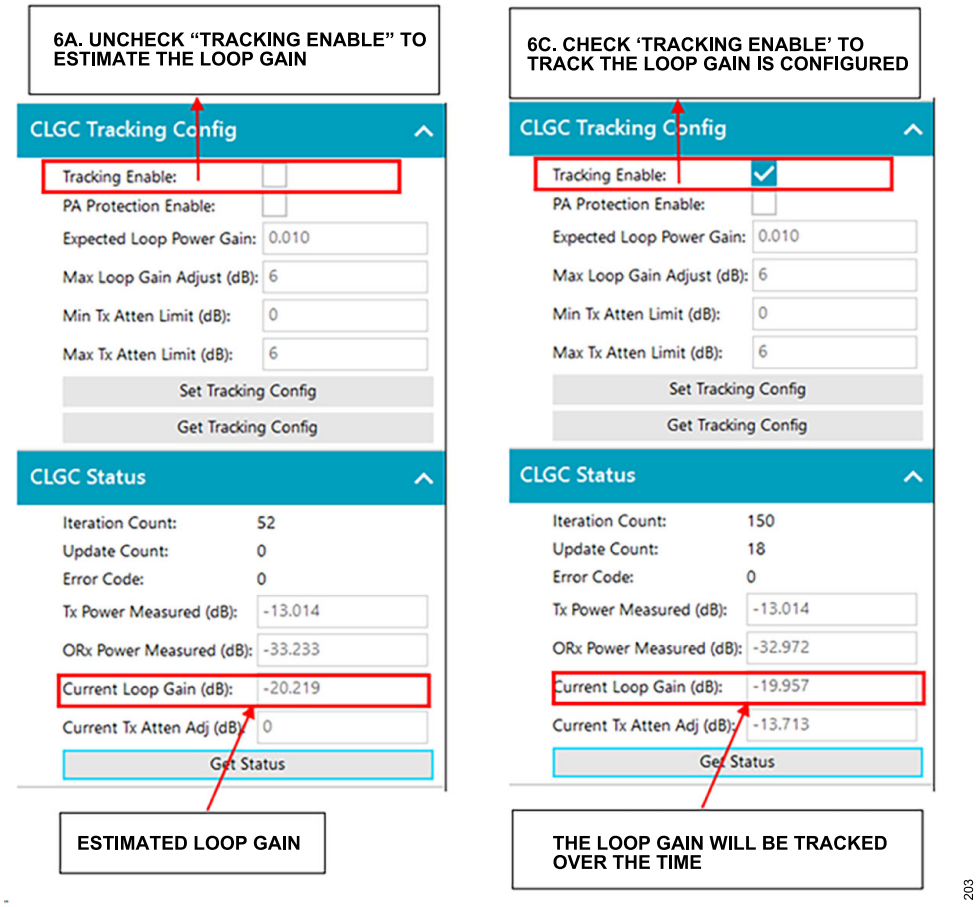


Figure 109. Enabling CLGC: Step 6a and Step 6c

VOLTAGE STANDING WAVE RATIO (VSWR)

HARDWARE PREREQUISITES

To evaluate VSWR , the transmitter and observation receiver must be connected via an RF switch so that the user can switch between forward and reverse paths . Figure 110 shows the setup for a VSWR evaluation in a lab without custom hardware. While designing custom hardware, forward and reverse couplers must be used as mentioned in the system development user guide.

HARDWARE SETUP

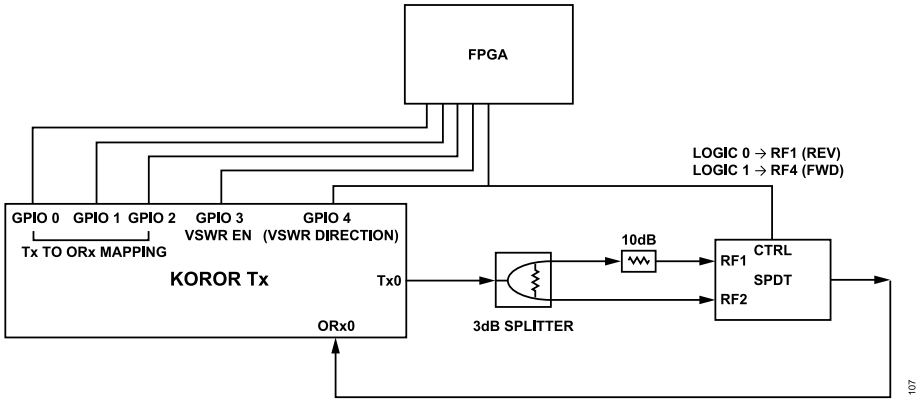


Figure 110. VSWR Measurement Setup

Figure 110 shows (eight pin modes showing only ORx0 path) how the mapping and the direction are set by using the assigned GPIO pins, and are driven by the FPGA. The same GPIO pins, which are fed to Koror transmitter and the same GPIO pins, are fed to the external switch as well.

The testing procedure is as follows:

1. **VSWR** is available under **Runtime** as shown in Figure 111.

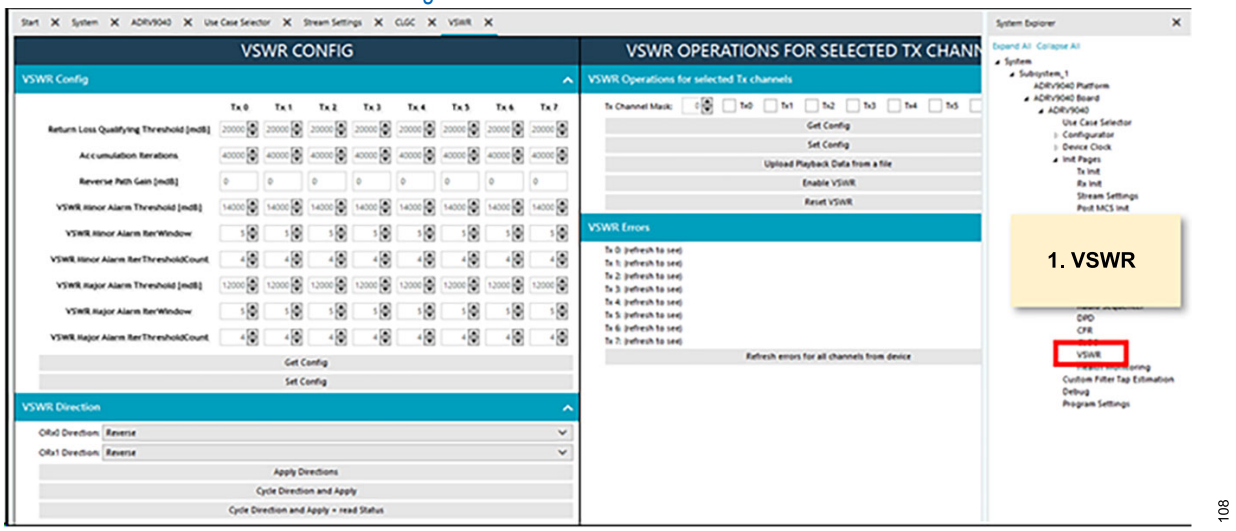


Figure 111. VSWR

2. Enable the Tx and ORx channels with 0 dB attenuation. Ensure that Tx to ORx mapping is configured correctly as per the physical connections.
3. Enter the **VSWR Config** parameters like return loss qualifying threshold, accumulation iterations, and major and minor alarm thresholds as per testing, and then select **Set Config** as shown in Figure 112. The **VSWR Config** provides test options by programming the thresholds. Maximum and minimum ranges for all the **VSWR Config** parameters are defined in the system development user guide (SDUG).

VOLTAGE STANDING WAVE RATIO (VSWR)

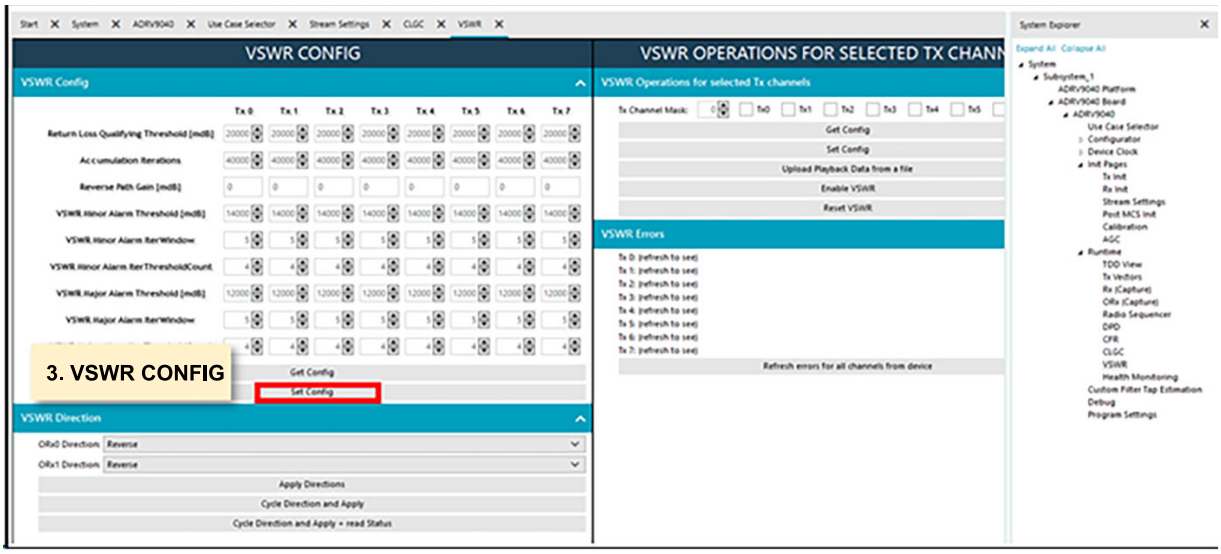


Figure 112. VSWR Configuration

4. Select the Tx channel mask for VSWR feature testing as shown in Figure 113.
5. Load test RAM data waveform. Test RAM data can be generated from ACE GUI or can be loaded as a file. Select **Upload Playback data from a file** to upload a pregenerated test RAM waveform. Note that these waveforms must be generated for different use cases. Contact Analog Devices for a waveform file until the generate option is available in the GUI.
6. Select **Enable VSWR** as shown in Figure 113.
7. Set VSWR direction. Depending on the VSWR mode (PIN mode), the direction bits are controlled from FPGA and are given to the external switches. During API mode, the user must control the RF switch in VSWR forward and reverse directions. The switch needs to be toggled within four seconds for one update to take place. Under the **VSWR Direction** tab, the user can reverse direction of the switch by clicking **Cycle Direction and Apply**.

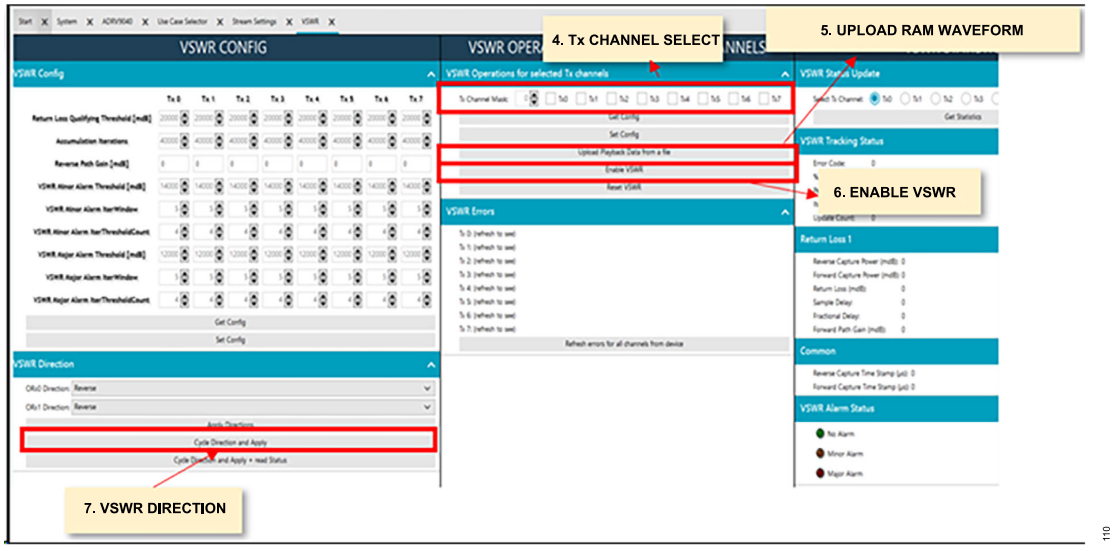


Figure 113. VSWR Direction

8. Set the VSWR tracking status and statistics. Once the forward and reverse switching happens, the user can read the VSWR tracking status and statistics in the **VSWR Statistics** window as shown in Figure 114 for the second and third iterations. The iteration and update count increments, and the percent complete shows 100%. From statistics, the user can report the reverse, forward powers in mdB, return loss, sample delay, fractional delay, forward path gain, and reverse the time stamp and forward time stamp as well.

VOLTAGE STANDING WAVE RATIO (VSWR)

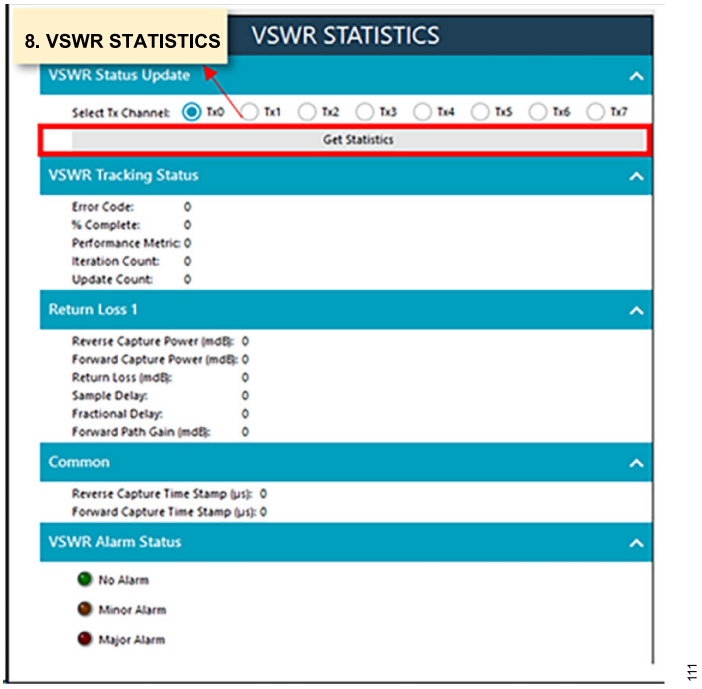


Figure 114. VSWR Statistics

SOFTWARE RESOURCE FILES

The resource files required for programming the ADRV904x device are listed in Table 9.

These include the **DeviceProfileTest.bin** and **initdata.c** files, which must be generated by the user for the desired ADRV904x configuration and initialization settings. These files can be generated using ACE with attached hardware. The ADRV904x can be programmed using ACE for generating these resource files.

Note that the ACE needs a hardware connection to the ADS10-V1EBZ/CE board system for generating the resource files during programming.

Table 9. Resource Files Essential for Programming the ADRV904x

Resource File	Purpose
ADRV9040_FW.bin	Precompiled firmware binary for the embedded dual core ARM processors in the ADRV904x.
ADRV9040_DFE_CALS_FW.bin	Precompiled firmware binary for the embedded A55 DFE processor in the ADRV904x.
DeviceProfileTest.bin	Profile binary consisting of filter coefficients, clock rates, and signal processing resources to be enabled/disabled for a particular use case.
initdata.c	Initialization data structures for setting up the ADRV904x subsystems. It can be generated with either C89 or C99 compatibility to integrate with the user application code base. The difference between a C89- and C99-compatible data structure is illustrated in Table 10.
RxGainTable.csv	Front end gain lookup table for the ADRV904x receiver.
RxGainTable_GainCompensated.csv	Receiver gain table to use when digital gain compensation is enabled.
stream_image.bin	Binary file for the stream co processor in the ADRV904x, which is mainly used for setting up and controlling the Tx/Rx datapaths when certain events occur, such as Tx/Rx enable.

Table 10. Member Representations Compared Between C99 and C89 Data Structures

C99 Data Structure Example	C89 Data Structure Example
adi_adrv904x_Version_t initStructApiVersion = {2, 10, 0, 6};adi_adrv904x_CpuFwVersion_t initStructArmVersion = { {2, 10, 0, 6} , ADI_ADRV904X_CPU_FW_BUILD_RELEASE};adi_adrv904x_Version_t initStructStreamVersion = {2, 10, 0, 6};adi_adrv904x_Init_t deviceInitStruct ={.spiOptionsInit ={.allowSpiStreaming = 1,.allowAhbAutoIncrement = 1,.allowAhbSpiFifoMode = 1,},	adi_adrv904x_Version_t initStructApiVersion = {2, 10, 0, 6};adi_adrv904x_CpuFwVersion_t initStructArmVersion = { {2, 10, 0, 6} , ADI_ADRV904X_CPU_FW_BUILD_RELEASE};adi_adrv904x_Version_t initStructStreamVersion = {2, 10, 0, 6};adi_adrv904x_Init_t deviceInitStruct ={ { // spiOptionsInit 1, // allowSpiStreaming 1, // allowAhbAutoIncrement 1, // allowAhbSpiFifoMode},

RESOURCE FILE GENERATION USING ACE

ACE can be used to generate the resource files needed for programming the ADRV904x by connecting and programming the evaluation hardware using the ADRV904x plugin. ACE outputs the resource files to the resource folder path **C:\Users\%USERNAME%\AppData\Local\Analog Devices\ACE\PluginFiles\Board.ADRV9040\Local\resources** as shown in Figure 115.

Note that ACE clears the contents of the resource folder with every program before writing new resource files. Any resource files required by the user should be copied to a different location before attempting to program the ADRV904x again.

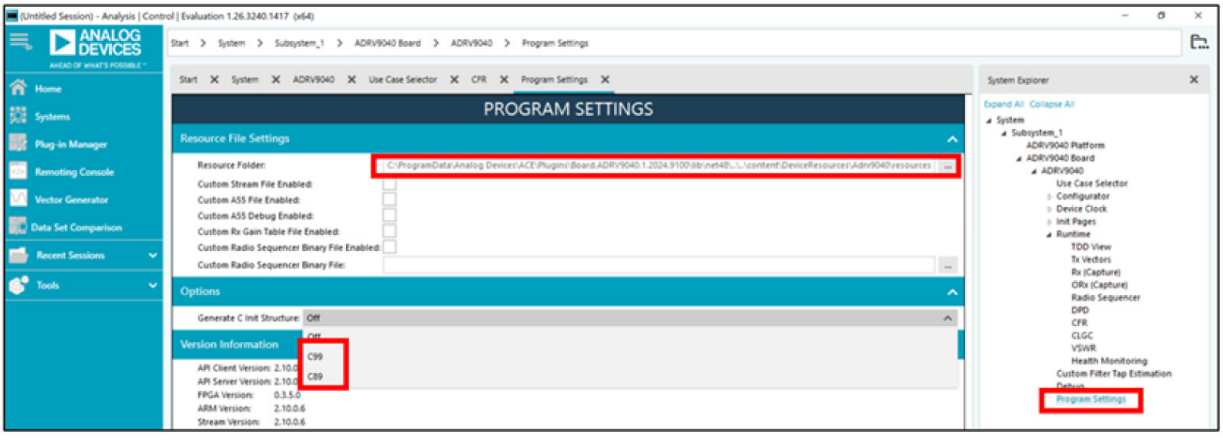


Figure 115. Resource File Generation Using ACE, C89 or C99 Compatibility Can be Selected for Initdata.c

IRONPYTHON SCRIPTING

ACE enables the user to interface with the ADRV904x evaluation system using a scripting language such as IronPython. To run scripts from within ACE, the user must refer to the following steps:

1. Provide a path to the host PC IronPython installation under ACE **Settings** > **Scripting** > **Path** as shown in Figure 116. This step only needs to be completed once after installing ACE.

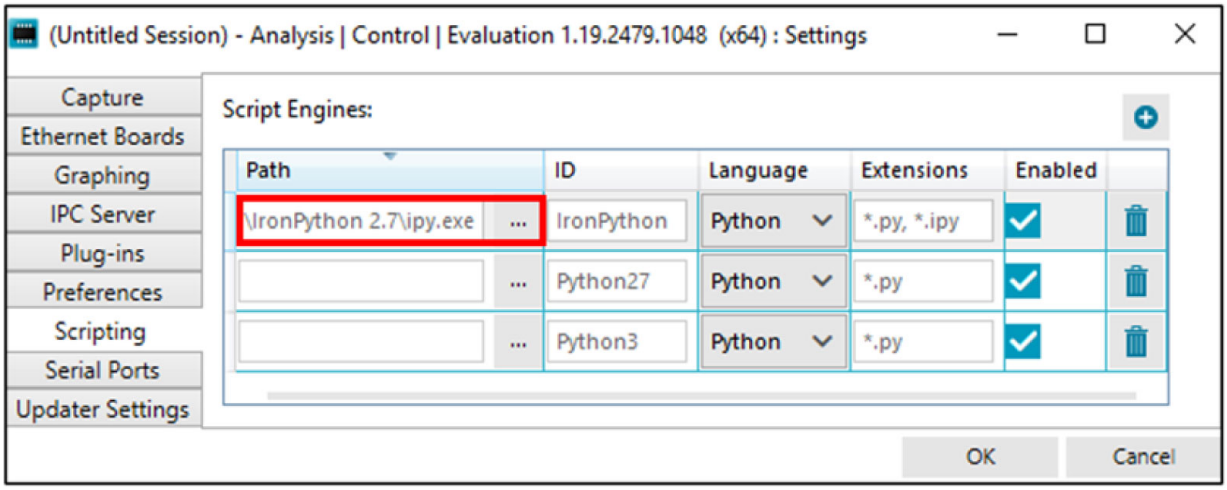


Figure 116. Providing IronPython Path to ACE for Enabling Script Execution

2. Open a script from **Tools** > **Platform API Logger** > **Open Script** as shown in Figure 117. A template script for interfacing with the ADRV904x device is included with the plugin and can be opened from **Create New**. Scripts open as new tabs in ACE.

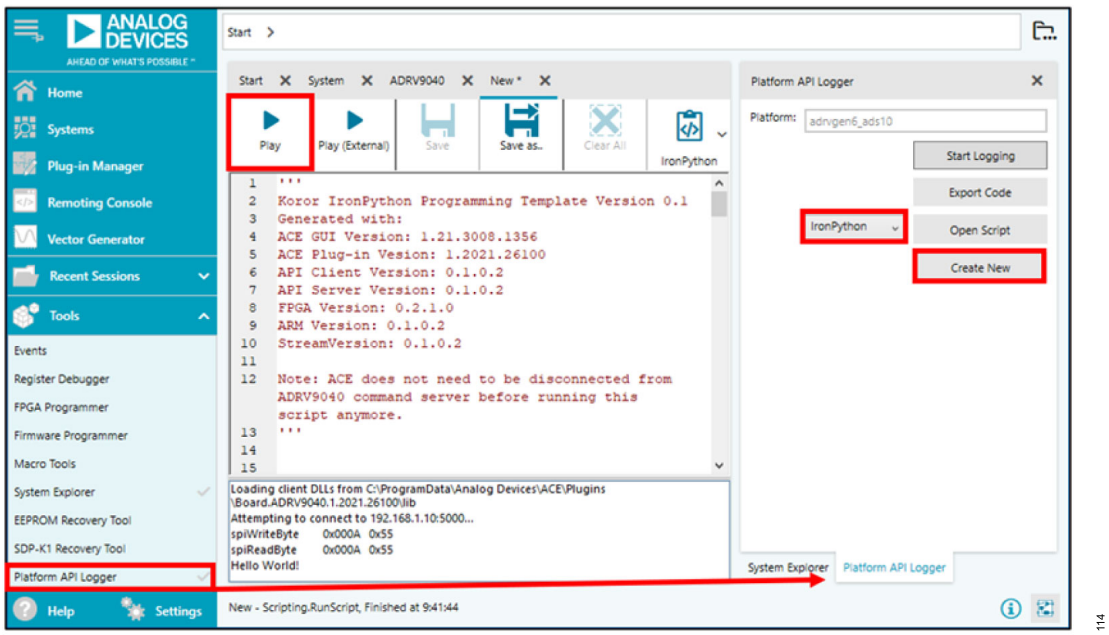


Figure 117. Using Platform API Logger to Open and Execute IronPython Scripts from Within ACE

APPENDIX

UNINSTALLING OLDER ACE

Uninstalling ACE is not necessary to update the ACE core to a newer release. However, if errors are seen during the installation of a new ACE core version, any previous versions of ACE core can be removed from the host PC as outlined below. Note that administrator privileges are required for these steps as follows:

1. Close any running instances of ACE. Task manager can be used to confirm that no background ACE processes are running.
2. Navigate to Windows **Start** > **Add or Remove Programs** > **ACE** > **Uninstall**.
3. Select **ScrubUninstall** in the ACE uninstall wizard as shown in Figure 118. This is necessary to remove any older ACE plugin versions, but it also removes any custom files, settings, and data exports previously stored by the user. Note that this step must only be performed as a fallback option if ACE installation appears corrupted, and it is necessary to start from a clean slate.

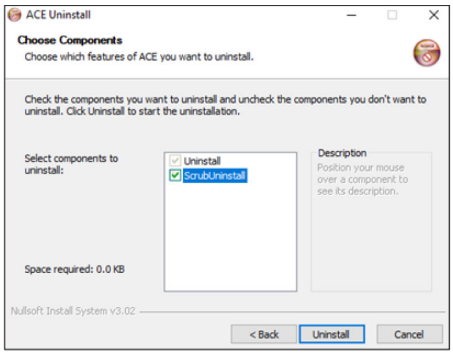


Figure 118. ScrubUninstall Used to Troubleshoot Erroneous ACE Installation

4. When prompted, select **No** to additionally uninstall system demonstration platform (SDP) drivers, LRF drivers, and ADIThon from previous ACE installation.
5. Attempt to reinstall ACE by running the included ACE installer with default components selections as shown in Figure 119.

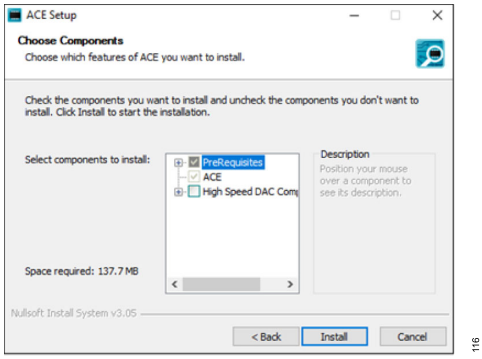


Figure 119. Component Selections Used when Attempting a New Installation of ACE

More information about the ACE uninstallation process is available on the ACE wiki https://wiki.analog.com/resources/tools-software/ace/installscrub.

UNINSTALLING OLDER PLUGIN USING PLUGIN MANAGER

Any previously installed ACE plugin, such as an ADRV903X plugin, can be uninstalled using ACE plugin manager as shown in Figure 120. The steps are as follows:

1. Open the plugin manager from the ACE left panel.
2. Select the plugin from the list of installed packages. Find the plugin to be uninstalled via the search bar.
3. Click **Uninstall Selected**. Restarting ACE is needed to complete this step.

APPENDIX

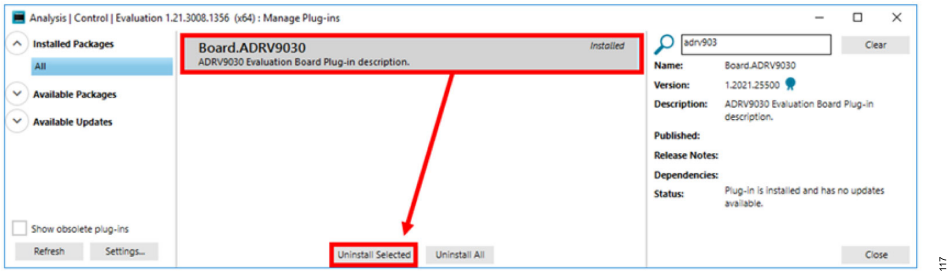


Figure 120. Using ACE Plugin Manager to Uninstall Older Version of the ADR903x Plugin (Board ADRV9010)

INSTALLING THE ADRV904X PLUGIN USING THE PLUGIN MANAGER

The user can install the ADRV904x plugin by providing the plugin **.acezip** file path to ACE under **Settings** as shown in Figure 121. The steps are as follows:

1. Open ACE **Settings** and select the **Plug-ins** tab.
2. Add a new plugin by clicking on the **+** button under **Zipped Plugin Sources** as shown in Figure 121.

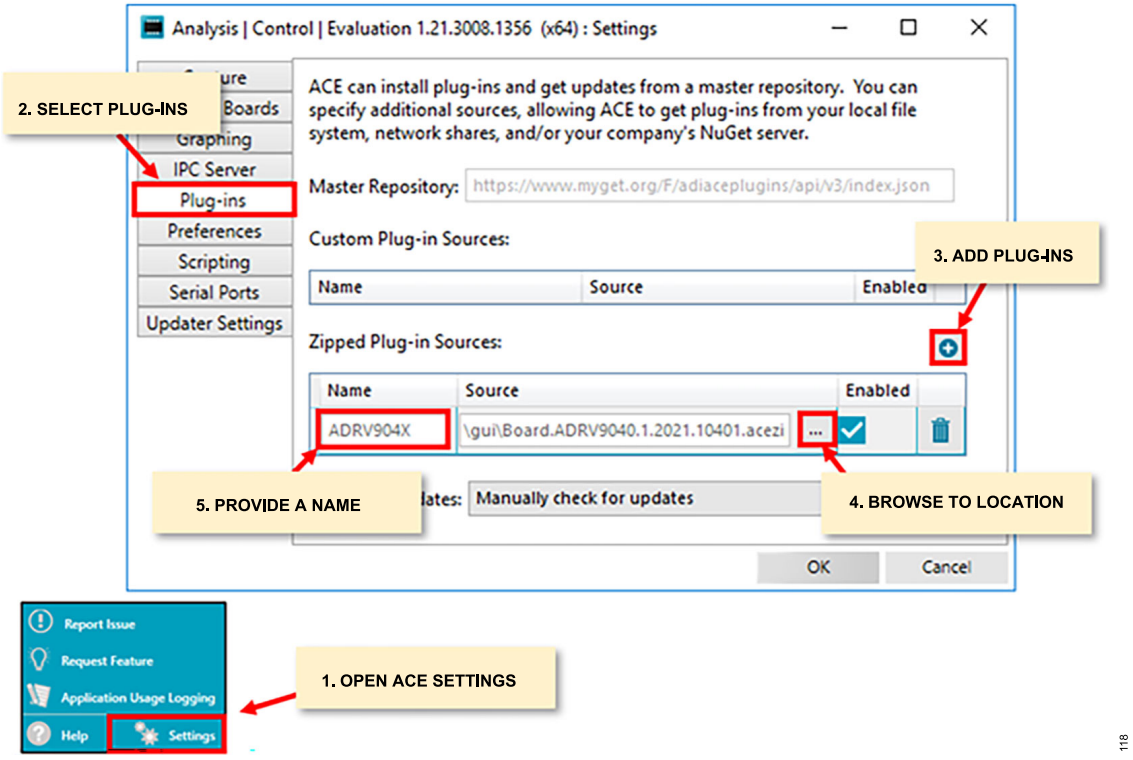


Figure 121. Adding ADRV904x Plugin as a Zipped Source in ACE Settings, Once Added, Run ACE Plugin Manager to Install the Plugin

3. Click on **…** to navigate to the **Board ADRV9040.acezip** file location to populate the source field.
4. Provide a name for this plugin source. The name choice is arbitrary and can be chosen by the user.
5. Launch plugin manager, then select and install **Board.ADRV9040** from the list of **Available Packages** as shown in Figure 122.

APPENDIX

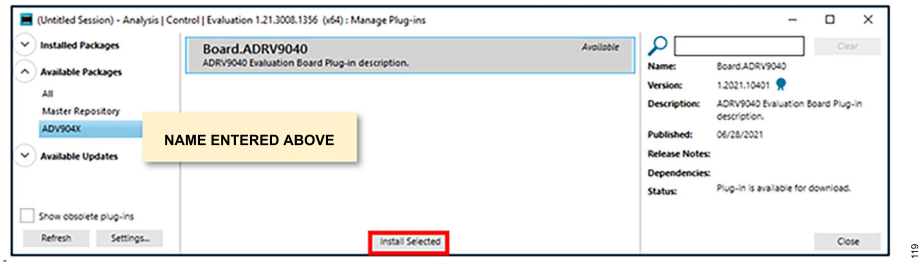


Figure 122. ADRV904x Plugin Installed Using ACE Plugin Manager

DISCONNECTING ACE FROM ADS10-V1EBZ COMMAND SERVER

The user may disconnect ACE from the ADS10-V1EBZ command server to enable other applications to communicate with the evaluation hardware. ACE can be disconnected from the ADS10-V1EBZ as shown in Figure 123. The steps to disconnect ACE from the ADS10-V1EBZ command server are as follows:

1. Navigate to ACE **System** tab.
2. Click on the **USB** icon on the **ADRV904x Platform Controller** to open the **Acquire/Release Hardware** dialog box.
3. Select **Operate without hardware**. This selection updates the buttons on the dialog box to show **Release**.
4. Click **Release**. This step disconnects ACE from the evaluation hardware. The status of ACE connection to the hardware can be checked from either of the following:
   - **System** > **ADRV904x Platform Controller** > USB icon. This icon turns from green to gray once disconnected.
   - **ADRV904x Board** connection indicator. The green light turns red once the board is disconnected.

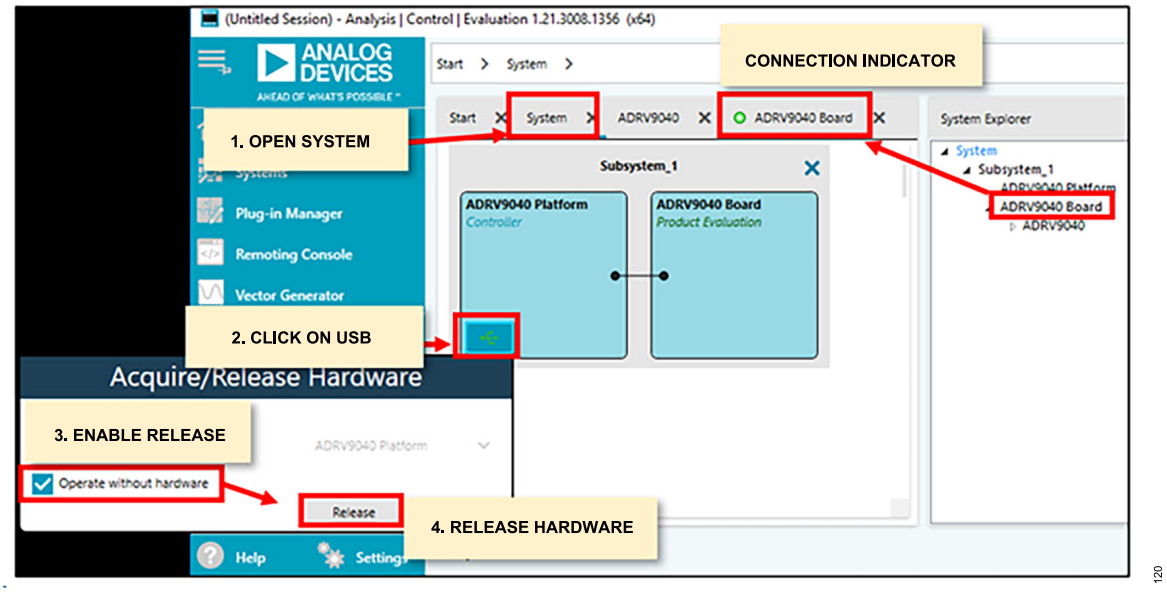


Figure 123. Steps for Disconnecting ACE from the Evaluation Hardware

RECONNECTING ACE TO THE ADS10-V1EBZ COMMAND SERVER

The process for reconnecting ACE to the evaluation hardware is similar to the disconnecting procedure as shown in Figure 124. The steps to reconnect ACE to the ADS10-V1EBZ command server are as follows:

1. Navigate to ACE **System** tab.
2. Click on the USB icon on the **ADRV904x Platform Controller** to open the **Acquire/Release Hardware** dialog box.
3. Deselect **Operate without hardware**. This updates the buttons on the dialog box to show **Acquire**.
4. Click **Acquire**. Reestablishing the connection updates the following:
   - **System** > **ADRV904x Platform Controller** > USB. The icon turns green.

APPENDIX

- **ADRV904x Board** tab. The connection indicator turns green.

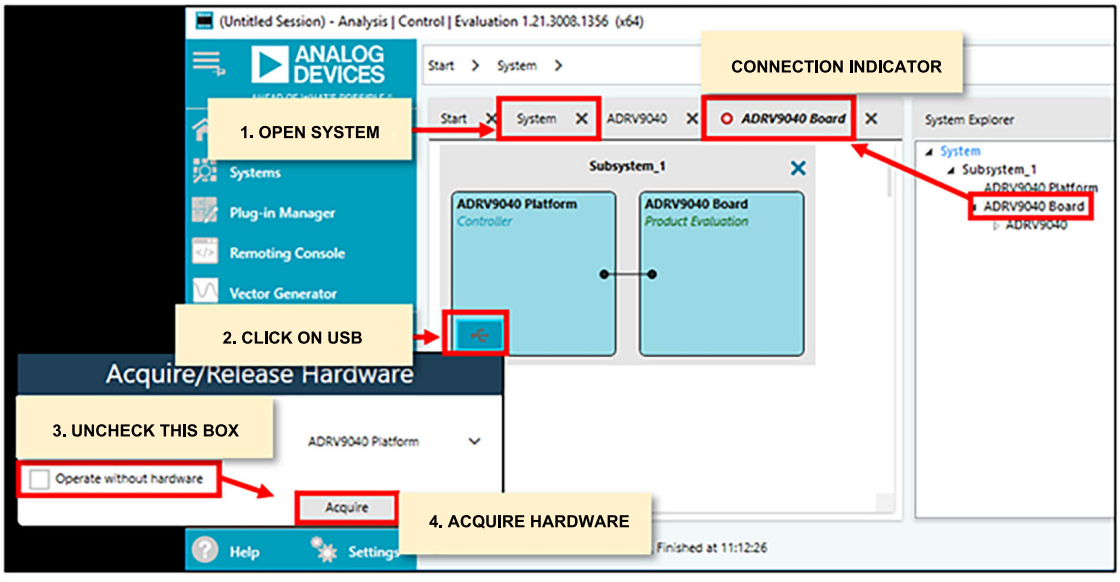


Figure 124. Steps for Reconnecting ACE to the Evaluation Hardware

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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