

ADRV904x Evaluation System User Guide

INTRODUCTION

The ADRV904x family evaluation system enables customers to evaluate an ADRV904x device without having to develop custom hardware or software. The system is comprised of an ADRV904x customer evaluation (CE) board and an ADS10-V1EBZ motherboard with accompanying wall adapter power supplies for both. The evaluation software uses the Analysis, Control, Evaluation (ACE) software developed by Analog Devices, Inc., extended by an ADRV904x specific board plugin. This plugin can be run with ACE on a Windows host PC communicating with the ADS10-V1EBZ motherboard using Ethernet. The ADS10-V1EBZ functions as a baseband processor running an application (ADRV904x command server) for controlling and communicating with the ADRV904x device.

This document also serves as a quick startup guide for the ADRV904x configurator, which is built into the ADRV9040 board plugin for ACE. The ADRV904x configurator allows the user to explore various configurations of an ADRV904x device to arrive at a desired use case configuration. The ADRV904x configurator also provides an overview of the frequency responses of the receiver (Rx), transmitter (Tx), and the observation receiver (ORx) datapaths for a chosen configuration.

This user guide details the steps required to install the ADRV904x evaluation software, program an existing use case, and evaluate the ADRV904x transmitter, receiver, and observation receiver datapaths. The configurator sections of this user guide enable the user to generate a new use case and view its corresponding datapath configurations and filter graphs for the ADRV904x. Note that this document updates as the configurator development progresses and as additional functionalities are added to the tool.

INITIAL SETUP

The ACE GUI is the graphical user interface (GUI) used to communicate with the evaluation platform. The GUI can run with or without evaluation hardware connected. When ACE runs without the hardware connected, the GUI can be fully configured for a particular operating mode. If the evaluation hardware is connected, the desired operating parameters can be setup with ACE and then the software can program the evaluation hardware. When the transceiver is configured, the evaluation software can be used to transmit waveforms generated from the internal numerically controlled oscillator (NCO) block or using custom waveform files as well as to observe signals received on one of the receiver or observation input ports.

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HARDWARE KIT

The ADRV904x evaluation system consists of the following hardware:

- ▶ One (1) ADRV904x CE board with a field programmable gate array mezzanine card (FMC) connector.
- ▶ One (1) 12 V, 3 A wall connector power supply cable for the CE board.
- One (1) ADS10-V1EBZ motherboard with an FMC connector.
- ▶ One (1) 12 V, 16.6 A power supply for powering the ADS10-V1EBZ.
- ▶ One (1) FMC adapter for ADS10-V1EBZ.
- ▶ Two (2) secure digital (SD) cards along with the evaluation kit.
 - ADS10-V1EBZ transmitter V1.0 SD card (used for booting Linux on ADS10-V1EBZ and running the ADRV904x command server application).
 - ▶ SD card type is 16 GB size, Class 10.

Note that the ADRV904x CE board can be any of the ADRV904X-MB/PCBZ, ADRV904X-HB/PCBZ, and ADRV904X-LB/PCBZ. The ADS10-V1 motherboard is not included in the ADRV904x evaluation board and must be purchased separately.

SOFTWARE REQUIREMENTS

The host PC running the ACE evaluation software must meet the following requirements:

- ▶ The operating system on the controlling PC must be Windows 10 (x86 and x64).
- ▶ The PC must have a free Ethernet port to establish a dedicated connection over the following ports:
 - ▶ Port: 22—secure shell (SSH) protocol.
 - ▶ Port: 5000—for communicating with the command server on ADS10-V1EBZ.

If the Ethernet port is occupied by another local area network (LAN) connection, a USB to Ethernet adapter can be used.

- ▶ ADRV904x customer software package—contact your Analog Devices representative to obtain access to this software.
- ► The user must have administrative privileges.
- ▶ The PC must have access to the internet to run automatic software updates.

If internet access is restricted, a manual software update can be performed. Do not upgrade to newer ACE versions as this may cause issues.

HARDWARE SETUP

To setup the evaluation hardware, follow these steps in conjunction with Figure 1:

- 1. Insert the SD card that comes with the evaluation kit into the ADS10-V1EBZ MicroZED MicroSD card slot (J6).
- 2. Mount the FMC adapter on the ADS10-V1EBZ. This step is to protect the ADS10-V1EBZ FMC connector from multiple reinsertions.
- Connect the ADRV904x customer evaluation board and the ADS10-V1EBZ motherboard together. Use the high pin count (HPC) FMC connector (P1001/P2), ensuring the connectors are properly aligned.
- 4. On the ADRV904x evaluation board, provide a reference clock source (122.88 MHz is the default, or use Reference A (REFA) frequency from AD9528 clock settings), at a +7 dBm power level to the J901 connector. This signal drives the reference clock into the AD9528 clock generation chip on the board. The REFA/REFA_N pins of the AD9528 generate the DEV_CLK for the device and REF_CLK for the FPGA on the ADS10-V1EBZ platform.
- 5. Connect the included 12 V, 16.6 A power supply to the ADS10-V1EBZ motherboard through the P2 header.
- 6. Connect the ADS10-V1EBZ to the host PC with an Ethernet cable (connect to P3). No driver installation required.

A USB to Ethernet adapter can be used if no Ethernet port is available on the host PC.

- ▶ On the Ethernet connection dedicated to the ADS10-V1EBZ platform, the user must manually configure the IP address (see Figure 2):
 - IPv4 address: 192.168.1.xyz, where xyz can be assigned such that no other device on the user local network uses the same IP address. Note that xyz must not be equal to 10 because 192.168.1.10 is used by the ADRV904x command server on the ADS10-V1EBZ.
 - IPv4 subnet mask: 255.255.255.0.
- ▶ The user must ensure that the following ports are not blocked by the host PC firewall:
 - ▶ Port: 22
 - ▶ Port: 5000
- ▶ Power up the CE board using the included 12 V, 3 A wall connector power supply.

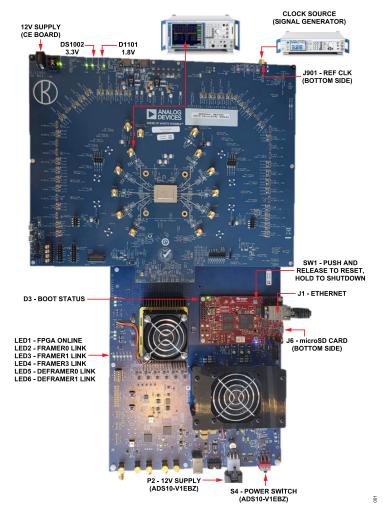


Figure 1. ADRV904x CE Board and ADS10-V1EBZ Motherboard with Instruments Required for Transmitter Testing

Ethernet 3 Status	\times	Ethernet 3 Properties ×	Internet Protocol Version 4 (TCP/IPv4) Properties X
General		Networking Sharing	General
Connection IPv4 Connectivity: IPv6 Connectivity: Media State: Duration:	No network access No network access Enabled 14:22:33	Connect using: Realtek PCIe GBE Family Controller #2 Configure This connection uses the following items:	You can get IP settings assigned automatically if your network supports this capability. Otherwise, you need to ask your network administrator for the appropriate IP settings. O Obtain an IP address automatically (Use the following IP address:
Speed: Details	1.0 Gbps	Clear for Microsoft Networks Pie and Printer Sharing for Microsoft Networks Gross Packet Scheduler Subscheduler Accession Network Adapter Multiplexor Protocol Acrosoft Network Adapter Multiplexor Protocol Acrosoft LLDP Protocol Driver	IP address: 192.168.1.192 Subnet mask: 255.255.255.0 Default gateway: .
Sent — Bytes: 44,650,447	10	Internet Protocol Version 6 (TCP/IPv6) Install Uninstall Properties Description	Obtain DNS server address automatically Use the following DNS server addresses: Preferred DNS server: Alternate DNS server:
Properties Disable	Diagnose	Transmission Control Protocol/Internet Protocol. The default wide area network protocol that provides communication across diverse interconnected networks.	Validate settings upon exit Advanced
	Close	OK Cancel	OK Cancel

Figure 2. IP Settings for Ethernet Port Dedicated to ADS10-V1EBZ Motherboard. The Last Number in the IP Address Is Chosen by the User.

SOFTWARE SETUP

The ADRV904x configurator uses the ACE software, which is a desktop application that allows the evaluation and control of various products from across the Analog Devices portfolio. ACE consists of a common framework (core) that can be extended by plugins for evaluating products such as the ADRV904x. ACE is designed to educate the user in the functional operation of a product and to enable access to the product evaluation system at a higher level of abstraction.

The ADRV904x evaluation software can be set up and updated to use the latest customer software package provided by Analog Devices. This update process requires the user to perform the following steps:

- 1. Install (or update) ACE on the host Windows PC.
- 2. Install (or update) the ADRV904x board plugin.
- 3. Update the ADS10-V1EBZ platform files. This step requires setting up a hardware connection.

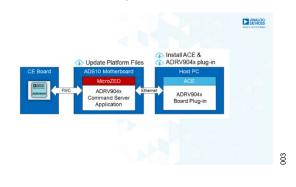


Figure 3. ADRV904x Evaluation Software Components

ACE CORE INSTALLATION

The ADRV904x evaluation software consists of an ACE core (shared framework) and an ACE plugin unique to the ADRV904x. The ACE core can be installed by running the ACE installer included in the customer software package provided by Analog Devices.

The installer consists of a single executable file with the ACE core version number included in the file name. The user can start ACE installation by double clicking on the installer and going through the recommended settings to install ACE. Administrator privileges are required for this installation.

If an older version of ACE was previously installed on the host PC, installing the included ACE version is strongly recommended to get the latest features and bug fixes. In case installation errors are seen, see the Uninstalling Older ACE section to start from a fresh install. Additional ACE documentation is available on wiki.analog.com/resources/tools-software/ace/user guide.

ADRV904X PLUGIN INSTALLATION

The ADRV904x ACE plugin is also included with the customer software package as a Board.ADRV9040.acezip file.

Once ACE is installed, the ADRV904x plugin can be installed by double clicking on the included **.acezip** file. This launches ACE with the ADRV904x plugin listed in the **Explore Without Hardware** section as **ADRV9040 Board** (see Figure 4). The plugin may take a moment to load on ACE first launch. Alternatively, ACE plugin manager can be used for installing the plugin as described in the Installing the ADRV904x Plugin Using the Plugin Manager section. The uninstallation process for plugins is also described in the Appendix section.

With the ADRV904x plugin installed, the search bar on ACE **Start** page can be used to navigate to the plugin with the ID **ADRV9040 Board**. The user can then verify that the installed plugin version number matches the version in the **.acezip** file name. Once the desired ADRV904x plugin version is installed in ACE, it can be run either:

- Without hardware. Double click on the ADRV904x plugin row under Explore Without Hardware or select the plugin row and click on Add Selected Subsystem(s) to start as shown in Figure 4.
- With hardware. Configure a hardware connection between ACE and the ADRV904x command server running on the ADS10-V1EBZ motherboard and update platform files, then double click the ADRV9040 Board icon.

Important: if the host PC already has an ADRV903x board plugin installed, the user may need to uninstall this ARDV903x plugin before the ADRV904x plugin can be run (see the Appendix section). This issue will be resolved in upcoming releases such that ADRV903x and ADRV904x plugins can coexist within ACE as needed.

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Events 🗸	Plugin ID	Version	Compatible	e Controllers	Verified			
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Firmware Programmer	Description:		Dependencies:					
Macro Tools	ADRV9040 Evaluation Board Plug-in description.			LAUNCH F				
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EEPROM Recovery Tool								
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Figure 4. ACE Startup Screen Showing the Installed ADRV904x Plugin Which can be Double Clicked to Start the Configurator Without Hardware

HARDWARE CONNECTION

The ADRV904x plugin can be used standalone (without hardware) as a use case configurator for the ADRV904x family. See the ADRV904x Configurator section to explore the plugin without connecting to ADS10-V1EBZ/CE board evaluation hardware.

If the user is evaluating with hardware, ACE must first be configured to connect to the ADRV904x command server application running on the ADS10-V1EBZ motherboard. By default, the ADRV904x command server listens for incoming connections from the host PC on the IP address 192.168.1.10 and port 5000. The same IP address and port information can be provided to ACE by taking the following steps:

- 1. Open ACE Settings and navigate to the Ethernet Boards tab.
- 2. Click on + to make a new server connection.
- 3. Enter server settings as shown in Figure 5. ADRV904x Platform must be selected for platform.
- 4. Click OK to connect ACE to the ADRV904x server running on ADS10-V1EBZ.

Setting up this connection allows ACE to update the ADRV904x command server running on ADS10-V1EBZ. This process can take a moment, and the user must monitor events associated with updating and starting the ADRV904x command server by displaying the **Events** panel from **Tools** then **Events** on the left panel of ACE.

Once the command server has been started successfully, the **Start** page updates to list the **ADRV9040 Board** under **Attached Hardware** (Figure 6). In case the **ADRV9040 Board** does not show under **Attached Hardware**, refer to the Hardware Setup section to ensure that the

hardware is powered properly. Verify the command server IP address configured under ACE Settings > Ethernet Boards and ensure that no other software application (or ACE instance) is accessing the IP address 192.168.1.10:5000.

The Appendix section additionally covers disconnecting from and reconnecting ACE back to the command server application running on ADS10-V1EBZ.

ADS10-V1EBZ PLATFORM FILES UPDATE

The ADS10-V1EBZ platform files must be updated to use the platform files included with the ADRV904x plugin The user may then click the **Update Platform Files** button on the **ADRV9040 Board** icon to update the ADS10-V1EBZ to use the platform files included with the plugin. A loading screen is shown while the update is in progress. This process takes about a minute.

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Application Usage Logging	Automatically Scroll Ne	ew Events					Show all eve	nts	ignore current events
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Figure 5. Providing ADRV904x Command Server Application IP Address, Port, and Platform Type to ACE

Home Systems Plug-in Manager Remoting Console	Start X SUCCESSFUL CONNECTION TO ADRV904X SERVER
Vector Generator Recent Sessions Tools Events	Version 1.2021.26100 * * Add Hardware Refresh Attached Hardware
Register Debugger FPGA Programmer Firmware Programmer Macro Tools	Events Add Selected Subsystem(s) Timestamp Level Source Name Type Description
System Explorer	

Figure 6. ADRV9040 Board Gets Populated Under Attached Hardware When ACE Successfully Interfaces to ADS10-V1EBZ

If the loading screen is not seen, the user can attempt to update the platform files again. In case issues persist, the user may navigate to **Tools** > **System Explorer** > **Debug**, and read back FPGA Address 0x43000000 to compare against a good setup.

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A Home	Start		
Systems	Attached Hardware		
Plug-in Manager			
Remoting Console	ADRV9040 Board No daughterboards delected		
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Firmware Programmer	Events Updating platform files. This may take a while		×
Macro Tools	Timestamp Level Source Name Type Description		
System Explorer			
EEPROM Recovery Tool			
SDP-K1 Recovery Tool			
Platform API Logger			
Line Check For Updates			
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Application Usage Logging	Automatically Scroll New Events Show all events		ents
Help Settings	Ready	i	2



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QUICK START GUIDE

Start 🗙 System 🗙 ADRV9040 🗙 Use Case Selector	X CFR X Program Settings X Debug X		System Explorer
SPI REGISTERS	FPGA (DEBUG)	CPU MEMORY DUMP	Expand All Collapse All
SPI Write	FPGA Write	CPU Memory Dump	▲ Subsystem_1 ADR/9040 Platform
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Write Read	Write Read	Dump Memory	Program Settings

Figure 8. Platform Files Version Can Be Verified by Reading Back FPGA Address 0x43000000 from the Debug Page

CPU memory dump can be taken for analysis as shown in Figure 8. Browse to the directory. Once the directory is selected, the memory dump automatically gets saved.

The ADRV904x plugin can be launched with a hardware connection from the **Start** page by double clicking the **ADRV9040 Board** icon under **Attached Hardware**. It can also be run in configurator only mode, without hardware, to explore various ADRV904x configurations. The plugin looks and feels the same when launched with or without hardware, but a hardware connection is essential for programming the ADRV904x device and evaluating performance through runtime pages.

The **Tools** menu on the ACE panel can be used to display **System Explorer** for navigating the different pages included with the ADRV904x plugin. These pages are briefly described, and can be navigated as follows:

- ▶ **Configurator** pages: create, modify, program, and export ADRV904x use cases by setting up the following:
 - ► Top Level Config (see Figure 10): maps various Tx/Rx Profile Assignment and ORx Profile Assignment channels to profiles, export the current state of the configurator as a JSON use case, view the device Open Help File, and access the Configurator pages.
 - Subsequent Configurator pages can be used to configure the local oscillator (LO), carrier digital up conversion (DUC), transmitter, carrier digital down conversion (DDC), receiver, observation receiver, and JESD settings to arrive at and validate a desired ADRV904x use case.
 - Power Analysis: estimate power consumption in time division duplex (TDD) and frequency division duplex (FDD) modes for a configured use case.
- **Use Case Selector**: load and program a previously generated ADRV904x use case. This page allows the following:
 - Loading the Configurator pages above with an existing use case as a starting point, and then the user modifies settings as needed to derive a new use case.
 - Bypassing the **Configurator** pages and programming an existing use case as is.
- ▶ AD9528 Clock Settings: generate the desired ADRV904x device clock using the AD9528 clock chip on the CE board.
- ▶ Init Pages: set ADRV904x initialization parameters including the following:
 - Tx Init and Rx Init settings, calibrations, post multichip synchronization (MCS) init TRX_CTRL pin assignments, and transmitter to observation receiver mappings.
- Program the ADRV904x (if connected with hardware) from the following:
 - Use Case Selector: if running the selected use case default settings, refer to Figure 11. If running a modified use case, use a ADRV904x configurator at the top level as shown in Figure 11.
 - ▶ Track the ADRV904x device programming phases though the ACE **Events** window, as shown in Figure 11.
- Program Settings: enable exporting software resource files for the chosen configuration and init parameters. These files can then be integrated into the user application code.
- ▶ Runtime: evaluate the ADRV904x device performance through the following:
 - Transmitting JESD data or NCO tones using the Tx Vectors page.
 - Capturing receiver data using either on-chip random access memory (RAM) or JESD through the Rx (Capture) page.
 - ► Capturing observation receiver data using on-chip RAMs or JESD through the ORx (Capture) page.

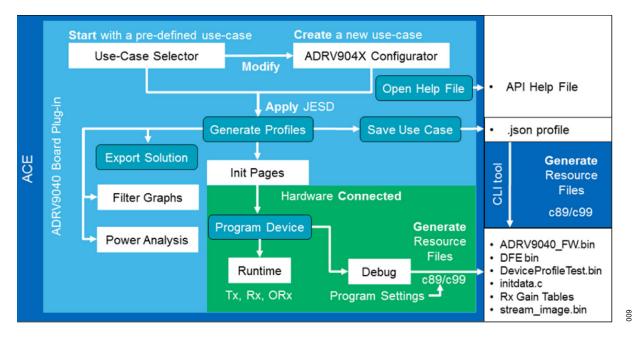


Figure 9. A Typical ADRV904x Programming Flow Where the User Programs a Use Case and Generates Software Resource Files

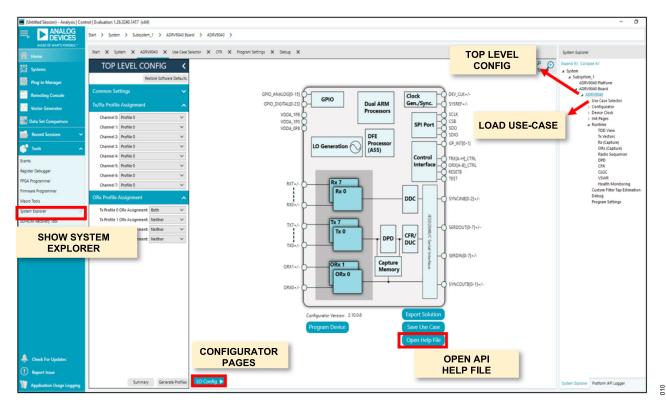


Figure 10. Launching the ADRV904x Plugin Opens the ADRV904x Configurator Top Level Config Page

USE CASE SELECTOR

This page allows the user to load the ADRV904x configurator with a predefined use case by taking the following steps:

- 1. Select the desired use case from Use Case Selector as shown in Figure 11.
- 2. Click Generate Profiles to load the selected use case settings into the ADRV904x configurator pages, or

3. Click **Program** to program the ADRV904x device using the default settings from the selected use case. Clicking **Program** automatically runs **Generate Profiles**, overriding any previous user inputs to the **Configurator** pages.

New use cases can also be added to the **Use Case Selector** page by either providing a directory to load multiple JSON files from or by providing direct paths to each JSON file to be added. To add new use cases, take the following steps:

- 1. Navigate to System Explorer > Use Case Selector.
- 2. Click Add Use Case Source to add a new directory to the use case list. This directory is then displayed as a new tab.
- 3. Alternatively, the user can add one JSON file at a time by selecting Load Use Case. This creates a new Misc. Files tab and multiple use cases can be added to this tab as well.

Once the **Configurator** pages are loaded by generating profiles, the user must then modify the selected use case default settings as shown in Figure 11. Such a modified use case must be programmed from the ADRV9040 **Top Level Config** page as previously shown in the ADRV904x Plugin Overview section. The modified use case can also be exported as a .json file from the ADRV9040 **Top Level Config** page.

Important: the ADRV904x device can be programmed from two different pages within the plugin. Programming behavior changes between these two buttons, and care must be taken to retain and program any configuration changes intended by the user. The two different pages are as follows:

- ► Use Case Selector page > Program
 - Click the Program button to program the ADRV904x with the default configuration for a selected use case.
 - ▶ Clicking this button reloads the **Configurator** pages, which overrides any changes made by the user.
- ► ADRV904x Top Level Config page > Program device
 - Click the Program button to program the current state of the Configurator pages (as modified by the user).

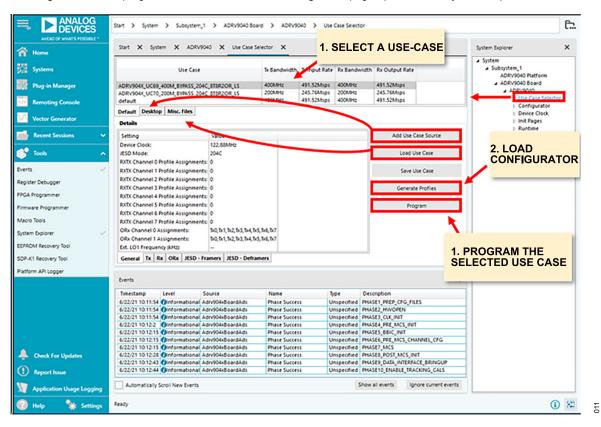


Figure 11. Loading a Predefined Use Case from Use Case Selector Page

DEVICE PROGRAMMING

Clicking either of the **Program** button from the **Top Level Config** page or the **Use Case Selector** page, which executes the 10 programming phases tabulated in Table 1.

Table 1. Description of ADRV904x Programming Phases and Order of Execution	n
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Phase	Description
PHASE1_PREP_CFG_FILES	This phase generates stream, central processing unit (CPU), digital front end (DFE), and profile binaries. This phase also copies resource files to a location available to the application processor interface (API) for the remainder of the program sequence.
PHASE2_HWOPEN	This phase calls open on the available devices on the board.
PHASE3_CLK_INIT	This phase sets up and initializes the AD9528 clock chip on the board.
PHASE4_PRE_MCS_INIT	This phase calls the ADRVGen6 PreMcsInit broadcast API function. This includes loading the CPU, stream, and profile binaries, along with the Rx gain tables.
PHASE5_BBIC_INIT	This phase sets up and initializes the available baseband processor (ADS10-V1EBZ FPGA).
PHASE6_PRE_MCS_CHANNEL_CFG	This phase calls the ADRVGen6 PreMcsInit non broadcast API function.
PHASE7_MCS	This phase calls the ADRVGen6 Multi-Chip Sync (MCS) API sequence.
PHASE8_POST_MCS_INIT	This phase calls the ADRVGen6 PostMcsInit API function and initializes calibrations.
PHASE9_DATA_INTERFACE_BRINGUP	This phase initializes the data interface on the board (JESD204B/C).
PHASE10_ENABLE_TRACKING_CALS	This phase enables tracking calibrations after full initialization and post data interface bring up.

PROGRAMMING ERRORS

Setup issues with the evaluation system, such as the CE board missing a power or clock input can cause the ADRV904x device programming to error out. ACE Tools > Events window allows the user to monitor programming progress across multiple phases and identify a phase that may have triggered an error event as shown in Figure 12. Detailed error messages can be accessed from ACE AppTrace.log file: C:\Users\%USERPROFILE%\AppData\Local\Analog Devices\ACE\AppTrace.log.

Note that this log gets overwritten every time the user restarts ACE. Occasionally, multiple **AppTrace.log** files may be generated, and the most recently modified log file contains error information from the last programming attempt.

ACE Report Issue can be used for accessing AppTrace.log and reporting any unclear errors to Analog Devices for support.

Table 2. Common Programming Errors and Error Resolution

Programming Error	Resolution
There was a problem programming the device (Phase: PHASE3_CLK_INIT). See the trace log for more information.	Check the REFA clock input to AD9528. Also verify that the REFA input from the clock source matches the REFA clock frequency set on the AD9528 clock settings
	page.
There was a problem programming the device (Phase: PHASE5_BBIC_INIT). See the trace log for more information.	Verify that platform files are up to date, see the ADS10-V1EBZ Platform Files Update section.
There was a problem programming the device (Phase: PHASE6_PRE_MCS_CHANNEL_CFG). See the trace log for more information.	Ensure that the CE board is powered up.

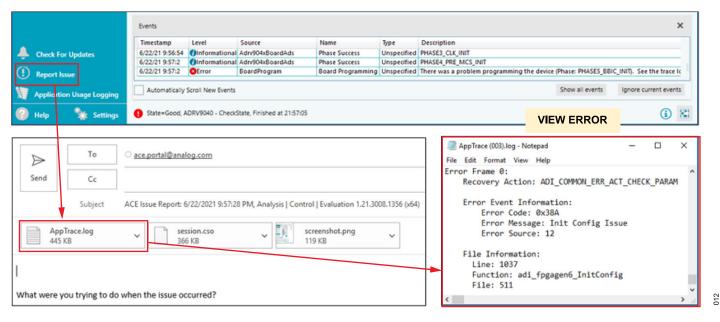


Figure 12. Procedure for Viewing Error Messages from ACE AppTrace.log File

The ADRV904x **Configurator** pages enable the user to arrive at a desired use case configuration by exploring different options available for configuring various subsystems of the ADRV904x, including the following:

- ▶ Setup of the CDUC, transmitter, CDDC, receiver, and observation receiver datapaths.
- > Preview of the frequency graphs (analog, digital, and composite) for the receiver, transmitter, and observation receiver.
- ▶ JESD data interface parameters for the framers and deframers.
- ▶ LO settings.

The user must start from a known state by loading a use case from the **Use Case Selector** page and clicking on **Generate Profiles** to load the ADRV904x **Configurator** pages with a desired configuration. This function generates the transmitter, receiver, and observation receiver datapath configurations along with their corresponding filter responses for each enabled profile, as described in the following sections. Alternatively, the user can start from the default state of the **Configurator** pages (as preloaded when the ADRV904x plugin is launched) and then provide inputs to the various **Configurator** pages.

TOP LEVEL CONFIGURATION

On the **Top Level Config** page, the user can assign profiles for each of the transmitter, receiver, and observation receiver channels as shown in Figure 13. The configurator pairs receiver and transmitter channels together for profile assignment. For example, the user can assign Tx0/Rx0 to one profile and Tx1/Rx1 to a different profile. However, each ORx channel can be assigned separate profiles as needed. This grouping of channels for profile assignment is not a hardware constraint but it is a consequence of the current configurator format. Profile assignment flexibility allows an 8T8R ADRV904x device configuration to be split in various ways, such as two 4T4R configurations.

Note that the term profile is not the same as a use case. A use case refers to an ADRV904x device configuration, which consists of one or more profiles, where profiles are a set of configuration parameters applied to a group of transmitter/receiver/observation receiver datapaths. This grouping by profile minimizes the time needed to set up a use case as each datapath is not configured individually.

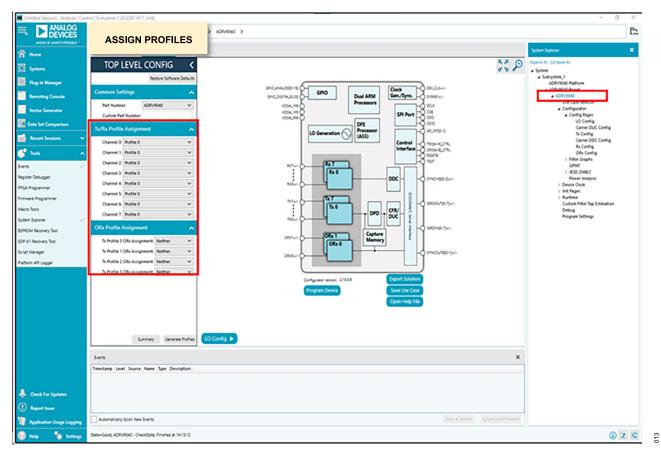


Figure 13. Top Level Config Page Showing All Tx/Rx/ORx Assigned to Profile 0

LO CONFIGURATION

After setting the desired profile mappings on the **Top Level Config** page, the user can navigate to the **LO Config** page. Click on the **LO Config** button at the bottom of the **Top Level Config** page as shown in Figure 14.

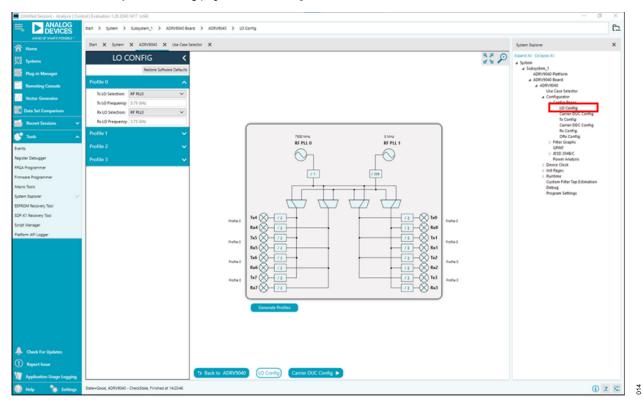


Figure 14. LO Config Page Showing ADRV904x LO Generation Setup for Given LO Frequency

On the LO Config page, the user can set the LO frequency for each of the receiver and transmitter channels per profile, as assigned on the Top Level Config page. The LO Selection dropdown box allows the user to select between RF PLL0 and RF PLL1 as the source of each LO. The accompanying block diagram is then updated when the user clicks on Generate Profiles.

Note that profile generation requires all the **Configurator** pages to be set up correctly, otherwise errors might occur. An error is also displayed if the user selects an out of range or invalid setting for any of the available parameters. These error messages can be accessed from the left panel of the ACE under **Tools** > **Events**. If at any point the configurator is put into a bad state, the user can click on **Restore Software Defaults** to return to a known good state as shown in Figure 14.

Once profiles are generated without error, the LO diagram updates to show a high level view of the LO generation setup inside the ADRV904x device for all assigned profiles, which includes the mux connections, radio frequency (RF) phase locked loop (PLL) voltage controlled oscillator (VCO) frequencies, and dividers used per receiver and transmitter channels. Figure 14 shows the LO Config page with the LO set to 3.75 GHz.

LO Frequency Change Steps

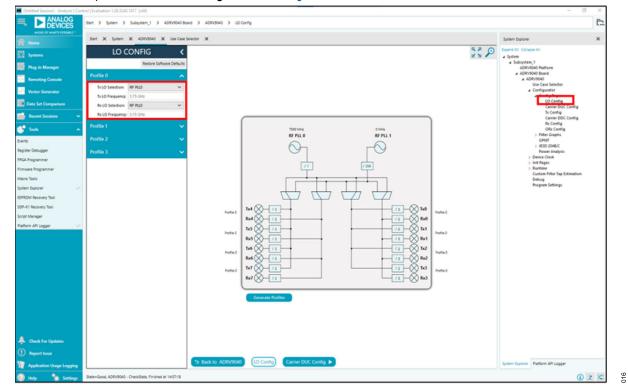
The following steps describe the LO frequency change and other procedures associated with configuration changes:

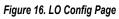
1. Select the desired use case from Use Case Selector and Generate Profiles as shown in Figure 15.

CAD OF WHAT'S POSSIBLE -	Start X System X ADRVS	040 🗙 Use Case Selector 🗙									System Explorer	
-		Use Case	Tx Bandwidth	Tx Input Rate	Rx Bandwidth	Rx Output Rate	To Carrier Bate	To Castier Bill	Rx Carrier Rate		Expand All Collapse All	
in Manager		UN CAN	Band O. OMHI	Band D. Ohlsps	Band D. Chillio	Band O. Ohips	CO. 122.88Msps		CO 122.88Mips		System Subsystem_1 ADR/9040 Platform	
			Band 1: OMHz	Band 1: OMsps	Band 1: CMIHz	Band 1: Chilsps	C1: OMsps C2: OMsps	C1: 0MHz C2: 0MHz	C1: 0Msps C2: 0Msps	C11C	ADRV9040 Example	
ting Console	ADRV904X_UC74_1x100M_CA_37508	M_LO_204C_BTBR2OR					C3: OMsps C4: OMsps C5: OMsps	C3: 0MHz C4: 0MHz C5: 0MHz	C3: OMsps C4: OMsps C5: OMsps	CB-C CA-C CS-C	Use Care Selector	
Serverator							C6: 0Msps C7: 0Msps	CE OMHE C7: OMHE	C6: 0Msps C7: 0Msps	C6 C	Config Pages LO Config	
t Comparison			Band 0: 0MHz Band 1: 0MHz	Band 0: OMsps Band 1: OMsps	Band 0: 0AHz Band 1: 0AHz	Band 0: Ohtsps Band 1: Ohtsps	CD: 122.88Msps C1: 61.44Msps CD: 014ms	C1: SOMHE		C0:8 C1:5 C2:0	Carrier DUC Config	
t Sessions 🗸 🗸	ADRV904X_UC75_40M_50M_80M_CA	A_204C_8T8R2OR					C2: OMsps C3: OMsps C4: 61.44Msps C5: OMsps C6: OMsps	C2: 0MHz C3: 0MHz C4: 40MHz C5: 0MHz C6: 0MHz	C2: DMsps C3: DMsps C4: 61,44Msps C5: DMsps C6: DMsps	C3 C C4 4	Tx Centig Carrier DDC Config	
~										CS: 0 C6: 0	Rx Config ORx Config	
			Band 0: 0MHz Band 1: 0MHz	Band D: OMsps Band 1: OMsps	Band D. OMMIZ Band 1: OMMIZ	Band 0: Ohtsps Band 1: Ohtsps	C7: 0Msps C0: 122.88Msps C1: 122.88Msps	C7: 0MHz C0: 100MHz C1: 100MHz	C7: 0Msps C0: 122.88Msps C1: 122.88Msps	CT: C C0: 1 C1: 1	 Filter Graphs GPNT 	
iger	ADRV904X_UC78_2x100M_CA_600M	IN NO PULL IN THE PLAT		band it strings	Desired of Amount	same is simply	C2: OMsps C3: OMsps C4: OMsps	C2 0MH2 C3 0MH2	C2: 0Msps C3: 0Msps	C2-0	 JESD 2048/C Power Analysis 	
ner	ADRIVIDE OCTO 2X100H CALICOL	(23,040,0044,00,2040,8184204						C4: OMIH2 C5: OMIH2 C6: OMIH2	C4: 0Msps C5: 0Msps C6: 0Msps	C& C CS: 0 C6: 0	 Device Clock Init Pages 	
ammer			Band C: OMHz	Band D: OMsps	Band D: OARIS	Band O: Ohtops	C7: 0Msps C0: 122.88Msps	C7. 05/842	C7: 0Mips C0: 122.88Mips	C7.0	 Runtime Custom Filter Tap Estimation 	
			Band 1: 0MHz	Band 1: OMsps	Band 1: 04942	Band 1: Ohtsps	C1: 122.88Msps C2: 0Msps	C1: 100MHz C2: 0MHz	C1: 122.86Msps C2: 0Msps C3: 0Msps	C2: 0	Debug Program Settings	
ery Tool	ADRV904X_UC79_2x100M_CA_600M	U16_DPD_DUAL_LO_204C_8T8R2OR					C3: OMsps C4: OMsps C5: OMsps	C3: 0MHz C4: 0MHz C5: 0MHz	C4 0Msps C5: 0Msps	C3: C C4: C C5: C		
ery Tool							C& OMsps C7: OMsps	CR: DMHz C7: DMHz	C6: 0Msps C7: 0Msps	CR C CT: C		
e			Band 0: 0MHz Band 1: 0MHz	Band 0: OMsps Band 1: OMsps	Band D: OMH2 Band 1: OMH2	Band 0: OMsps Band 1: OMsps	CD: 122.88Msps C1: 122.88Msps C2: 0Msps	CD 100MHz C1 100MHz C2 0MHz	C0: 122.88Msps C1: 122.88Msps C2: 0Msps	C0 1 C1 1 C2 C		
oper 💛	ADR/904X_UC80_2/100M_CA_600M	L2G_DPD_SINGLE_L0_204C_8T8R2OR					C3: OMsps C4: OMsps C5: OMsps	C3: 0MHz C4: 0MHz	C3: 0Msps C4: 0Msps	Ch C CR C CR C		
	Default											
	Details							-				
	Setting Part Number:	Value ADRV9040							Use Case Source			
	Device Clock: JESD Mode:	122.88M94z 204C							Load Use Case			
	RXTX Channel © Profile Assignment RXTX Channel 1 Profile Assignment	ts: 0							Save Use Case			
	RXTX Channel 2 Profile Assignment	ts: 0						6	enerate Profiles			
	RXTX Channel 3 Profile Assignment RXTX Channel 4 Profile Assignment								Program			
	RXTX Channel 5 Profile Assignment RXTX Channel 6 Profile Assignment								enerate Init Files			
For Updates	RXTX Channel 7 Profile Assignment ORx Channel 0 Assignments:											
rt Issue	ORx Channel 0 Assignments: ORx Channel 1 Assignments: Ext. LO1 Frequency 8/H2:	Tel2, Tel2, Tel2, Tel2, Tel4, Tel5, Tel6, Tel7 Tel2, Tel2, Tel2, Tel2, Tel4, Tel5, Tel6, Tel7										

Figure 15. Generate Profiles

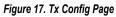
2. Update the RF PLL frequencies under LO Config as shown in Figure 16.





3. Update Tx Synthesis BW Upper Edge and Tx Synthesis BW Lower Edge from the Tx Config as shown in Figure 17.

TX CONFI	G <	55 P	Expand All Collapse All
General	^		▲ ADRV9040 Board
			▲ ADRV9040 Use Case Selector
Datapath Mode: AUTO	~		# Configurator
Profile 0	^		 Config Pages LO Config
Tx Sample Rate (Band 0):	122.88 Msps		Carrier DUC Config Tx Config
Tx Signal BW (Band 0):	100 MHz		camer obc comig
LO Frequency:	3.75 GHz		Rx Config ORx Config
Tx RF Center Freq (Band O):	3.75 GHz		Filter Graphs
Enable Band 1:	False		GPINT b JESD 2048/C
Tx Sample Rate (Band 1):	0 Msps		Power Analysis
Tx Signal BW (Band 1):	0 Hz	Tx Config	 Device Clock
LO Frequency:	3.75 GHz		 Init Pages Runtime
Tx RF Center Freq (Band 1):	0 Hz	Profile 0 vvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvvv	Custom Filter Tap Estimation
Tx Synthesis BW Upper Edge	: 3.9625 GHz		Debug Program Settings
Tx Synthesis BW Lower Edge	3.5375 GHz		
Tx Synthesis Bandwidth:			
DPD On Chip:			
LUT Count:	40	CPR Insuit DPD Caleful 12 12 Read 0.00 C Insuit 1471 For	
LUT Depth:	32 🗸	DUC: 12238 Maps 0 MHz 12238 MHz 481.52 MHz End DUC Latency 0 no DUC: 0 MHz 12238 MHz Currier DUC Latency 12166 no	
DPD Mode:	1	JED Latency 200 ms	
Linear Term:	3	Generate Profiles Tx Filter Graph	
Ct DPD Enable:	1		
Actuator Sample Rate:	0 Msps		
Sample Count:	10		
Profile 1	~		
Profile 2	~		
rofile 3	<u> </u>		



4. This step is optional for profiles with CDUC/CDDC enabled only. Go to **Carrier DUC Config** as shown in Figure 18 and **Carrier DDC Config** as shown in Figure 19, and update carrier NCO frequencies.

	Profile 0	nfig v								Tx Cor Carrier
	Filter	Rate	BW	Center				_	MED O MH2	Rx Cor ORx C
Carrier 0	90	♥ 122.88	Maps 100 MHz	3.75 GHz		Π	Atten		-O-(; Bard	Filter Grag GPINT JESD 2048
Carrier 1	Filter Off	v 0	Maps 0 Hz	0 Hz		-	Atten	 - [1]-		⇒ Jesto Zoke Power An ⊳ Device Clock ⊳ Init Pages
Carrier 2	Filter Off	ب ٥	Maps 0 Hz	0 Hz		-	Atten	 - <u>†</u> 1-	BEER O MHz) Runtime Custom Filter Debug Program Setti
Carrier 3	Filter Off	v 0	Maps 0 Hz	0 Hz		H,	Atten	 - [† 1]-		and a set of the set o
Carrier 4	Filter Off	v 0	Maps 0 Hz	0 Hz	Defam	Crossbar	Atten	 - [1]-		
Carrier 5	Filter Off	v 0	Maps 0 Hz	0 Ha			Attan	 - [1]-		
Carrier 6	Filter Off	¥ 0	Maps 0 Hz	0 Hz			Atten	 - [1]-	DICO O MHz	
Carrier 6	Filter Off	v 0	Maps 0 Hz	0 Hz		-	Atten	 - † 1		

Figure 18. Carrier DUC Config Page

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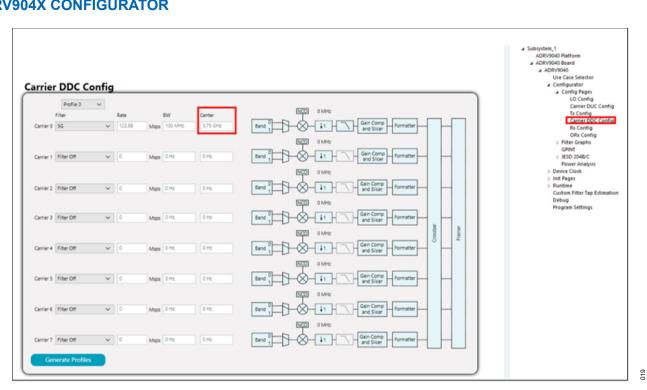


Figure 19. Carrier DDC Config Page

5. Click on Program Device as shown in Figure 20. Once the part is programmed successfully, the updated LO frequency is ready to use.

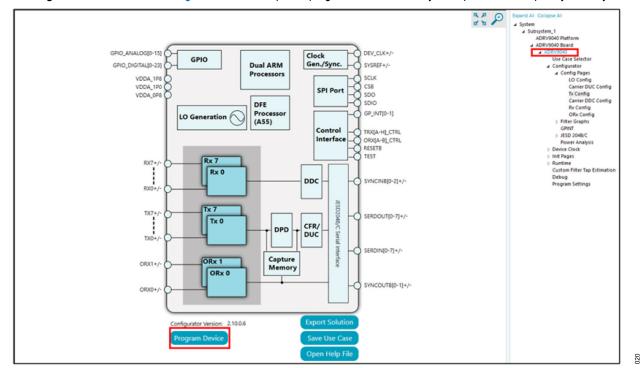


Figure 20. Top Level Program Page

TRANSMITTER CONFIGURATION

CDUC Configuration

The CDUC is a part of the ADRV904x DFE on the transmit path and performs the function of filtering and up converting the baseband signal centered on DC to a higher sample rate. The CDUC has five half-band filters that support up to 32× interpolation. A maximum of eight carriers are supported by the CDUC. The output of the CDUC is passed to one of the two band digital upconverters (BDUC) to combine the composite carriers into a passband signal.

The CDUC configurator helps reduce the implementation time by compiling the most efficient CDUC configuration for a given set of carrier requirements. The ADRV904x CDUC supports the LTE and new radio (NR) air interface standards. To access the **Carrier DUC Config** page, navigate to ADRV9040 > **Configurator** > **Config Pages** > **Carrier DUC Config** in the system explorer window as shown in Figure 21.

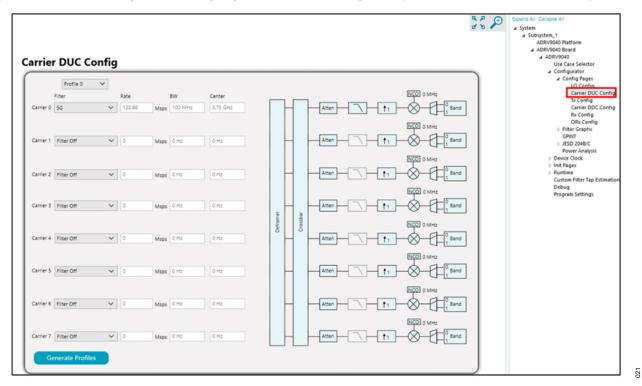


Figure 21. CDUC Configurator Page

Unless the user has loaded an existing use case with carriers enabled, the **Carrier DUC Config** page launches in carrier DUC bypassed mode. The user can configure the carriers by following the compilation flow below (refer to Figure 22):

- 1. Select one of the four profiles for which to apply the CDUC settings.
- 2. Select the channel filtering option appropriate for the carrier as described in Table 3.
- 3. Configure the carrier settings including the sample rate for the carrier as described in Table 3, which indicates the bandwidth of the carrier and the RF center frequency of the carrier. Note that the carriers must be arranged in descending order of sample rates with Carrier 0 assigned to the carrier with the highest sample rate, and Carrier 7 assigned to the carrier with the lowest sample rate.
- 4. Once the carrier settings are entered, click on Generate Profiles to ensure that the carrier settings for the use case entered are valid. The Tx Config, ORx Config, and JESD pages must also be updated before this step can be completed successfully, as described below:
 - ▶ The CDUC configurator automatically resolves the interpolation rate from the carrier configuration entered by the user in Step 3.
 - The CDUC configurator automatically resolves the carrier NCO shift and the band assignment (Band 0 or Band 1) based on the separation between the carriers and to minimize the net bandwidth per band.

Note that additional parameters must be updated while compiling and generating the profiles in the **Carrier DUC Config** page settings, including the following:

- The digital predistortion (DPD) analysis bandwidth (transmitter synthesis bandwidth) and internal DPD enable must be entered on the Tx Config page as shown in Figure 23.
- The ORx sample rate for the ORx, which is mapped to the transmitter that corresponds to the CDUC being configured (see the Observation Receiver Configuration section).
- ▶ The JESD settings and sample crossbar assignments (see the JESD Configuration section).

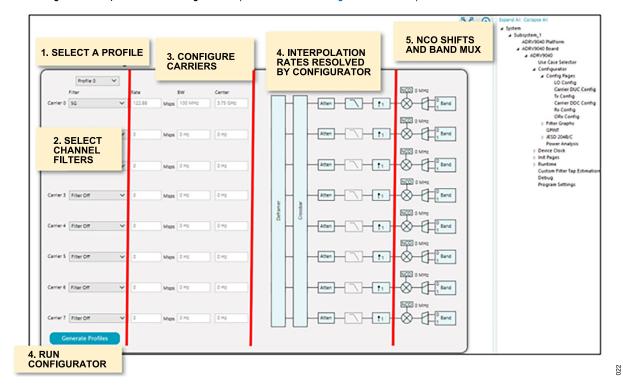


Figure 22. Compilation Flow of CDUC Settings

Filter Option	Carrier Bandwidth (MHz)	Recommended Carrier JESD Sample Rate (MSPS)	Comments
LTE	5	7.68	
	10	15.36	
	20	30.72	
5G NR	15, 20, 25	30.72	
	30, 40, 50	61.44	
	60, 70, 80, 90, 100	122.88	
High Bandwidth 5G NR	100	122.88	Recommended when there are more than two NR100 carriers
Filter Off (Carrier En)	N/A	N/A	Offers NCO shift only without any channel filtering
Filter Off	N/A	N/A	Disables CDUC (bypass mode)

The ADRV904x transceiver supports a maximum of 800 MHz synthesis bandwidth for DPD analysis. The transmitter synthesis upper and lower edges must be configured in the **Tx Config** page to generate profiles successfully in the **Carrier DUC Config** page.

Refer to the example shown in Figure 24 where the passband consists of 3× NR100 carriers centered at 3.4 GHz, 3.6 GHz, and 3.7 GHz, respectively. The gray shaded region shown in Figure 24 represents the 800 MHz synthesis bandwidth spanning from 3.1 GHz (transmitter synthesis BW lower edge) to 3.9 GHz (transmitter synthesis BW upper edge). For this example, configure the transmitter synthesis BW upper edge as 3.9 GHz and the transmitter synthesis BW lower edge as 3.1 GHz on the **Tx Config** page as shown in Figure 23.

Start X System X ADRV9040 X CFR X	Program Settings X Use Case Selector X	System Explorer
TX CONFIG Restore Software Defaults Centres 1 Designer Moder Designer Moder Rasse Software Defaults Profile 0 Tr Sample Rate (Band 0) Dio Software Defaults Dio Software Defaults To Sample Rate (Band 0) Dio Tregumony To Software Profile O Ta Sample Rate (Band 0) Dio Tregumony To Software Profile Rate (Band 1) Ta Sample Rate (Band 1) Ta Software Profile Domotion Diff On Onig Uff Contri Diff Domotion Diff Domotione	Tx Config	System Explore # System # Subjectures.3 # ADRYODD Insures. # ADRYODD Insures. # ADRYODD Insures. # ADRYODD Insures. # Conceptone Configuration # Control Doc Config. # Co
Actuator Sample Rate: 0 Msps Sample Count: 10		
Profile 1 🗸 🗸		
Profile 2 🗸 🗸		
Profile 3 🗸		
ridad 3		
	Back to ADRV9040 Carrier DUC Config R Config Carrier DDC Config	Platform API Logger System Explorer

Figure 23. Tx Synthesis BW Configuration

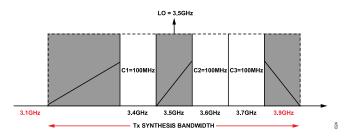


Figure 24. Tx Synthesis Bandwidth Configurator for CDUC Configurator

Transmitter Datapath Configuration

After configuring the **Carrier DUC Config** page as desired, click on the **Tx Config** to navigate to the **Tx Config** wizard as shown in Figure 25. **Tx Config** can also be accessed from under **Config Pages** in system explorer.

On the **Tx Config** page, the user can assign the following parameters for different profiles as mapped to transmitter channels on the top level configuration page as follows:

- Datapath mode to set the data path interpolation rate, effectively selecting the transmitter DAC rate.
- ▶ Transmitter synthesis bandwidth. DPD correction BW as specified by the upper and lower edge user inputs.
- ▶ Enable on-chip DPD.

The transmitter sample rates, RF center frequencies, signal bandwidths, and Band 1 enable are solved by the configurator based on the user inputs to the **Carrier DUC Config** page. The configurator solved outputs populate correctly only after all the configurator pages have been setup and the user clicks on **Generate Profiles**, which is accessible from various pages. Once generated, the **Tx Config** figure updates to show the transmitter data path configuration for the profile selected as shown in Figure 25. Blocks colored blue are enabled and blocks that remain opaque are bypassed. Calculated datapath latencies are also shown.

Note that the Tx sample rates displayed in the **Tx Config** wizard on the left panel are different from the DUC0/DUC1 sample rates displayed in the **Tx Config** figure. The wizard sample rates are the input rates to the carrier DUC, and the figure sample rates are calculated based on the interpolation ratios resolved on the **Carrier DUC Config** page as shown in Figure 22. This is visualized and summarized in Table 4.

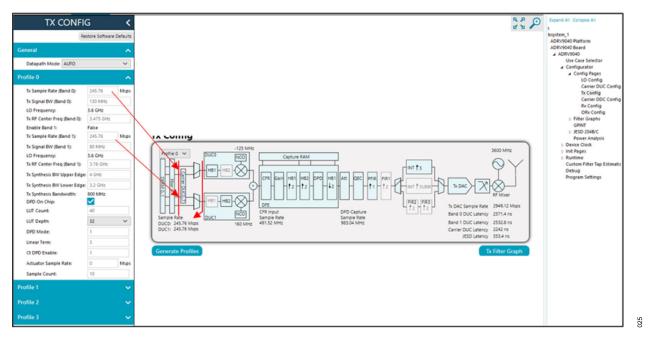


Figure 25. Transmitter Configuration Setup Diagram

Table 4. Comparison of Tx Sample Rates Displayed in the Tx Config Wizard and the Tx Datapath Figure

Location	Parameter	Description
Tx Config Panel	Tx sample rate (Band 0) and Tx sample rate (Band 1)	This is the carrier DUC input sample rate
Tx Config Figure	DUC0 sample rate and DUC1 sample rate	This is the carrier DUC output sample rate, and the band DUC input rate

Transmitter Filter Graph

Corresponding transmitter filter graphs for the profile selected on the **Tx Config** page can be viewed by clicking on the **Tx Filter Graph** button. This helps the user understand the frequency response of the selected transmitter profile. An example is shown in Figure 26.

The transmitter filter graph includes the band and carrier digital composite responses, the programmable finite impulse response (PFIR) to RF response, the analog composite response (including the transmitter DAC), and the full composite response. The user can change the profile selection on the **Tx Config** page to display the filter graphs corresponding to the selected profile.

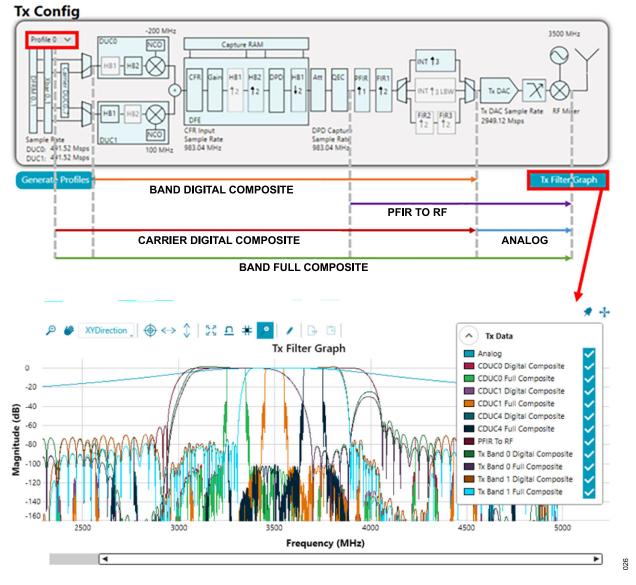


Figure 26. Transmitter Datapath Filter Graphs

RECEIVER CONFIGURATION

CDDC Configuration

The CDDC on the ADRV904x DFE offers the capability to convert a receiver passband signal into composite carriers centered at DC. The ADRV904x CDDC supports LTE and NR air interface standards, and a maximum of eight carriers. Similar to the CDUC, there are five half-band filters per carrier that support a maximum decimation rate of 32×.

To access the **Carrier DDC Config** page, navigate to ADRV9040 > **Configurator** > **Config Pages** > **Carrier DDC Config** in the system explorer window as shown in Figure 28.

me	r DDC Cor	ntig						▲ ADRV9040 Use Case Selector
	Profile 0	~						Configurator Config Pages
	Filter		Rate		BW	Center	NCO 0 MHz	LO Config Carrier DUC Con
Carrier 0		~	122.88	Mene	80 MHz	3.76 GHz	Band 0 Gain Comp Formatter	Tx Config
contract o	~			mapa			and Slicer	Carrier DDC Col Rx Config
							NCO 40 MHz	ORx Config
Carrier 1	5G	~	61.44	Mses	50 MHz	3.435 GHz	Band 1	 Filter Graphs GPINT
								JESD 2048/C Power Analysis
							NCO 0 MHz	Device Clock
Carrier 2	Filter Off	~	0	Msps	0 Hz	0 Hz	Band 0	 Init Pages Runtime
								Custom Filter Tap Estin
							NCO 0 MHz	Debug Program Settings
Carrier 3	Filter Off	~	0	Msps	0 Hz	0 Hz	Band 1	
							45 MHz	
Carrier 4	5G	~	61,44	Msps	40 MHz	3.52 GHz	Band 0 - 44 - Gain Comp - Formatter - Form	
							ICO 0 MHz	
Carrier 5	Filter Off	~	0	Msps	0 Hz	0 Hz	Band 1	
							NCO 0 MHz	
Carrier 6	Filter Off	~	0	Msps	0 Hz	0 Hz	Band 1	
							NCO 0 MHz	
	Etc. 04	~	0		Cons.	0 Hz	Band 0 Formatter	
Jamer 7	Filter Off	~		Msps	0 Hz	0 Hd	Band 1 +1 +	
~	nerate Profiles							

Figure 27. CDDC Configuration in the ADRV904x Configurator GUI

Unless the user loads an existing use case with carriers enabled, the **Carrier DDC Config** page launches in carrier DDC bypassed mode. The user can then configure the carriers by following the compilation flow as shown in Figure 29 or taking the following steps:

- 1. Select one of four profiles for which to apply the CDDC settings.
- 2. Select the channel filtering option appropriate for the carrier as described in Table 3.
- 3. Configure the carrier settings including the sample rate for the carrier as described in Table 3, the bandwidth of the carrier, and the RF center frequency of the carrier. Note that the carriers must be arranged in descending order of sample rates with Carrier 0 assigned to the carrier with the highest sample rate and Carrier 7 assigned to the carrier with the lowest sample rate.
- 4. Once the carrier settings are entered, click on Generate Profiles to ensure that the carrier settings for the use case entered are valid. Note that the JESD configuration must be updated, which include sample crossbar assignments, in parallel with updating the carrier settings to arrive at a valid configuration.
- 5. The CDDC configurator automatically resolves the decimation rates, carrier NCO shifts, and band assignments from the carrier configuration entered by the user in Step 3.

SELECT A PROFILE	- 3. C	CONFIGURE		5. BAND MUX, NCO SHIFTS, INTERPOLATION AS RESOLVED BY CONFIGURATOR	I Subsystem_1 ADRV9040 Platform ▲ ADRV9040 Board ▲ ADRV9040 Use Case Selector ▲ Configurator
Profile 0 🗸 🗸					∡ Config Pages
Filter	Rate	BW	Center		LO Config Carrier DUC Config
Carrier 0 5G 🗸	122.88	Msps 80 MHz	3.76 GHz	Band 1 - Formatter	Tx Config Carrier DDC Config
				NCO 40 MHz	Rx Config ORx Config
Carrier 1 5G 🗸 🗸	61.44	Msps 50 MHz	3.435 GHz	Band 1 Formatter	Filter Graphs GPINT
					JESD 204B/C Power Analysis
2. SELECT					 Device Clock Init Pages
CHANNEL FILTERS	0	Msps 0 Hz	0 Hz		Runtime Custom Filter Tap Estimation
			1949-1949 - 1949 - 1949 - 1949 - 1949 - 1949 - 1949 - 1949 - 1949 - 1949 - 1949 - 1949 - 1949 - 1949 - 1949 - 1		Debug Program Settings
Carrier 3 Filter Off 🗸 🗸	0	Msps 0 Hz	0 Hz	Band 1 - Formatter - Formatter	
Carrier 4 5G 🗸 🗸	61.44	Msps 40 MHz	3.52 GHz	Band 1	
Carrier 5 Filter Off 🗸 🗸	0	Msps 0 Hz	0 Hz	Band 1 - Formatter	
Carrier 6 Filter Off 🗸 🗸	0	Msps 0 Hz	0 Hz	Band 1 Gain Comp And Slicer	
				INCO 0 MHz	
Carrier 7 Filter Off 🗸 🗸	0	Msps 0 Hz	0 Hz	Band 1 Formatter	
Generate Profiles					
4. RUN	-				
ONFIGURATOR					



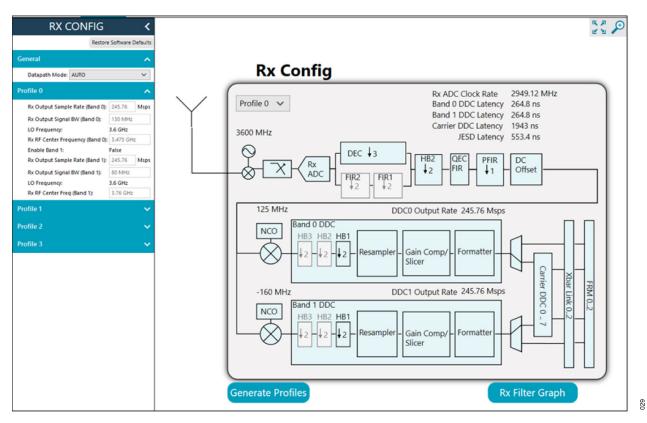


Figure 29. Receiver Configuration Wizard and Datapath Diagram Updated After Generating Profiles

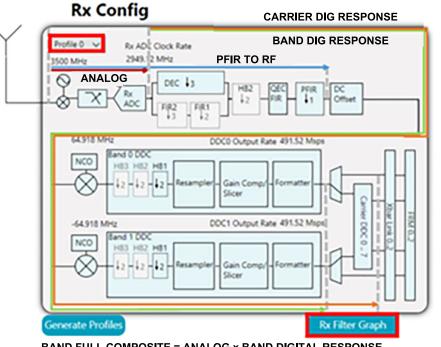
Receiver Datapath Configuration

The user can navigate to the **Rx Config** page found under the **Carrier DDC Config** page or by using the ACE system explorer. The **Rx Config** page allows the user to change the Rx datapath decimation to select a different ADC rate through the datapath mode drop down menu.

Once the carrier DDC is resolved and profiles are generated, the **Rx Config** page updates to show the receiver datapath configuration and latencies as shown in Figure 29. Note that the profiles can only be generated successfully after all configurator pages have been setup. A dropdown box on the top left corner of the **Rx Config** page allows the user to view configurator solutions for different profiles as defined from the Top Level Configuration section. Blocks that are colored blue are enabled and blocks that remain opaque are bypassed.

Receiver Filter Graph

A corresponding receiver filter graph of the profile can be viewed via the **Rx Filter Graph** button. This helps the user understand the frequency response of the selected receiver profile. An example is shown in Figure 30. The Rx filter graph includes the digital composite response, Rx ADC response, and the analog composite response. The user can change the profile selection on the **Rx Config** page to see the corresponding filter response for the selected profile.



BAND FULL COMPOSITE = ANALOG x BAND DIGITAL RESPONSE CARRIER FULL COMPOSITE = ANALOG x CARRIER DIGITAL RESPONSE

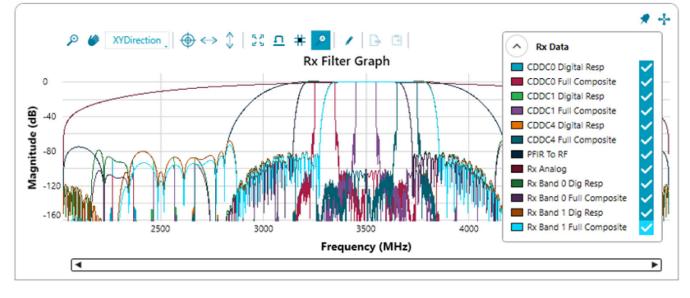


Figure 30. Receiver Datapath Filter Graphs

OBSERVATION RECEIVER CONFIGURATION

Observation Receiver Datapath

On the ORx Config page, the user can set the following:

- ▶ Observation receiver ADC CLK rate mode to switch between ADC rates.
- ▶ Observation receiver enables for ORx0/ORx1.
- ▶ Output sample rates for the enabled ORx channels.

Figure 31 shows the **ORx Config** input fields on the left panel. After configuring the remaining configurator pages and clicking **Generate Profiles**, which can be accessed from multiple **Configurator** pages, the observation receiver datapath figure is updated. Switch the displayed parameters of the figure between different profiles and ORx configurations via the drop down boxes at the top left corner of the datapath figure. Blocks that are colored blue are enabled and blocks that remain opague are bypassed.

Note that once the **Carrier DUC** page is populated, the **ORx Config** page sample rates must be updated to allow the configurator to solve for an appropriate transmitter DPD rate. In case the configurator is unable to resolve the DPD rate, Figure 32 shows the error message. The user must then try alternative carrier DUC rates or modify the observation receiver sample rates.

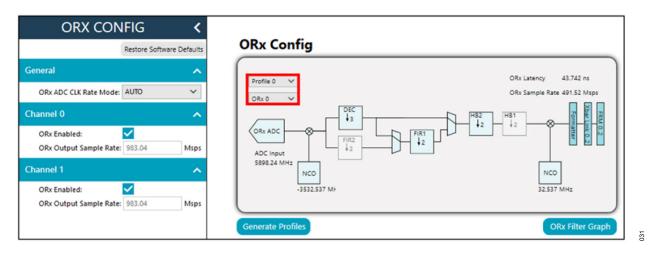


Figure 31. Observation Receiver Configuration Setup Diagram

Events						
Timestamp	Level	Source	Name	Туре	Description	1
4/8/21 5:16:12	SError	GenerateProfiles	Generate Configuration	ValueInvalid	Could not generate a combined configuration with with all these profiles	032

Figure 32. One Possible Error if the Configurator is Unable to Resolve the Tx DPD Rate

Observation Receiver Filter Graph

A corresponding observation receiver filter graph of the profile can be viewed via the **ORx Filter Graph** button. This helps the user understand the frequency response of the selected observation receiver profile. An example is shown in Figure 33.

In the current configurator version, only the digital composite response of the observation receiver datapath is displayed, but analog filter contributions are not included. The user can change the profile selection on the **ORx Config** page to see the corresponding filter response for a selected profile.

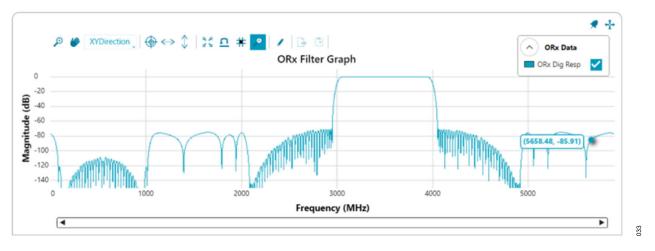


Figure 33. Observation Receiver Digital Filter Composite Frequency Response

JESD CONFIGURATION

The ADRV904x transceiver supports JESD interface standards for the serializer/deserializer (SERDES) link between the baseband unit and the transceiver to facilitate high-speed high bandwidth data transfer. The JESD interface on the ADRV904x transceiver supports JESD 204B and JESD 204C standards, and SERDES lane rates of up to 24.3 Gbps over eight serial lanes.

The JESD configuration pages can be accessed by expanding the menu under ADRV9040 > **Configurator** > **JESD 204B/C** in the system explorer window. The user can start with the basic JESD page as shown in Figure 34, and navigate to the appropriate sample crossbar settings page depending on whether the CDUC or CDDC is enabled, as described in Table 6 and Table 7. The JESD configuration inputs required from the user are listed in Table 6 and Table 7.

JESD Configuration Page	Description
Basic JESD	JESD 204B/C mode selection
	Framer/deframer NP and L assignments
	Framer/deframer lane crossbar assignments
	Framer/deframer selections for Rx/Tx/ORx sample crossbar auto assignment
Component Carrier Sample Crossbar	Converter sample crossbar settings for enabled deframer(s) when CDUC is enabled Converter sample crossbar settings for enabled framer(s) when CDDC is enabled
General Sample Crossbar	Converter sample crossbar settings for enabled deframer(s) when CDUC is bypassed Converter sample crossbar settings for enabled framer(s) when CDDC is bypassed

Table 5. Overview of JESD Configuration Pages

BASIC JESD <					53 P	Expand All: Collapse All: A System
Restore Software Defaults						a subtystem_t
						ADRV9040 Platform ADRV9040 Board
General A	Deframer0	Clane 0 v	Framer0	LS Framer Out 0 V	-OLane 0	ADRV9040
Enable 204C Input: 🗹		Clane 1 Y		0 Mbps Framer Out 1 V		Use Case Selector
Framer 0 LS Enable:	10 Rate 10 77 Mana	Ulane 2 V	Lane Rate 16220.16 Mbps IQ Rate 30.72 Msps	0 Mopt Pramer Out 2 V		A Config Pages
Framer 1 LS Enable:	M 128	Clane 3 V	M 128	0 Framer Out 3 V		LO Config
Framer Inputs	1	Unused V Unused V	L 4	0 Unused V Unused V		Carrier DUC Config Tx Config
		Unused V	F 64	0 Unused V		Carrier DDC Config
Framer 0 Np Input: 16 V			NP 16	0 Unused V		Rx Config
Framer 0 M Input: 128	5 1		5 1	0		ORx Config Filter Graphs
Framer OL Input: 4	1 1		E 1	0		GPINT
Framer 1 No Input: 16 V	Scramble O		Scramble O			 IESD 2046/C
	JESO204C Enabled 🔾		RS0254C Enabled 🔘	0		Basic Jesd Component Carrier
Framer 1 M Input: 0						Component Carrier Sample Crossbar
Framer 1 L Input: 0	Denameri	Unused V Unused V	Framer1	LS Unused V Unused V		Component Carrier Sample Crossbar Lane Mapping
Framer 2 Np Input: 16 V	Lane Rate 0 Mops	O timest M	Lane Rate 0 Mbps	0 Mbgs		General Sample Crossbar Power Analysis
Framer 2 M Input: 0		O lineard he	IQ Rate 0 Maps	0 Maps Unused V		Device Clock
	1. ° K	Unused 🤟		o Unuted V	-Olane 4	Init Pages
Framer 2 L Input: 0		O Unused ❤	, 0	0 Unuted V) Runtime
LS Framer Inputs		O Unused Y	κ 0	0 Unused V	0	Custom Filter Tap Estimation Debug
		Unused V	NP 0	0 Unuted V	-Olane 7	Program Settings
Framer Assignment	5 0		5 0	0		
	Scanble O		Scramble O	•		
Rx0: None V	JESD204C Enabled O		/ES0204C Enabled O	0		
Rx1: None V						
Rx2 None V			Framer2	Unuted 🗸	-OLane 0	
Rx3: None V			Lane Rate O Mbpt	Unused 🛩		
			IQ Rate 0 Maps	Unused V		
			м 0	Unuted V Unuted V		
RxS: None V			L 0	Unuted V Unuted V		
Rx6: None 🗸				Unuted V		
Rx7: None 🗸			NP 0		-Olane 7	
ORx0 None Y			5 0			
	Auto-Assign Sample Crossbars		E 0			
ORx1: None V			Scramble O /ES0204C Enabled O			
Rx Framer Sample Assignment	Apply /ESD Settings		Assess Paper 0			
Framer 0: Band 0/Band 1 ~						
Framer 1: Sand 0/Sand 1 🗸 🗸						
Deframer inputs	Back to ADRV9040	x Config Ba	component C	arrier Sample Crossbar 🕨		System Explorer Platform API Logger

Figure 34. Basic JESD Configuration Page

Table 6. ADRV904x JESD Deframer Configuration Parameters

JESD Deframer (Tx Side) Configuration					
Parameters	Description				
Deframer Lane Crossbar	Lane crossbar settings between the deserializer and the deframer in the Tx path.				
DAC Sample Crossbar	Sample crossbar settings between the deframer output and the DAC input.				
Μ	Number of virtual digital to analog converters on the transmitter side. Each carrier is mapped to a virtual pair of 30.72 MSPS DAC converters. For example, if each transmitter is transmitting three carriers at 30.72 MSPS, then the total number of virtua converters = 8 channels × 3 carriers per channel × 2 converters for I and Q per carrier = 48 virtual converters. To consider another example, if each transmitter is transmitting three carriers at 61.44 MSPS, then the total no. of virtual converters = 8 channels × 3 carriers per channel × 2 converters for I and Q per carrier × 2 = 96 virtual converters, where the last factor of two is sample rate (61.44 MSPS) ÷ virtual converter rate (30.72 MSPS).				
NP	DAC sample bit-width.				
L	Number of input lanes at the ADRV904x deserializer input.				
F	Number of DAC bytes per frame of data.				

Table 7. ADRV904x JESD Framer Configuration Parameters

JESD Framer (Rx Side) Configuration

Parameters	Description
Framer Lane Crossbar	Lane crossbars settings between the framer and the serializer in the Rx path.
ADC Sample Crossbar	Sample crossbar settings between the ADC output and framer input.
Μ	Number of virtual analog to digital converters on the receiver side. Each carrier is mapped to a virtual pair of ADC converters. For example, if each receiver is transmitting three carriers, then the total number of virtual converters = 8 channels × 3 carriers per channel × 2 converters per carrier = 48 virtual converters.
NP	ADC sample bit width.
L	Number of output lanes at the ADRV904x serializer output.
F	Number of ADC bytes per frame of data.

Basic JESD

The user can select between JESD 204B and JESD 204C under **General** settings. Additionally, the user can configure **NP** and **L** under **Framer Inputs** or **Deframer Inputs**, and assign serial lanes to selected framers/deframers on the figure itself. Note that the JESD parameters displayed in Figure 36 are calculated and updated once the configurator runs successfully and generates the desired profiles. Profiles can be generated from the basic JESD page via **Apply JESD Settings**, but the sample crossbar settings must be updated before profiles can be generated without error.

To simplify the JESD configuration process, the **Basic JESD** page supports automatic assignment of sample crossbar settings, which means that the user can select assignments for framers and deframers for the receiver, observation receiver, and transmitter samples. Additional flexibility is provided where the user can select either Rx Band 0, Rx Band 1, or both Rx Band 0/Rx Band 1 samples to be assigned to a given framer under **Rx Framer Sample Assignment**. ORx samples can be assigned to any framer(s) or left unassigned as desired. **Sample Assignment** dropdowns are only enabled for framers with valid NP and receiver assignments.

In the example shown in Figure 35, all Rx channels are mapped to Framer 0 such that both Band 0 and Band 1 samples are assigned to Framer 0. This way, the user can autoassign each receiver band to separate framers, or leave one or both bands unassigned. Alternatively, observation receiver samples are left unassigned such that observation receiver data are not sent over JESD. If desired, observation receiver samples can be assigned to a framer under **Framer Assignment**. However, band sample selections do not apply to the observation receiver. Therefore, the **Rx Framer Sample Assignment** section only needs to reflect the desired receiver band sample assignments.

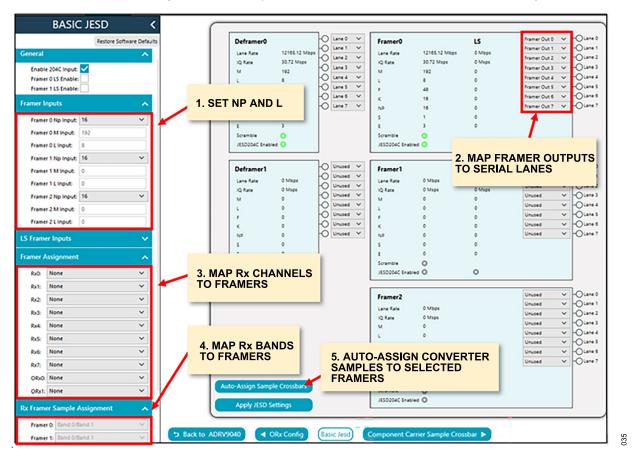


Figure 35. Steps to Configure JESD Framers and Specify User Preferences for Sample Crossbar Auto Assignment

On the transmitter side, the user can configure the deframer NP and L settings and assign serial lanes to deframer inputs. The user can also map transmitter channels and bands to either deframer for setting up sample crossbar auto assignment. Sample assignment dropdowns are only enabled for deframers with valid NP and transmitter assignments. In the example shown in Figure 36, all transmitter channels Band 0 and Band 1 samples are mapped to Deframer 0.

Once framer/deframer assignments and band selections are made, the user can click on **Auto-Assign Sample Crossbars** to automatically populate the sample crossbar pages. Clicking **Apply JESD Settings** runs the configurator, and the framer/deframer figures are updated to display the JESD parameters solved by the configurator.

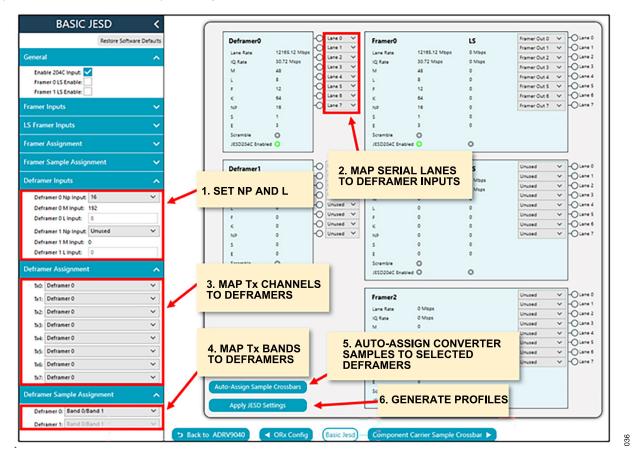


Figure 36. ADRV904x JESD Deframer Configuration

Note that if the carrier configuration is updated at any time through either the **Carrier DUC** or **Carrier DDC** pages, the user can rerun **Auto-Assign Sample Crossbars** to eliminate any configurator errors associated with stale sample crossbar assignments (from a previous carrier configuration).

Important: the current implementation of the **Basic JESD** page does not expose observation receivers deinterleaving parameters. This will be addressed in upcoming releases.

Component Carrier Sample Crossbar

The sample crossbar page is used to assign CDUC/CDDC samples to enabled deframers/framers. The sample crossbar assignments can be auto populated as described in the Basic JESD section. Auto assignment can serve as a starting point, and the sample assignments can be modified manually as desired.

The user can navigate between different deframers and framers through the drop down menus at the bottom of the figure. Note that deframer/framer Entry 0 through Entry 191 are split across six assignment pages, which can also be switched from the dropdown menus at the bottom. Each entry can be assigned to the desired component carrier sample by selecting a channel and a corresponding carrier sample on each row as shown in Figure 37.

Once the sample crossbar is configured as desired, the user can click on Apply JESD Settings to generate profiles.

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ADRV904X CONFIGURATOR

I	Channel 0	~	Component Carrier 01	~	0	Channel 0	~	Component Carrier 01
1	Channel 0	~	Component Carrier 0 Q	~	1	Channel 0	~	Component Carrier 0 Q
	Channel 0	~	Component Carrier 01	~	2	Channel 0	~	Component Carrier 01
	Channel 0	~	Component Carrier 0 Q	~	3	Channel 0	~	Component Carrier 0 Q
	Channel 0	~	Component Carrier 01	~	4	Channel 0	~	Component Carrier 0 1
	Channel 0	~	Component Carrier 0 Q	~	5	Channel 0	~	Component Carrier 0 Q
	Channel 0	~	Component Carrier 01	~	6	Channel 0	~	Component Carrier 0 1
	Channel 0	~	Component Carrier 0 Q	~	7	Channel 0	~	Component Carrier 0 Q
	Channel 0	~	Component Carrier 11	~	8	Channel 0	~	Component Carrier 11
	Channel 0	~	Component Carrier 1 Q	~	9	Channel 0	~	Component Carrier 1 Q
	Channel 0	~	Component Carrier 1 I	~	10	Channel 0	~	Component Carrier 1 I
	Channel 0	~	Component Carrier 1 Q	~	11	Channel 0	~	Component Carrier 1 Q
	Channel 0	~	Component Carrier 11	~	12	Channel 0	~	Component Carrier 1 I
	Channel 0	~	Component Carrier 1 Q	~	13	Channel 0	~	Component Carrier 1 Q
	Channel 0	~	Component Carrier 1 I	~	14	Channel 0	~	Component Carrier 1 1
	Channel 0	~	Component Carrier 1 Q	~	15	Channel 0	~	Component Carrier 1 Q
	Channel 0	~	Component Carrier 41	~	16	Channel 0	~	Component Carrier 4 1
	Channel 0	~	Component Carrier 4 Q	~	17	Channel 0	~	Component Carrier 4 Q
	Channel 0	~	Component Carrier 41	~	18	Channel 0	~	Component Carrier 41
	Channel 0	~	Component Carrier 4 Q	~	19	Channel 0	~	Component Carrier 4 Q
	Channel 0	~	Component Carrier 41	~	20	Channel 0	~	Component Carrier 4 1
	Channel 0	~	Component Carrier 4 Q	~	21	Channel 0	~	Component Carrier 4 Q
	Channel 0	~	Component Carrier 41	~	22	Channel 0	~	Component Carrier 4 1
	Channel 0	~	Component Carrier 4 Q	~	23	Channel 0	~	Component Carrier 4 Q
	Channel 1	~	Component Carrier 01	~	24	Channel 1	~	Component Carrier 0 1
	Channel 1	~	Component Carrier 0 Q	~	25	Channel 1	~	Component Carrier 0 Q
	Channel 1	~	Component Carrier 01	~	26	Channel 1	~	Component Carrier 0 1
	Channel 1	~	Component Carrier 0 Q	~	27	Channel 1	~	Component Carrier 0 Q
	Channel 1	~	Component Carrier 01	~	28	Channel 1	~	Component Carrier 01
	Channel 1	~	Component Carrier 0 Q	~	29	Channel 1	~	Component Carrier 0 Q
	Channel 1	~	Component Carrier 01	~	30	Channel 1	~	Component Carrier 01
	Channel 1	~	Component Carrier 0 Q	~	31	Channel 1	~	Component Carrier 0 Q
	Deframer 0	~	Ĵ 1 of6 Page 1	0	1 of 3	Framer 0	~ 0	1 of 6 Page 1 🗸

Figure 37. Component Carrier Sample Crossbar Showing Auto Assigned Samples

General Sample Crossbar

This sample crossbar page is used to assign DAC/ADC samples to enabled deframers/framers when CDUC/CDDC is bypassed. The sample crossbar assignments can be auto populated as described in the Basic JESD section. Auto assignment can serve as a starting point, and the sample assignments can be modified manually as desired.

The user can navigate between different deframers and framers through the drop down menus at the bottom of the figure. Note that framer Entry 0 through Entry 63 are split across two assignment pages, which can also be switched from the drop down menu underneath the framer selection. Each entry can be assigned to the desired converter sample by selecting a sample on each row as shown in Figure 38.

Once the sample crossbar is configured as desired, the user can click on Apply JESD Settings to generate profiles.

Sample 0	~	0	Rx0 Band 0 I	~
Sample 1	~	1	Rx0 Band 0 Q	~
Sample 2	~	2	Rx1 Band 01	~
Sample 3	~	3	Rx1 Band 0 Q	~
Sample 4	~	4	Rx2 Band 0 I	~
Sample 5	~	5	Rx2 Band 0 Q	~
Sample 6	~	6	Rx3 Band 0 I	~
Sample 7	~	7	Rx3 Band 0 Q	~
Sample 8	~	8	Rx4 Band 0 I	~
Sample 9	~	9	Rx4 Band 0 Q	~
Sample 10	~	10	Rx5 Band 0 I	~
Sample 11	~	11	Rx5 Band 0 Q	~
Sample 12	~	12	Rx6 Band 0 I	~
Sample 13	~	13	Rx6 Band 0 Q	~
Sample 14	~	14	Rx7 Band 01	~
Sample 15	~	15	Rx7 Band 0 Q	~
Unused	~	16	Unused	~
Unused	~	17	Unused	~
Unused	~	18	Unused	~
Unused	~	19	Unused	~
Unused	~	20	Unused	~
Unused	~	21	Unused	~
Unused	~	22	Unused	~
Unused	~	23	Unused	~
Unused	~	24	Unused	~
Unused	~	25	Unused	~
Unused	~	26	Unused	~
Unused	~	27	Unused	~
Unused	~	28	Unused	~
Unused	~	29	Unused	~
Unused	~	30	Unused	~
Unused	~	31	Unused	~
1 of 2 Defram			1 of 3 Framer 0	v 1
Derram			1 of 2 Page 1	

Figure 38. General Sample Crossbar Page Showing Auto Assigned Samples

POWER ANALYSIS

A separate **Power Analysis** page provides power estimates for the ADRV904x configuration set using the preceding configurator pages. The user can navigate to this page from the **Power Analysis** button underneath the **General Sample Crossbar** or by using the ACE system explorer.

Figure 39 shows a snapshot of the **Power Analysis** page.

The **Power Analysis** page displays the current draw and power consumed per voltage supply rail, as split between the transmitter, receiver, observation receiver, and common blocks. The common block shows the combined power consumed by the VCOs, dividers, JESD blocks, general purpose input/output (GPIO) blocks, and certain digital blocks.

On the left panel, the user can switch between configuration options to compare the associated power consumption as follows:

ADRV904X CONFIGURATOR

- Datapath Mode sets transmitter/receiver datapath interpolation/decimation rations to select different transmitter DAC and receiver ADC rates.
- ORx ADC CLK Rate Mode selects between observation receiver ADC clock rates.
- Tx Attenuation sets transmitter attenuation per channel, or copy Channel 0 attenuation setting to all channels by ticking the Use Shared Tx Attenuation Value checkbox. Tx Attenuation is set to 6 dB by default.
- **DPD** parameters input resource utilization for a desired DPD model. Two examples are shown in Figure 40.

neral		^	Power An	nalysis			B
Dutapath Mode: ORx ADC CLK Rate Mod	AUTO M AUTO	~	Block	1.8V (mA)	1.0V (mA)	0.8V (mA)	
Attenuation		^	Tx	970	1141	11162	EXPORT DISPLAYED
Use Shared Tx Attenuat	tion Value:		ORx	126	485	635	POWER NUMBERS
Channel 0: Channel 1:	6	d5 d5	Rx	72	620	1715	2121
Channel 2	6	et	Common	405	886	375	1915
Channel 3	6	45	Common	4/2	609	3/3	1915
Channel 4:	6	48	1	Duty Cycle (%): Tx 70	Total Current (mA):	Total Power(mW): 17073
Channel Sc	6	đđ		Rx 30	1.8V 1573 1.0V 3132	Use FDD Mo	de
Channel &	6	dB	1	ORx 70			
	6 ed here are only used fo hey do not program the		Generate Profile		all process, vol factors: 1.8V 1.0V	tage, and temperatu / -> add 10% / -> add 20%	nominal values. To determine maximum ranges re (PVT) conditions, apply the following scaling
Attenuation values liste estimate calculation. Th levels. file O	hey do not program the	r the power attenuation	UPDATE PO	OWER	all process, vol factors: • 1.8% • 1.0% • 0.8%	tage, and temperatu / -> add 10% / -> add 20% / -> add 15% + 3125	re (PVT) conditions, apply the following scaling mA
Attenuation values liste estimate calculation. Th levels. office 0 DPD On Chip:		r the power attenuation		OWER	all process, vol factors: 1.8% 1.0% 0.8% All current and	tage, and temperatu / -> add 10% / -> add 20% / -> add 15% + 3125 / power figures are av	re (PVT) conditions. apply the following scaling
Attenuation values liste estimate calculation. In levels. file 0 DPD On Chip: LUT Count	hey do not program the	r the power attenuation	UPDATE PO	OWER	all process, vol factors: 1.8% 1.0% 0.8% All current and occur during in	tage, and temperatu / -> add 10% / -> add 20% / -> add 15% + 3125 i power figures are a ormal operation or ir	re (PVT) conditions, apply the following scaling mA rerage values and do not account for transients
Attenuation values liste estimate calculation. Th levels. Gile O DPD On Chip: LUT Count:	tey do not program the	ri the power attenuation	UPDATE PO	OWER	all process, vol factors: 1.8v 0.6v All current and occur during n All current and Current consu	tage, and temperatu / -> add 10% / -> add 20% / -> add 15% + 3125 / power figures are a ormal operation or ir power figures assum mption values report	re (PVT) conditions, apply the following scaling mA verage values and do not account for transients total internal calibrations are enabled. real tracking calibrations are enabled.
Attenuation values late estimate calculation. Th levels. Alle O DPD On Chip: LUT Count: LUT Count: LUT Count: LUT Count: LUT Ought: DPD Mode: Linear Term:	tey do not program the	ri the power attenuation	UPDATE PO	OWER	all process, vol factors: 1.8v 0.6v All current and occur during n All current and Current consu	tage, and temperatu / -> add 10% / -> add 20% / -> add 15% + 3125 / power figures are a ormal operation or ir power figures assum mption values report	re (PVT) conditions, apply the following scaling mA verage values and do not account for transients vitial internal calibration. ne all tracking calibrations are enabled.
Attenuation values lata estimate calculation. Th levels. DPD On Ohip: LUT Count: LUT Count: LUT Cogen: LUT Depth: DPD Mode: Linear Term: Ct DPD Enable:	ey do not program the 40 32 1 3 1	rt be pover attenuation	UPDATE PO	OWER	all process, vol factors: 1.8v 0.6v All current and occur during n All current and Current consu	tage, and temperatu / -> add 10% / -> add 20% / -> add 15% + 3125 / power figures are a ormal operation or ir power figures assum mption values report	re (PVT) conditions, apply the following scaling mA verage values and do not account for transients total internal calibrations are enabled. real tracking calibrations are enabled.
Attenuation values lata estimate calculation. Th levels. Ville O DPO On Chip: LUT Ceunt: LUT Ceunt: LUT Cesthi DPO Mode: Linear Term: Ct DPO Enable: Actuator Sample Rate:	ey do not program the 40 32 1 3 1	ri the power attenuation	UPDATE PO	OWER	all process, vol factors: 1.8v 0.6v All current and occur during n All current and Current consu	tage, and temperatu / -> add 10% / -> add 20% / -> add 15% + 3125 / power figures are a ormal operation or ir power figures assum mption values report	re (PVT) conditions, apply the following scaling mA verage values and do not account for transients total internal calibrations are enabled. real tracking calibrations are enabled.
Attenuation values lata estimate calculation. Th levels. Ville O DPO On Chip: LUT Ceunt: LUT Ceunt: LUT Cesthi DPO Mode: Linear Term: Ct DPO Enable: Actuator Sample Rate:	rey do not program the 40 32 1 3 1 0	rt be pover attenuation	UPDATE PO	OWER	all process, vol factors: 1.8v 0.6v All current and occur during n All current and Current consu	tage, and temperatu / -> add 10% / -> add 20% / -> add 15% + 3125 / power figures are a ormal operation or ir power figures assum mption values report	re (PVT) conditions, apply the following scaling mA verage values and do not account for transients total internal calibrations are enabled. real tracking calibrations are enabled.
Attenuation values lata estimate calculation, TN levels. Affle O DPD On Chip: LUT Count. LUT Count. LUT Corpor. DPD Mode: Linear Term: Ct DPD Enable: Actuator Sample Rate: Sample Count.	rey do not program the 40 32 1 3 1 0	r De power Riternation	UPDATE PO	OWER	all process, vol factors: 1.8v 0.6v All current and occur during n All current and Current consu	tage, and temperatu / -> add 10% / -> add 20% / -> add 15% + 3125 / power figures are a ormal operation or ir power figures assum mption values report	re (PVT) conditions, apply the following scaling mA verage values and do not account for transients total internal calibrations are enabled. real tracking calibrations are enabled.
Attenuation values lata estimate calculation, Tri levels. VELO DPD On Onip: LUT Count: LUT Count: LUT Cogetiv: DPD Mode: Linear Term: CLDPD Enable: Actuator Sample Rate: Sample Count: VELO	rey do not program the 40 32 1 3 1 0	r Da pouer Miteraution	UPDATE PO	OWER	all process, vol factors: 1.8v 0.6v All current and occur during n All current and Current consu	tage, and temperatu / -> add 10% / -> add 20% / -> add 15% + 3125 / power figures are a ormal operation or ir power figures assum mption values report	re (PVT) conditions, apply the following scaling mA verage values and do not account for transients total internal calibrations are enabled. real tracking calibrations are enabled.

Figure 39. Power Analysis Settings and Estimates

Typical 200M	IHz DPD Resources	Maximum	DPD Resources
DPD On Chip:	✓	DPD On Chip:	✓
LUT Count:	26	LUT Count:	50
LUT Depth:	64 🗸 🗸	LUT Depth:	64 🗸
Complex Multiplier Count:	6	Complex Multiplier Count:	29
Sample Count:	8	Sample Count:	15
Sample Count.	0	Sample Courts	15

Figure 40. Example DPD Model Parameters for Power Analysis

On **Power Analysis**, the user can enter the TDD duty cycle for the transmitter, receiver, and observation receiver channels to get an estimate of the power consumed in TDD mode. The **Use FDD Mode** button allows the user to get the total power consumed when all transmitter, receiver, and observation receiver channels are enabled, which essentially sets the duty cycle to 100% for receiver/transmitter and observation receiver modes. The user must click on **Generate Profiles** to update the power numbers.

ADRV904X CONFIGURATOR

A typical usage of the **Power Analysis** is to get an estimate of the power consumed in different states of the ADRV904x as shown in Figure 41 to Figure 45. The displayed power numbers can also be exported to a CSV file by using the export button to the top left of the **Power Analysis** diagram.

Standby Mode

This mode represents the total standby current consumed when all transmitter, receiver, and observation receiver channels are in the off state.

Block	1.8V (mA)	1.0V (mA)	0.8V (mA)	Total (mW)
Тх	226	539	0	945
ORx	9	159	0	175
Rx	30	209	184	410
Common	385	1009	0	1702
	Duty Cycle (%): Tx 0 Rx 0 ORx 0	Total Current (mA): 1.8V 650 1.0V 1916 0.8V 184	Total Power(mW):	3233

Figure 41. Example of Current Consumed in Standby Mode

Transmitter Only Mode

Transmitter only mode represents the total current consumed when only the transmit channels are enabled. All receiver and observation receive channels are in the off state.

ower	Analysis			
Block	1.8V (mA)	1.0V (mA)	0.8V (mA)	Total (mW)
Тх	1317	1466	18938	18987
ORx	9	159	0	175
Rx	30	209	184	410
Common	405	1009	188	1888
	Duty Cycle (%): Tx 100 Rx 0 ORx 0	Total Current (mA): 1.8V 1761 1.0V 2843 0.8V 19310	Total Power(mW):	21461



Observation Receiver Only Mode

Observation receiver only mode represents the total current consumed when only observation receive channel/s are enabled. All transmit and receive channels are in the off state.

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ADRV904X CONFIGURATOR

Tx ORx	226	539 693	0 933	945	
Rx Common	30 385	209	184	410	

Figure 43. Current Consumed in ORx Only Mode

Transmitter + Observation Receiver Only Mode

Transmitter + observation receiver only mode represents the total current consumed when only the transmit channel and observation receive channel/s are enabled. All receive channels are in the off state.

Power	Analysis				Ð
Block	1.8V (mA)	1.0V (mA)	0.8V (mA)	Total (mW)	
Tx	1317	1466	18938	18987	
ORx	180	693	933	1764	
Rx	30	209	184	410	
Common	405	1009	188	1888	
	Duty Cycle (%): Tx 100 Rx 0 ORx 100	Total Current (mA): 1.8V 1932 1.0V 3377 0.8V 20243	Total Power(mW):	23049	

Figure 44. Current Consumed in Tx + ORx Only Mode

Receiver Only Mode

Receiver only mode represents the total current consumed when only receive channels are enabled. All transmit and observation receive channels are in the off state.

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ADRV904X CONFIGURATOR

Power	Analysis				Ð
Block	1.8V (mA)	1.0V (mA)	0.8V (mA)	Total (mW)	
Тх	226	539	0	945	
ORx	9	159	0	175	
Rx	240	1925	7853	8640	
Common	405	1009	188	1888	
	Duty Cycle (%): Tx 0 Rx 10 ORx 0	Total Current (mA): 1.8V 880 1.0V 3632 0.8V 8041	Total Power(mW):	11648	

Figure 45. Current Consumed in Rx ONLY Mode

It is recommended that the user must estimate the TDD power by configuring ACE into the transmitter + observation receiver only mode as shown in Figure 44 and record the total power. Then the user can configure ACE in receiver only mode as shown in Figure 45 and record the total power. Finally, the user can take a weighted average of the two to get to the correct TDD power consumed for different receiver/transmitter/observation receiver duty cycles.

Note that the values reported here are steady state current and power numbers. These numbers do not account for the transients that occur during calibration.

It is also important to note that the power numbers reported here are only an estimate. Analog Devices does not run exhaustive testing to cover for all cases that can be set up using the configurator. The user must contact Analog Devices for any issues with the power consumption numbers reported by the tool.

INIT PAGES

The **Init Pages** can be used to set initialization parameters for ADRV904x device datapaths.

POST MCS INIT

If using pin mode, the **Post MCS Init** page can be used to assign TRX_CTRL pins as enables for various ADRV904x transmitter and receiver channels through user specified channel masks as shown in Figure 46. Refer to the following steps:

- 1. Set Pin Select bit mask to 1 for each TRX_CTRL pin to be configured as an enable. For instance, setting Pin Select to 0x3 selects TRXA_CTRL and TRXB_CTRL to be used as channel enables.
- 2. Set Config Select bits to select whether pin controls are updated for transmitter, transmitter alt, receiver, and receiver alt settings.
- 3. If configuring transmitter enables, map the transmitter channel mask to be enabled per TRX_CTRL pin. For example, mapping 0xFF to TRXA_CTRL allows all eight transmitter channels to be enabled by TRXA_CTRL.
- 4. If configuring receiver enables, map the receiver channel mask to be enabled per TRX_CTRL pin. For example, mapping 0xFF to TRXC_CTRL allows all eight receiver channels to be enabled by TRXC_CTRL.
- 5. Transmitter alt and receiver alt pin mappings can be assigned in the same way.
- 6. The user can program these TRX_CTRL mappings by clicking on program device from the **Top Level Config** page. Alternatively, clicking on **Configure Mappings** applies the pin mappings after initialization.

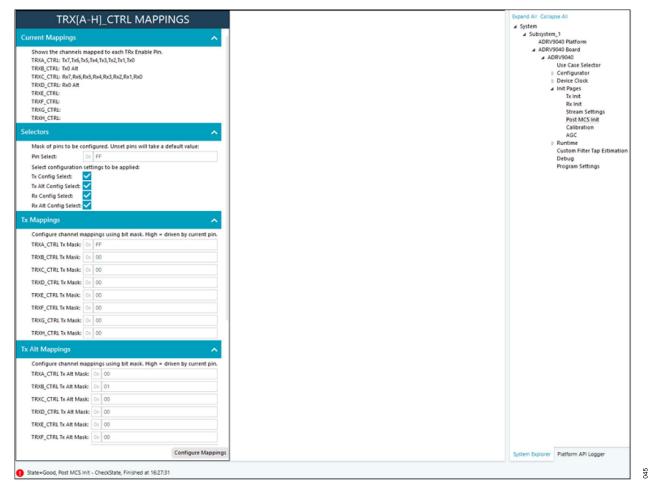


Figure 46. TRXA_CTRL to TRXH_CTRL Pins Mapped as Tx/Rx Datapath Enables on Post MCS Init Page

CALIBRATION

Device calibrations to be run during ADRV904x initialization can be enabled/disabled from **Init Pages > Calibration**. Refer to the release notes accompanying a given customer software package for more information regarding supported calibrations.

INIT PAGES

Start 🗙 System 🗙 ADRV90	40 X	Use Case Selector	×	Post MCS Init	×	Calibration	×	System Explorer
CALIBRATION SETT	TING:							Expand All Collapse All System Subsystem_1 ADRV9040 Platform
RX DC Offset init calibration: ADC Rx init calibration: ADC Orx init calibration:	Y Y Y Y							 ▲ ADRV9040 Board ▲ ADRV9040 Use Case Selector ▷ Configurator ▷ Device Clock
ADC Tx loopback init calibration Tx DAC init calibration: Tx BB filter init calibration: Tx LB filter init calibration:								✓ Init Pages Tx Init Rx Init Stream Settings
Tx LB path delay init calibration HRM init calibration: TxQEC init calibration:	~							Post MCS Init Calibration AGC D Runtime
TxLOL init calibration: Tracking Calibration	~							Custom Filter Tap Estimation Debug Program Settings

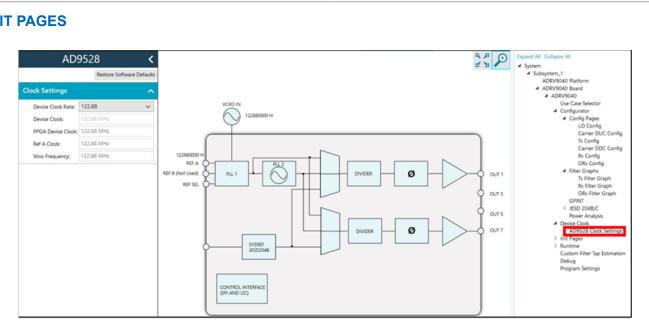
Figure 47. Calibration Page is Used to Update the Init Calibration Mask Run During Initialization

AD9528 CLOCK SETTINGS

The CE board comes with an AD9528 clock generator that takes a **Ref A Clock** input and generates the ADRV904x device clock and the FPGA device clock as outputs. The CE board includes a crystal oscillator running at 122.88 MHz voltage-controlled crystal oscillator (VCXO).

The AD9528 page can be used to program the ADRV904x using a clock input different from the default. After configuring this page, the user must program the ADRV904x from the **Top Level Config** page, the ADRV9040.

INIT PAGES



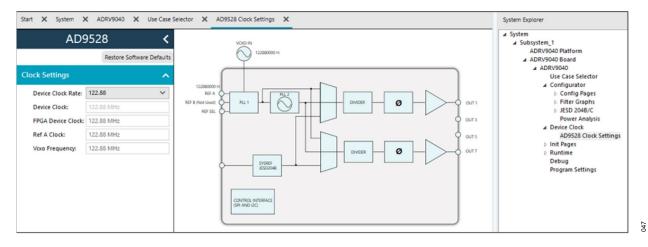


Figure 48. AD9528 Page for Changing Clock Generator Settings

Once programmed, the runtime pages can be used for testing the performance of different ADRV904x datapaths. These runtime pages provide data sourcing capability for the transmitters, and capturing functionality for the receivers and observation receivers.

TRANSMITTER VECTORS

Transmitter performance can be evaluated by sending data over the JESD link, or by generating test tones using ADRV904x on-chip NCO in each baseband of a transmitter datapath. The vector generator of ACE can be used for creating new data vectors or importing vectors from existing data files, and can also be used to change attenuation settings for each enabled transmitter.

Generating JESD Data Vectors

For illustration, a single tone vector can be generated using the following steps:

- 1. Launch Tx Vectors from System Explorer > Runtime > Tx Vectors as shown in Figure 49.
- 2. Click on Vectors to open the vector generator of ACE.
- 3. Create a new single tone vector by clicking on + besides the Single Tone Vector under common waveforms as shown in Figure 50.
- 4. Set the vector's data rate to match the transmitter sample rate (as configured in the Use Case Selector section or LO Frequency Change Steps section).
 - ▶ Data rate must match the carrier sample rate for CDUC/CDDC profiles.
 - ▶ For FDD, the play length (time) must be equal for each carrier. For example, the record length of a 122.88 MHz carrier should be four times the record length of a 30.72 MHz carrier.
 - ► Change the record length of the vector as per the sample rate.
- 5. Set the desired baseband frequency of the tone.
- 6. Select Generate Complex Data to generate a data vector containing I and Q samples.
- 7. Preview the vector to verify parameters. If needed, this vector can be exported to a text file by clicking on Export.
- 8. Switch back to the **Tx Vectors** page. However, do not close the **Vector Generator** tab completely by pressing **x**. The **Vector Generator** must remain open as a background tab for the vectors to be selectable on the **Tx Vectors** page.
- 9. Enable the desired transmitter channel(s) and transmitter observability from the Tx Vectors page.
- 10. Configure each transmitter channel data input to the intended vector, as named and defined on the Vector Generator.
 - ▶ For profiles with CDUC/CDDC enabled: user can map a specific vector to each carrier as shown in Figure 52.
- 11. Update Tx Attenuation (dB) field as needed.
- 12. Enable the QEC and LOL tracking calibrations.
- **13. Play** transmitter data continuously over JESD as shown in Figure 51. This updates the waveform and fast Fourier transform (FFT) plots to preview the loaded vectors. The transmitter RF output can then be captured using a spectrum analyzer as shown in Figure 52.
- 14. Stop halts the data transmission.

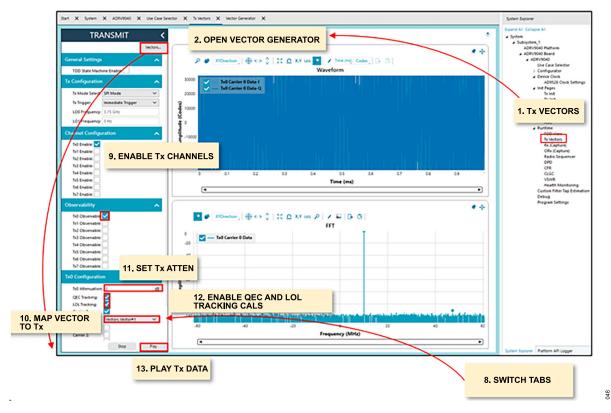


Figure 49. Tx Vectors Page is Used to Enable Tx Channels, Map Vectors to Each Enabled Tx, and Plot the Baseband Vectors

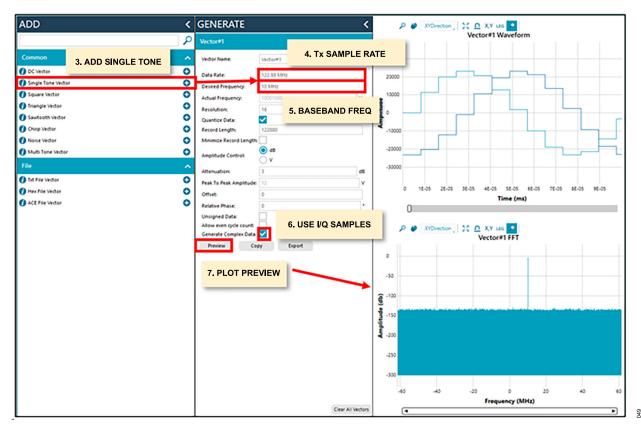


Figure 50. Steps for Generating a Complex Single Tone Vector Using ACE Vector Generator

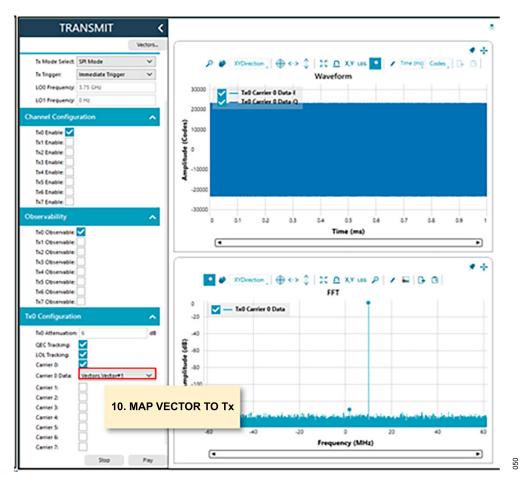


Figure 51. Tx Vector Mapping to Each Carrier

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Keysight Sp		and the second se								
KI I	RF		AC			SENSE:INT	A	ul en Dun		Jun 23, 2021
Average	/Hold	Numbe	er 100	JNO: Feet	Trig: Fre	e Run	Avgiyp	e: Log-Pwr	TRAC TYP	
		NFI		PNO: Fast 🖵 Gain:Low	Atten: 2				DE	NNNNN
				Junit				Mbr	4 2 77	5 0 GHz
			_					IVINI		79 dBm
odB/div	Ref 1	10.00 d	вm						-0.1	a delli
- ^v g										
0.00										
							1			
10.0										
20.0										
30.0										
40.0				_						
50.0										
60.0										
		Ý				2				
70.0										
						1. 1				
80.0 Hilling	dia dia d			BORNE T			din this		Stabilitions.	
at hit.	and with		1.11.1		- Martin ba	a starting the	101 (0) (101)	and the states	րեններու	الالوا المعمارية
Center 3.	76500	GHz							Span 1	00.0 MHz
Res BW				#VBW	3.0 kHz		Sv	veep 25		1001 pts)

Figure 52. Tx0 Single Tone Spectrum as Captured by a Spectrum Analyzer

Exporting and Importing JESD Data Vectors

The Vector Generator page also allows exporting and importing of vectors. The user can export a vector from Vector Generator by clicking on Export from the Generate panel as shown in Figure 53. This writes the vector out to a .txt file in the ACE export data directory C:\Users\%USERPROFILE%\AppData\Local\Analog Devices\ACE\ExportData.

This vector can be imported back into the **Vector Generator** as follows:

- 1. Click + to add a .txt file vector.
- 2. Select Complex Interleaved. ACE generated .txt vectors are a single column with I- and Q-samples interleaved.
- 3. Match data rate to the transmitter sample rate (as configured by in the Use Case Selector section or LO Frequency Change Steps section).
- 4. Click on **Preview** to confirm the vector parameters.

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ADD	< (GENERATE	< 🔎 🥔 XYDirection 💥	
	P	Vector#2	Vector#2 Wa	aveform
Common	^	Vector Name: Vector#2	# 4unplitude	
1 DC Vector	0	File Format: Complex - Interleaved	^ W .2000	XX
1 Single Tone Vector	0	File Path: Real Vector	0 5E-06 1E-05	1.5E-05 2E-05
Square Vector	0	Second File Path: Complex - Interleaved	Tir	ne (ms)
1 Triangle Vector	•	Resolution: Complex - Separate Files	0	
() Sawtooth Vector	•	Data Rate: 983.04 MHz		
() Chirp Vector	•	Preview Copy	P 🍎 XYDirection 53 Vector#2	
1 Noise Vector	0	Copy	원 0	
Multi Tone Vector	0		9 -100	
File	~		9 -100 100 100 100 100 100 100	
🚺 Txt File Vector	0			250 300 350 400 450
🕖 Hex File Vector	0			ncy (MHz)
ACE File Vector	•	c	ar All Vectors	< >

Figure 53. Importing a .txt File Vector into a Vector Generator

Setting Transmitter Attenuation

Transmitter attenuation can be set in dB for each enabled transmitter channel individually.

Note that transmitter attenuation changes are only applied when the user clicks Play.

RX (CAPTURE)

Receiver data can be captured over JESD and analyzed using the **Rx (Capture)** page as shown in Figure 54. The user must do the following:

- 1. Navigate to System Explorer > Runtime > Rx (Capture).
- 2. Confirm that the desired receiver channels are enabled. If using a link sharing profile, ensure that no observation receiver channels are enabled at this time. Observation receiver channels can be disabled from the System Explorer > Runtime > ORx (Capture) page.
- 3. Click Run Once or Run Continuously to capture data.
- 4. For profiles with CDDC enabled, the user can specify each carrier to monitor as shown in Figure 55.

Other than capturing data over JESD, the user can also capture data internally using ADRV904x RAMs. However, this method limits the data capture size and takes longer to execute. To use the internal RAM, the user must only have one receiver channel enabled on the **Rx Capture** page (and all obsrevation receivers disabled on the **ORx Capture** page). Then, the user can select DDC0/DDC1 output as **Capture Mode** and run the capture. Enabled DDC paths can be viewed from the **Rx Configuration** page.

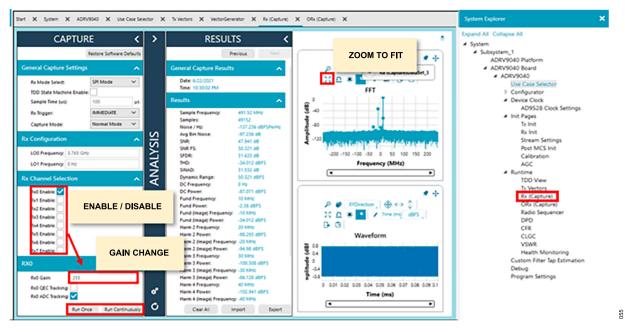


Figure 54. Rx (Capture) is Used to Capture and Analyze Receiver Outputs over JESD



Figure 55. Rx Capture with Carriers Selection

Setting Receiver Gain

The gain index for any enabled receiver channel can be changed by either entering a new gain index or by using the arrowheads to increment/decrement the gain index in steps of one. Gain changes are applied to the ADRV904x as soon as the values are updated, regardless of the data capture state whether halted or running continuously.

Enabling Receiver QEC Tracking

The user can additionally enable quadrature error correction (receiver QEC tracking) calibration for each enabled receiver as shown in Figure 56.

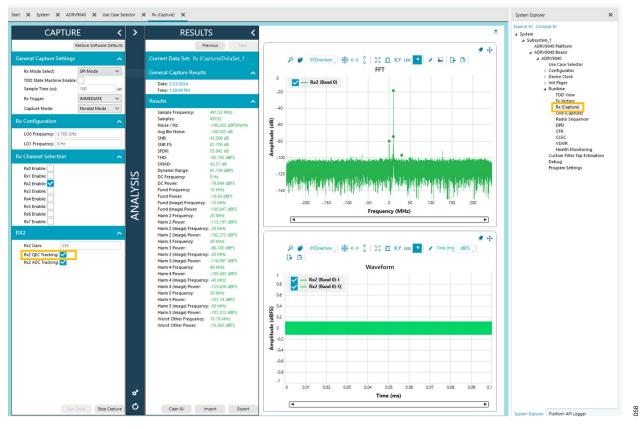


Figure 56. Rx Capture Performed after Enabling Rx QEC Tracking for Rx0

It is important to take note of the following if using a link sharing profile:

- > Only receiver channels must be enabled when attempting to capture receiver data.
- Currently the user must disable any additionally enabled observation receiver channels from the ORx (Capture) page before receiver data can be captured over the shared JESD link.
- ▶ The user can click on **Zoom to Fit** to correctly rescale the FFT plot when switching between receiver and observation receiver.

ORX (CAPTURE)

The process for capturing observation receiver data is similar to the **Rx (Capture)** process as shown in Figure 57. The process is as follows:

- 1. Navigate to System Explore > Runtime > ORx (Capture).
- Confirm that the desired observation receiver channels are enabled. Not that when using a link sharing profile, ensure that no receiver channels are enabled at this time. Receiver channels can be disabled from the System Explore > Runtime > Rx (Capture) as shown in Figure 57.
- 3. Under Capture Mode, select Normal Mode, which captures observation receiver data over the JESD link.
- 4. Click on Run Once or Run Continuously to capture data.

CAPTUR	E	<	RESUL	.TS <	*	Expand All Collapse All
	Restore Software I	Defaults		Previous Next	*	✓ System ✓ Subsystem_1
Seneral Capture Settings		^	General Capture Result	s 🔨	DRx (Capture)DataSet 1	ADRV9040 Platform ADRV9040 Board
Mode Select: TDO State Machine Enable	SPI Mode	~	Date: 6/28/2021 Time: 11:27:46 AM		FFT	ADRV9040 Use Case Selector
TDO State Machine Enable Sample Time (us):	100	µs	Results	^	a°	Configurator Device Clock
ORx Tripper:	IMMEDIATE Normal Mode	¥	Sample Frequency: Samples:	963.04 MHz	99 -40	AD9528 Clock Settings Init Pages
Capture Mode:	Linear Mode	<u>^ </u> {		96304 -147-222 dBFSPerHz		Tx Init Rx Init Stream Settings
ORid: 0				107.153 dB	-400 -300 -200 -100 0 100 200 300 400	Post MCS Init Calibration
ORx1: 0			SNR FS: SFDR:	57.227 48	Frequency (MHz)	AGC A Runtime
Rx Channel Selection		^ *	THD:	0.994 dB		TDD View Tx Vectors
ORx0 Enable: 🗸 ORx1 Enable: 🗸			SINAD:	43,247 d8 -35,746 d8	P ● XYDirection ⊕ <> \$ \$\$ □ # ●	Rx (Capture) ORx (Capture)
ORX0		^	Dynamic Range: DC Frequency:	\$7:327 d8F3 8 HE	V Time (ms) dBFS	Radio Sequencer DPD
ORx0 ADC Tracking:		^	DC Power:	104.737 dBFS	2 0.8 2 0.4	CFR CLGC
ORx1 ADC Tracking:			Fund Frequency: Fund Power:	156.06 MHz		VSWR Health Monitoring Custom Filter Tap Estimation
			Fund (Image) Frequency Fund (Image) Power:	-156.06 MHz	- Current and a second and a se	Debug Program Settings
			Harm 2 Frequency:	312.12 MHz	0 0.01 0.02 0.03 0.04 0.05 0.06 0.07 0.08 0.09 0.1 Time (ms)	
Run Or	ce Run Conti	No.4V	Harm 2 Power: Clear All	-135-233 (125) Import Export	۹ کې	

Figure 57. ORx0 and ORx1 Data Captured over JESD Link, with Tx LO + 10MHz Input Tone Applied to ORx0

Setting Observation Receiver Attenuation

Observation receiver attenuation can be entered in dB for each observation receiver channel. Attenuation changes are applied to the ADRV904x as soon as the user clicks on **Enter** in data capture state (halted or running continuously).

Setting ORx1 attenuation through the **ORx (Capture)** page might not work as expected. This is expected to be addressed in the upcoming releases of the ADRV904x plugin.

RADIO SEQUENCER

The ADRV904x features an internal timing generator called a **Radio Sequencer**. It defines the timing of the internal signals that control Tx, Rx, and ORx enable. It also creates any output timing signal required through any of the GPIO or Analog_GPIO available in the ADRV904x. This configuration can be applied after the part is programed and overwritten as many times as needed, but the signals that the radio sequencer can take control over have to be configured in the use case JSON file.

Settings

The Settings tab contains the following inputs:

- ▶ Enable, which needs to be set to enable the radio sequencer.
- ▶ Settings, which is the path for the configuration file (JSON) for the radio sequencer.
- Numerology, which is the subcarrier spacing that the radio sequencer will use to generate the timings. All 4G and 5G numerology timings are supported.
- **Sync Mode**, wherein two options are available:
 - ▶ Internal: SSB_sync is generated internally. The timing depends on the configuration done during initialization.
 - External: Every SSB_sync from external source is used to track and shift the internal SSB_sync to ensure the skew across ADRV904x is maintained without intervention of baseband processor (BBP).
- **SSB Period**, which indicates the period of the SSB_sync signal.
- ▶ **GPIO**, which is used to input the SSB_sync external signal.
- ▶ Generate Image, which generates the binary file than can later be loaded to the ADRV904x.
- ► Generate Profiles, which loads changes to the profile if needed.

	^
(Hz): 0	
None	~
None	~
0	m
None	~
e Image	
Profiles	
	None 0 None e Image

Figure 58. Radio Sequencer Settings

090

Table 8 provides the details of the numerology selection in Figure 58, which includes symbols per slot and number of frames.

Table 8. Numerology vs. Slots

μ	N ^{slot} symb	N ^{frame, µ} slot	N ^{subframe, µ} slot
0	14	10	1
1	14	20	2
2	14	40	4
3	14	80	8
4	14	160	16

Sequencer

This section explains the creation of the radio sequencer timing configuration. The configuration is created as a JSON file format that defines the different signals that the radio sequencer controls and its timings. Figure 59 shows an example of the radio sequencer timing configuration and JSON update.

The different levels that can be programmed are as follows:

- Patterns. Multiple patterns can be defined to enable multiple configurations to be loaded. The pattern played by the Radio Sequencer can be selected at runtime using API. The selected pattern repeats every SSB_sync period.
- ▶ Sequences. The total duration of the pattern can be divided in sequences.
- ▶ Timing definitions. The timing behavior of the signals. Each sequence can contain multiple timing definitions.

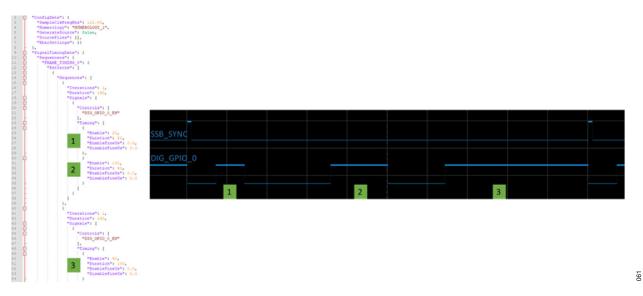


Figure 59. Example of Radio Sequencer Timing Configuration

To create a timing definition, the procedure is as follows as shown in Figure 61:

- 1. In the Sequencer Select dropdown menu, select the sequencer to which the configuration is applied.
- 2. In the Number of Sequences and Number of Patterns dropdown menus, select the number of sequences and patterns for the configuration.
- 3. In the Sequencer Pattern and Pattern Sequence dropdown menus, select the sequence and pattern index to which the inputs apply.
- 4. In the Select Timing Definitions dropdown menu, select the number of timing definitions that is created for that pattern.
- 5. Add the desired timing definition values into the input boxes as shown in Figure 60.
 - a. Timing enable. Select the symbol index at which the signal enable starts.
 - b. Timing duration. Select how many symbols the enable signal lasts.
 - c. Timing enable fine. Delay in µs to apply before the signal is enabled after the starting symbol.
 - d. Timing disable fine. Delay in µs to apply before the signal is disabled after the last symbol.
- 6. Select the signals that are controlled by the selected sequencer in the Signals section as shown in Figure 60.
- 7. Apply the current configuration by selecting **Apply Sequencer Settings**. This updates the view in the **Settings Preview** screen with the new configuration.

1	Rart X System X ADRVI	1040 X Radio Sequencer X				System Explorer
		RADIO SEQUENCER		SETTIN	IGS PREVIEW	Expand All Collapse All
nager			Configuration			A Subsystem 1 ADRV5040 Platform
	Sample Clock Frequency (kHz)	: 0				A ADRV9040 Board
lonsole	Enable					
rator	Settings					Configurator Device Clock
nperison	Numerology:	None	~			> Init Pages
<u> </u>	Sync Mode:	None	~			A Runtime TDD View
ions 🗸	SS8 Period:	0	ms			Tx Vectors
~	GRO	None	~			Rx (Capture) ORx (Capture)
		Generate Image				Radio Sequencer
		Generate Profiles				0PD CFR
			<u>^</u>			CLGC VSWR
		Apply Sequencer Settings				Health Monitorin
		Reset Sequencer Settings				Custom Filter Tap Est Debug
		Reload Radio Sequencer				Program Settings
		Export Configuration				
	Sequencer Selecti	Frame Timing 0	~			
	Number of Sequences	1	×			
	Number of Patterns:		~			
	Sequencer Pattern:		~			
	Pattern Sequence:					
			~			
	Sequence Timing Definitions	1	~			
	Sequence iterations:	0				
	Sequence Duration:	•				
	Timing 0 Enable (symbols):	•				
	Timing 0 Duration (symbols):	•				
	Timing 0 Enable Fine:	0	µ5			
	Timing 0 Disable Fine	•	us.			
	Timing 1 Enable (symbols):	•				
	Timing 1 Duration (symbols):	•				
	Timing 1 Enable Fine:	•	P1			
	Timing 1 Disable Fine:	0	ps.			
	Timing 2 Enable (symbols):	0				
	Timing 2 Duration (symbols):	0				
	Timing 2 Enable Fine:	0	µ5			
	Timing 2 Disable Fine:	٥	pt.			
	Timing 3 Enable (symbols):	0				
	Timing 3 Duration (symbols):	0				
	Timing 3 Enable Fine:	0	µS			
	Timing 3 Disable Fine:	0	us			

Figure 60. Radio Sequencer Timing Settings

Start 🗙 System 🗙 ADRV	9040 🗙 Radio Sequer	ter X	System Explorer	×
RADIO SEQI	UENCER	SETTINGS PREVIEW	Expand All Collapse All 4 System	
Settings Sample Clock Frequency (kHz Enable: Settings: Numerology: Sync Mode: SSB Period: GPIO: Generate In Generate In	None V None V None V None V mage	Configuration	 Subsystem,1 ADRV9040 Platform ADRV9040 Platform ADRV9040 Board ADRV9040 Use Case Selector Configurator Device Clock AD9528 Clock Settings Init Pages Tk Init Stream Settings Post MCS Init Calibration AGC 	
Sequencer Apply Sequence Reset Sequence Reload Radio S Export Config	er Settings equencer		Runtime TDD View TX Vectors Rx (Capture) ORx (Capture) Radio Sequence DPD CR CLGC	
Sequencer Select: Number of Sequences: Number of Patterns: Sequencer Pattern: Pattern Sequence: Sequence Timina Definitions:	Frame Timing 0 1 1 ~ 1 ~ 1 ~ 1 ~ 1 ~ 1 ~ 1 ~		VSWR Health Monitoring Custom Filter Tap Estimation Debug Program Settings	

Figure 61. Radio Sequencer Tab

A new pattern or sequencer can be selected to create a new configuration. After clicking on the **Apply Sequencer Settings**, the new configuration is merged with the previous configuration, which allows the creation of multiple sequencers and patterns in sequence. The current configuration can be deleted and restarted by clicking on **Reset Sequencer Settings**.

Once the configuration is created, if the ADRV904x is already programmed with a user case, the **Radio Sequencer** can be loaded by first selecting **Generate Image** to create the binary file and then selecting **Reload Radio Sequencer** to load the same binary.

Export Configuration is used to store the configuration in a file, and review and load at initialization by selecting it in **Settings** before programming the part.

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TDD VIEW

This section explains the setup TDD timings for each TRX_CTRL pin configured during post MCS init. The procedure is as follows:

- Enter start and stop times to specify a time range for driving each TRX_CTRL pin. Four start and stop time ranges can be specified per pin. LTE presets can also be applied to each CTRL pin from under LTE Presets. Figure 62 applies 4G LTE 0 (Tx) preset to TRXA_CTRL LTE and 4G LTE 0 (Rx) preset to TRXB_CTRL LTE.
- 2. Click Apply to plot the TDD timings for review. This only updates the plot, but it does not enable TDD.
- Click Configure to configure the TDD state machine using the specified timings. This enables the TDD state machine (the Enable TDD FSM checkbox). To perform data sourcing and capture in TDD mode, the user must additionally modify capture settings on the Runtime pages, as illustrated in Figure 63.

Delay Settings on the TDD View page can be used to add delays per JESD link between the enable inputs and data outputs.

Miscellaneous settings can be used to loop the TDD frame timings continuously.

TDD can be disabled by unselecting the **Enable TDD FSM** checkbox. Note that clicking **Configure** is not required for disabling TDD FSM as **Configure** reselects the **Enable TDD FSM** checkbox.

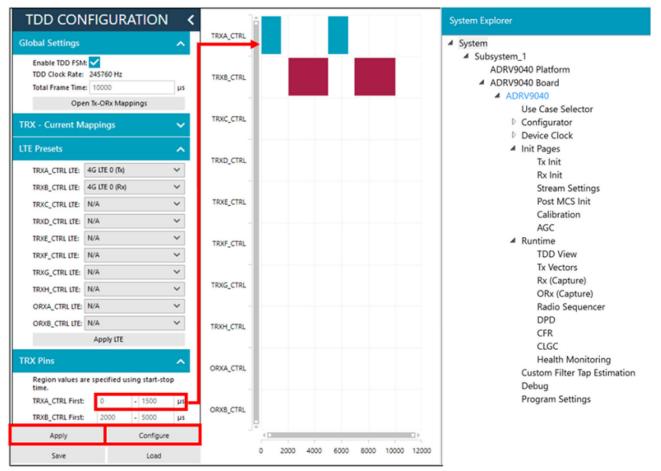


Figure 62. TDD Configuration Page Used to Specify Enable Timings for Each CTRL Pin and Configure the TDD State Machine

TRANS	SMIT	<
	()	/ectors
General Settings		^
Tx Mode Select:	Pin Mode	~
TDD State Machine Enabl Use NCO Tones:	e: 🗸	
Tx Trigger:	TDD State Machine	• •
Open Tx-O	Rx Mappings	
Go to '	TDD View	
		_
CAPTI	Restore Softwar	e Defaults
CAPIC General Capture Settir	Restore Softwar	e Defaults
	Restore Softwar	^
General Capture Settir	Restore Softwar	^
General Capture Settin Rx Channel:	Restore Softwar ngs 0, 1, 2, 3, 4, 5, Pin Mode	^
General Capture Settin Rx Channel: Rx Mode Select:	Restore Softwar ngs 0, 1, 2, 3, 4, 5, Pin Mode	^
General Capture Settin Rx Channel: Rx Mode Select: TDD State Machine Ena	Restore Softwar ngs 0, 1, 2, 3, 4, 5, Pin Mode able:	^
General Capture Settin Rx Channel: Rx Mode Select: TDD State Machine Ena Sample Time (us):	Restore Softwar ngs 0, 1, 2, 3, 4, 5, Pin Mode able: 10000	^

Figure 63. Runtime Pages Updated to Trigger Data Source and Capture Using the TDD State Machine for Rx

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FFT ANALYSIS

On the **Rx (Capture)** and **ORx (Capture)** pages (see Figure 56 and Figure 57), each provides data analysis tab that allows the user to manipulate the FFT calculations to best fit their requirements. The user can configure FFT analysis settings, manipulate FFT durations, and perform simple spur analysis. On both **Rx (Capture)** and **ORx (Capture)** pages, the **Analysis** tab provides information about the received signal. This tab is directly related to the **Results** tab, such that the selections determine the information presented to the user.

Analysis Settings

The user can select the preference of how results of the FFT analysis is generated, and determine what is presented on the **Results** tab. The following are the key options available to the user:

- ▶ Select preference tones power measurements in dBc or dBFS.
- ▶ Selection specifies a 1- or 2-tone analysis for information on harmonics or intermodulation.
- Options for strategy used to find the fundamental tones, such as the following:
 - ▶ Highest bin.
 - Mirror image.
 - Fixed.
- Selection for type of windowing used in FFT spectrum generation, such as the following:
 - Blackman Harris 4 (default).
 - Blackman Harris 7.
 - ▶ Blackman Harris 7 scaled.
 - ► Hann.
 - None.

- ▶ Specify number of harmonics reported, such as the following:
 - ► Harmonics. Single tone analysis.
 - ▶ Intermodulations. Two tone analysis.
- ▶ Specify number of bins used during the FFT analysis power calculations for the following:
 - ► Fundamental tones.
 - ▶ DC component.
 - ▶ Worst other (spurs).

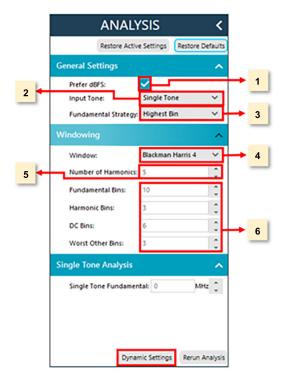


Figure 64. Analysis Tab with Default Parameters

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FFT Ranges

For some operations, the user does not need the FTT analysis to cover the full capture duration, especially during TDD operations where the duration of capture is much larger than the duration of the desired signal. The rest of this section explains how to use this feature through the framework of a TDD operation outlined in Figure 65. For this example, the Tx0 and Tx4 outputs tones of 10 MHz and 30 MHz delta from LO, respectively. The two transmitters are then combined using a splitter and the resulting signal is sent into another splitter, which is then fed to ORx0 and Rx1.

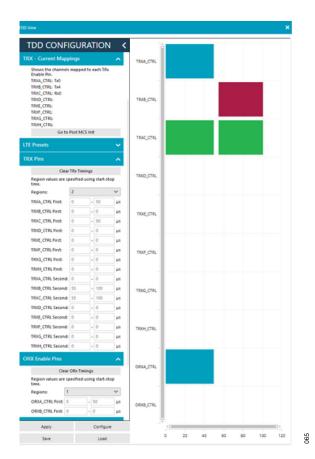


Figure 65. Example TDD Configuration to Demonstrate Dynamic FFT Duration Feature

Adding an FFT Range

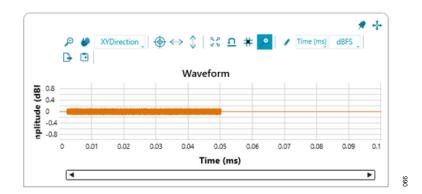
On the **ORx (Capture)** page with a capture period equal to the TDD frame of 100 μ s, a regular capture does not produce a true FFT representation of the signal received during the slot seen in Figure 66. Therefore, it is essential to use the FFT duration feature available though the **Dynamic Settings** available on the **Analysis** tab as shown in Figure 64.

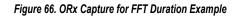
Upon clicking the Dynamic Settings, a pop-up window, as shown in Figure 67, appears. To add an FFT range, take the following steps:

- 1. Click on + to create an instance of the FFT range.
- 2. Select the appropriate channel.
- 3. Set the starting sample index in reference to the capture period.
- 4. Set the number of samples used for analysis.

Take note of the following:

- > All numerical inputs involved with adding an FFT range is in terms of samples.
- ▶ The start index and max sample count define the range of the FFT analysis.
- ▶ For each channel, only one FFT range is allowed.
- ▶ Each FFT range addition or update must be followed by clicking on Rerun Analysis on the Analysis tab.





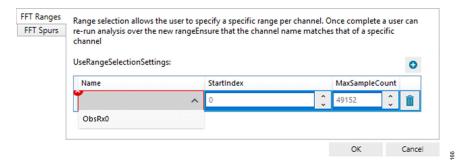
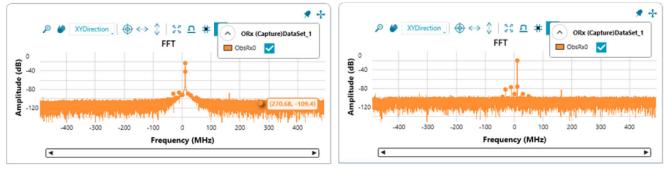


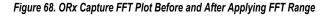
Figure 67. FFT Range Settings Window



(A) BEFORE FFT RANGE

(B) AFTER FFT RANGE

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Inserting Spur

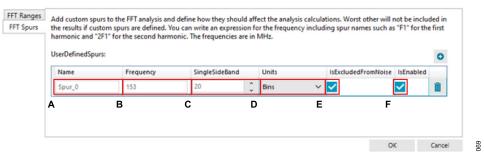
The user can perform simple spur analysis by inserting spurs to track the power measurements of a specific spur. This feature can be accessed through the **Dynamic Settings** as shown in Figure 64. The following outlines the use of this feature.

For this demonstration, the ORx is used to capture a 20 MHz tone. Because of the direct conversion from the RF, there is a significant spur at approximately 153 MHz. The following steps are recommended for adding a spur:

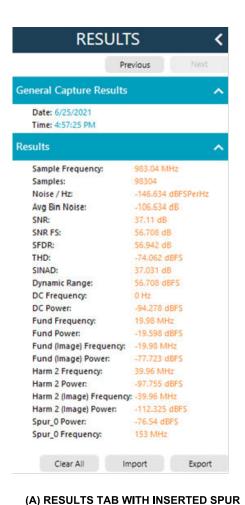
- 1. Upon clicking the Dynamic Settings, a pop-up window appears.
- 2. Navigate to the FFT Spurs tab. From there, a window as shown in Figure 69 appears.
- 3. Set the following parameters:
 - a. Prove a Name for administrative purposes.
 - b. Set Frequency in MHz.
 - c. Set spur SingleSideBand (SSB).

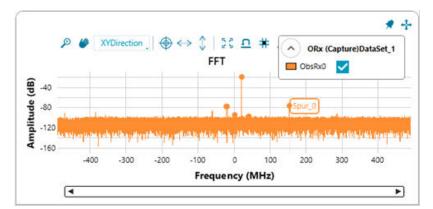
- d. Select Units of SSB.
- e. Specify whether spur is considered in noise calculations.
- f. Enable or disable spur.

4. Click OK followed by clicking Rerun Analysis on the Analysis tab.

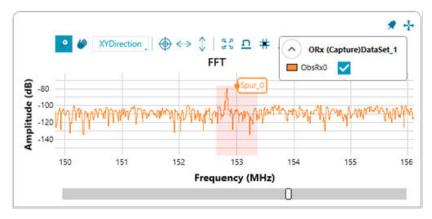








(B) FFT PLOT WITH INSERTED SPUR



(C) FFT PLOT ZOOMED ONTO INSERTED SPUR

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Figure 70. Results and FFT Plot After Spur Inserted at 153 MHz

Exporting Captured Data

This section seeks to explain the feature of exporting captured data. The user can perform non native measurements or operations on the received signal. Found on both the **Rx (Capture)** and **ORx (Capture)** pages, the **Results** tab provides the ability to export data via the **Export** button as shown in Figure 71. The process is as follows:

analog.com

- 1. Upon clicking Export, a pop-up window prompts the user to the save an XML file.
 - ▶ Note that the name of the file is the base name of the generated files in CSV format.
 - ▶ Default naming convention is [CapturePage]DataSet_#_DDMonthYYY_HH_MM_SS.
 - ▶ Default path follows as C:\Users\\$UserFolder\$\AppData\Local\Analog Devices\ACE\ExportData\ADRV9040.
- 2. The total number of additional files generated depends on the number active channels during the capture.
 - ► Key files and brief descriptions.
 - ▶ FFT. File with FFT plot data with additional summary information.
 - Raw sample. Raw data in an interleaving format of I and Q samples. Each column corresponds to a different channel. This file is used for importing data to the **Results** tab.
 - ▶ Waveform. File with waveform plot data with additional summary data.
 - ► Samples are interleaved by I and Q samples.
 - ▶ Multiple waveform files are generated depending on number of active channels during capture.
 - ▶ File name follows as [CapturePage]DataSet #_waveform_[Channel]_ DDMonthYYY_HH_MM_SS.



Figure 71. ORx (Capture) Page Results Tab with Plots

DPD

Hardware Prerequisites

To evaluate DPD, ensure that a gain line up is connected to the transceiver similar to Figure 72. Tune the power levels appropriately to ensure that the observation receiver is not saturating. Once the gain line up is connected, proceed to transmit data in TDD/FDD mode as described in the Transmitter Vectors section and verify the output on a spectrum analyzer.

For an FDD use case, the TDD flag needs to be set to false from the profile/use case and it must be true in case of TDD.

Ensure that the power amplifier (PA) is turned off while programming the device to avoid damages from high-power tones transmitted by ADRV904x calculations.

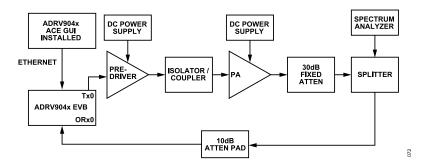


Figure 72. Hardware Connections for Evaluating DPD

Once the transmit data is verified, proceed to check that the ORx data is correct following the instructions described in the ORx (Capture) section.



Figure 73. Verify the ORx Data for DPD

Following successful verification of the ORx data, proceed to DPD configuration and enable DPD tracking in the **DPD** window under the **Runtime** page as shown in Figure 74.

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RUNTIME

	ADRV9040 X	Use Case Selector	ORx (Capture)	Tx Vectors	Vector Generator	KDPD_2.7.0.7 (1).py	C DPD X	System Explorer
DPD								Expand All Collapse All System
PD Models	~							 Subsystem_1 ADRV9040 Platform
								ADRV9040 Platform
PD Capture Confi	ig 🗸							▲ ADRV9040 Use Case Selector
PD Tracking	~							Use Case Selector ▷ Configurator
- o macking								Device Clock
PD Status	\sim							Init Pages A Runtime
								TDD View
PD Statistics	~							Tx Vectors
								Rx (Capture)
								ORx (Capture) Radio Sequencer
								DPD
								CFR
								CLGC
								VSWR
								Health Monitoring
								Custom Filter Tap Estimat
								Debug Program Settings

Figure 74. DPD Configuration Window

Proceed to load the DPD model as shown in Figure 75. The DPD model configuration is included as a metadata at the top of the DPD model file. The DPD model library is part of the software package.

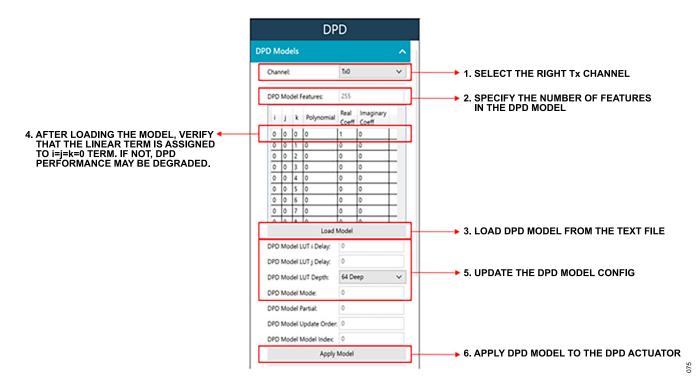


Figure 75. DPD Model Loading User Interface

Select the DPD capture configuration as shown in Figure 76.

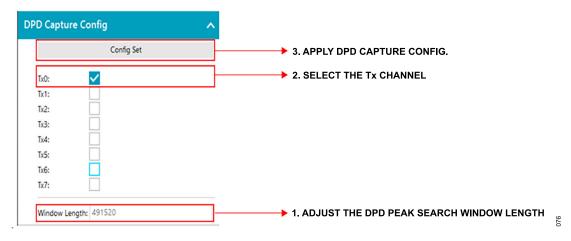


Figure 76. DPD Capture Configuration User Interface

Adjust the DPD tracking configuration and enable the DPD tracking calibration on the appropriate Tx channel.

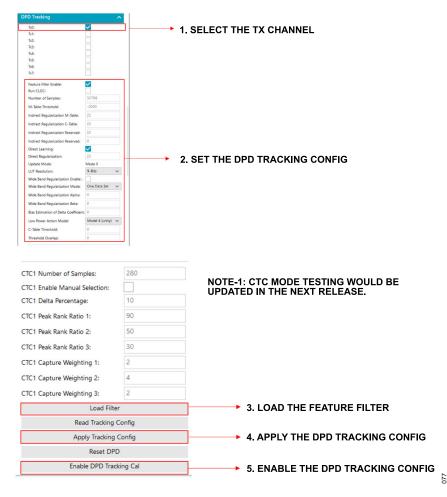


Figure 77. DPD Tracking Configuration User Interface

After the DPD tracking calibration is enabled, verify the adjacent channel leakage ratio (ACLR) correction on the spectrum analyzer. Monitor the DPD status to ensure that the DPD update counts are incrementing and that there is no error as shown in Figure 78.

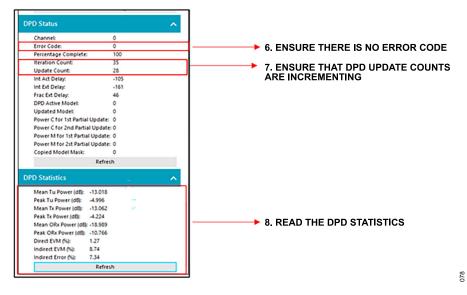


Figure 78. DPD Status User Interface

Support for DPD charge trap correction (CTC) mode is in an upcoming software release.

CFR

CFR Block on the Runtime: Step 0

The CFR block is under Runtime. When clicked, CFR Configuration, Channel Configuration, and CFR Statistics are displayed as shown in Figure 79.

CFR CONFIG	URATION	CHANNEL CONFIGURATION	CFR STATISTICS	Expand All Collapse All
ofile 0 CFR Configuration	n 🔨	CFR Channel Selection	CFR Statistics	✓ System ✓ Subsystem_1 ACR/PO40 Platform
	Config One	CFR Tx Channel Made: 01 00	Window Enable:	ADR/9040 Board
Active Configuration:	Config Two	Tx Channel Mask Bit 0	Clear Stats:	ADRV9040 Use Case Selector
Set Active C		Tx Channel Mask Bit 1:	Get Statistics	Configurator
		Tx Channel Mask Bit 2:		Device Clock
Load Pu		Tx Channel Mask Bit 3:	Channel 0 Engine 1 Peaks Detected: 0	Init Pages A Runtime
Apply Configurat	ion Settings	Tx Channel Mask Bit 4:	Channel 0 Engine 2 Peaks Detected: 0	TOD View
		Tx Channel Mask Bit 5:	Channel 0 Engine 3 Peaks Detected: 0	Tx Vectors
Configuration 1		Tx Channel Mask Bit 6:	Channel 0 Engine 1 Peaks Skipped Weight FIFO: 0	Rx (Capture) ORx (Capture)
CER Instance Enabled:	~	Tx Channel Mask Bit 7:	Channel 0 Engine 2 Peaks Skipped Weight FIFO: 0	Cito (Capiture) Radio Sequencer
	3 ~	Enable CFR Configuration	Channel 0 Engine 3 Peaks Skipped Weight FIFO: 0 Channel 0 Engine 1 Peaks Skipped Peak FIFO: 0	000
		Post CFR Digital Gain: 1	Channel 0 Engine 2 Peaks Skipped Peak FIFO: 0	0 📥 cfr
Peak Threshold:	0.45	Post CPR Digital Galet	Channel 0 Engine 3 Peaks Skipped Peak FIFO: 0	CLGC VSWR
Correction Threshold Scaler:	0.98	Post CFR Digital Gain Readback	Channel 0 Engine 1 Peaks Skipped CPC Module: 0	Health Monitoring
Engine 1 Peak Threshold Scaler:	0.98	5.0. 1	Channel 0 Engine 2 Peaks Skipped CPC Module: 0	Custom Filter Tap Estimation
Engine 1 Peak Duration:	30	5.5 1	Channel 0 Engine 3 Peaks Skipped CPC Module: 0	Debug Program Settings
		Tx 2: 1		Program persenge
Engine 1 Delay:	512	Tr 3: 1	Channel 1 Engine 1 Peaks Detected: 0	
Engine 2 Peak Threshold Scaler:	0.985	7x4: 1	Channel 1 Engine 2 Peaks Detected: 0 Channel 1 Engine 3 Peaks Detected: 0	
Engine 2 Peak Duration:	30	Tx 5: 1	Channel 1 Engine 1 Peaks Skipped Weight FIFO: 0	
Engine 2 Delay:	512	Tx 6: 1 Tx 7: 1	Channel 1 Engine 2 Peaks Skipped Weight FIFO: 0	
		87. 1	Channel 1 Engine 3 Peaks Skipped Weight FIFO: 0	
Engine 3 Peak Threshold Scaler.	0.99		Channel 1 Engine 1 Peaks Skipped Peak FIFO: 0	
Ingine 3 Peak Duration:	30		Channel 1 Engine 2 Peaks Skipped Peak FIFO: 0	
Ingine 3 Delay:	512		Channel 1 Engine 3 Peaks Skipped Peak FIFO: 0	
	4		Channel 1 Engine 1 Peaks Skipped CPC Module: 0	
Nise Length:	1024		Channel 1 Engine 2 Peaks Skipped CPC Module: 0	
			Channel 1 Engine 3 Peaks Skipped CPC Module: 0	
	Single Shot		Channel 2 Engine 1 Peaks Detected: 0	
Hard Clipper Enable:			Channel 2 Engine 2 Peaks Detected: 0	
Configuration 2			Channel 2 Engine 3 Peaks Detected: 0	
		1	Channel 2 Engine 1 Peaks Skipped Weight FIFO: 0	
CFR Instance Enabled			Channel 2 Engine 2 Peaks Skipped Weight FIFO: 0	
Number of Engines Used:	o 🗸		Channel 2 Engine 3 Peaks Skipped Weight FIFO: 0	
Peak Threshold:	0		Channel 2 Engine 1 Peaks Skipped Peak FIFO: 0	
Correction Threshold Scaler:	0		Channel 2 Engine 2 Peaks Skipped Peak FIFO: 0	
Interpolation:	4		Channel 2 Engine 3 Peaks Skipped Peak FIFO: 0	
	0		Channel 2 Engine 1 Peaks Skipped CPC Module: 0	
Pulse Length:	v		Channel 2 Engine 2 Peaks Skipped CPC Module 0	
Pulse RAM Selection:	Single Shot		Channel 2 Engine 3 Peaks Skipped CPC Module: 0	System Explorer Platform API Logger

Figure 79. CFR Block in Runtime

Transmitter Channel Configuration: Step 1

First, the transmitter channel needs to be selected so that the CFR function is added to the selected transmitter channel. In Figure 80, one channel, **Tx Channel Mask Bit 0**, is selected.

X System X ADRV	9040 X Use Case Select	tor X ORx (Capture) X Tx Vectors X Vector Generator	X OR X	System Explorer
CFR CONFIG	URATION	CHANNEL CONFIGURATION	CFR STATISTICS	Expand All Collapse All
file 0 CFR Configuratio	n ^	CFR Channel Selection	CFR Statistics	✓ System ✓ Subsystem_1 ADRV9040 Platform
	Config One	CFR Tx Channel Mask: 0x 01	Window Enables	ADRV9040 Board ADRV9040
Active Configuration:	Config Two	Tx Channel Mask Bit 0:	Clear Stats	Use Case Selector
Set Active (Config	Tr Channel Mask Bit 1:	Get Statistics	Configurator
Load Pu	ha	Is Channel Mask Bt 2 Channel celo	ction: 0 Engine 1 Peaks Detected: 0	Device Clock Init Pages
		Tx Channel Mask Bit 3:	Channel O Engine 1 Peaks Detected: 0 Channel O Engine 2 Peaks Detected: 0	# Runtime
Apply Configurat	ton Settings	Tr Channel Mask Bit 4:	Channel 0 Engine 2 Peaks Detected: 0 Channel 0 Engine 3 Peaks Detected: 0	TDD View
Configuration 1		Tr. Channel Mask Bit S:	Channel 0 Engine 1 Peaks Skipped Weight FIFO: 0	Ta Vectors Rx (Capture)
comparation i		Tx Channel Mask Bit 6:	Channel 0 Engine 2 Peaks Skipped Weight FIFO: 0	Rx (Capture) ORx (Capture)
CFR Instance Enabled:	✓	Tr Channel Mask Bit 7:	Channel 0 Engine 3 Peaks Skipped Weight FIFO: 0	Radio Sequencer
Number of Engines Used:	3 ~	Enable CFR Configuration	Channel 0 Engine 1 Peaks Skipped Peak FIFO: 0	DPD
Peak Threshold	0.45	Post CFR Digital Gain: 1	Channel 0 Engine 2 Peaks Skipped Peak FIFO: 0	CR
			Channel 0 Engine 3 Peaks Skipped Peak FIFO: 0	VSWR
Correction Threshold Scaler:	0.98	Post CFR Digital Gain Readback	Channel 0 Engine 1 Peaks Skipped CPC Module: 0	Health Monitoring
Engine 1 Peak Threshold Scaler	0.98	Tx 0: 1	Channel 0 Engine 2 Peaks Skipped CPC Module: 0	Custom Filter Tap Estimation Debug
Ingine 1 Peak Duration:	30	Tx 1: 1	Channel 0 Engine 3 Peaks Skipped CPC Module: 0	Program Settings
Ingine 1 Delay.	512	1/2 1	Channel 1 Engine 1 Peaks Detected: 0	
		1×3: 1	Channel 1 Engine 2 Peaks Detected: 0 Channel 1 Engine 2 Peaks Detected: 0	
Engine 2 Peak Threshold Scaler	0.985	h4: 1	Channel 1 Engine 3 Peaks Detected: 0	
Engine 2 Peak Duration:	30	1x5x 1 1x6x 1	Channel 1 Engine 1 Peaks Skipped Weight FIFOI 0	
Engine 2 Delay:	512	1x 6: 1 7x 7: 1	Channel 1 Engine 2 Peaks Skipped Weight FIFO: 0	
		18.71 1	Channel 1 Engine 3 Peaks Skipped Weight FIFO: 0	
Engine 3 Peak Threshold Scaler			Channel 1 Engine 1 Peaks Skipped Peak FIFO: 0	
Engine 3 Peak Duration:	30		Channel 1 Engine 2 Peaks Skipped Peak RFO: 0	
Engine 3 Delay:	512		Channel 1 Engine 3 Peaks Skipped Peak FIFO: 0	
interpolation:	4		Channel 1 Engine 1 Peaks Skipped CPC Module: 0	
Pulse Length:	1024		Channel 1 Engine 2 Peaks Skipped CPC Module: 0	
	Single Shot		Channel 1 Engine 3 Peaks Skipped CPC Module: 0	
Hard Clipper Enable	single shot		Channel 2 Engine 1 Peaks Detected: 0	
naro copper chase.			Channel 2 Engine 2 Peaks Detected: 0	
Configuration 2			Channel 2 Engine 3 Peaks Detected: 0	
			Channel 2 Engine 1 Peaks Skipped Weight FIFO: 0	
CFR Instance Enabled:			Channel 2 Engine 2 Peaks Skipped Weight FIFO: 0	
Number of Engines Used:	• ~		Channel 2 Engine 3 Peaks Skipped Weight FIFO: 0	
leak Threshold	0		Channel 2 Engine 1 Peaks Skipped Peak FIFO: 0	
Correction Threshold Scaler:	0		Channel 2 Engine 2 Peaks Skipped Peak FIFO: 0	
Interpolation	4		Channel 2 Engine 3 Peaks Skipped Peak FIFO: 0	
Pulse Length:	0		Channel 2 Engine 1 Peaks Skipped CPC Module: 0 Channel 2 Engine 2 Peaks Skipped CPC Module: 0	
	-		Channel 2 Engine 2 Peaks Skipped CPC Module: 0 Channel 2 Engine 3 Peaks Skipped CPC Module: 0	
Pulse RAM Selection:	Single Shot		control cognetion and any period of the movie of	System Explorer Platform API Logger

Figure 80. Tx Channel Selection for Adding CFR Block

Inactive Configuration 1 and Active Configuration 2: Step 2 and Step 3

To set **Config One**, set it to inactive for it not to impair the transmitter channel when the CFR correction pulse and parameters are loaded to the inactive **Configuration 1**.

Once **Config Two** is active, the configuration is ready to be updated with the CFR correction pulse and CFR parameters as shown in Figure 81 and Figure 82.

Image: Configure Image: Co	CFR CONFIGURATION	CHANNEL CONFIGURATION	CFR STATISTICS	Expand All Collapse All
Consignation Consignation Construction C	le 0 CFR Configuration	CFR Channel Selection	CFR Statistics	4 Subsystem_1
A mesone Chennel 2 Copine 2 Dopine 2 Parks Stopen Park FED. 0 Chennel 2 Copine 2 Dopine 3 Parks Stopen Park FED. 0 amplifiation 4	Configuration Confi	OPE Ib: Channel Mark 0 01 10: Channel Mark Ib: 0 1 1 10: 1 1 1 10: 1 1 1 10: 1 1 1 10: 1 1 1 10: 1 1 1 10: 1 1 1 10: 2 1 1 10: 2 1 1 10: 4 1 1 10: 5 1 1 10: 6 1 1 10: 7: 1 1 1	Weden Enable Get Statistics Care do Expres 1 Anis Dented: 0 Onamol D Expres 2 Anis D Expected: 0 Onamol D Expres 2 Anis D Expected: 0 Ocared D Expres 2 Anis D Expected: 0	A Catricito S Parton A CATRICAL A CATRICAL Configuration Confi
			Channel 2 Engine 2 Peaks Skipped Peak FIFO: 0 Channel 2 Engine 3 Peaks Skipped Peak FIFO: 0	

Figure 81. Inactive Config One, Active Config Two: Step 2

off 2 CR2 Conjugation CR2 Control Selection CR2 Statistics Image: Conjugation Ame Conjugation CR2 Control Math Image: Conjugation CR2 Control Math Image: Conjugation	CFR CONFIG	URATION	CHANNEL CONFIGURATION	CFR STATISTICS	Expand All Collapse All
And Configurini	ofile 0 CFR Configuration	n 🔨	CFR Channel Selection	CFR Statistics	# Subsystem_1
Alex Certification 5: Owner Muss Bs 0 Image: Certification Image: Ceritification Image: Certification Im		Config One	CFR Ts Channel Mask: Ct 01	Window Enable:	# ADRV9040 Board
ist Asias Config 3 ist Ability 10 Over Wast B 1 ist Ability 10 Over Wast B 1 Add Character 10 Over Wast B 1 Configuration Simpling 10 Over Wast B 1 Control Wast B 2 10 Over Wast B 2 Configuration Simpling 10 Over Wast B 2 Control Wast B 2 10 Over Wast B 2 Control Wast B 2 10 Over Wast B 2 Control Wast B 2 10 Over Wast B 2 Control Wast B 2 10 Over Wast B 2 Control Wast B 2 10 Over Wast B 2 Control Wast B 2 10 Over Wast B 2 Control Wast B 2 10 Over Wast B 2 Control Wast B 2 10 Over Wast B 2 Control Wast B 2 10 Over Wast B 2 Control Wast B 2 10 Over B 2 Control Wast B 2 10	Active Configuration:		To Channel Mark Br D	Clear Stats:	
Lead Haw 10 Outer Muss 82 0 0 Outer Muss 82 0 0 Outer Muss 82 0 App/ Calignation Simple 10 Outer Muss 82 0 0 Outer 8 Opting 1 Nais Detects				Get Statistics	
List Num 10 Over Must Bis 1 Our de Organ 1 Nais Decest: 0 10 Part Addy Conver Must Bis 1 Our de Organ 2 Nais Decest: 0					
App Companies Margin To Owner Mass Bs 2 Control Mass Bs 2 Control Mass Bs 2 Cardiguration 1 In Owner Mass Bs 2 Control Mass Bs 2 Contro					
Configurátion 1 10. Oucord Muest Bis 1 0. Oucord Bigling 3 Neus Dispect Minist 100.0 0. Oucord Bigling 3 Neus Dispect Minist 100.0 0. Oucord Bigling 3 Neus Dispect Minist 100.0 Char Mich end fungines Used 0 0 0 0. Oucord Bigling 3 Neus Dispect Minist 100.0 0. Oucord Bigling 3 Neus Dispect Minist 100.0 Number of Dispes Used 0 0 0 0. Oucord Bigling 3 Neus Dispect Minist 100.0 0. Oucord Bigling 3 Neus Dispect Minist 100.0 Davie of Dispes Used 0 0 0 0 0 0 Dispect Final Thread Dispect Chart 0 0 0 0 0 Dispect Final Thread Dispect Chart 0 0 0 0 0 Dispect Final Thread Dispect Chart 0 0 0 0 0 Dispect Final Thread Dispect Chart Allows Dispect Allows Dispect Chart Allows Dispect Chart Allows Dispect Allows Dispect Allows Dispect Chart Allows Dispect Allows Dispect Allow	Apply Configurati	ion Settings			
10. Outrow Mass Bré					
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Number of Digons Loss 0 <th0< th=""> 0 <th0< th=""> <th0< th=""></th0<></th0<></th0<>	CER Instance Enabled	V	Tx Channel Mask Bit 7:		
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Unput P May	Correction Threshold Scaler:	0.98	Post CFR Digital Gain Readback		
Depres Park Doursen D Ist is is Ist is is Cannot Depres Parks Descrete Decempendence Decempendence <thdecempendence< th=""> Decempen</thdecempendence<>	Engine 1 Peak Threshold Scaler:	0.98			Custom Filter Tap Estimation
Spin Spin <th< td=""><td></td><td></td><td>Tc1: 1</td><td>Channel 0 Engine 3 Peaks Skipped CPC Module: 0</td><td></td></th<>			Tc1: 1	Channel 0 Engine 3 Peaks Skipped CPC Module: 0	
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Toping 3 hait Newhold Soles 00 Nace High Darks Set "Config1 Inactive" Set Config2 Active Charant Toping 3 hait Speech Nat HIGO Nace High Darks Set Config2 Active Nace High Darks 00 Convert Toping 3 hait Speech Nat HIGO 0 Charant Toping 3 hait Speech Nat HIGO <td< td=""><td>Engine 2 Delay</td><td>512</td><td></td><td>Channel 1 Engine 2 Peaks Skipped Weight FIFO: 0</td><td></td></td<>	Engine 2 Delay	512		Channel 1 Engine 2 Peaks Skipped Weight FIFO: 0	
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Nate MAX Besterion Sogle pot United Opper Faile 0 Configuration 2 0 Configuratin 2 0 Configurat	Pulse Length:	1024	Set Config2 Active		
Nack 2 Open Fuel 0 Configure Fuel 0 Configure Fuel 0 Configure Fuel 0 Configure Fuel 0 Chard 2 Open Flass Oncode 0 Chard 2 Open Flass Sheed Sheed HD 0 0 Chard 2 Open Flass Sheed Sheed HD 0 0 Chard 2 Open Flass Sheed Sheed HD 0 0 Nach or Open Flass Sheed HB 0 0 Chard 2 Open Flass Sheed HB 0	Pulse RAM Selection:	Single Shot	Set Comig2 Active	Chamber 1 Engine a reaks skipped CPC Module 0	
Criedwardshow 2 hours				Channel 2 Engine 1 Peaks Detected: 0	
CR Indram Fundset:				Channel 2 Engine 2 Peaks Detected: 0	
CRI: Name of Explaint Overval 2 Topine 2 Nams Stopped Waget FED 0 Name of Explaint Data 0 Charred 2 Topine 3 Nams Stopped Waget FED 0 Name of Explaint Data 0 Charred 2 Topine 3 Nams Stopped Waget FED 0 Control Control Topine 3 Nams Stopped Waget FED 0 Charred 2 Topine 3 Nams Stopped Nams FED 0 Charred 2 Topine 3 Nams Stopped Nams FED 0 Control Topine 3 Nams Stopped Nams FED 0 Charred 2 Topine 3 Nams Stopped Nams FED 0 Charred 2 Topine 3 Nams Stopped Nams FED 0 Rule Langth: 0 Charred 2 Topine 3 Nams Stopped Topine 1 Nams Stopped Topine 1 Nams Stopped Topine 2 Nams Stopped Topine 1 Nams Stopped Topine 2 Nams Stopped Topine 1 Nams Stopped Topine 2 Nams Stopped Topine 1 Nams Stopped Topine 1 Nams Stopped Topine 2 Nams Stopped Topine 1 Nams Stopped	Configuration 2				
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Alat Threahold O Olared 2 Ergine 1 Nats Stipped Nat FIGO O Connection Threahold Scale 0 Connection Threahold Scale 0 Chrende Threahold Scale Connect Engine 1 Nats Stopped Nat FIGO 0 Interpretation Connect Engine 1 Nats Stopped Nat FIGO 0 Alat Length 0 Connect Engine 2 Nats Stopped Nat FIGO 0					
Team metanika Channel 2 frigine 2 Nesis Skipped Avak FIGO. 0 Connection Thread Skipped Channel 2 frigine 2 Nesis Skipp		0			
Convestion Internatival Soster 0 Octore 3 Press Stepson Press Free Stepson Press Free Stepson Press	Peak Threshold:	0			
Interplation: 4 Channel 2 Engine 1 Pails Skipped CPC Module 0 Public Length: 0 Channel 2 Engine 1 Pails Skipped CPC Module 0 Channel 2 Engine 2 Pails Skipped CPC Module 0	Correction Threshold Scaler:	0			
Public Length: 0 Chevnel 2 Engine 2 Peaks Stopped CPC Module 0	Interpolation:	4			
		ð			
Pulse RAM Selection: Single Shot Channel 2 Engine 3 Peaks Skipped CPC Module: 0 System Explorer Platform API Logger		Single Shot		Channel 2 Engine 3 Peaks Skipped CPC Module: 0	

Figure 82. Inactive Config One, Activate Config Two: Step 3

Loading CFR Correction Pulse: Step 4

To upload the CFR correction pulse, click on the Load Pulse button as shown in Figure 83.

refile 0 of R.Configuration (R. Channel Selection (Configuration (Configura	CFR CONFIGU	URATION	CHANNEL CONFIGURATION	CFR STATISTICS	Expand All Collapse All
Atter Configuration:	rofile 0 CFR Configuration	n 🔥	CFR Channel Selection	CFR Statistics	# Subsystem_1
Interpolation: 4 Channel 2 Engine 1 Peaks Skipped CPC Module: 0	Active Configuration Set Active Configuration Configuratio	Config One Config Two config	CR: Ib: Channel Mark 01 To: Channel Mark 01 </td <td>Winder Dabie </td> <td>Addrolda Partium Addrolda Barell Addrolda Barell Addrolda Addrold</td>	Winder Dabie	Addrolda Partium Addrolda Barell Addrolda Barell Addrolda Addrold

Figure 83. Loading CFR Correction Pulse of Configuration 1: Step 4

Once selected, the directory and CFR correction pulse location are shown as in Figure 84, assuming the CFR correction pulse exists.

CFR CONFIGURATION	CHANNEL CONFIGURATION	CFR STATISTICS		Expand All Collapse All
file 0 CFR Configuration	CFR Channel Selection	CFR Statistics	<u>~</u>	 Subsystem_1 ADR/9040 Platform
Active Configuration:	CRR Tr Channel Mark E0 C	Window Endlet: Cer Stat: Caroli 0 Expire 1 Pasis Detected: Ocaroli 0 Expire 1 Pasis Detected: Ocaroli 0 Expire 1 Pasis Detected: Ocaroli 0 Expire 1 Pasis Skyped Hittpi FEG 0 Ocaroli 0 Expire 2 Pasis Skyped Hittpi FEG 0 Ocaroli 0 Expire 3 Pasis Skyped Hittpi FEG 0	×	A DRIVING Runi A DRIVING Runi A DRIVING Run Use Cas Selector Compared Compared Band Regen A Butches TOD View Recent Band Regen Rada Seguetare DO Rune Rada Seguetare DO Rom Coco
eak threshold ← → × ↑ 📑 > This PC > correction Threshold	Desktop > AKororSW0p3 > Pulse	✓ & Search Pulse	م	VSWR Health Monitoring
Organize New folder			H • 🖬 😶	Custom Filter Tap Estimation
Ingine 1 Peak Durati 🖈 Quick eccess Ingine 1 Delay: 🗾 Desktop	Name	10/6/3021 2:30 PM Text Document	52e 418	Debug Program Settings
Engine 2 Peak Threst 🕹 Downloads	2carrierNR100M1001_1024.bt 3carrierNR100M1101UC75Modifi	ed. 512.bt 10/7/2021 11:18 AM Text Document	7 KB 6 KB	
Engine 2 Peak Durati 👔 Documents	3carrierNR100M1101UC75Modify		11.63	
Engine 2 Delay: Reference	Non_Contiguous_3C_165_80_160	MHz_20_ 9/1/2021 1:49 PM Text Document	9 KB	
Engine 3 Peak Threat DPD_enabled	Non_Contiguous_3C_170_85_155	MHz_20 8/31/2021 8:16 PM Text Document	5 KB	
Engine 3 Peak Durati	Non_Contiguous_3C_170_85_155	MHz_20 8/31/2021 8:37 PM Text Document	9.13	
Engine 3 Delay: Interpolation: Pythe Length: Pulse RAM Selection: Mind Closer Finable:		Correction Pulse to "C	Config1 InActive"	
Eleanne	carrierNR100M1001_1024.txt	(hd.") hd	~	
Configuration 2	and the second second			
CFR Instance Enables		Qpen	Cancel	
Number of Engines Used: 0 🗸		Channel 2 Engine 3 Peaks Skipped Weight FIFO: 0		
Peak Threshold: 0		Channel 2 Engine 1 Peaks Skipped Peak FIFO: 0		
Correction Threshold Scaler: 0		Channel 2 Engine 2 Peaks Skipped Peak FIFO: 0		
Interpolation: 4		Channel 2 Engine 3 Peaks Skipped Peak FIFO: 0 Channel 2 Engine 1 Peaks Skipped CPC Module: 0		
Pulse Length: 0		Channel 2 Engine 2 Peaks Skipped CPC Module: 0 Channel 2 Engine 2 Peaks Skipped CPC Module: 0		
Pulse RAM Selection: Single Shot		Channel 2 Engine 3 Peaks Skipped CPC Module: 0		System Explorer Platform API Logger

Figure 84. Loading CFR Correction Pulse of Configuration 1: Step 5-1

Once the CFR correction pulse is loaded correctly, a message displays as shown in Figure 85

CFR CONFIGU	RATION	CHANNEL CONFIGURATION	CFR STATISTICS	Expand All. Collapse All
ofile 0 CFR Configuration	^	CFR Channel Selection	CFR Statistics	✓ System ✓ Subsystem, 1
one o crit conngoration	· · · · · · · · · · · · · · · · · · ·			ADRV9040 Platform # ADRV9040 Board
Active Configuration:	Config One	CFR Tx Channel Mask: Ox 01	Window Enable:	# ADR/9040
Construction (Construction)	Config Two	Tx Channel Mask Bit 0.	Clear Stats:	Use Case Selector
Set Active Con	nhg	Tx Channel Mask Bit 1:	Get Statistics	Configurator Device Clock
Load Pulse		Tx Channel Mask Bit 2:	Channel 0 Engine 1 Peaks Detected: 0	E Device Clock
Apply Configuration	Cattions	Tx Channel Mask Bit 3:	Channel O Engine 1 Peaks Detected: 0 Channel O Engine 2 Peaks Detected: 0	4 Runtime
Hopy comparison	(seconds	Tx Channel Mask Bit 4:	Channel 0 Engine 3 Peaks Detected: 0	TDD View Ta Vectors
Configuration 1		Tx Channel Mask Bit 5:	Channel 0 Engine 1 Peaks Skipped Weight FIFO: 0	tx vectors Rx (Capture)
	_	Tx Channel Mask Bit 6:	Channel 0 Engine 2 Peaks Skipped Weight FIFO: 0	ORx (Capture)
CFR Instance Enabled:		Tx Channel Mask Bit 7:	Channel 0 Engine 3 Peaks Skipped Weight FIFO: 0	Radio Sequencer DPD
Number of Engines Used: 3	×	Enable CFR Configuration	Channel 0 Engine 1 Peaks Skipped Peak FIFO: 0	OPD CFR
Peak Threshold: 0	.45	Post CFR Digital Gain: 1	Channel 0 Engine 2 Peaks Skipped Peak FIFO: 0	CLGC
Correction Threshold Scaler:	98		Channel 0 Engine 3 Peaks Skipped Peak FIFO: 0	VSWR
		Post CFR Digital Gain Readback	Channel 0 Engine 1 Peaks Skipped CPC Module: 0	Health Monitoring Custom Filter Tap Estimation
Engine 1 Peak Threshold Scaler 0		Tx 0: 1 Tx 1: 1	Channel 0 Engine 2 Peaks Skipped CPC Module: 0 Channel 0 Engine 3 Peaks Skipped CPC Module: 0	Debug
Engine 1 Peak Duration: 3	0	h t 1 h 2 1	Channel 0 Engine 3 Peaks Skipped CPC Module: 0	Program Settings
Engine 1 Delay: 5	42	12 1	Channel 1 Engine 1 Peaks Detected: 0	
Engine 2 Peak Threshold Scaler: 0	685	3.4 1	Channel 1 Engine 2 Peaks Detected: 0	
		Tx S: 1	Channel 1 Engine 3 Peaks Detected: 0	
Engine 2 Peak Duration: 3		Tx 6: 1	Channel 1 Engine 1 Peaks Skipped Weight FIFO: 0	
Engine 2 Delay: 5	12	Tic 7: 1	Channel 1 Engine 2 Peaks Skipped Weight FIFO: 0	
Engine 3 Peak Threshold Scaler: 0	.99		Channel 1 Engine 3 Peaks Skipped Weight FIFO: 0 Channel 1 Engine 1 Peaks Skipped Peak FIFO: 0	
Engine 3 Peak Duration: 3	0		Channel 1 Engine 1 Peaks Skipped Peak FIFO: 0 Channel 1 Engine 2 Peaks Skipped Peak FIFO: 0	
			Channel 1 Engine 2 Peaks Skipped Peak FIFO: 0	
- for the letter of the letter	12		Channel 1 Engine 1 Peaks Skipped CPC Module: 0	
Interpolation: 4			Channel 1 Engine 2 Peaks Skipped CPC Module: 0	
	024		Channel 1 Engine 3 Peaks Skipped CPC Module: 0	
	ngle Shot			
Hard Clipper Enable:			Channel 2 Engine 1 Peaks Detected: 0 Channel 2 Engine 2 Peaks Detected: 0	
Configuration 2			Channel 2 Engine 2 Peaks Detected: 0 Channel 2 Engine 3 Peaks Detected: 0	
conjunction a			Channel 2 Engine 3 Peaks Detected: 0 Channel 2 Engine 1 Peaks Skipped Weight FIFO: 0	
CFR Instance Enabledt			Channel 2 Engine 2 Peaks Skipped Weight FIFO: 0	
Number of Engines Used: 0	×		Channel 2 Engine 3 Peaks Skipped Weight FIFO: 0	
Peak Threshold			Channel 2 Engine 1 Peaks Skipped Peak FIFO: 0	
Correction Threshold Scaler: 0			Channel 2 Engine 2 Peaks Skipped Peak FIFO: 0	
			Channel 2 Engine 3 Peaks Skipped Peak FIFO: 0	
			Channel 2 Engine 1 Peaks Skipped CPC Module: 0	
Pulse Length: 0			Channel 2 Engine 2 Peaks Skipped CPC Module: 0 Channel 3 Engine 3 Peaks Skipped CPC Module: 0	
Pulse RAM Selection: Sir	ngle Shot		Channel 2 Engine 3 Peaks Skipped CPC Module: 0	System Explorer Platform API Logger
nts				×
estamo Level	Source	Name Type Description		

Figure 85. Loading CFR Correction Pulse of Configuration 1: Step 5-2

Setting CFR Parameters

All CFR parameters can be placed, which depend on the target peak to average ratio (PAR) and the RMS crest factor reduction (CFR) input power. The current **Peak Threshold** 0.3814 is calculated based on the two inputs, namely PAR at 8.0 dB and CFR input at -16.3 dBFS.

CFR CONFLIGURATION CHANNEL CONFLIGURATION CFR STATISTICS Nie 0 CFR Configuration C (R Channel Statesticin) C (R Channel Statesticin) C (R Channel Statesticin) Active Configuration C (R Channel Statesticin) C (R Channel Statesticin) C (R Channel Statesticin) Statestic Configuration C (R Channel Statesticin) C (R Channel Statesticin) C (R Channel Statesticin) Statestic Configuration C (Channel Statesticin) C (Channel Statesticin) C (Channel Statesticin) Control Mast B 1:: C Channel Mast B 1:: C (Channel Mast B 1:: C (Channel Statesticin) Control Mast B 1:: C (Channel Mast B 1:: C (Channel Statesticin) C (Channel Statesticin) Control Mast B 1:: C (Channel Statesticin) C (Channel Statesticin) C (Channel Statesticin) Control Mast B 1:: C (Channel Statesticin) C (Channel Statesticin) C (Channel Statesticin) Control Mast B 1:: C (Channel Statesticin) C (Channel Statesticin) C (Channel Statesticin) Control Mast B 1:: C (Channel Statesticin) C (Channel Statesticin) C (Channel Statesticin) Control Mast B 1:: C (Channel Statesticin) C (Channel Statesticin) C (Channel Statesticin)	elector 🗶 ORx (Capture) 🗶 Tx Vectors 🗶 Vector Generator		System Explorer
Stat Alexe Configuration B A Alexe Configuration Stat Alexe Configuration Configuration <li< th=""><th></th><th></th><th>Expand All Collapse All # System # Subsystem_1</th></li<>			Expand All Collapse All # System # Subsystem_1
Convection Threadul Scale: 0 Outward 2 Expert 2 Mass Stope RNA FID: 0 Interpolation: 4 Outward 2 Expert 2 Mass Stope RNA FID: 0 Palaia Langth: 0 Outward 2 Expert 2 Mass Stope RNA FID: 0 Nata Langth: 0 Outward 2 Expert 2 Mass Stope RNA FID: 0 Durate 2 Expert 2 Mass Stope RCM Module: 0 Outward 2 Expert 2 Mass Stope RCM Module: 0 Nata RAM Melecion: Stopie Stope Outward 2 Expert 2 Mass Stope RCM Module: 0	CR tr Outword Mass to 01 to Counce Mass to 0 1 to 0	Windee Toulie:	ADMOGG Partem ADMOGG Partem ADMOGG Partem ADMOGG Partem Comparison Comparison Participatio

Figure 86. Setting CFR Parameters of Configuration 1, Step 6-1

Once all required parameters are set, click on **Apply Configuration Settings** as shown in Figure 87. Once the parameters are loaded to the inactive **Configuration 1**, the event message is shown as in Figure 87.

CFR CONFIGURATION	CHANNEL CONFIGURATION	CFR STATISTICS	Expand All Collapse All
ofile 0 CFR Configuration	CFR Channel Selection	CFR Statistics	 System Subsystem_1
Active Configuration: Configuration: Set Active Config Lead Pube Apply Configuration Settings Configuration 1 CPR Instance Funded: CPR Instance Funded: Set Active Configuration Settings CPR Instance Funded: Set Active Configuration Settings Configuration 1 CPR Instance Funded: Set Active Configuration Settings Configuration Se	CIR to Cannot Selection CIR to Cannot Mark CIR to Cannot Mark	CFR Schedulat Window Tradei: Care Start: Care Start: Care Start: Chared Diright Phase Detects Oxered Tiright Phase Detects	 Ansystem, 1 Ansystem, 1 Ansystem Ansystem Ansystem Configuration Configuration Configuration Configuration A strate TOD for A strate Configuration Configuration

Figure 87. Apply Configuration 1 Settings: Step 6-2 and Step 6-3

Next, both CFR correction pulse and CFR configuration parameter of **Configuration 1** must be enabled by clicking on **Enable CFR Configuration**. The event message as shown in Figure 88 confirms that **Configuration 1** (inactive) is loaded.

CFR CONFIGURATION	CHANNEL CONFIGURATION	CFR STATISTICS	Expand All Collapse All
			 System Subsystem, 1
ofile 0 CFR Configuration	CFR Channel Selection	CFR Statistics	ADRV9040 Platform
Config One	CFR Tr Channel Mask: 0x 01	Window Enable:	ADR/9040 Board ADR/9040
Active Configuration: Config Two	Tx Channel Mask Bit 0	Oear Stats:	ADRV9040 Use Case Selector
Set Active Config	Tx Channel Mask Bit 1:	Get Statistics	Configurator
	Ty Channel Mark Bit 2		Device Clock
Load Pulse	Tx Channel Mask 8it 3:	Channel 0 Engine 1 Peaks Detected: 0	1) Init Pages
Apply Configuration Settings	Tx Channel Mask Bit 4:	Channel 0 Engine 2 Peaks Detected: 0	TDD View
	Tx Channel Mask Bit S	Channel 0 Engine 3 Peaks Detected: 0	Te Vectors
Configuration 1	Tr Channel Mask Bit 6:	Channel 0 Engine 1 Peaks Skipped Weight FIFO: 0	Rx (Capture) ORx (Capture)
CFR Instance Enabled:	Tx Channel Mask Bit 7:	Channel 0 Engine 2 Peaks Skipped Weight FIFO: 0	Citic (Capiture) Radio Sequencer
Number of Engines Used: 3	Enable CFR Configuration 👉 7-1	Channel 0 Engine 3 Peaks Skipped Weight FIFO: 0 Channel 0 Engine 1 Peaks Skipped Peak FIFO: 0	DPD
	Post CFR Digital Gain: 1	Channel 0 Engine 1 Peaks Skipped Peak FIFO: 0 Channel 0 Engine 2 Peaks Skipped Peak FIFO: 0	CFR
Peak Threshold: 0.45	figuration to "Config1 Inactive"	Channel 0 Engine 2 Peaks Skipped Peak FIFO: 0	CLGC VSWR
Correction Threshold Scaler:	Rest CFR Digital Gain Readback	Channel 0 Engine 1 Peaks Skipped CPC Module: 0	Health Monitoring
Engine 1 Peak Threshold Scaler: 0.98	Tx 0: 1	Channel 0 Engine 2 Peaks Skipped CPC Module: 0	Custom Filter Tap Estimation
Engine 1 Peak Duration: 30	3(1) 1	Channel 0 Engine 3 Peaks Skipped CPC Module: 0	Debug Program Settings
Engine 1 Delay: 512	h2 1 h2 1	Channel 1 Engine 1 Peaks Detected: 0	- top an acting
and the second sec	54 1	Channel 1 Engine 2 Peaks Detected: 0	
Engine 2 Peak Threshold Scaler: 0.985	5.5 1	Channel 1 Engine 3 Peaks Detected: 0	
Engine 2 Peak Duration: 30	5.6 1	Channel 1 Engine 1 Peaks Skipped Weight FIFO: 0	
Engine 2 Delay: 512	76.72 1	Channel 1 Engine 2 Peaks Skipped Weight FIFO: 0	
Engine 3 Peak Threshold Scaler 0.99		Channel 1 Engine 3 Peaks Skipped Weight FIFO: 0	
and the second sec		Channel 1 Engine 1 Peaks Skipped Peak FIFO: 0	
Engine 3 Peak Duration: 30		Channel 1 Engine 2 Peaks Skipped Peak FIFO: 0	
Engine 3 Delay: 512		Channel 1 Engine 3 Peaks Skipped Peak FIFO: 0	
Interpolation: 4		Channel 1 Engine 1 Peaks Skipped CPC Module: 0	
Pulse Length: 1024		Channel 1 Engine 2 Peaks Skipped CPC Module: 0 Channel 1 Engine 3 Peaks Skipped CPC Module: 0	
Pulse RAM Selection: Single Shot		Channel 1 Engine 3 Peaks Skipped CPC Module 0	
Hard Clipper Enable:		Channel 2 Engine 1 Peaks Detected: 0	
	-	Channel 2 Engine 2 Peaks Detected: 0	
Configuration 2		Channel 2 Engine 3 Peaks Detected: 0	
CFR Instance Enabled		Channel 2 Engine 1 Peaks Skipped Weight FIFO: 0	
		Channel 2 Engine 2 Peaks Skipped Weight FIFO: 0	
	U	Channel 2 Engine 3 Peaks Skipped Weight FIFO: 0	
Peak Threshold: 0		Channel 2 Engine 1 Peaks Skipped Peak FIFO: 0 Channel 2 Engine 2 Peaks Skipped Peak FIFO: 0	
Correction Threshold Scaler: 0		Channel 2 Engine 2 Peaks Skipped Peak FIFO: 0 Channel 2 Engine 3 Peaks Skipped Peak FIFO: 0	
Interpolation: 4		Channel 2 Engine 3 Peaks Skipped CPC Module: 0	
Pulse Length: 0	1	Channel 2 Engine 1 Peaks Skipped CPC Module: 0	
Pulse RAM Selection: Single Shot		Channel 2 Engine 3 Peaks Skipped CPC Module: 0	And a second
Public Novin Selection: Single Shot			System Explorer Platform API Logger
ints			×
mestamp Level Source	Name Type Description		
18/24 10:35:3 minformational CfrConfigEnal		1 Enabled 👍 7-2 Events : Configuration enabled	to "Config1 Inactive"

Figure 88. Enable CFR Configuration 1: Step 7-1 and Step 7-2

Lastly, click on Config One and then Set Active Config as shown in Figure 89.

CFR CONFIGURATION	CHANNEL CONFIGUR	ATION CFR STATISTICS	Expand All Collapse All
ofile 0 CFR Configuration	CFR Channel Selection	CFR Statistics	 System Subsystem, 1 ADR/9040 Platform
Adve Configuration A Active Configuration Configuration Configuration Configuration Configuration Series Set Assoc Config Active Active Active Active Active Configuration Series Configuration 1 CONFIGURATION C	CHE Channel Selection CHE Channel Selection CHE Channel Selection CHE Channel Mark 10:0 CHE Channel Mark 10:0 CHE CHE Channel Mark 10:0 CHE	Window Institute Cell Status Cell Status Cell Status Channel & Engine 1 Raska Denotest Channel & Engine 1 Raska Denotest Channel & Engine 2 Raska Denotest Cell Channel & Engine 1 Raska Denotest Cell Channel & Engine 1 Raska Denotest Cell Cell Cell Cell Cell Cell Cell Cel	

Figure 89. Activate CFR Configuration 1: Step 8-1 and Step 8-2

Before **Config One** is enabled, check that the original ACLR and Gaussian complementary cumulative distribution function (CCDF) of spectrum analyzer are confirmed. After CFR **Config One** is enabled, it is observed that ACLR is by 0.1 dB degraded and PAR is reduced to 8.10 dB at 0.01% from 9.65 dB at 0.01% as shown in Figure 91.



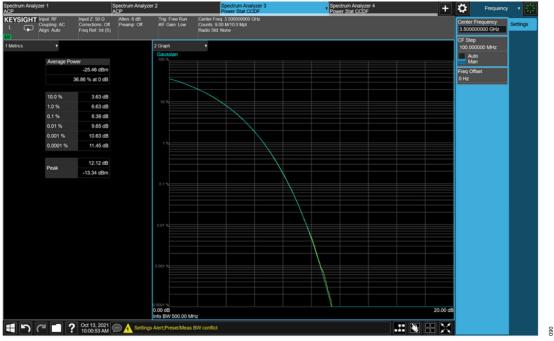


Figure 90. Initial CFR Configuration 1: ACPR and CCDF

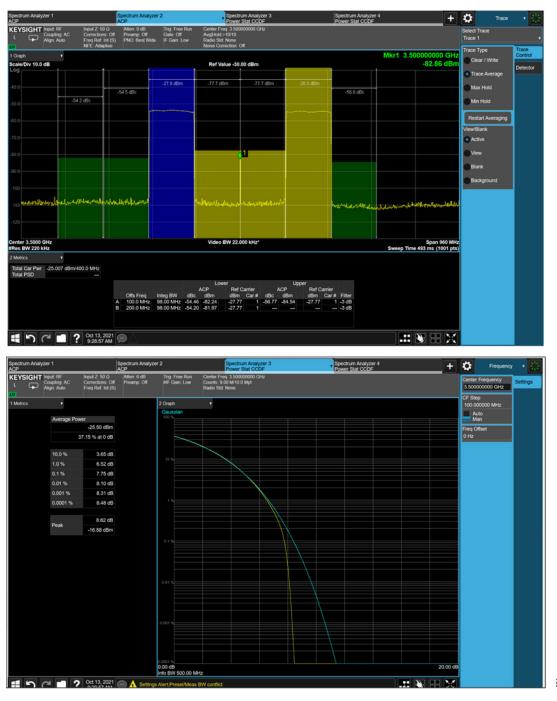


Figure 91. After Enabling Set CFR Configuration 1: ACPR and CCDF

Using statistics in the GUI, check that there is no peak skipping with **Configuration 1**. Before clicking on **Get Statistics**, **Window Size** needs to be filled with the range 15 as shown in Figure 92. It can be executed by clicking on **Get Statistics** to get the CFR statistics. As shown in Figure 93, the peaks of signals over the three engines are detected but no peak skipping is observed.

RUNTIME

CFR CONF	GURATION		CHANNEL CONFIGURATION	CFR STATISTICS		Expand All. Collapse All
ofile 0 CFR Configura		^	CFR Channel Selection	CFR Statistics		 System Subsystem_1 ADR/9040 Platform
Active Configuration: Set A Lo Apply Cent Configuration 1 CFR Instance Enabled: Number of Engines Used: Peak Threshold:	Config One Config Two ctive Config ad Pulse guration Settings 0 0.45	<	CR C Annel Selection CR To Annel Market CR To Annel	Ork Statistical Worker Forain Worker Forain Worker Stat Tast Prevba Worker Orker Stat Get Statistic Get Statistic Get Statistic Orkers 0 Egypt 1 Neis Directed Orkers 1 Egypt 1 Neis Directed Orkers 1 Egypt 1 Neis Orkers 1 Egypt Neis Directed Orkers	4 9-1	
Correction Threshold Scale threspolation: Nate Langth: Nate Editors: Nate RMN Selection: Nate Clapter Chable Configuration 2 CRE Instance Exabled: Number of Explose Used: Nate Arreshold Correction Threshold Scale threspolation: Nate RMN Selection: Nate RMN Selection: Nate RMN Selection:	4 1024 Stope Stort 0 0 0 4 0 Single Short 	×	Perc CR Diput Gan Resoluci 10 0 11 1 15 1 1 15 2 1 15 2 1 15 2 1 15 4 1 15 5 1 15 6 1 15 7 1	Cannot Dispot Press Staged Part 100 0 Cannot Dispot Press Staged Part 100 0 Cannot Dispot Press Staged Part 100 0 Cannot Dispot Press Staged CPK Made 0 Cannot Dispot Press Staged CPK Made 0 Cannot Dispot Park Staged CPK Made 0 Cannot Tispot Park Staged CPK Made 0 Cannot Tispot Park Staged CPK Made 0 Cannot Tispot Park Staged Part 100 0 Cannot Tispot Park Staged Park 100 0		I tot Page I tot Page I tot Page I tot Vee I tot Vee I to Vee I to Vee I to Vee I tot Vee I tott Vee I tott Vee I tott Vee I tot Vee I tot Vee I
file 1 CFR Configura file 2 CFR Configura file 3 CFR Configura nmon	tion	> > ^		Okanel 2 logier 1 hala Deschell Okanel 2 logier 1 hala Staged Mart 150 0 Okanel 2 logier 1 hala Nate 150 0 Okanel 2 logier		System Explorer Partform API Logger

Figure 92. Get Statistics of Configuration 1: Window Size

CFR CONFIGURATION	CHANNEL CONFIGURATION	CFR STATISTICS		Expand Al Collapse Al System Subsystem_1 ADRV9040 Board
Active Config Order Set Active Config Order Set Active Config Tree Set Active Config Tree Set Active Config Tree Configuration 1 Centropuration 1 Centropuration Scheduled Centropuration Scheduled Centropuration Scheduled Centropuration Scheduled Centropuration Scheduled Configuration Scheduled Centropuration Schedul	Of R. Downed Matic 61 10. Observed Matic 62 10. Observed Matic 74 10. Observed Matic 74 <t< td=""><td>Window Doale Image: Control State Stat</td><td> 9-2 Statistics of "Config1 Activity </td><td>ADR/9040 Use Case Selector Configurator Device Cock Init Pages Runtime TDD View</td></t<>	Window Doale Image: Control State Stat	 9-2 Statistics of "Config1 Activity 	ADR/9040 Use Case Selector Configurator Device Cock Init Pages Runtime TDD View

Figure 93. Get Statistics of Configuration 1

Configuration 2

The sequence of **Configuration 2** is the same as that of **Configuration 1**. Therefore, only figures without an auxiliary explanation are added to enable **Configuration 2**.

Activate Configuration 1 and Inactive Configuration 2: Step 10 and Step 11

To set **Configuration 2**, it must be inactive to not impair the Tx channel when the CFR correction pulse and parameters are loaded to the inactive **Configuration 2**.

CFR CONFIGURATION	CHANNEL CONFIGURATION	CFR STATISTICS	Expand All Collapse All
			a System
ofile 0 CFR Configuration	CFR Channel Selection	CFR Statistics	ADRV9040 Platform
Alle D CIR Configuration Alter Configuration Alter Configuration Stit Alter Centry S	To Charace Mark B(1) Image: Charace Mark B(2) Image: Char	CRE. Statistics Image: Creating Statistics Window Exable: Window	 Subgrings, Samo Barris, Samo Samo Samo Samo Samo Samo Samo Samo

Figure 94. Activate Configuration 1 and Inactive Configuration 2: Step 10

Once selected, **Configuration 1** is active and configuration is ready to be updated with the CFR correction pulse and CFR parameters in Figure 94 and Figure 95.

Start X System X ADRV9040 X Use Case Selecto	Y X CFR X		System Explorer
CFR CONFIGURATION	CHANNEL CONFIGURATION	CFR STATISTICS	Expand All Collapse All
Profile 0 CFR Configuration	CFR Channel Selection	CFR Statistics	▲ Subsystem_1 ADRV9040 Platform
Attive Configuration Attive Configuration Attive Configuration Attive Configuration Attive Configuration Apply Configuration Apply Configuration Apply Configuration Apply Configuration Apply Configuration Configuration Apply Ap	CPR 1:: Obunnet Mark © 1 1:: Channet Mark © 1 1:: Channet Mark D 1 1:: Channet Mark	Window Sze: Image: State	ADR/NO40 Band ADR/NO40 Uni Cas Stetter Configuration Double Stetter Configuration Double Stetter Tob View Tob View Tob View Tob View Cold (castron) Ray Regulatories Ray Regulatories Cold (castron) Cold (castron)

Figure 95. Activate Configuration 1 and Inactive Configuration 2: Step 11

Loading CFR Correction Pulse: Step 4 for Config Two

To upload the CFR correction pulse, click on Load Pulse as shown in Figure 96.

095

art 🗙 System 🗙 ADRV9040 🗶 Use Case Selec	or X CFR X		System Explorer
CFR CONFIGURATION	CHANNEL CONFIGURATION	CFR STATISTICS	Expand All Collapse All
ofile 0 CFR Configuration	CFR Channel Selection	CFR Statistics	✓ System ▲ Subsystem_1 ADR/S040 Platform
Active Configuration Config Drom Configuration Cardiguration Cardigurati	CR: to Channel Mark to Criterio Criterio Criterio Control Mark to Criterio Control Mark to Criterio Control Mark to Criterio Mark to Criteria Mark to Criterio	Window Enable: Image: Second	A JORTSKO Band A JORTSKO Band Unclass Sketorr Consumer Consumer Consumer Service Case Sketorr Consumer TOD View Turding TOD View Turding Gold case Consumer Sketorr Sketor

Figure 96. Loading CFR Correction Pulse of Configuration 2: Step 12

Once clicked, the directory and the CFR correction pulse can be located in Figure 97, assuming that the CFR correction pulse exists.

at X System X ADRV90	40 🗙 Use Case Selecti	Y X CFR X						System Explorer	
CFR CONFIGU	JRATION	CHANNEL CONFIGU	JRATION	CFR STATISTICS	5			Expand All Collapse All	
ofile 0 CFR Configuration	^	CFR Channel Selection	^	CFR Statistics	~			A Subsystem_1 ADRV9040 Pt	atform
Active Configuration: Set Active Co Load Puls Apply Configuratio		CFR.Ts Channel Mask B 0 ✓ Ts Channel Mask B 0 ✓ Ts Channel Mask B 1: Ts Channel Mask B 2: Ts Channel Mask B 2: Ts Channel Mask B 4:		Window Enable: Window Size: Read Previous Window: Clear Stats: Get Statistics	15			⇒ Confi ⇒ Devic ⇒ Init Pi ∡ Runti	0 lase Selector gurator e Clock bges me DD View
Configuration 1		Analysis Control Evaluation				×		R	(Vectors (Capture)
CFR Instance Enabled:	~	(AkarorSWig3 > Pulse 		6 Search Pub	A			Rx (Capture) adio Sequencer
Number of Engines Used:	3 ~	Downleads	d A Name	A Data modified	Tate	See			PD
Peak Threshold	0.45	Documents	/ 2carried4	R100M1001_512.64		410		a	LGC
Correction Threshold Scaler:	0.95	Pictures OPD, enabled		R100M1001_0024.54 - 10/7/2021 11/8 A0	Text Document	7 KB 6 KB			SWR ealth Monitoring
Engine 1 Peak Threshold Scaler	0.95	DPD_enabled		R100M1101UCT9A668Fed_512A8 10/7/2021111/8 A/ R100M1101UCT9A668Fed_1024 10/7/202110.57 A/		6 KB 11 KB		Custo	m Filter Tap Estimatio
Engine 1 Peak Duration:	30	Pube		Higwows, 3C, 145, 80, 160MPHz, 20. 9/1/2021 1:49 PM Higwows, 3C, 170, 85, 155MPHz, 20. 8/31/2021 6:16 PM		9 KB 5 KB		Debu Progr	g am Settings
Engine 1 Delay:	512	Python Scott		ntgurus_IC_170_85_155MHg_20 6/31/2321 637 PM		9.13			-
Engine 2 Peak Threshold Scaler	0.985	CheDrive - Analog Devices, Inc	0.1			0.00	A		
Engine 2 Peak Duration:	30	This PC	Select H	alf CFR Correction P	ulse to	Config2 li	nActive"		
Engine 2 Delay:	512	30 Objects							
Engine 3 Peak Threshold Scaler:	0.99	Desittop	¥						
Engine 3 Peak Duration:	30	File geme: 2canie/5810	041001_512.64		✓ 84 (*.64)	~			
Engine 3 Delay:	512		1	Channel 1 Engine 3 Peaks Skipped Peak	Dpm FIFO: 0	Cancel			
interpolation:	4			Channel 1 Engine 1 Peaks Skipped CPC I					
Pulse Length:	٥		I	Channel 1 Engine 2 Peaks Skipped CPC 1 Channel 1 Engine 3 Peaks Skipped CPC 1					
Pulse RAM Selection: Hard Clipper Enable:	Single Shot			Channel 2 Engine 1 Peaks Detected:	0				
Configuration 2				Channel 2 Engine 2 Peaks Detected: Channel 2 Engine 3 Peaks Detected:	0				

Figure 97. Loading CFR Correction Pulse of Configuration 2: Step 13-1

Once loaded correctly, the message is displayed as shown in Figure 98.

660

RUNTIME

art X System X ADRV9040	X Use Case Selecto	X OR X			System Explorer
CFR CONFIGUE		CHANNEL CONFIGURATION		CFR STATISTICS	Expand All Collapse All System Subsystem 1
Active Configuration: Set Active Configuration: Configuration 1 CPR Instance Enabled: Park Threshold Configuration: CPR Instance Enabled: Park Threshold Configuration: Engine 1 Peak Threshold Scaler: Engine 1 Peak Threshold Scaler: Engine 1 Peak Threshold Scaler: Engine 1 Peak Duration: Engine 2 Peak Duration: Engine 2 Peak Duration: Engine 3 Peak Durati	Settings 3 3 3 4 3 3 4 5 4 5 4 5 5 5 5 5 5 5 5 5	CFR Channel Selection CPR to Channel Maik © 01 Is Channel Maik B 0 Is Channel Maik B 0 Is Channel Maik B 0 Is Channel Maik B 2 Is	Claims Cl	Enable: See: 15 Hous Window:	Lobysten,1 AchiveSholds Partners AchiveSholds User Cars States User Cars States Dence Cool Dence Cool Dence Cool Dence Cool Dence Cool Too View Too View Too View Ro Caluted Doo Crit Crit Cool Crit Crit Cool Crit Crit
vents				Events :Half CFR Correction Pu	Ise written to "Config2 Inactive"
imestamp Level	Source	Name	Type	Description	
12/21 9:10:51 Oinformational		CFR Load Pulse	Unspecified		
12/21 9:20:17 Oinformational			ation Unspecified		
0/12/21 9:23:7 Oinformational		CFR Enable	Unspecified		4 13-2
	LoadPulse	CFR Load Pulse			

Figure 98. Loading CFR Correction Pulse of Configuration 1: Step 13-2

Setting CFR Parameters for Configuration 2

All CFR parameters can be placed, which depend on the target PAR and the RMS CFR input power. The current **Peak Threshold** 0.3814 is calculated based on the two inputs, namely PAR at 8.0 dB and CFR input at -16.3 dBFS.

X System X ADRV904	U A Usé Case Selecto	X A UK A				System Explorer
CFR CONFIGU	RATION	CHANNEL CONFIGURATION	CFR STATISTICS			Expand All Collapse All
	(9	System Subsystem_1
Engine 3 Peak Threshold Scaler.	0.99	CFR Channel Selection	CFR Statistics	~		ADRV9040 Platform
Engine 3 Peak Duration:	30	and a survey for the survey of the	Window Enable:			ADRV9040 Board
Ingine 3 Delay:	512	CFR Tx Channel Mask: 0x 01				# ADRV9040
	216	Tx Channel Mask Bit 0. 🗸	Window Size:	15		Use Case Selector
nterpolation	4	Tx Channel Mask Bit 1:	Read Previous Window:	\sim		 Configurator
Pulse Length:	0	Tx Channel Mask Bit 2	Clear Stats			 Device Clock
Pulse RAM Selection:	Single Shot	Tx Channel Mask Bit 3:	Get Statistics			Init Pages A Runtime
fand Clipper Enable:		Tx Channel Mark Bit &	OR SOMEOUS			TDD View
		Tx Channel Mask Bit S				Tx Vectors
Configuration 2			Channel 0 Engine 1 Peaks Detected: Channel 0 Engine 2 Peaks Detected:	8154 735		Rx (Capture)
	-	Tx Channel Mask Bit 6:	Channel 0 Engine 2 Peaks Detected: Channel 0 Engine 3 Peaks Detected:	3		ORx (Capture)
	<u>~</u>	Tx Channel Mask Bit 7:	Channel 0 Engine 1 Peaks Skipped Weight FIFG	20		Radio Seguencer
Number of Engines Used:	3 🗸	Enable CFR Configuration	Channel 0 Engine 2 Peaks Skipped Weight FIFO			DPD
Peak Threshold	0.45	Post CFR Digital Gain: 1	Channel 0 Engine 3 Peaks Skipped Weight FIFO			CFR CLGC
		· · · · · · · · · · · · · · · · · · ·	Channel 0 Engine 1 Peaks Skipped Peak FIFO:	0		VSWR
Correction Threshold Scaler:	0.98	Post CFR Digital Gain Readback	Channel 0 Engine 2 Peaks Skipped Peak FIFO:	0		Health Monitoring
Ingine 1 Peak Threshold Scaler	0.98	Tx0 1	Channel 0 Engine 3 Peaks Skipped Peak FIFO:	0		Custom Filter Tao Estima
		101 1	Channel 0 Engine 1 Peaks Skipped CPC Module			Debug
Ingine 1 Peak Duration:	30	1/2 1	Channel 0 Engine 2 Peaks Skipped CPC Module			Program Settings
Engine 1 Delay	512	103 1	Channel 0 Engine 3 Peaks Skipped CPC Module	e 0		
		Tx4: 1	Channel 1 Engine 1 Peaks Detected:	8117	1	
Engine 2 Peak Threshold Scaler.	0.965	Tx S: 1	Channel 1 Engine 2 Peaks Detected:	714		
Ingine 2 Peak Duration:	30	Tx 6: 1	Channel 1 Engine 3 Peaks Detected	1		
Ingine 2 Delay:	512	Tx 7: 1	Channel 1 Engine 1 Peaks Skipped Weight FIFO	2.0		
ingine z velay:	316		Channel 1 Engine 2 Peaks Skipped Weight FIFO			
Engine 3 Peak Threshold Scaler.	0.99		Channel 1 Engine 3 Peaks Skipped Weight FIFO			
Ingine 3 Peak Duration:	30	14-1	Channel 1 Engine 1 Peaks Skipped Peak FIFO:	0		
		1	Channel 1 Engine 2 Peaks Skipped Peak FIFO:	0		
Ingine 3 Delay:	512 Place n	arameters to "Config2 Inactive"	Channel 1 Engine 3 Peaks Skipped Peak FIFO:			
nterpolation:	4		Channel 1 Engine 1 Peaks Skipped CPC Module		1	
Pulse Length:	0		Channel 1 Engine 2 Peaks Skipped CPC Module			
Aulse RAM Selection:	Single Shot		Channel 1 Engine 3 Peaks Skipped CPC Module	E 0		
Hard Clipper Enable:			Channel 2 Engine 1 Peaks Detected:	0		
	Post Att		Channel 2 Engine 2 Peaks Detected:	0		
Hard Clipper Selection:	Post Att		Channel 2 Engine 3 Peaks Detected:	0		
Hard ClipperThreshold:	0		Channel 2 Engine 1 Peaks Skipped Weight FIFO	0:0		
			Channel 2 Engine 2 Peaks Skipped Weight FIFC	0:0		
ile 1 CFR Configuration	~		Channel 2 Engine 3 Peaks Skipped Weight FIFO	0.0	1	

Figure 99. Setting CFR Parameters of Configuration 1: Step 14-1

Once all required parameters are set, click on **Apply Configuration Settings** as shown in Figure 100. Once the parameters are loaded to the inactive **Configuration 2**, the event message is shown as in Figure 100.

CFR CONFIGURATION	CHANNEL CONFIGURATION	CFR STATISTICS	Expand All Collapse All
			a System
file 0 CFR Configuration	CFR Channel Selection	CFR Statistics	ADR/9040 Platform
Althe Configuration Athe Configuration Athe Configuration StatAthe Configuration StatAthe Configuration StatAthe Configuration StatAthe Configuration Ather Configuration StatAthe Configuration StatAthe Configuration StatAther Configuration StatAt	CIR Concerd Statestion CIR to Quarter Mark CIR to Quarter Mark CIR to Quarter Mark CIR To Quarter Mark CIR	CRE Solutation Image: Creation of the solution of the	 Selegtant, 1 Abiridoli Barian Activity Barian Activity Barian Activity Barian Barian Activity Barian

Figure 100. Apply Configuration 1 Settings: Step 14-2 and Step 14-3

Next, both CFR correction pulse and CFR configuration parameter of **Configuration 2** must be enabled by clicking on **Enable CFR Configuration**. The event message as shown in Figure 101 confirms that **Configuration 2** (inactive) is loaded.

CFR CONFIGU	IRATION	CHANNEL CONFIGURATION	ON CFR STATISTICS	Expand All Collapse All
file 0 CFR Configuration	^	CFR Channel Selection	CFR Statistics	∠ System ∠ Subsystem,1 AD#V9040 Platform
Athle Configuration: Set Athle Configuration Configuration 1 Configuration 1 Configurat	■ n Settings 3 ▼ 0.45 0.90 0.90 512 0.905 50 512 0.905 50 512	CR to Council Mate () () to Caracter Mate () () to C	Channell Engling Frains Staget O'C. Mondell E Channell Engling Frains Staget O'C. Mondell E Channell Toginer Frains Ortestell Channell Toginer Frains Ortestell Channell Toginer Frains Ortestell Channell Toginer Frains Staget Waget FFRO & Channell Toginer Frains Staget Frain FFO & Channell Toginer Frains Staget O'C. Mondule & Channell Toginer Frains Staget O'C. Mondule & Channell Toginer Frains Staget O'C. Mondule & Channell Zoginer Frains Staget Waget FFFO & Channell Zoginer Frains Staget Waget FFFO &	ADD/NOU Stand ADD/NOU ADD/NOU Configuration Configuration Configuration Prove Conk In Init's Pays Turner Turner
Configuration 2			Channel 2 Engine 3 Peaks Skipped Weight PIPO: 0	
nts				×
testamp Level 12/21 9:10:51 (Informational	Source	Name CFR Load Pul	Bype Description Unspecified CFR Correction pulse 1 written to the device	a using channel mark (n2
12/21 9:20:17 (Informational			guration Unspecified Set configuration 1 with config settings 1 s	
12/21 9:23:7 Oinformational		CFR Enable	Unspecified CFR Configuration 1 Enabled	
12/21 9:44:26 Oinformational		CFR Load Pul		z using channel mask 0x3
12/21 9:49:7 Oinformational			guration Unspecified Set configuration 2 with config settings 2 of	using chagnel mask 3
12/21 9.51:34 OInformational		CFR Enable	Unspecified CFR Configuration 2 Enabled	15-2

Figure 101. Enable CFR configuration 1: Step 15-1 and Step 15-2

Lastly, click on Config Two and then Set Active Config as shown in Figure 102.

CED CONFICE	DATION			Expand All Collapse All	
CFR CONFIGU	JRAHON	CHANNEL CONFIGURATION	CFR STATISTICS	4 System	
ofile 0 CFR Configuration		CFR Channel Selection	CFR Statistics	4 Subsystem 1	
one of CER Configuration	^	CFR Channel Selection	CPR Statistics	ADRV9040 F	
	Config One	CFR Tx Channel Mask: 0x 01	Window Enable:	▲ ADRV9040 8	
Active Configuration:		6-1x Channel Mask Bit 0	Window Size: 15	ADRV90	40 Case Selector
		Tx Channel Mask Bt 1:	Read Previous Window:		ligurator
Set Active Co		Tx Channel Mark Bt 2:	Clear Stats:		ce Clock
Load Puls	• 16-2	Tx Channel Mask Bt 2		> Init i	
Apply Configuratio	in Settings		Get Statistics	# Run	ine DD View
		Tx Channel Mask Bt 4:			bD View x Vectors
Configuration 1		Tx Channel Mask Bt S:	Channel 0 Engine 1 Peaks Detected: 8154		tx (Capture)
	_	Tx Channel Mask Bit 6:	Channel 0 Engine 2 Peaks Detected: 735		ORx (Capture)
CFR instance Enabled:	✓	Tx Channel Mask Bit 7:	Channel 0 Engine 3 Peaks Detected: 3		ladio Sequencer
Number of Engines Used:	3 🗸	Enable CFR Configuration	Channel 0 Engine 1 Peaks Skipped Weight FIFO: 0 Channel 0 Engine 2 Peaks Skipped Weight FIFO: 0		DPD DFR
Peak Threshold	0.45	Post CFR Digital Gain: 1	Channel 0 Engine 3 Peaks Skipped Weight FIFO: 0		160
			Channel 0 Engine 1 Peaks Skipped Peak FIFO: 0		SWR
Correction Threshold Scaler:	0.96	Post CFR Digital Gain Readback	Channel 0 Engine 2 Peaks Skipped Peak FIFO: 0		lealth Monitoring
Engine 1 Peak Threshold Scaler	0.98	Tx 0: 1	Channel 0 Engine 3 Peaks Skipped Peak FIFO: 0		om Filter Tap Estimation
Engine 1 Peak Duration:	30	Tx 1: 1 Tx 2: 1	Channel © Engine 1 Peaks Skipped CPC Module: 0	Deb	ram Settings
		1x2 1 1x3 1	Channel © Engine 2 Peaks Skipped CPC Module: 0 Channel © Engine 3 Peaks Skipped CPC Module: 0		and proceeds
Engine 1 Delay:	512	7/4 1	Contract of the press property of mouse of		
Engine 2 Peak Threshold Scaler	0.965	Tx 5: 1	Channel 1 Engine 1 Peaks Detected: 8117		
Engine 2 Peak Duration:	30	Tx 6: 1	Channel 1 Engine 2 Peaks Detected: 714		
		Tx 7: 1	Channel 1 Engine 3 Peaks Detected: 3		
Engine 2 Delay:	512		Channel 1 Engine 1 Peaks Skipped Weight FIFO: 0 Channel 1 Engine 2 Peaks Skipped Weight FIFO: 0		
Engine 3 Peak Threshold Scaler	0.99		Channel 1 Engine 2 Peaks Skipped Weight FIFO: 0 Channel 1 Engine 3 Peaks Skipped Weight FIFO: 0		
Engine 3 Peak Duration:	30		Channel 1 Engine 1 Peaks Skipped Peak FIFO: 0		
			Channel 1 Engine 2 Peaks Skipped Peak FIFO: 0		
Engine 3 Delay:	512		Channel 1 Engine 3 Peaks Skipped Peak FIFO: 0		
Interpolation	4		Channel 1 Engine 1 Peaks Skipped CPC Module: 0 Channel 1 Engine 2 Peaks Skipped CPC Module: 0		
Pulse Length:	0		Channel 1 Engine 3 Peaks Skipped CPC Module: 0		
Pulse RAM Selection:	Single Shot				
Hard Clipper Enable:			Channel 2 Engine 1 Peaks Detected: 0		
Configuration 2			Channel 2 Engine 2 Peaks Detected: 0		
Corriguistion 2			Channel 2 Engine 3 Peaks Detected: 0 Channel 2 Engine 1 Peaks Skipped Weight FIFO: 0		
CFR Instance Enabled			Channel 2 Engine 1 Peaks Skipped Weight FIPO: 0 Channel 2 Engine 2 Peaks Skipped Weight FIFO: 0		
	1		Channel 2 Engine 3 Peaks Skipped Weight FIFO: 0		

Figure 102. Activate CFR Configuration 1: Step 16-1 and Step 16-2

Before **Config Two** is enabled, check that the original ACLR and Gaussian CCDF of spectrum analyzer are confirmed. After CFR **Config Two** is enabled, it is observed that ACLR is by 0.1 dB degraded and PAR is reduced to 8.10 dB at 0.01% from 9.65 dB at 0.01% as shown in Figure 104.

Spectrum Analyzer 1 ACP	SA	pectrum Analyzer CP	2		um Analyzer 3 Stat CCDF		Spectrum Analyze Power Stat CCDF	¥ 4	+	🗘 Trace	· *
KEYSIGHT Input: RF L Align: Auto	Input Z: 50 Ω Corrections: Off Freq Ref: Int (S) NFE: Adaptive	Atten: 0 dB Preamp: Off PNO: Best Wide	Trig: Free Run Gate: Off IF Gain: Low	Center Freq: 3.500 Avg Hold: 7/10 Radio Std: None Noise Correction:						Select Trace Trace 1	
1 Graph v Scale/Div 10.0 dB				Ref Value -30	.00 dBm			Mkr1 3.50	0000000 GHz -83.03 dBm	Trace Type Clear / Write	Trace Control
Log	i									Trace Average	Detector
10.0			-27.8 dBm	-77.9 dBm	-77.7 dBm						
-40.0		54.1 dBc					-56.3 dBc	1		Max Hold	
-50.0 -5	3.9 dBc									Min Hold	
-60.0										Restart Averaging	
										View/Blank	
-70.0										 Active 	
-80.0					1					View	
-90.0										Blank	
										Background	
	runintralan	white		k.postilai.k.as	diktrostotostostot		udaliling Merse	anthrough the	konnorskiple		
-120											
Center 3.5000 GHz #Res BW 220 kHz				Video BW 22	000 kHz*			: Sweep Time	Span 960 MHz 493 ms (1001 pts)		
2 Metrics ¥											
Total Car Pwr -24.971 dBm/ Total PSD	400.0 MHz										
1000 100				Lower		Upper					
		Offs Freq Ir	nteg BW dBc		Carrier ACP Car# dBc dB		ler ar# Filter				
	AB	100.0 MHz 9	8.00 MHz -54.1 8.00 MHz -53.9	2 -81.88 -27.7	5 1 -56.30 -84		1 -3 dB				
	в	200.0 MHZ 9	0.00 mnz -53.8	-21.1	J 1						
4 7 7 1 1	Oct 13, 2021										
والكالكر بهاليها	10:02:46 AM										

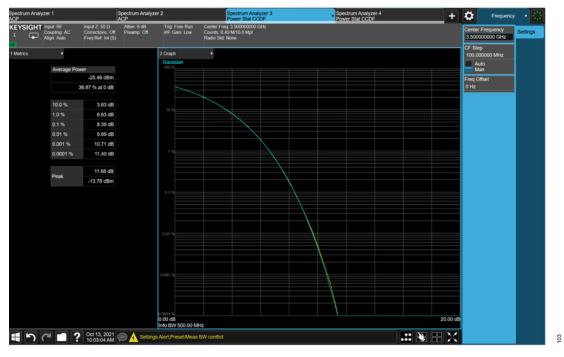


Figure 103. Initial CFR Configuration 2: ACP and CCDF



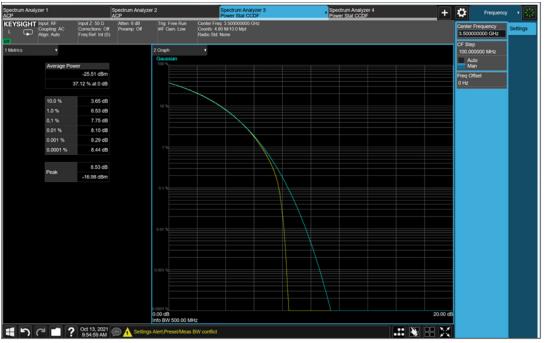


Figure 104. After Enabling Set CFR Configuration 2: ACP and CCDF

Using statistics in the GUI, check that there is no peak skipping with the **Configuration 2**. Before clicking on **Get Statistics**, **Window Size** needs to be filled with the range 15 as shown in Figure 105. It can be executed by clicking on **Get Statistics** to get the CFR statistics. As shown in Figure 106, the peaks of signals over the three engines are detected but no peak skipping is observed.

CFR CONFIGURAT	ON CHANNEL CONFIGURATION	CFR STATISTICS		Expand All Collapse All
file 0 CFR Configuration	CFR Channel Selection	CFR Statistics		▲ System ▲ Subsystem_1
Active Configuration C Co Set Active County Load Nave Apply Configuration Settin Configuration Settin Configuration Settin Configuration State Park Threehold Settin Sections Threach Section Set Sections Threach Section Section Sections Threach Section Section Sections Threach Section Section Sections Threach Section Section Section Section Section Section Section Section Section Section	fig One CFR Tx Channel Mask: © 01 fig Two Tx Channel Mask B0 © Tx Channel Mask B1 E Tx Channel Mask B1 E Tx Channel Mask B1 B B Tx Channel Mask B1 B	Characteristics Window Exable: Window Exable: Window Case Road Previous Window: Cell States Connoil 6 Inguer 1 Prais Defective Cell States Connoil 6 Inguer 1 Prais Defective The Connoil 6 Inguer 2 Prais Therefore Connoil 6 Inguer 2 Prais Therefore Connoil 6 Inguer 1 Prais Therefore Connoil 6 Inguer 1 Prais Therefore Connoil 6 Inguer Therefore Therefore Connoil 6 Inguer Therefor	• 17-1	Abhrydd Parform Abhrydd Parform Abhrydd Burd Bornes Comparison Comparison Device Cless Interne Toto Burdine Device Cless Interne Toto Burdine Device Cless Interne Toto Burdine Device Cless Interne Comparison Device Comparison Compariso
topper Doray 132 project Porty Control Scale forgine 2 Peak Porty Scale forgine 2 Peak Porty Scale forgine 2 Peak Porty Scale forgine 3 Peak Porty Scale for	164 1 169 1 166 1 167 1	Owner! 1 Page 1 Pasis Defende 8117 Owner! 1 Page 2 Pasis Defende 714 Owner! 1 Page 3 Pasis Defende 714 Owner! 1 Page 3 Pasis Deged Wayd FFP0 0 700 Owner! 1 Page 3 Pasis Deged Wayd FFP0 0 700 Owner! 1 Page 3 Pasis Deged Wayd FFP0 0 700 Owner! 1 Page 3 Pasis Deged Wayd FFP0 0 700 Owner! 1 Page 3 Pasis Deged Park FF0 0 700 Owner! 1 Page 3 Pasis Staged Park FF0 0 700 Owner! 1 Page 3 Pasis Staged Park FF0 0 700 Owner! 1 Page 3 Pasis Staged Park FF0 0 700 Owner! 1 Page 3 Pasis Staged FAR FF0 0 700 Owner! 1 Page 3 Pasis Staged FAR Mode 0 700 Owner! 1 Page 3 Pasis Staged FAR Mode 0 700 Owner! 1 Page 3 Pasis Staged FAR Mode 0 700 Owner! 2 Page 3 Pasis Staged FAR Mode 0 700 Owner! 2 Page 3 Pasis Staged FAR Mode 0 700 Owner! 2 Page 3 Pasis Staged FAR Mode 0 700 Owner! 2 Page 3 Pasis Staged FAR Mode 0 700 Owner! 2 Page 3 Pasis Staged FAR Mode 0 700 Owner! 2 Page 1 Pasis Staged FAR Mode 0 700 Owner! 2 Page 1 P		

Figure 105. Get Statistics of Configuration 2: Window Size

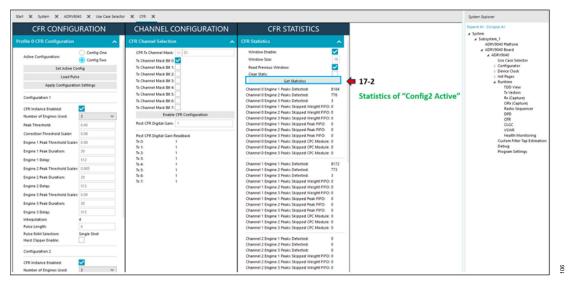


Figure 106. Get Statistics of Configuration 2

CLGC (CLOSED LOOP GAIN CONTROL)

Hardware Prerequisites

To evaluate CLGC, ensure that a gain line up is connected to the transceiver as shown in Figure 72, and ensure that the transmitter path is connected back to the feedback/observation receiver channel as per the transceiver configuration. Tune the power levels to ensure that the observation receiver is not saturating.

Ensure that there is a sufficient headroom for the transmitter attenuation to adjust it as part of the CLGC tracking. Note that DPD is a prerequisite for the CLGC to run. The summary of the minimum sequence to enable CLGC is as follows:

- 1. Program the desired profile, then transmit the carriers.
- 2. Setup transmitter to observation receiver mapping.
- 3. Load the DPD model.
- 4. Reset DPD.
- 5. Reset CLGC tracking.

- 6. Set up DPD tracking configuration.
- 7. Set up DPD capture configuration.
- 8. Set up CLGC capture configuration.
- **9.** Set up CLGC tracking configuration.
- **10.** Enable DPD tracking.
- 11. Run CLGC.

It is assumed that the user has already configured DPD (not enabled) following the steps mentioned in the DPD section. Note that DPD must be disabled to proceed with the CLGC configuration. The additional steps to configure/enable CLGC are as follows:

1. Select the CLGC option from Runtime under System Explorer.

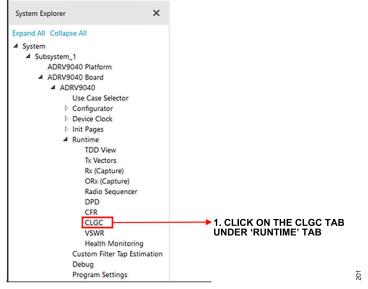
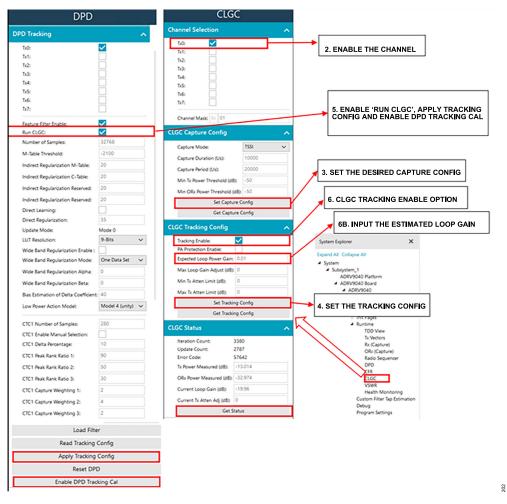
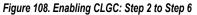


Figure 107. CLGC Tab Under Runtime

- 2. Enable the channel from Channel Selection as shown in Figure 108.
- 3. Set the desired **Capture Config**. There are two modes for capturing the signal. One is transmitter signal strength indicator (TSSI) and the other is peak detect mode.
- 4. Set the desired CLGC Tracking Config, which consists of Min Tx Atten Limit (dB) and Max Tx Atten Limit (dB) expected loop gain (if known already) that is to be tracked by the CLGC calibration.
- 5. In the DPD tab, ensure that DPD is configured and click the box beside Run CLGC, then click Apply Tracking Config and Enable DPD Tracking Cal.
- 6. Set the Tracking Enable option as follows:
 - a. As shown in Figure 109, to estimate the current open loop gain, unselect the box next to Tracking Enable.
 - b. Enter the estimated loop gain in Current Loop Gain (dB) under CLGC Tracking Config.
 - c. Select the box next to Tracking Enable. The same loop gain is maintained by the CLGC calculation by adjusting the Tx attenuation. To track the loop gain, select the box next to Tracking Enable.
- 7. From the CLGC status, the user can observe that the expected loop gain is maintained, and it also shows the current Tx attenuation. If the CLGC is running, CLGC iteration count and update count must be incrementing.





RUNTIME

6A. UNCHECK "TRAC ESTIMATE THE LOOP			6C. CHECK 'TRACKING FRACK THE LOOP GAIN					
CLGC Tracking Config	^	c	LGC Tracking Config	^				
Tracking Enable:			Tracking Enable:	\checkmark				
PA Protection Enable:			PA Protection Enable:					
Expected Loop Power Gain:	0.010		Expected Loop Power Gain:	0.010				
Max Loop Gain Adjust (dB)	: 6		Max Loop Gain Adjust (dB)	6				
Min Tx Atten Limit (dB):	0		Min Tx Atten Limit (dB):	0				
Max Tx Atten Limit (dB):	6		Max Tx Atten Limit (dB):	6				
Set Trackin	g Config		Set Tracking Config					
Get Trackin	g Config		Get Trackin	g Config				
CLGC Status	^	c	LGC Status	~				
Iteration Count:	52		Iteration Count:	150				
Update Count:	0		Update Count:	18				
Error Code:	0		Error Code:	0				
Tx Power Measured (dB):	-13.014		Tx Power Measured (dB):	-13.014				
ORx Power Measured (dB):	-33.233		ORx Power Measured (dB):	-32.972				
Current Loop Gain (dB):	-20.219		Current Loop Gain (dB):	-19.957				
Current Tx Atten Adj (dB)	0		Current Tx Atten Adj (dB):	-13.713				
Get St	atus		Ge St	atus				
ESTIMATED LOOP	GAIN		THE LOOP GAIN WIL OVER THE TIME	L BE TRACKED				



VOLTAGE STANDING WAVE RATIO (VSWR)

HARDWARE PREREQUISITES

To evaluate VSWR, the transmitter and observation receiver must be connected via an RF switch so that the user can switch between forward and reverse paths. Figure 110 shows the setup for a VSWR evaluation in a lab without custom hardware. While designing custom hardware, forward and reverse couplers must be used as mentioned in the system development user guide.

HARDWARE SETUP

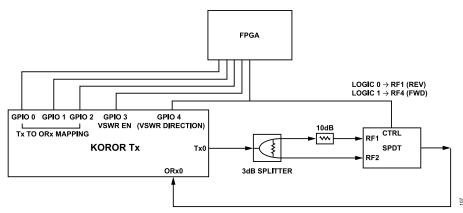


Figure 110. VSWR Measurement Setup

Figure 110 shows (eight pin modes showing only ORx0 path) how the mapping and the direction are set by using the assigned GPIO pins, and are driven by the FPGA. The same GPIO pins, which are fed to Koror transmitter and the same GPIO pins, are fed to the external switch as well.

The testing procedure is as follows:

1. VSWR is available under Runtime as shown in Figure 111.

art 🗙 System 🗙 ADRV9040 🗶 Us	e Case Selector 🗙 Stream Set	tings 🗙 CLGC 🛪	VSHR X			System bajoner X
	VSWR CONFI	G			VSWR OPERATIONS FOR SELECTED TX C	HANN Control All College All
SWR Config				^	VSWR Operations for selected Tx channels	 Subsystem_1 ADR/VIO40 Partform
Return Loss Qualitying Threshold (md3) Accumulation Revelons, Reverse Joth Gain (md3) VSHR minor Alarm Threshold (md3)	Tx 0 Tx 1 Tx 2 20000 (0) 20000 (0) 20000 (0) 40000 (0) 40000 (0) 40000 (0) 0 0 0 14000 (0) 14000 (0) 14000 (0)		Tx 3 Tx 4 20000 20000 20000 40000 40000 0 0 0 14000	40000	To Channel Marik: 0 0 160 161 162 163 164 0 Get Config Upload Physics Odd trian a file Enable VSIRR Reset VSIRR	16 ADRYDOE Daved ADRYDOE Daved ADRYDOE Daved Un Case Sentern Confugurator Denvar Clock Init Ages To Init Biret Stream Settings Point Stream Settings Point Stream Settings Point Stream Settings Point Stream Settings Point MCS Init Stream Settings <li< th=""></li<>
VSWR Hinor Alarm Rer Window	30 30 3	5 5 5	50 S0	3	VSWR Errors Is 0 petrols to see	
VSWR Hinor Alarm BerThresholdCount VSWR ragor Alarm Threshold (mdl) VSWR Rajor Alarm BerWindow VSWR Rajor Alarm BerThresholdCount	40 40 40 10000 10000 10000 50 50 50 40 40 40		40 40 120000 120000 50 50 40 40	12000	the profession proj The profession profession The 2 profession profession The 4 profession profession The 4 profession profession The 6 profession The	1. VSWR
	Get Config Set Config				Rafresh errors for all channels from device	VSWR Report Montoning Cuttorn Filter Tag Estimation Debug Program Settings
SWR Direction				^		Program Settings
Oilud Direction Revense Oilut Direction Revense				*		
	Apply Directions					
	Cycle Direction and Ap Cycle Direction and Apply + 1					

Figure 111. VSWR

- 2. Enable the Tx and ORx channels with 0 dB attenuation. Ensure that Tx to ORx mapping is configured correctly as per the physical connections.
- Enter the VSWR Config parameters like return loss qualifying threshold, accumulation iterations, and major and minor alarm thresholds as per testing, and then select Set Config as shown in Figure 112. The VSWR Config provides test options by programming the thresholds. Maximum and minimum ranges for all the VSWR Config parameters are defined in the system development user guide (SDUG).

VOLTAGE STANDING WAVE RATIO (VSWR)

	VS	WR C	ONFIC	6				VSWR CONFIG						
SWR Config A								VSWR Operations for selected Tx channels		✓ System ✓ Subsystem,1 ADRV9040 Pattorm				
	Tx 0	Te 1	74.2	Tx3	Tx 4	Tx 3	Tx 6	Tx 7	Is Channel Mask: 0	В м м м м м м	ADITV9040 Board ADITV9040 Use Case Selector			
Return Loss Qualifying Threshold [mdB]	20000	20000	20000	20000	20000	20000	20000	20000		Get Config	> Configurator			
Accumulation Iterations	40000	40000	40000	40000	40000	40000	40000	40000		Set Config	 Device Clock Init Pages 			
										Upload Playback Data from a file	Taint			
Reverse Path Gain (mdB)	0	0	•	•	0	0	0	0		Enable VSWR	Ra Ind			
VSWR Hinor Alacm Threshold (mdB)	14000	14000	14000	14000	14000	14000	14000	14000		Reset VSINR	Stream Settings Post MCS init			
VSWR Hinor Alarm Rer Window	3	3	5	\$	5	5	3	5	VSWR Errors		Calibration AGC Eurotime			
VSWR Hinor Alarm Ber ThresholdCount	4	4	4	4	4	4	4	4 💽	Tx 0: (refresh to see) Tx 1: (refresh to see)		TDD View To Vectors			
VSWR Hajor Alarm Threshold (md8)	1,2000	12000	12000	12000	1,2000	12000	1,2000	12000	To 2: petresh to seej To 3: petresh to seej		Rx (Capture) ORx (Capture)			
VSWR Hajor Alarm BerWindow	3	3	1	5	5	3	3	5	Tx 4: petresh to seej Tx 5: petresh to seej		Radio Sequencer CPD			
	40	4	4	40	40	4	40	4	To 6: petresh to see) To 7: petresh to see)		CFR CLSC			
3. VSWR CONFIG		640	antig							Refresh errors for all channels from device	VSWR			
3. VSWK CONFIC	i i n		antig	-							Health Monitoring Custom Filter Tap Estimation			
				_				-			Dethug			
SWR Direction								^			Program Settings			
Oilud Direction Revene								*						
ORx1 Direction Reverse								~						
		Apply D	vections											
	0	yde Directi	on and App	w.										
	Curle Da	-	Apply - rei	of Challen					1					

Figure 112. VSWR Configuration

- 4. Select the Tx channel mask for VSWR feature testing as shown in Figure 113.
- 5. Load test RAM data waveform. Test RAM data can be generated from ACE GUI or can be loaded as a file. Select Upload Playback data from a file to upload a pregenerated test RAM waveform. Note that these waveforms must be generated for different use cases. Contact Analog Devices for a waveform file until the generate option is available in the GUI.
- 6. Select Enable VSWR as shown in Figure 113.
- 7. Set VSWR direction. Depending on the VSWR mode (PIN mode), the direction bits are controlled from FPGA and are given to the external switches. During API mode, the user must control the RF switch in VSWR forward and reverse directions. The switch needs to be toggled within four seconds for one update to take place. Under the VSWR Direction tab, the user can reverse direction of the switch by clicking Cycle Direction and Apply.

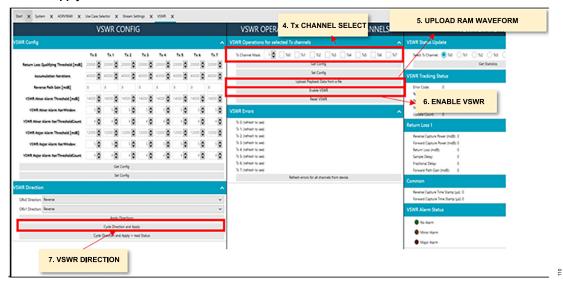


Figure 113. VSWR Direction

8. Set the VSWR tracking status and statistics. Once the forward and reverse switching happens, the user can read the VSWR tracking status and statistics in the VSWR Statistics window as shown in Figure 114 for the second and third iterations. The iteration and update count increments, and the percent complete shows 100%. From statistics, the user can report the reverse, forward powers in mdB, return loss, sample delay, fractional delay, forward path gain, and reverse the time stamp and forward time stamp as well.

VOLTAGE STANDING WAVE RATIO (VSWR)

8. VSWR STATISTICS VSWR STATISTICS
VSWR Status Update
Select Tx Channet: Tx1 Tx2 Tx3 Tx4 Tx5 Tx6 Tx7
Get Statistics
VSWR Tracking Status
Error Code: 0 % Complete: 0 Performance Metric: 0 Retailion Count: 0 Update Count: 0
Return Loss 1
Reverse Capture Power (mdB): 0 Forward Capture Power (mdB): 0 Return Loss (mdB): 0 Sample Delay: 0 Fractional Delay: 0 Forward Path Gain (mdB): 0
Common
Reverse Capture Time Stamp (µs): 0 Forward Capture Time Stamp (µs): 0
VSWR Alarm Status
 No Alarm Minor Alarm Major Alarm
 magvi svarini

Figure 114. VSWR Statistics

SOFTWARE RESOURCE FILES

The resource files required for programming the ADRV904x device are listed in Table 9.

These include the **DeviceProfileTest.bin** and **initdata.c** files, which must be generated by the user for the desired ADRV904x configuration and initialization settings. These files can be generated using ACE with attached hardware. The ADRV904x can be programmed using ACE for generating these resource files.

Note that the ACE needs a hardware connection to the ADS10-V1EBZ/CE board system for generating the resource files during programming.

Resource File	Purpose
ADRV9040_FW.bin	Precompiled firmware binary for the embedded dual core ARM processors in the ADRV904x.
ADRV9040_DFE_CALS_FW.bin	Precompiled firmware binary for the embedded A55 DFE processor in the ADRV904x.
DeviceProfileTest.bin	Profile binary consisting of filter coefficients, clock rates, and signal processing resources to be enabled/disabled for a particular use case.
initdata.c	Initialization data structures for setting up the ADRV904x subsystems. It can be generated with either C89 or C99 compatibility to integrate with the user application code base. The difference between a C89- and C99-compatible data structure is illustrated in Table 10.
RxGainTable.csv	Front end gain lookup table for the ADRV904x receiver.
RxGainTable_GainCompensated.csv	Receiver gain table to use when digital gain compensation is enabled.
stream_image.bin	Binary file for the stream co processor in the ADRV904x, which is mainly used for setting up and controlling the Tx/Rx datapaths when certain events occur, such as Tx/Rx enable.

Table 10. Member Representations Compared Between C99 and C89 Data Structures

C99 Data Structure Example	C89 Data Structure Example
adi_adrv904x_Version_t initStructApiVersion = {2, 10, 0, 6};adi_adrv904x_CpuFwVersion_t initStructArmVersion = { {2, 10, 0, 6} , ADI_ADRV904 X_CPU_FW_BUILD_RELEASE};adi_adrv904x_Version_t initStructStreamVersion = {2, 10, 0, 6};adi_adrv904x_Init_t deviceInitStruct ={.spiOptionsInit ={.allowSpiStreaming = 1,.allowAhbAutoIncrement = 1,.allowAhbSpiFifoMode = 1,}	adi_adrv904x_Version_t initStructApiVersion = {2, 10, 0, 6};adi_adrv904x_CpuFwVersion_t initStructArmVersion = { {2, 10, 0, 6}, ADI_ADRV904X_CPU_FW_BUILD_RELEASE};adi_adrv904x_Version_t initStructStreamVersion = {2, 10, 0, 6};adi_adrv904x_Init_t deviceInitStruct ={ { // spiOptionsInit 1, // allowSpiStreaming 1, // allowAhbAutoIncrement 1, // allowAhbSpiFifoMode},

RESOURCE FILE GENERATION USING ACE

ACE can be used to generate the resource files needed for programming the ADRV904x by connecting and programming the evaluation hardware using the ADRV904x plugin. ACE outputs the resource files to the resource folder path C:\Users\%USERNAME%\AppData\Lo-cal\Analog Devices\ACE\PluginFiles\Board.ADRV9040\Local\resources as shown in Figure 115.

Note that ACE clears the contents of the resource folder with every program before writing new resource files. Any resource files required by the user should be copied to a different location before attempting to program the ADRV904x again.

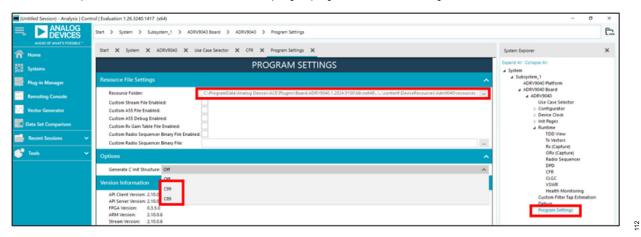


Figure 115. Resource File Generation Using ACE, C89 or C99 Compatibility Can be Selected for Initdata.c

IRONPYTHON SCRIPTING

ACE enables the user to interface with the ADRV904x evaluation system using a scripting language such as IronPython. To run scripts from within ACE, the user must refer to the following steps:

1. Provide a path to the host PC IronPython installation under ACE Settings > Scripting > Path as shown in Figure 116. This step only needs to be completed once after installing ACE.

Capture	Script Engines:						•
Ethernet Boards		 					0
Graphing	Path	ID	Languag	e	Extensions	Enabled	
IPC Server	\IronPython 2.7\ipy.exe	 IronPython	Python	~	*.py, *.ipy		Â
Plug-ins							-
Preferences		 Python27	Python	~	*.py	\checkmark	Î
Scripting		 Python3	Python	~	*.py		龠
Serial Ports							-
Updater Settings							

Figure 116. Providing IronPython Path to ACE for Enabling Script Execution

2. Open a script from Tools > Platform API Logger > Open Script as shown in Figure 117. A template script for interfacing with the ADRV904x device is included with the plugin and can be opened from Create New. Scripts open as new tabs in ACE.

	Start >	Ē
AHEAD OF WHAT'S POSSIBLE "		
秴 Home	Start X System X ADRV9040 X New* X Platform API Logger	×
Q Systems	Piatorm: adrogen6_ads10	
Plug-in Manager	Play Play (External) Save Save as. Clear All IronPython Start Logging	
Remoting Console	2 Koror IronPython Programming Template Version 0.1 Export Code 3 Generated with:	
Vector Generator	3 Generated with: 4 ACE GUI Version: 1.21.3008.1356 5 ACE Plug-in Version: 1.2021.26100	_
📑 Recent Sessions 🔹 🗸	6 API Client Version: 0.1.0.2 7 API Server Version: 0.1.0.2	- 1
💕 Tools 🔹 🔨	8 FPGA Version: 0.2.1.0 9 ARM Version: 0.1.0.2	
Events	10 StreamVersion: 0.1.0.2	
Register Debugger	12 Note: ACE does not need to be disconnected from	
FPGA Programmer	ADRV9040 command server before running this script anymore.	
Firmware Programmer	13 ***	
Macro Tools	14 15 v	
System Explorer 🗸 🗸	Loading client DLLs from C:\ProgramData\Analog Devices\ACE\Plugins \Board.ADRV9040.1.2021.26100\lib	
EEPROM Recovery Tool	Attempting to connect to 192.168.1.10:5000	
SDP-K1 Recovery Tool	spiWriteByte 0x000A 0x55 spiReadByte 0x000A 0x55	
Platform API Logger 🛛 🗸	Hello World! System Explorer Platform API Logger	
🕜 Help 🏻 🙀 Settings	New - Scripting.RunScript, Finished at 9:41:44	

Figure 117. Using Platform API Logger to Open and Execute IronPython Scripts from Within ACE

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APPENDIX

UNINSTALLING OLDER ACE

Uninstalling ACE is not necessary to update the ACE core to a newer release. However, if errors are seen during the installation of a new ACE core version, any previous versions of ACE core can be removed from the host PC as outlined below. Note that administrator privileges are required for these steps as follows:

- 1. Close any running instances of ACE. Task manager can be used to confirm that no background ACE processes are running.
- 2. Navigate to Windows Start > Add or Remove Programs > ACE > Uninstall.
- Select ScrubUninstall in the ACE uninstall wizard as shown in Figure 118. This is necessary to remove any older ACE plugin versions, but it also removes any custom files, settings, and data exports previously stored by the user. Note that this step must only be performed as a fallback option if ACE installation appears corrupted, and it is necessary to start from a clean slate.

Choose Components Choose which features of i	8	
Check the components you uninstall. Click Uninstall to s		the components you don't want to
Select components to uninstall:	 ✓ Uninstall ✓ ScrubUninstall 	Description Position your mouse over a component to see its description.
Space required: 0.0 KB		
ullsoft Install System v3.02 -		

Figure 118. ScrubUninstall Used to Troubleshoot Erroneous ACE Installation

- 4. When prompted, select No to additionally uninstall system demonstration platform (SDP) drivers, LRF drivers, and ADIThon from previous ACE installation.
- 5. Attempt to reinstall ACE by running the included ACE installer with default components selections as shown in Figure 119.

ACE Setup		-		×
Choose Components				
Choose which features of ACE	you want to install.			
Check the components you wa install. Click Install to start the	nt to install and uncheck the comp installation.	onents you dor	n't want t	0
Select components to install:	PreRequisites Image: Comparison of the second se	Description Position you over a comp see its descr	onent to	
Space required: 137.7 MB	< >>			
Nullsoft Install System v3.05				
	< Back	Install	Can	cel

Figure 119. Component Selections Used when Attempting a New Installation of ACE

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More information about the ACE uninstallation process is available on the ACE wiki https://wiki.analog.com/resources/tools-software/ace/ installscrub.

UNINSTALLING OLDER PLUGIN USING PLUGIN MANAGER

Any previously installed ACE plugin, such as an ADRV903X plugin, can be uninstalled using ACE plugin manager as shown in Figure 120. The steps are as follows:

- 1. Open the plugin manager from the ACE left panel.
- 2. Select the plugin from the list of installed packages. Find the plugin to be uninstalled via the search bar.
- 3. Click Uninstall Selected. Restarting ACE is needed to complete this step.

APPENDIX

Installed Packages	Board.ADRV9030	Installed	Adrv903		Clear
All	ADRV9030 Evaluation Board Plug-in description.		Name:	Board.ADRV9030	
Available Packages			Version:	1.2021.25500 👷	
Available Packages			Description:	ADRV9030 Evaluation Boar	d Plug-in
Available Updates				description.	
			Published:		
			Release Notes:		
			Dependencies		
			Status:	Plug-in is installed and has available.	no updates
				available.	
Show obsolete plug-ins	· · · · · · · · · · · · · · · · · · ·				

Figure 120. Using ACE Plugin Manager to Uninstall Older Version of the ADR903x Plugin (Board ADRV9010)

INSTALLING THE ADRV904X PLUGIN USING THE PLUGIN MANAGER

The user can install the ADRV904x plugin by providing the plugin **.acezip** file path to ACE under **Settings** as shown in Figure 121. The steps are as follows:

- 1. Open ACE Settings and select the Plug-ins tab.
- 2. Add a new plugin by clicking on the + button under Zipped Plugin Sources as shown in Figure 121.

2. SELECT PLUG-INS Graphing IPC Server Plug-ins	specify additional sources, system, network shares, ar	nd get updates from a master allowing ACE to get plug-in: nd/or your company's NuGet //www.myget.org/F/adiaceplu	s from your lo server.	cal file	×	
Preferences Scripting	Custom Plug-in Sources:				3. ADD PLUG-INS	
Serial Ports	Name	Source		Enablea		
Updater Settings	Zipped Plug-in Sources: Name Source ADRV904X \gui\Bo	oard.ADRV9040.1.2021.10401.a	_	abled		
5. PROVIDE	A NAME lates: Manu	ally check for updates	4.	BROWSE		
			ОК	Ca	incel	
Report Issue Request Feature Application Usage Logging Help Kettings	1. OPEN ACE SETTINGS					

Figure 121. Adding ADRV904x Plugin as a Zipped Source in ACE Settings, Once Added, Run ACE Plugin Manager to Install the Plugin

- 3. Click on ... to navigate to the **Board ADRV9040.acezip** file location to populate the source field.
- 4. Provide a name for this plugin source. The name choice is arbitrary and can be chosen by the user.
- 5. Launch plugin manager, then select and install Board.ADRV9040 from the list of Available Packages as shown in Figure 122.

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APPENDIX

	ADRV9040 Evaluation Board Plug-In	description.	Available	Name:	Cear Board ADRV9040
Available Packages				Version:	1.2021.10401
All Master Repository				Description:	ADRV9040 Evaluation Board Plug-In description.
ADV904X	NAME ENTERED ABOVE			Published:	06/28/2021
Available Updates	NAME ENTERED ABOVE		Release Notes	1	
				Dependencies	1
				Status:	Plug-in is available for download.
Show obsolete plug-ins				JUNUE	

Figure 122. ADRV904x Plugin Installed Using ACE Plugin Manager

DISCONNECTING ACE FROM ADS10-V1EBZ COMMAND SERVER

The user may disconnect ACE from the ADS10-V1EBZ command server to enable other applications to communicate with the evaluation hardware. ACE can be disconnected from the ADS10-V1EBZ as shown in Figure 123. The steps to disconnect ACE from the ADS10-V1EBZ command server are as follows:

- 1. Navigate to ACE System tab.
- 2. Click on the USB icon on the ADRV904x Platform Controller to open the Acquire/Release Hardware dialog box.
- 3. Select Operate without hardware. This selection updates the buttons on the dialog box to show Release.
- 4. Click **Release**. This step disconnects ACE from the evaluation hardware. The status of ACE connection to the hardware can be checked from either of the following:
 - ▶ System > ADRV904x Platform Controller > USB icon. This icon turns from green to gray once disconnected.
 - ▶ ADRV904x Board connection indicator. The green light turns red once the board is disconnected.

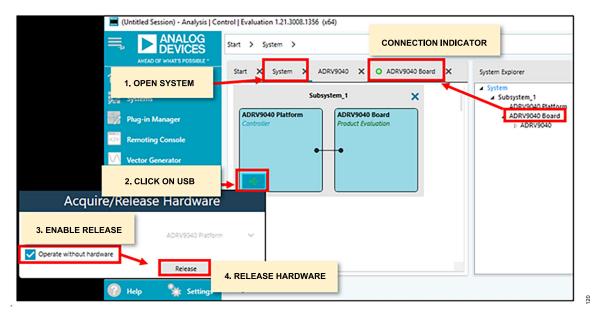


Figure 123. Steps for Disconnecting ACE from the Evaluation Hardware

RECONNECTING ACE TO THE ADS10-V1EBZ COMMAND SERVER

The process for reconnecting ACE to the evaluation hardware is similar to the disconnecting procedure as shown in Figure 124. The steps to reconnect ACE to the ADS10-V1EBZ command server are as follows:

- 1. Navigate to ACE System tab.
- 2. Click on the USB icon on the ADRV904x Platform Controller to open the Acquire/Release Hardware dialog box.
- 3. Deselect Operate without hardware. This updates the buttons on the dialog box to show Acquire.
- 4. Click Acquire. Reestablishing the connection updates the following:
 - System > ADRV904x Platform Controller > USB. The icon turns green.

APPENDIX

► ADRV904x Board tab. The connection indicator turns green.

🧮 (Untitled Session) - Analysis Co	ontrol Evaluation 1.21.3008.1356 (x64)		
	Start > System >	CONNECTION INDICATO	R
1. OPEN SYSTEM	Start X System X ADRV9040 X		iystem Explorer
😥 Systems	Subsystem_1	×	▲ Subsystem_1 ADRV9040 Platform
Plug-in Manager	ADRV9040 Platform ADRV904 Controller Product Ev		ADRV9040 Postorn ADRV9040 Board ADRV9040
Remoting Console			
Vector Generator	•••		
2. CLICK ON USB	<u>→ 🔫</u>		
Acquire/Release Hardware			
3. UNCHECK THIS BOX	n v		
Operate without hardware	1		
C Help Settings	4. ACQUIRE HARDWARE	at 11:12:26	

Figure 124. Steps for Reconnecting ACE to the Evaluation Hardware



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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