

Evaluating the ADN4622/ADN4624 5.7 kV rms/1.5 kV rms, Quad-Channel LVDS 2.5 Gigabit Isolators

FEATURES

- Isolated ground planes (logic side and bus side)
- High-speed layout supports 2.5 Gigabit operation and precision jitter measurements (<1 ps rms for random jitter)
- ▶ Convenient connections through SMA terminals
 - ▶ 1.8 V power on Side 1 (V_{DD1}) and Side 2 (V_{DD2})
 - ADN4622: 3.3 V power for LVDS receivers on Side 1 (V_{IO1}) and Side 2 (V_{IO2})
 - ▶ Ground on Side 1 (GND₁) and ground on Side 2 (GND₂)
 - LVDS input signals: D_{IN1+}, D_{IN1-}, D_{IN2+}, D_{IN2-}, D_{IN3+}, D_{IN3-}, D_{IN4+}, D_{IN4-}
 - ► LVDS output signals: D_{OUT1+}, D_{OUT1-}, D_{OUT2+}, D_{OUT2+}, D_{OUT2+}, D_{OUT3+}, D_{OUT3+}, D_{OUT3+}, D_{OUT4+}, D_{OUT4-}
- ► Jumper-selectable refresh mode
- ▶ Termination resistors on all LVDS receivers

EVALUATION KIT CONTENTS

▶ EVAL-ADN4622EB1Z or EVAL-ADN4624EB1Z

DOCUMENTS NEEDED

ADN4622/ADN4624 data sheet

EQUIPMENT NEEDED

- Signal generator
- Oscilloscope
- Power supply

GENERAL DESCRIPTION

The EVAL-ADN4622EB1Z and EVAL-ADN4624EB1Z allow quick and simple evaluation of the ADN4622 and ADN4624 low-voltage differential signaling (LVDS) isolators respectively, without the need for external components. The ADN4622/ADN4624 employ Analog Devices, Inc., *i*Coupler[®] technology to combine a 4-channel isolator with LVDS receivers and drivers into a single, 28-lead wide-body SOIC package with finer pitch. The devices are capable of running at data rates of up to 2.5 Gbps with low jitter.

The EVAL-ADN4622EB1Z and EVAL-ADN4624EB1Z have a separate ground and power plane for each side of the isolator. This separation enables the evaluation of the ADN4622/ADN4624 with galvanic isolation between both sides of the device. 1.8 V power supplies are required on each side of the ADN4622/ADN4624 device, and the ADN4622 additionally requires a 3.3 V power supply on each side.

For full details on the ADN4622/ADN4624, see the ADN4622/ ADN4624 data sheet, which must be consulted in conjunction with this user guide when using the EVAL-ADN4622EB1Z or EVAL-ADN4624EB1Z.

EVALUATION BOARD PHOTOGRAPHS



Figure 1. EVAL-ADN4622EB1Z Photograph



Figure 2. EVAL-ADN4624EB1Z Photograph

TABLE OF CONTENTS

Features 1	
Evaluation Kit Contents1	
Documents Needed1	
Equipment Needed1	
General Description1	
Evaluation Board Photographs1	

Evaluation Board Configuration	3
Setting Up the Evaluation Board	
Evaluation Board Schematics and Artwork	6
Ordering Information	12
Bill of Materials	12

REVISION HISTORY

10/2022-Rev. 0 to Rev. A

dded ADN4622 and EVAL-ADN4622EB1Z Throughout and Figure 1; Renumbered Sequentially
hanges to General Description Section and Figure 2 Caption1
hanges to Setting up the Evaluation Board Section
dded Figure 43
hanges to Table 1 Title, Table 3 Title, and Table 44
dded Table 24
dded Figure 6 and Figure 76
dded Figure 8 and Figure 97
dded Figure 10 and Figure 11
dded Table 512

4/2021—Revision 0: Initial Version

EVALUATION BOARD CONFIGURATION

SETTING UP THE EVALUATION BOARD

To power Side 1 of the EVAL-ADN4622EB1Z, connect a 1.8 V power supply to the J18 subminiature Version A (SMA) connector and a 3.3 V power supply to the J17 SMA connector. To power Side 2, connect a 1.8 V power supply to the J19 SMA connector and a 3.3 V power supply to the J20 SMA connector (see Table 2). Similarly for the EVAL-ADN4624EB1Z, connect a 1.8 V power supply to the J17, J18, or J21 SMA connector for Side 1 and the J19, J20, or J22 SMA connector for Side 2 (see Table 3). At 1.25 GHz with a load resistance of 100 Ω , the maximum operating current from each 1.8 V power supply is 140 mA (175 mA for the EVAL-ADN4624EB1Z Side 1) and 14 mA on each side for the 3.3 V power supplies.

 V_{DD1} (Pin 1 and Pin 14 on the ADN4622/ADN4624) and V_{IO1} (Pin 3 on the ADN4622) are bypassed to GND₁ using 0.1 μ F capacitors. V_{DD2} (Pin 15 and Pin 28 on the ADN4622/ADN4624) and V_{IO2} (Pin 17 on the ADN4622) are bypassed to GND₂ by also using 0.1 μ F capacitors.

The ADN4622/ADN4624 integrate a refresh function to correct, if necessary, the output state in the absence of any input transitions. This function ensures the correct output state at power-up, for example. To reduce internal switching noise and provide even lower jitter, the refresh function can be disabled. This functionality is accessed on the EVAL-ADN4622EB1Z and EVAL-ADN4624EB1Z by changing the position of the P1 and P2 jumpers for Side 1 and Side 2, respectively, as described in Table 1.

Figure 4 and Figure 5 show an example operation of the EVAL-ADN4622EB1Z or EVAL-ADN4624EB1Z, respectively. The SMA connectors reveal all LVDS inputs and outputs for the EVAL-ADN4622EB1Z and EVAL-ADN4624EB1Z (see Table 4).

To evaluate Channel 1 on the EVAL-ADN4622EB1Z and EVAL-ADN4624EB1Z, connect a signal generator to the board using the J1 connector and J2 connector and set up a 1.25 GHz square wave clock with an amplitude of 200 mV (400 mV p-p) and an offset of 1.2 V. Connect the oscilloscope to the J9 connector and J10 connector to perform timing measurements, including propagation delay, skew, and jitter. A differential probe with an SMA connector is recommended, terminating each output trace to 50 Ω connected to 1.24 V (providing 100 Ω differential termination and matching the ADN4622/ADN4624 driver offset voltage (V_{OS})). Refer to Table 4 for the connectors to use to evaluate Channel 2, Channel 3, and Channel 4 similarly on the EVAL-ADN4622EB1Z and EVAL-ADN4624EB1Z.

Figure 3 shows a plot of the oscilloscope connected by the J9 connector and J10 connector. The oscilloscope shows the differential voltage, that is, $D_{OUT1+} - D_{OUT1-}$.



Figure 3. D_{OUT1-} and D_{OUT1+} with a 1.25 GHz Clock, Differential



Figure 4. Basic LVDS Isolator Evaluation Board Operation for the EVAL-ADN4622EB1Z

EVALUATION BOARD CONFIGURATION



Figure 5. Basic LVDS Isolator Evaluation Board Operation for the EVAL-ADN4624EB1Z

Table 1. Jumper Configuration for the EVAL-ADN4622EB1Z and EVAL-ADN4624EB1Z

Jumper	Position	Description
P1	1-2	Side 1 refresh disabled (quiet operation): REFRESH ₁ shorted to V _{DD1} .
	2-3	Side 1 refresh enabled (normal operation): REFRESH1 shorted to GND1.
P2	1-2	Side 2 refresh disabled (quiet operation): REFRESH ₂ shorted to V _{DD2} .
	2-3	Side 2 refresh enabled (normal operation): REFRESH ₂ shorted to GND ₂ .

Table 2. Power Supply Connector Descriptions for the EVAL-ADN4622EB1Z

Connector	Description
Side 1	
J17	Power supply, Side 1 I/O, connect 3.3 V
J18	Power supply, Side 1, connect 1.8 V to one connector option
Side 2	
J19	Power supply, Side 2, connect 1.8 V to one connector option
J20	Power supply, Side 2 I/O, connect 3.3 V

Table 3. Power Supply Connector Descriptions for the EVAL-ADN4624EB1Z

Connector	Description
Side 1	
J17, J18, J21	Power supply, Side 1, connect 1.8 V to one connector option
Side 2	
J19, J20, J22	Power supply, Side 2, connect 1.8 V to one connector option

Table 4. Input and Output Connector Descriptions for the EVAL-ADN4622EB1Z and EVAL-ADN4624EB1Z

Connector			
EVAL-ADN4622EB1Z	EVAL-ADN4624EB1Z	Description	
J1	J1	D _{IN1+} , noninverted LVDS input for Channel 1	
J2	J2	D _{IN1-} , inverted LVDS input for Channel 1	
J3	J3	D _{IN2+} , noninverted LVDS input for Channel 2	
J4	J4	D _{IN2-} , inverted LVDS input for Channel 2	
J13	J5	D _{IN3+} , noninverted LVDS input for Channel 3	
J14	J6	D _{IN3-} , inverted LVDS input for Channel 3	
J15	J7	D _{IN4+} , noninverted LVDS input for Channel 4	

EVALUATION BOARD CONFIGURATION

Table 4. Input and Output Connector Descriptions for the EVAL-ADN4622EB1Z and EVAL-ADN4624EB1Z

Connector		
EVAL-ADN4622EB1Z	EVAL-ADN4624EB1Z	Description
J16	J8	D _{IN4} -, inverted LVDS input for Channel 4
J9	J9	D _{OUT1+} , noninverted LVDS output for Channel 1
J10	J10	D _{OUT1-} , inverted LVDS output for Channel 1
J11	J11	D _{OUT2+} , noninverted LVDS output for Channel 2
J12	J12	D _{OUT2-} , inverted LVDS output for Channel 2
J5	J13	D _{OUT3+} , noninverted LVDS output for Channel 3
J6	J14	D _{OUT3-} , inverted LVDS output for Channel 3
J7	J15	D _{OUT4+} , noninverted LVDS output for Channel 4
J8	J16	D _{OUT4-} , inverted LVDS output for Channel 4



Figure 6. EVAL-ADN4622EB1Z Schematic



Figure 7. EVAL-ADN4622EB1Z Silkscreen



Figure 9. EVAL-ADN4622EB1Z Inner Layer 2, Ground



Figure 10. EVAL-ADN4622EB1Z Inner Layer 3, Power



Figure 11. EVAL-ADN4622EB1Z Solder Side



Figure 12. EVAL-ADN4624EB1Z Schematic



Figure 13. EVAL-ADN4624EB1Z Silkscreen



Figure 15. EVAL-ADN4624EB1Z Inner Layer 2, Ground



Figure 16. EVAL-ADN4624EB1Z Inner Layer 3, Power



Figure 17. EVAL-ADN4624EB1Z Solder Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 5. EVAL-ADN4622EB1Z Bill of Materials

Quantity	Reference Designator	Description	Manufacturer	Part Number
6	C6, C7, C9, C11, C15, C18	Capacitors, 0.1 μF, 0402	Kemet	C0402C104K4RACTU
4	C1, C13, C16, C19	Capacitors, 0.1 µF, 0603	AVX	06035C104KAT2A
18	C2 to C5, C8, C10, C12, C14, C17, C21 to C28, C30	Capacitors, 0402	Not fitted	Not applicable
20	J1 to J20	Connectors, SMA, edge	Johnson - Cinch	142-0701-851
2	P1, P2	3-pin, header (and jumper)	Molex (and Sullins)	22-23-2031 (and QPC02SXGN-RC)
4	R0, R1, R10, R11	Resistors, 100 Ω, 0201	Panasonic	ERJ-1GNF1000C
8	TP2, TP3, TP4, TP5, TP6, TP8, TP9, TP11	Test points	Components Corporation	TP104-01-01
1	X1	5.7 kV rms/1.5 kV rms, quad-channel LVDS 2.5 gigabit isolator	Analog Devices	ADN4622BRNZ

Table 6. EVAL-ADN4624EB1Z Bill of Materials

Quantity	Reference Designator	Description	Manufacturer	Part Number
8	C2, C4, C6, C7, C9, C11, C14, C18	Capacitors, 0.1 µF, 0402	Kemet	C0402C104K4RACTU
4	C15, C16, C19, C20	Capacitors, 10 μF, 0603	Murata	GRM188R60J106ME47D
12	C5, C8, C10, C12, C21 to C28	Capacitors, 0402	Not fitted	Not applicable
20	J1 to J20	Connectors, SMA, edge	Johnson - Cinch	142-0701-851
2	J21, J22	Connectors, SMA (not fitted)	Pasternack Enterprises	PE4117 (not fitted)
2	P1, P2	3-pin, header (and jumper)	Molex (and Sullins)	22-23-2031 (and QPC02SXGN-RC)
4	R0, R1, R2, R3	Resistors, 100 Ω, 0201	Panasonic	ERJ-1GNF1000C
8	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8	Test points	Components Corporation	TP104-01-01
1	X1	5.7 kV rms/1.5 kV rms, quad-channel LVDS 2.5 gigabit isolator	Analog Devices	ADN4624BRNZ



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NONINFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS (\$100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.



©2021-2022 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners. One Analog Way, Wilmington, MA 01887-2356, U.S.A.