Evaluating the ADL5960 10 MHz to 20 GHz Integrated Vector Network Analyzer Front End

FEATURES

- Full featured evaluation board for the ADL5960
- Integrated bidirectional bridge measures forward and reverse coupled signal

EQUIPMENT NEEDED

- Power supply
- One or two RF signal generators
- Spectrum analyzer or oscilloscope
- DC2026C (Linduino One) board (included in the ADL5960-KIT-EVALZ kit)
- Experimental impedances such as open, short, and load

GENERAL DESCRIPTION

The ADL5960-EVALZ allows evaluation of the ADL5960 vector network analyzer (VNA) front-end IC.

The ADL5960 with integrated bridge derives inline incident and reflected power samples at up to 20 GHz, while maintaining low insertion loss, approximately 1 dB to 2 dB depending on frequency. Integrated mixers downconvert the incident and reflected samples to IF while preserving phase information. The serial peripheral interface (SPI) port provides access to programmable local oscillator (LO) and offset mixer versatility features, plus programmable IF gain and bandwidth.

For optimal performance, the printed circuit board (PCB) RF transmission lines are 50 Ω controlled impedance on Rogers RO3003 low loss substrate material.

For full details on the ADL5960, see the ADL5960 data sheet, which must be consulted in conjunction with this user guide when using the ADL5960-EVALZ.

ADL5960-EVALZ BOARD PHOTOGRAPH

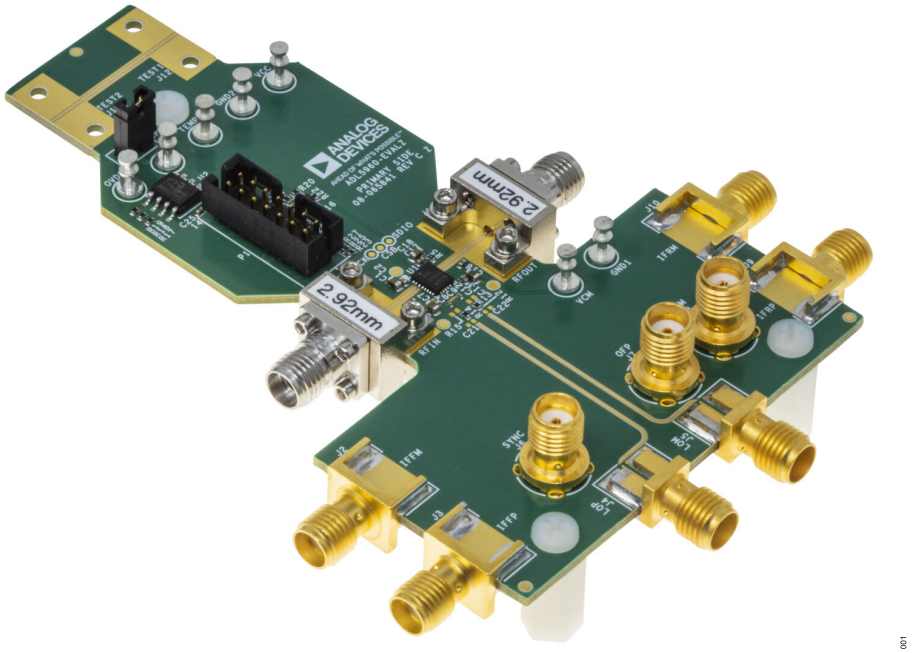

Figure 1. Evaluation Board Photograph

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REVISION HISTORY

7/2023—Revision 0: Initial Version

EVALUATION BOARD TEST SETUP

The ADL5960-EVALZ requires a 5 V power supply with a recommended minimum current rating of 500 mA.

An external 3.3 V for OVDD does not need to be supplied, because this is normally supplied by the DC2026C Linduino® One board.

The RFIN port requires an RF signal generator capable of operating at up to 20 GHz for full frequency range demonstration.

The RFOUT port can be connected to the spectrum analyzer or various impedance standards for demonstration, device calibration, or evaluating the insertion loss and directivity of the ADL5960 device.

The LO input port is differential via the LOP and LOM pins. The LO drive also functions well when simply driven single-ended, with the unused side terminated with 50 Ω surface-mount Type A (SMA) termination.

IF outputs are differential, via the IFFP and IFFM pins (forward channel) and the IFRP and IFRM pins (reverse channel), for forward and reverse paths, respectively. All IF outputs are AC-coupled, 50 Ω source impedance, and the outputs can be directly connected to a 50 Ω spectrum analyzer or oscilloscope for single-ended or differential measurement. Unused IF outputs can be either left open or terminated with 50 Ω.

A graphical user interface (GUI) program is provided by Analog Devices, Inc., for ADL5960 test and demonstration purposes. The program is freely available for download at www.analog.com/ADL5960 and runs in a Microsoft Windows environment. If not already installed, this program must be downloaded and installed before proceeding further. Installing the GUI program also installs the USB drivers necessary to support the DC2026C Linduino One hardware. Be sure to install the GUI program before connecting the USB of the DC2026C Linduino One board to the PC.

A DC2026C Linduino One is shipped with the ADL5960-KIT-EVALZ kit. The DC2026C Linduino One board has custom firmware preinstalled to support the GUI. The custom firmware installation is signified by an ADL5960 label adhered to the DC2026C Linduino One board, on the outer shell of the USB receptacle.

A 14-conductor ribbon cable provides SPI and regulated 3.3 V connections between the interface board and the ADL5960-EVALZ board. The 3.3 V from the DC2026C Linduino One powers the ADL5960 OVDD pin, thus powering the ADL5960 on-chip digital interface. Without this power source, the ADL5960 is not enabled and is not functional.

An RF test trace is provided near the top edge of the ADL5960-EVALZ board. This transmission line is provided for de-embedding purposes, having the same cross sectional dimensions as the RFIN and RFOUT printed transmission lines. The RF test trace connectors are not normally supplied but can be taken from the RFIN and RFOUT locations for test purposes, or purchased separately (see Table 2 for component information).

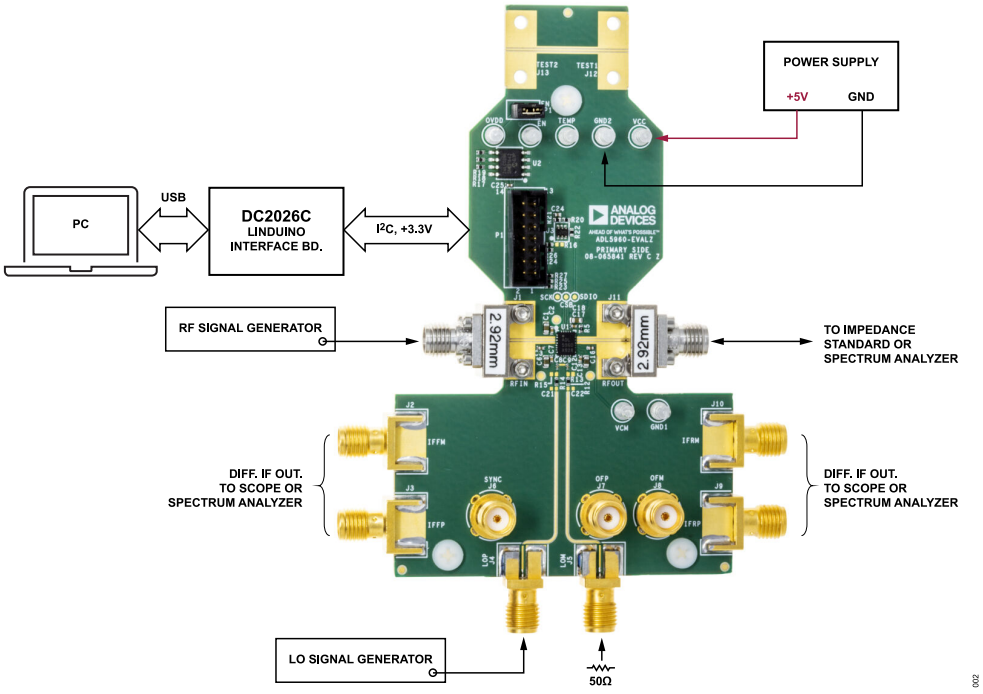

Figure 2. ADL5960-EVALZ Basic Test Setup

TEST PROCEDURE

Test setup begins with basic preparation and a power-up sequence that establishes SPI communications. See the Preparations for Testing section and Recommended Power Sequencing section for details. After setup, see the RF Functional Demonstration section for a functional demonstration procedure.

PREPARATIONS FOR TESTING

To prepare the ADL5960-EVALZ board for testing, complete the following steps:

1. Connect the DC2026C Linduino One board to the ADL5960-EVALZ board using the supplied 14-conductor ribbon cable. Keep the ribbon cable connected for the duration of testing.
2. Confirm the DC2026C Linduino One board has the correct firmware installed (as indicated by the ADL5960 label affixed to the DC2026C Linduino One board).
3. Verify on the DC2026C Linduino One board that VCCIO is set to 3.3 V, which is the normal configuration. See Figure 3.

Figure 3. Confirm Linduino 3.3 V, I/O Voltage Setting

4. Ensure that the EN jumper on the ADL5960-EVALZ board is installed, which is the default setup when the ADL5960-EVALZ ships. This jumper is seen at the top of the ADL5960-EVALZ, near the RF test trace.
5. Set up the 5 V power supply for at least 500 mA of current capability. Then turn the power source off. Connect the +5 V power supply and a ground return path to the VCC turret.
6. Ensure that the GUI demonstration software has been downloaded and installed on the PC. If not, download the software from www.analog.com/ADL5960.

RECOMMENDED POWER SEQUENCING

To prevent device damage, the following power-up sequence is recommended:

1. Apply 5 V of power to the ADL5960-EVALZ board VCC.
2. Connect the USB cable from the DC2026C Linduino One to the PC. Wait for the LEDs to stop blinking. When the LEDs stop blinking, the ADL5960 is enabled. The 5 V power nominally consumes approximately 120 mA of current.
3. Launch the GUI program on the PC.

The GUI **Connection** tab shows that the PC automatically discovers the DC2026C Linduino One (see Figure 4). Click **Connect** to connect to the ADL5960 IC under test. The **Main Controls** tab opens, which shows the register settings that can be changed (see Figure 5).

To power down the test setup, follow the power-up sequence in reverse:

1. Close the GUI program.
2. Disconnect the USB cable. The ADL5960 becomes disabled.
3. Turn off or disconnect the 5 V power source.

RF FUNCTIONAL DEMONSTRATION

The most fundamental ADL5960 demonstration occurs when an LO is supplied externally at a frequency offset by the desired IF output frequency, as follows:

1. Connect an RF signal generator to drive the RF port. Set the power level to 10 dBm and the frequency to 1 GHz.
2. Connect a second RF signal generator to the LO port. The unused differential LO port must be terminated with 50 Ω SMA termination. Set the LO drive power to 0 dBm, and the frequency to 1.01 GHz.
3. Leave the RFOUT port unconnected.
4. Connect both IF port outputs to an oscilloscope. If only a 2-channel oscilloscope is available, drive each oscilloscope channel single-ended with the downconverted IF incident and reflected signals. If oscilloscope has four channels, connect all four IF output connectors to the oscilloscope, and configure the oscilloscope to display two differential signals, incident and reflected.
5. Downconverted incident and reflected output signals can be observed on the oscilloscope at the difference frequency, 10 MHz. Increasing the IF gain register settings to approximately 20 dB typically result in a higher signal-to-noise ratio at the IF outputs without overdrive problems.
6. With the RFOUT port remaining unconnected (open), observe that there are large signals at both incident and reflected IF output ports. The reflected IF port signal is expected to be slightly lower than the incident port signal, because of ADL5960 insertion loss.
7. Install an RF short onto the RFOUT port. Observe that the IF incident and the reflected port magnitudes remain relatively constant, but the phase of the reflected IF port signal flips 180° compared to the prior RFOUT= open test condition.
8. Connect a 50 Ω SMA RF load (termination) to the RFOUT port. Observe that the IF incident port magnitude remains relatively constant, while the IF reflected port magnitude drops by a large amount, typically 30 dB, which is the approximate directivity specification of the ADL5960 device at 1 GHz. Note that the external SMA 50 Ω load termination on RFOUT must be accurate and wide band for this test. This measurement is

TEST PROCEDURE

never better than the directivity of the ADL5960, or the return loss performance of the 50 Ω termination on RFOUT.

GRAPHICAL USER INTERFACE

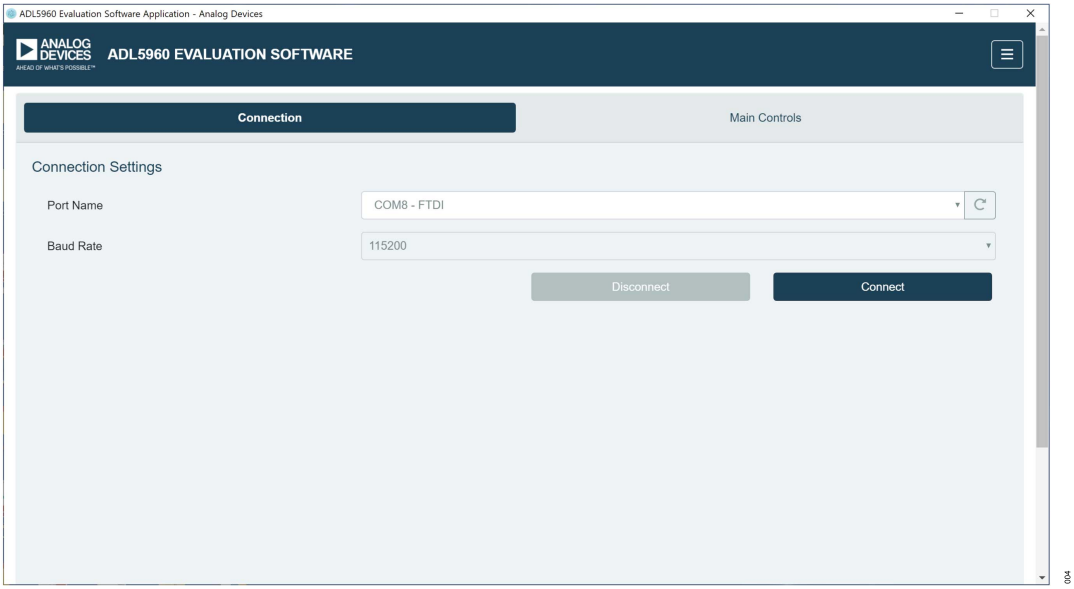

Figure 4. Connection Tab

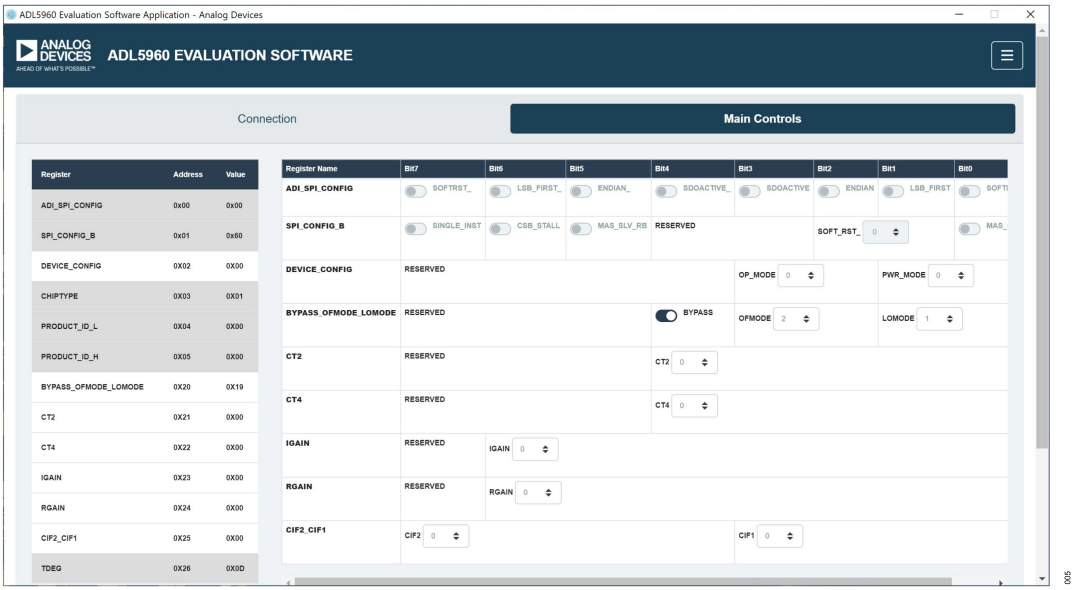

Figure 5. Main Controls Tab

GRAPHICAL USER INTERFACE

QUICK REFERENCE

For full and complete information, consult the ADL5960 data sheet.

Table 1. ADL5960 Registers Quick Reference

Bit Field Name	Description
Bypass	When asserted, this bit field sets the LO path to bypass the LO multipliers or dividers. OFMODE and LOMODE have no effect. When this bit field is deasserted, the LO path is via the selected LO multiplier or divider.
OFMODE	Configures the offset input dividers.
LOMODE	Configures the LO path multipliers and dividers.
CT2, CT4	CT2 and CT4 configure the LO chain ×2, and the ×4 filter frequency settings, respectively.
IGAIN, RGAIN	IGAIN and RGAIN configure the forward and reverse path IF gain settings, respectively.
CIF1, CIF2	CIF1 and CIF2 configure the first and second IF filter stage settings, respectively.
PWR_MODE	Mode 2 and Mode 3 disable the device.

EVALUATION BOARD SCHEMATIC AND ARTWORK

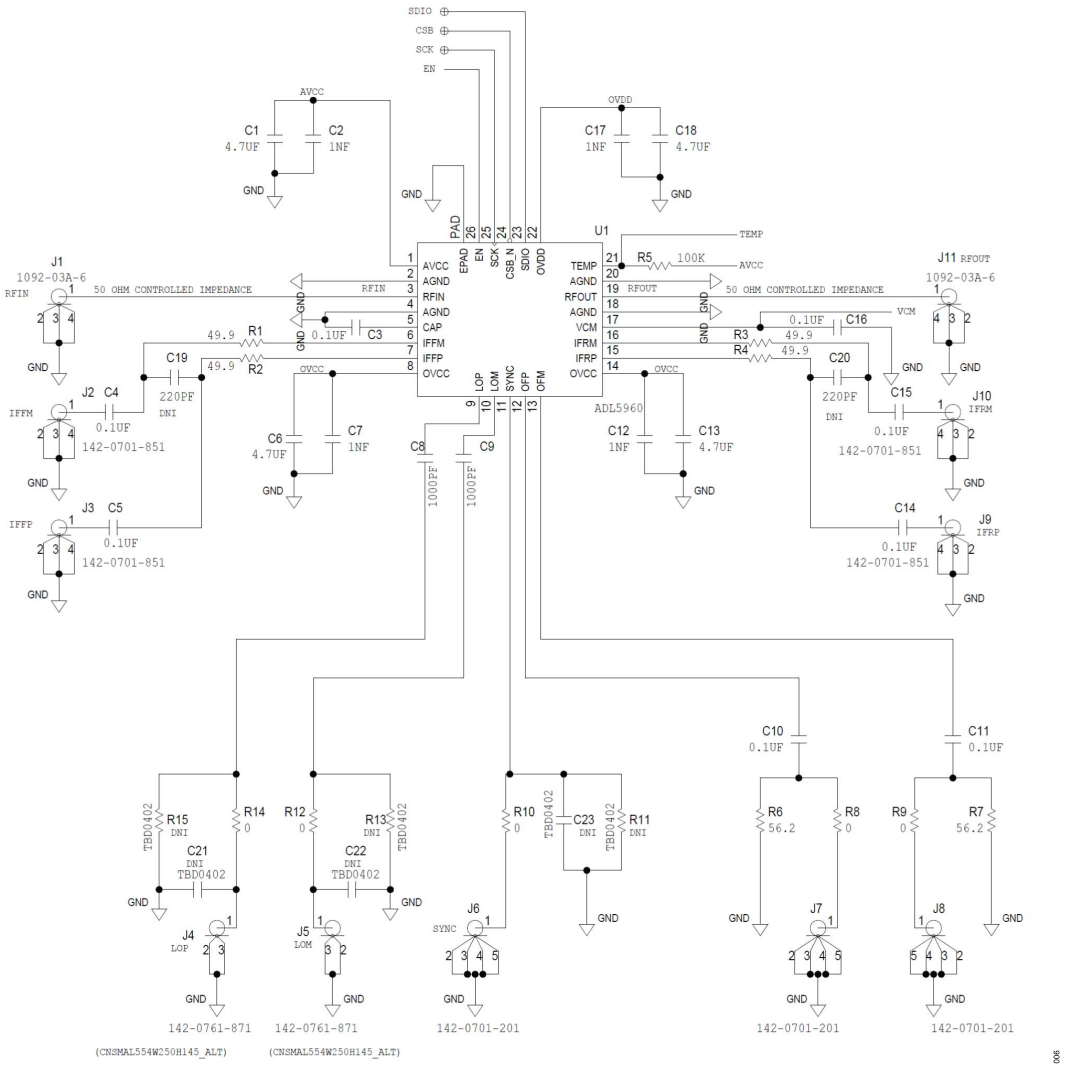

Figure 6. EVB Schematic Page 1 of 2 (DNI Denotes Do Not Install Those Components)

EVALUATION BOARD SCHEMATIC AND ARTWORK

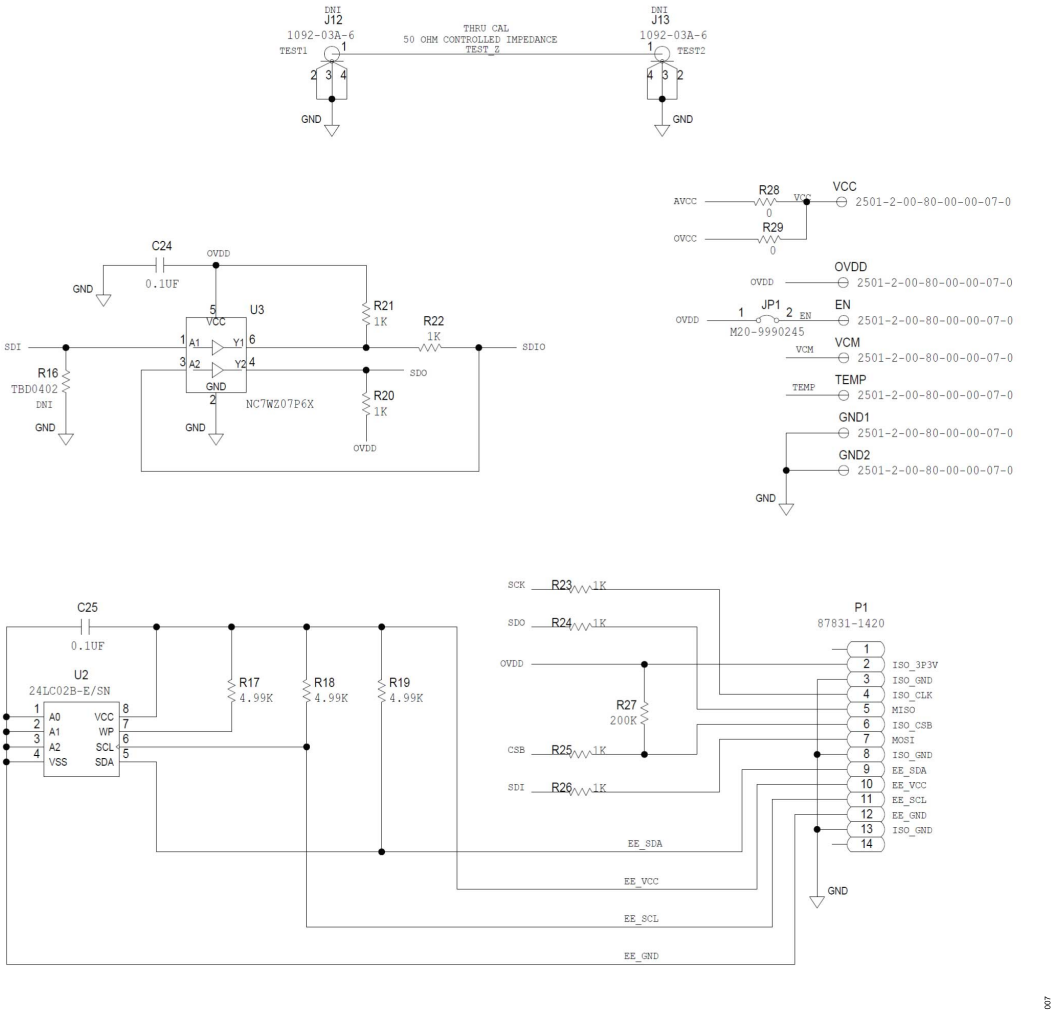

Figure 7. EVB Schematic, Page 2 of 2 (DNI Denotes Do Not Install Those Components)

EVALUATION BOARD SCHEMATIC AND ARTWORK

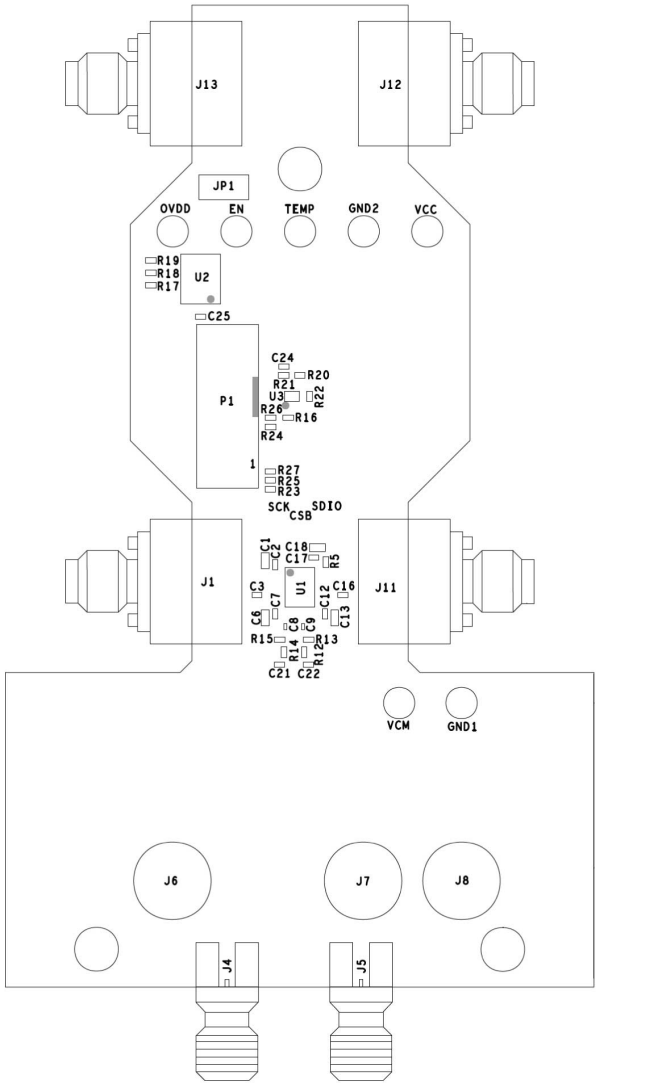

Figure 8. Assembly, Primary Side

EVALUATION BOARD SCHEMATIC AND ARTWORK

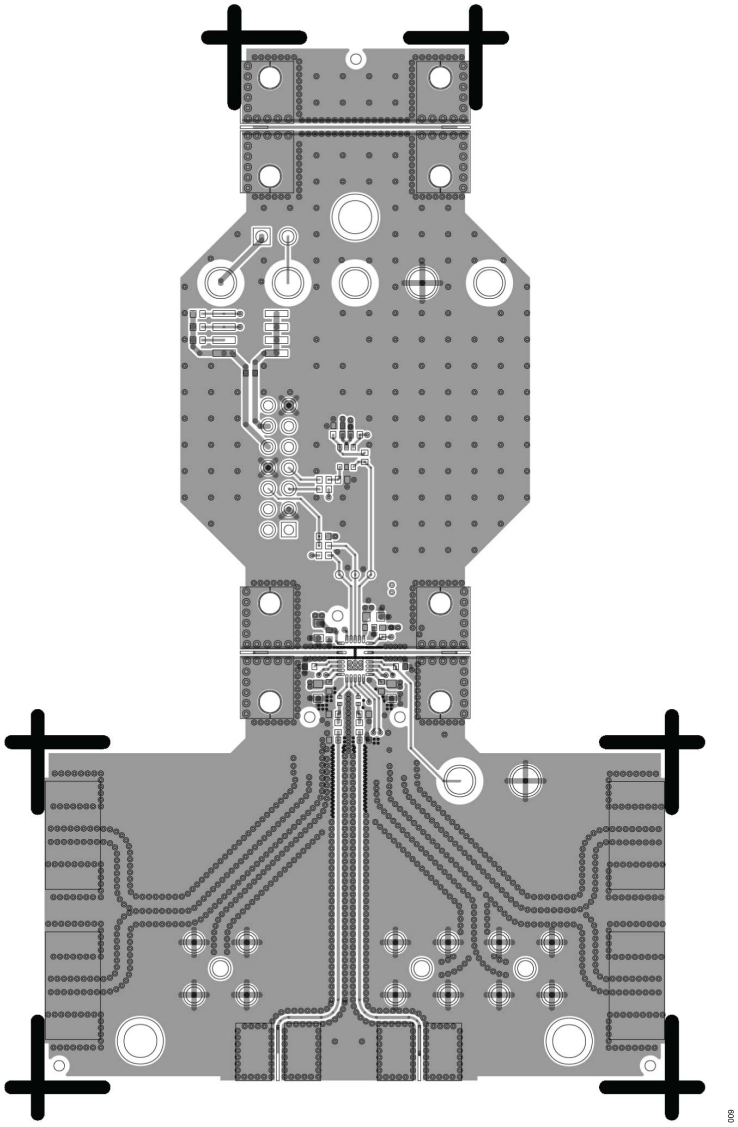

Figure 9. Layer 1

EVALUATION BOARD SCHEMATIC AND ARTWORK

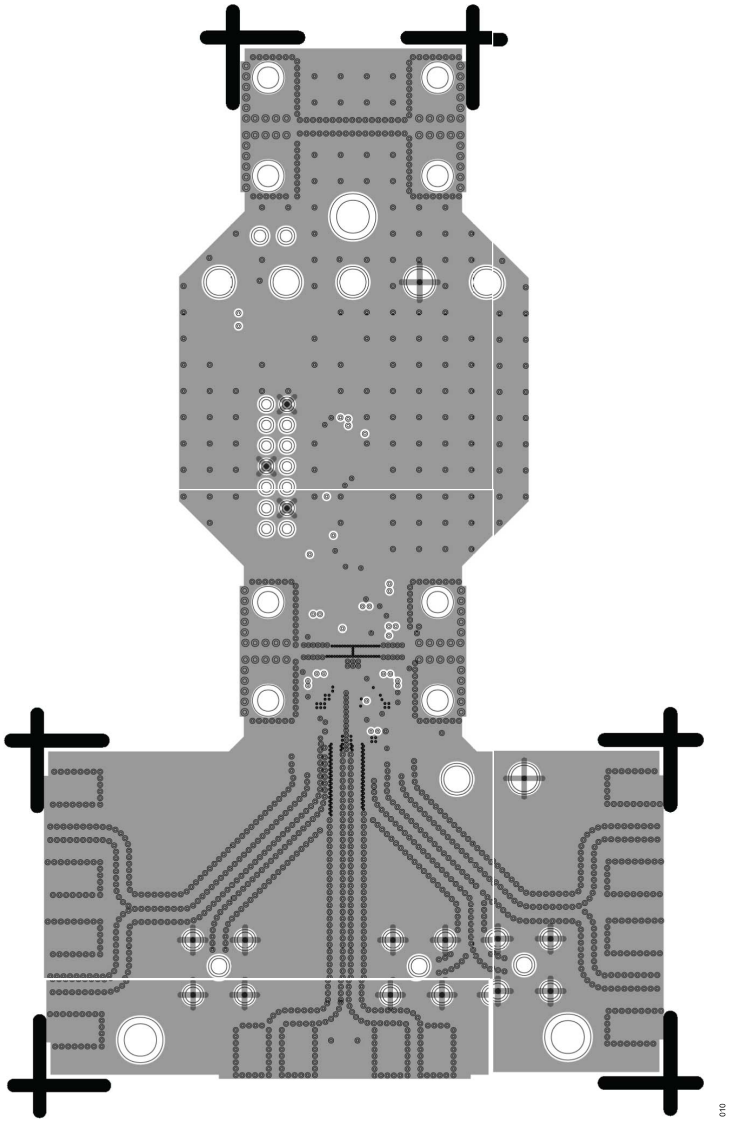

Figure 10. Layer 2

EVALUATION BOARD SCHEMATIC AND ARTWORK

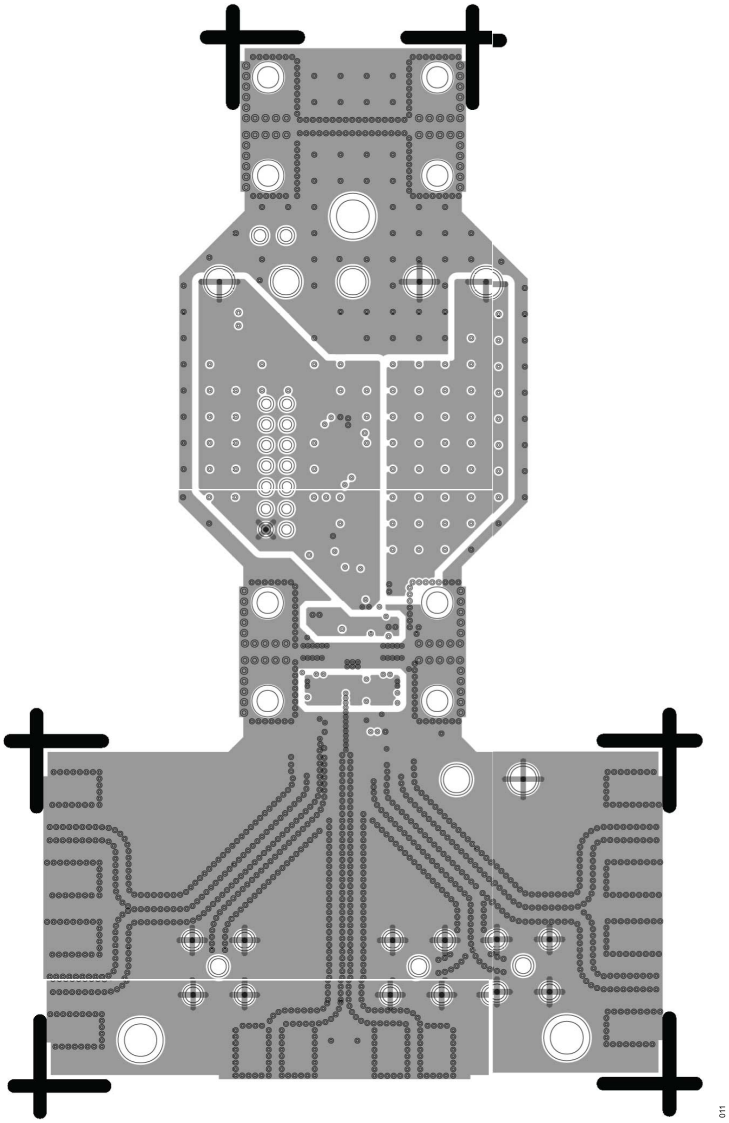

Figure 11. Layer 3

EVALUATION BOARD SCHEMATIC AND ARTWORK

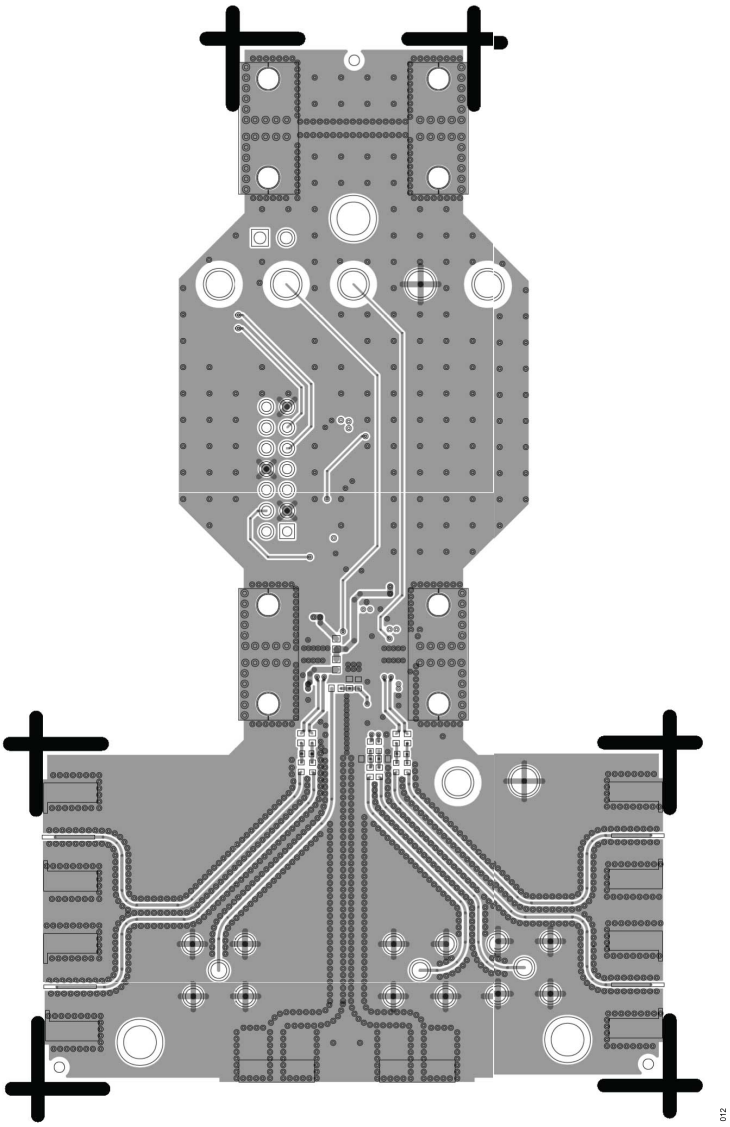

Figure 12. Layer 4

EVALUATION BOARD SCHEMATIC AND ARTWORK

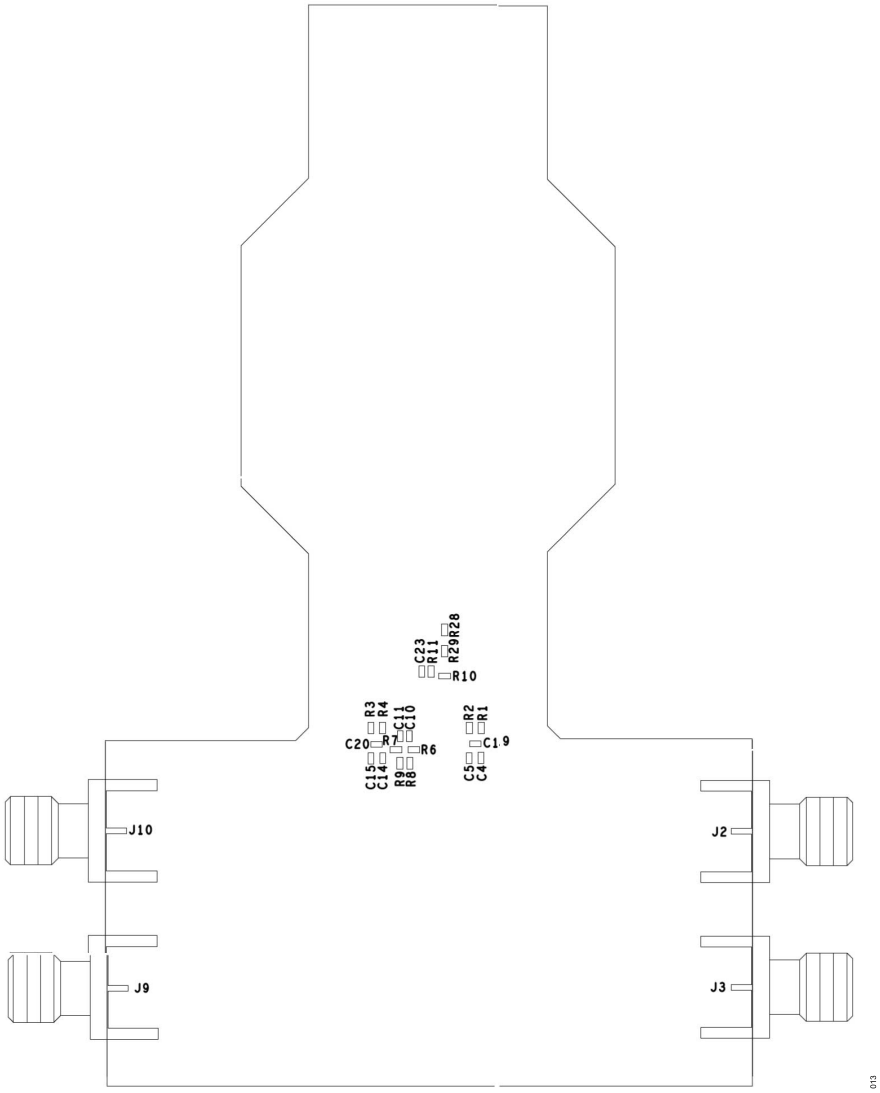

Figure 13. Assembly, Secondary Side (Flipped)

ORDERING INFORMATION

BILL OF MATERIALS

Table 2. Evaluation Board Components

Reference Designator	Description	Default Value	Manufacturer, Part Number
C1, C6, C13, C18	Ceramic capacitor, X5R, 0603	4.7 µF, 10 V, 10%	Taiyo Yuden LMK107BJ475KAHT
C3, C4, C5, C10, C11, C14, C15, C16	Ceramic capacitor, X7R, 0402	0.1 µF, 16 V, 10%	Kemet C0402C104K4RACTU
C2, C7, C12, C17	Ceramic capacitor, X7R, 0402	1 nF, 25 V, 10%	AVX 04023C102KAT2A
C8, C9	Ceramic capacitor, X7R, 0201	1000 pF, 25 V, 10%	Murata GCM033R71E102KA03D
J1, J11	Connector, end launch	2.92 mm female	Southwest Microwave 1092-03A-6
J2, J3, J9, J10	Connector, end launch	SMA female	Cinch 142-0701-851
J4, J5	Connector, end launch	SMA female	Emerson Network Power 142-0761-871
J6, J7, J8	Connector PCB, coaxial, straight	SMA female	Cinch Connectivity Solutions 142-0701-201
R1, R2, R3, R4	Resistor, SMD, 0402	49.9 Ω, 1%, 1/10 W	Panasonic ERJ-2RKF49R9X
R5	Resistor, SMD, 0402	100k Ω, 1%, 1/5 W	Panasonic ERJ-PA2F1003X
R6, R7	Resistor, SMD, 0402	56.2 Ω, 1%, 1/10 W	Panasonic ERJ-2RKF56R2X
U1	IC, 10 MHz to 20 GHz integrated VNA front end	ADL5960	Analog Devices, Inc., ADL5960ACRZ

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.