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Evaluating the ADRF5515 Dual-Channel, 3.3 GHz to 4.0 GHz, Receiver Front End

FEATURES

Full featured evaluation board for the ADRF5515
Easy connection to test equipment
Thru line for calibration

EQUIPMENT NEEDED

DC power supply
Signal generator
Spectrum analyzer
Network analyzer

GENERAL DESCRIPTION

The ADRF5515 is an integrated, dual-channel receiver front end ideally suited for time division duplexing (TDD) wireless infrastructure applications. The ADRF5515 consists of a high power switch and a two-stage low noise amplifier (LNA) on each channel.

This user guide describes the ADRF5515-EVALZ evaluation board, designed to easily evaluate the features and performance of the ADRF5515. A photograph of the evaluation board is shown in Figure 1.

The ADRF5515 data sheet provides full specifications for the ADRF5515. Consult the ADRF5515 data sheet in conjunction with this user guide when using the evaluation board.

EVALUATION BOARD PHOTOGRAPH

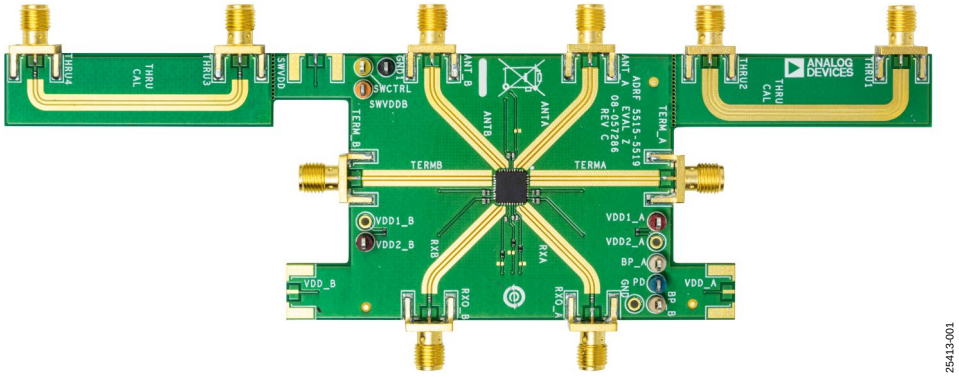

Figure 1.

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REVISION HISTORY

11/2020—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

OVERVIEW

The ADRF5515-EVALZ evaluation board is a connectorized board, assembled with the ADRF5515 and the application circuitry of the device. All components are placed on the primary side of evaluation board. An assembly drawing for the evaluation board is shown in Figure 5. An evaluation board schematic is provided in Figure 4. Table 4 provides the bill of materials (BOM) list for the evaluation board components.

BOARD LAYOUT

The ADRF5515-EVALZ is designed using RF circuit design techniques on an 8-layer printed circuit board (PCB). The PCB stackup is shown in Figure 2.

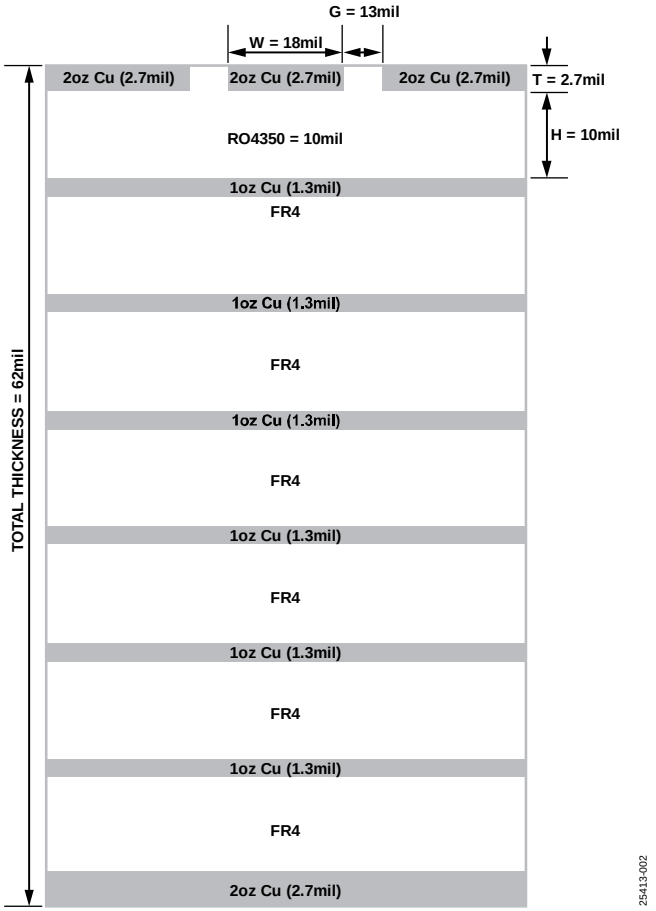

Figure 2. Evaluation Board Stackup

The outer copper layers are 2 oz (2.7 mil) thick and the inner layers are 1 oz (1.3 mil) thick.

The top dielectric material is 10 mil Rogers 4350B, which provides 50 Ω controlled impedance and optimizes high frequency performance. The remaining six dielectric layers are FR4 based filler layers that improve the mechanical strength of the board and meet the overall board thickness of approximately 62 mil.

All RF traces are routed on the top layer, and the remaining seven layers are ground planes that provide a solid ground for the RF transmission lines and manage the thermal rise on the evaluation board during high power operations.

The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a width of 18 mil and ground spacing of 13 mil, resulting in a characteristic impedance of 50 Ω. Ground via fences are arranged on both sides of a CPWG to improve isolation between nearby RF lines and other signal lines.

The exposed ground pad of the ADRF5515, which is soldered on the PCB ground pad, is the main thermal conduit for heat dissipation. The PCB ground pad is densely populated with filled through vias to provide the lowest possible thermal resistance path from the top to the bottom of the PCB. The connections from the package ground leads to ground are kept as short as possible.

POWER SUPPLY INPUTS

The ADRF5515-EVALZ evaluation board has five power supply inputs and one ground, as shown in Table 1. The dc test points are populated only on SWVDDB, VDD1_A, and VDD1_B, whereas VDD2_A and VDD2_B are shorted to VDD1_A and VDD1_B, respectively, via 0 Ω resistors. A single 5 V supply is connected to the dc test points on SWVDDB, VDD1_A, and VDD1_B. The typical total current consumption for the ADRF5515 is 180 mA.

Each supply pin for the LNAs of the ADRF5515 is decoupled with 1000 pF and 10 µF capacitors. A 10 µF capacitor is used on the supply line for the switches of the ADRF5515.

Table 1. Power Supply Inputs and Ground

Test Points	Description
VDD1_A	Supply LNA Stage 1 on Channel A
VDD2_A	Supply LNA Stage 2 on Channel A, do not insert (DNI)
VDD1_B	Supply LNA Stage 1 on Channel B
VDD2_B	Supply LNA Stage 2 on Channel B, DNI
SWVDDB	Supply switches on Channel A and Channel B
GND1	Ground

CONTROL INPUTS

The ADRF5515-EVALZ evaluation board has four control inputs, described in Table 2. Each control input is decoupled with a 100 pF capacitor.

Table 2. Control Inputs

Test Points	Description
BP_A	Bypass LNA Stage 2 on Channel A
BP_B	Bypass LNA Stage 2 on Channel B
PD	Power down all LNA stages on Channel A and Channel B
SWCTRL	Control switches on Channel A and Channel B

RF INPUTS AND OUTPUTS

The ADRF5515-EVALZ evaluation board has ten edge mounted Subminiature Version A (SMA) connectors for the RF inputs and outputs, as shown in Table 3. The ADRF5515 covers the 3.3 GHz to 4.0 GHz frequency range and does not require any external matching components.

By default, the evaluation board comes assembled and shipped without SMA connectors and series components on the thru lines. To measure and calibrate out the board loss effects, the user must connect these connectors and components. Use the thru line on THRU1 and THRU2 to calibrate out the ANT_A/ANT_B to TERM_A/TERM_B board loss. Use the thru line on THRU3 and THRU4 to calibrate out the RXO_A/RXO_B board loss.

Table 3. RF Inputs and Outputs

SMA Connectors	Description
ANT_A	Antenna input to Channel A
ANT_B	Antenna input to Channel B
TERM_A	Termination output from Channel A
TERM_B	Termination output from Channel B
RxO_A	Receiver output from Channel A
RxO_B	Receiver output from Channel B
THRU1	Thru line input/output, DNI
THRU2	Thru line input/output, DNI
THRU3	Thru line input/output, DNI
THRU4	Thru line input/output, DNI

TEST PROCEDURE

The ADRF5515-EVALZ evaluation board ships fully assembled and tested. Figure 3 provides a basic test setup diagram. Perform the following steps to complete the test setup and verify the operation of the ADRF5515-EVALZ evaluation board:

1. Connect the GND1 test point to the ground terminal of the power supply.
2. Connect the VDD1_A, VDD2_A, and SWVDDB test points to the voltage output terminal of the power supply.
3. Connect the BP_A, BP_B, PD, and SWCTRL test points to the ground terminal of the power supply for high gain receive operation.
4. Connect a signal generator to the ANT_A SMA connector. Set the signal generator to a −30 dBm output power at 3.6 GHz.
5. Connect a spectrum analyzer to the RxO_A SMA connector. Set the spectrum analyzer to a 3.3 GHz center frequency and the reference power level at 10 dBm.
6. Connect 50 Ω loads to the TERM_A, ANT_B, RxO_B, and TERM_B SMA connectors.
7. Turn on the 5 V supply that sources a current of approximately 180 mA.
8. Turn on the RF signal generator. The spectrum analyzer displays a tone of approximately 3 dBm at 3.3 GHz so that Channel A of the ADRF5515-EVALZ evaluation board has a receive gain of 33 dB.
9. Turn off the RF signal generator and then the power supply.
10. To repeat the test on Channel B, connect the test equipment to the ANT_B and RxO_B SMA connectors in Step 4 and Step 5 and connect 50 Ω loads to the TERM_A, TERM_B, ANT_A, and RxO_A SMA connectors in Step 6.

Additional test equipment is required to fully evaluate the device functions and performance.

The ADRF5515 can be configured in different modes by connecting the control test points to 5 V or ground. Use a separate power supply to evaluate the control input functions.

Use a network analyzer to evaluate the receive gain, transmit insertion loss and isolation, RF input and output return losses, and channel to channel isolation.

For noise figure evaluation, use either a noise figure analyzer or a spectrum analyzer with a noise option. The use of a low excess noise ratio (ENR) noise source is recommended.

For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high isolation power combiner is recommended.

For power compression and power handling evaluations, use a 2-channel power meter and a signal generator. A power amplifier with an output power rating of >200 W is recommended at the input. Test accessories, such as couplers and attenuators, must have sufficient power handling.

The ADRF5515-EVALZ features a support plate attached to the bottom side of the board. To ensure maximum heat dissipation and to reduce thermal rise on the evaluation board during high power evaluations, attach the support plate to a heat sink using thermal grease.

Note that the measurements performed at the SMA connectors of the ADRF5515-EVALZ include the losses of the SMA connectors and the PCB. The thru line must be measured to calibrate out the board effects. The thru line is the summation of an RF input line and an RF output line that are connected to the device and are equal in length.

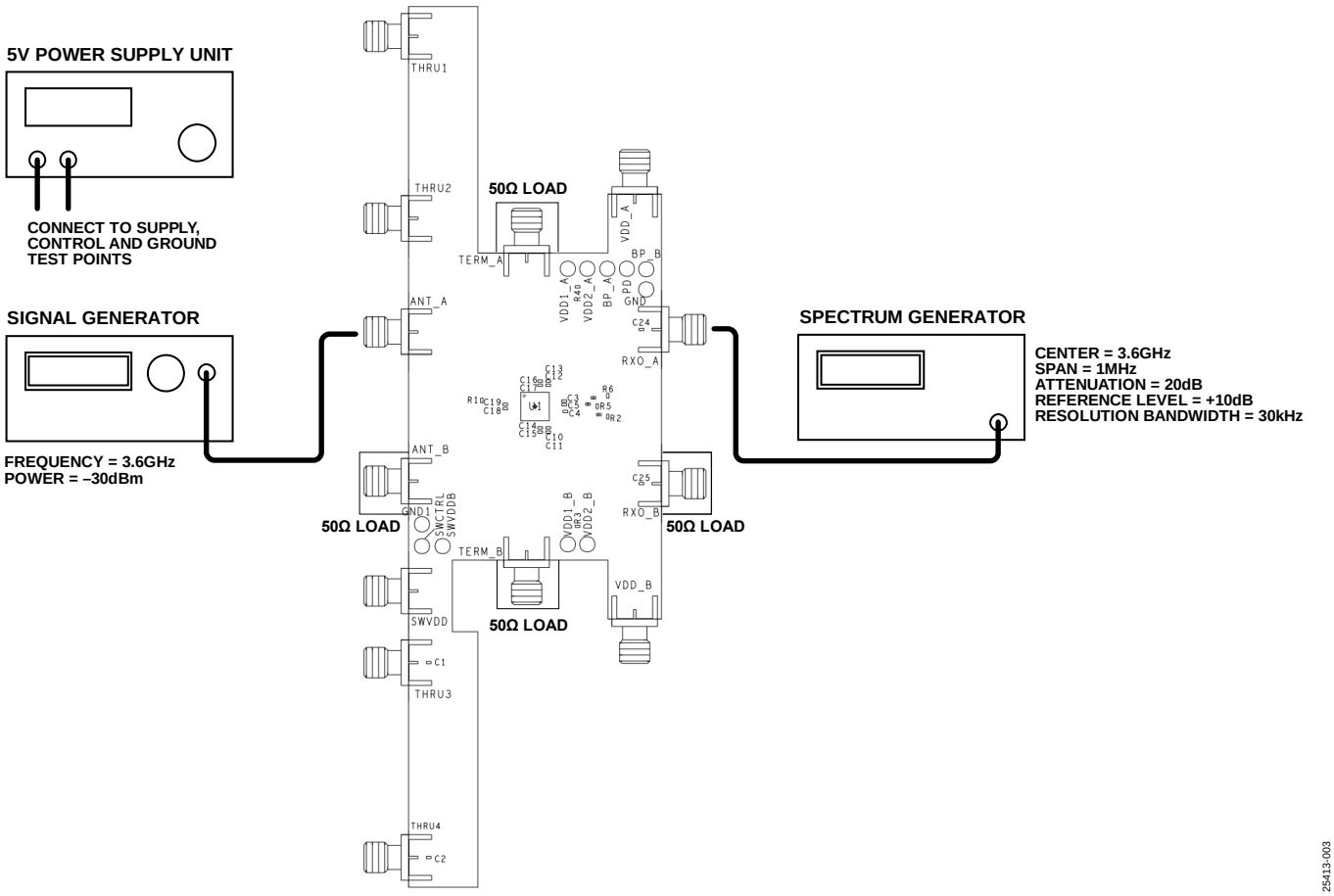

Figure 3. Test Setup Diagram

EVALUATION BOARD SCHEMATIC AND ARTWORK

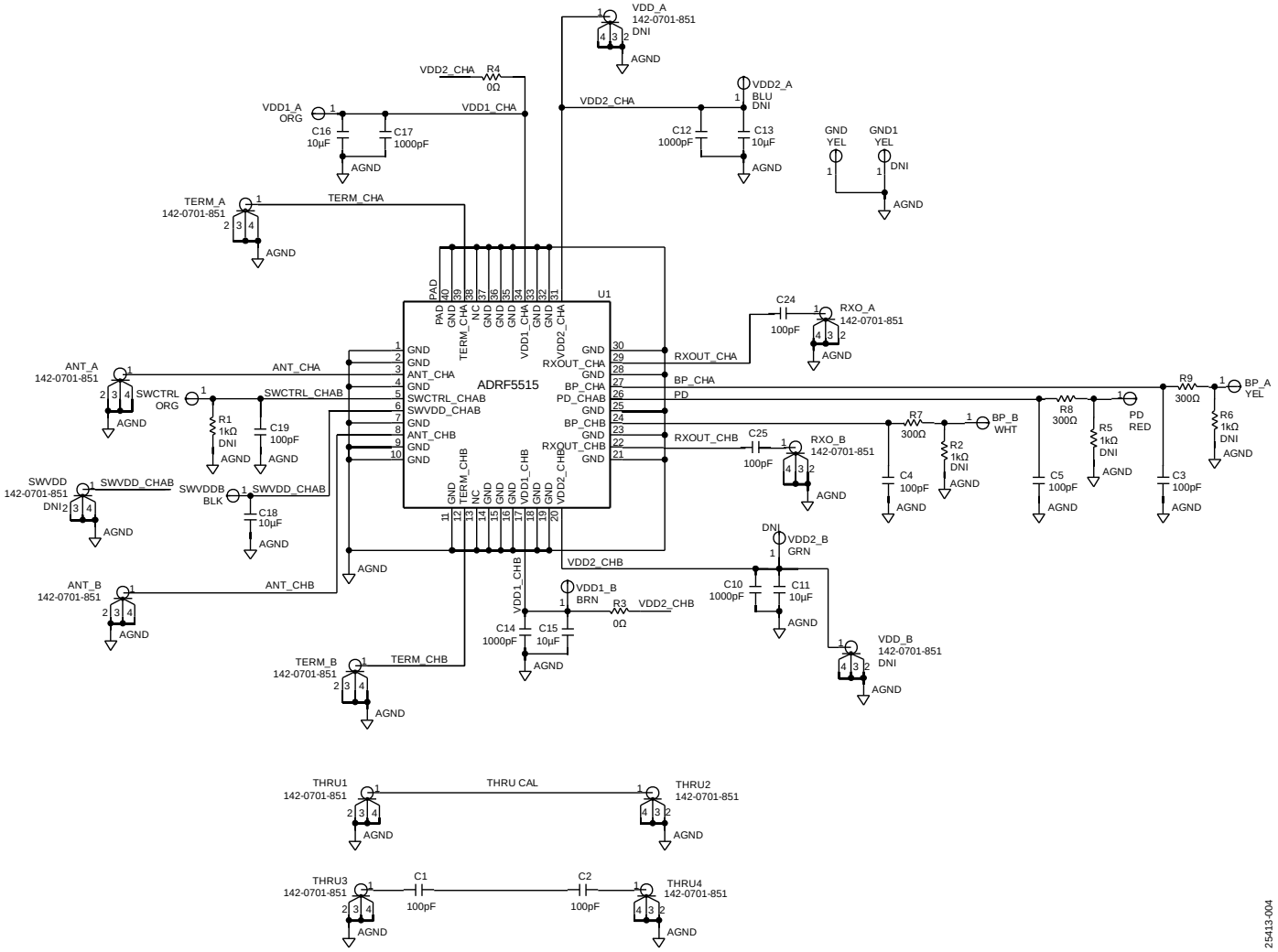

Figure 4. Evaluation Board Schematic

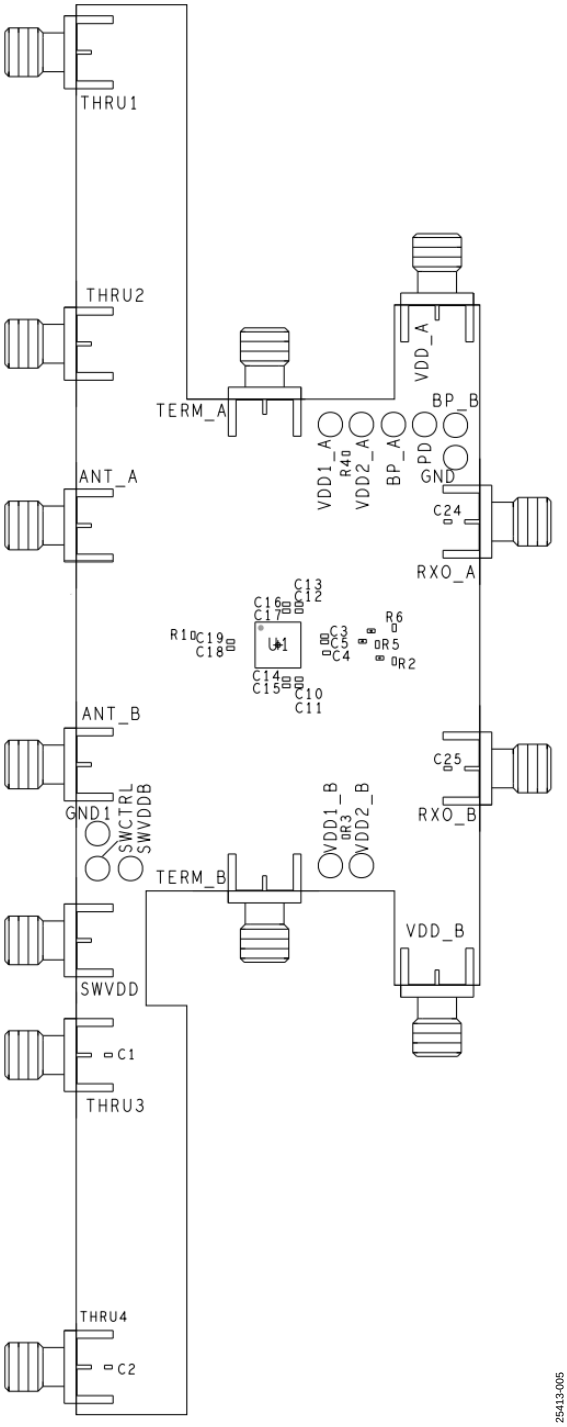

Figure 5. Evaluation Board Assembly Diagram

ORDERING INFORMATION

BILL OF MATERIALS

Table 4. Bill of Materials for the ADRF5515-EVALZ

Reference Designator	Description	Manufacturer	Part Number
ANT_A, ANT_B, RxO_A, RxO_B, TERM_A, TERM_B	PCB mount SMA connectors	Johnson/Cinch Connectivity Solutions	142-0701-851
C3, C4, C5	100 pF capacitors, 50 V, 0402 package	Murata Electronics	GCM1555C1H101JA16D
C1 ,C2, C19, C24, C25	100 pF capacitors, 200 V, 0402 package	KEMET	C0402C101J2GACTU
C10, C12, C14, C17	1000 pF capacitors, 25 V, 0402 package	TDK	CGJ2B2X7R1E102K050BA
C11, C13, C15, C16, C18	10 µF capacitors, 10 V, 0402 package	Samsung Electro-Mechanics	CL05A106MP5NUNC
R3, R4	0 Ω resistors, 0402 package	Panasonic Electronic Components	ERJ-2GE0R00X
R7, R8, R9	300 Ω resistors, 0402 package	Panasonic Electronic Components	ERJ-2GEJ301X
U1	RF front-end IC	Analog Devices, Inc.	ADRF5515
PCB	PCB	Analog Devices	08_057286C