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Evaluating the ADP5040 and ADP5041 Micropower Management Units (PMUs)

FEATURES

Full featured evaluation board for the ADP5040 or ADP5041
Simple device measurements, including line and load regulation demonstrable with
- **A single voltage supply**
- **A voltage meter**
- **A current meter**
- **Load resistors**

Easy access to external components
Cascading options to supply LDO regulators from the buck
Dedicated enable option for each channel
Mode option to change bucks from PFM to PWM operation
Voltage monitoring and watchdog for ADP5041

EVALUATION KIT CONTENTS

ADP5040CP-1-EVALZ or ADP5041CP-1-EVALZ evaluation board

EQUIPMENT NEEDED

A dc power supply
Digital multimeter
Electronic load

GENERAL DESCRIPTION

The evaluation board shown in Figure 1 is configured for the ADP5040 (the assembly for the ADP5041 is not included), but the board can be used for evaluation of the ADP5041. The ADP5040 and ADP5041 have one step-down regulator and two low dropout (LDO) regulators (LDO1 and LDO2).

The evaluation board also allows the evaluation of supervisory functions for the ADP5041. The evaluation board is available in standard voltage options and it can be reconfigured to user specific voltage options by replacing the assembled resistor networks (R2/R3, R4/R5, and R9/R10) as shown in Figure 11 and Figure 12. Voltage monitoring can also be performed in the ADP5041, as shown in Figure 4.

Full details on the ADP5040 and ADP5041 are provided in the ADP5040 and ADP5041 data sheets available from Analog Devices, Inc., which must be consulted in conjunction with this evaluation board user guide.

ADP5040CP-1-EVALZ PHOTOGRAPH

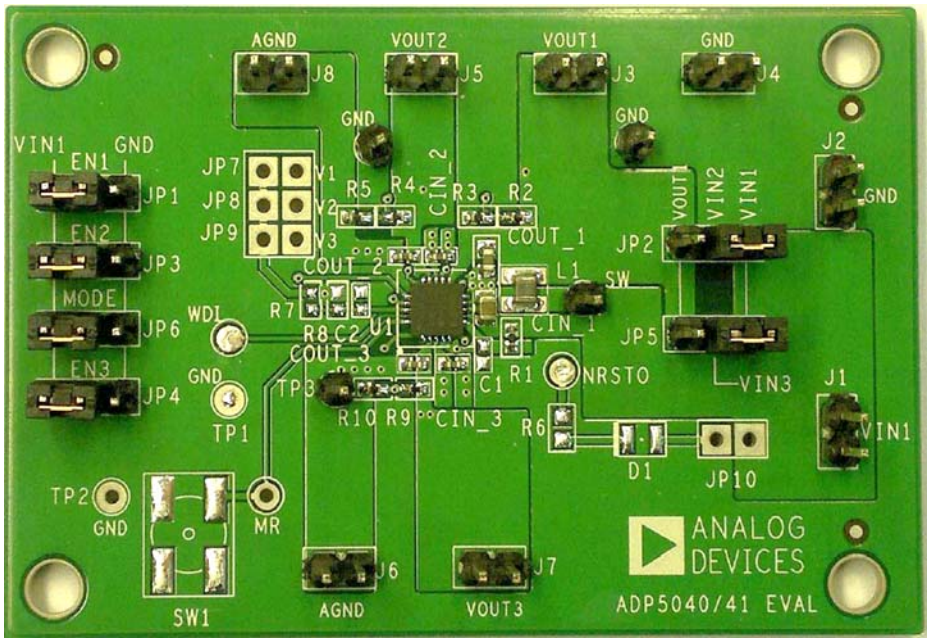

Figure 1.

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REVISION HISTORY

11/2020—Revision 0: Initial Version

USING THE EVALUATION BOARD

The ADP5040 and ADP5041 use a proprietary, high speed, current mode, constant frequency, pulse-width modulation (PWM) control scheme for optimal stability and transient response. To ensure the longest battery life in portable applications, the ADP5040 and ADP5041 feature a power save mode (PSM) that reduces the switching frequency under light load conditions, as well as the option to change the mode to fixed PWM operation. The 3 MHz switching frequency minimizes the size of the external components.

The ADP5041 contains supervisory circuits for monitoring a selected power supply voltage level and code execution integrity in microprocessor-based systems. The supervisory circuits also provide power-on reset signals and an on-chip watchdog timer that can reset the microprocessor if it fails to strobe within a preset timeout period.

JUMPERS

Regulator Configuration for ADP5040 and ADP5041

Table 1 provides the regulator configurations for the ADP5040CP-1-EVALZ/ADP5041CP-1-EVALZ board jumpers.

Table 1. ADP5040CP-1-EVALZ/ADP5041CP-1-EVALZ Jumper Functions

Connector Header	Connection
JP1	Shunt between EN1 and VIN1: buck enabled Shunt between EN1 and GND: buck disabled
JP2[1]	Shunt between VIN2 and VOUT1: LDO1 supplied from VOUT1 (buck) Shunt between VIN2 and VIN1: LDO1 supplied from external power supply
JP3	Shunt between EN2 and VIN1: LDO1 enabled Shunt between EN2 and GND: LDO1 disabled
JP4	Shunt between EN3 and VIN1: LDO2 enabled Shunt between EN3 and GND: LDO2 disabled
JP5[1]	Shunt between VIN3 and VOUT1: LDO2 supplied from VOUT1 (buck) Shunt between VIN3 and VIN1: LDO2 supplied from the external power supply
JP6	Shunt between MODE and VIN1: force PWM Shunt between MODE and GND: automatic PSM

[1] The output voltage settings for VOUT2 and VOUT3 must be changed if the input voltage for LDO1 and LDO2, respectively, is supplied from VOUT1.

Supervisory Configuration for ADP5041 Only

Table 2 provides the supervisory configurations for the ADP5041CP-1-EVALZ board jumpers.

Table 2. ADP5041CP-1-EVALZ Jumper Connections

Connector Header	Connection
JP7	Shunt on JP7: monitors VOUT1 (buck)
JP8	Shunt on JP8: monitors VOUT2 (LDO1)
JP9	Shunt on JP9: monitors VOUT3 (LDO2)
JP10	Shunt on JP10: enables NRSTO indicator LED

DEFAULT CONFIGURATION OF THE ADP5040CP-1-EVALZ/ADP5041CP-1-EVALZ BOARDS

Table 3. Regulator Channel Configuration

Channel	Regulator	Output Voltage (V)
1	Buck	1.2
2	LDO1	1.8
3	LDO2	3.3

The voltage monitor threshold, VTHR, for the ADP5041 is configured to 2.935 V by Resistors R7 and R8.

For other voltage options, see the Output Voltage Options section.

Table 4. Default Jumper Configuration

Connector Header	Connection
JP1, JP2, JP3, JP4, JP5, JP6 (ADP5040 and ADP5041)	Pin 2 and Pin 3.
JP7, JP8 (ADP5041 Only)	Not assembled.[1]
JP9 (ADP5041 Only)	Pin 1 and Pin 2. VOUT3 selected.
JP10 (ADP5041 Only)	Pin 1 and Pin 2.

[1] Assemble only one of the jumpers (JP7, JP8, or JP9).

POWERING UP THE EVALUATION BOARD

The ADP5040CP-1-EVALZ/ADP5041CP-1-EVALZ evaluation boards are delivered fully assembled and tested. Before applying power to the evaluation boards, enable the channel, select PWM or PWM/PSM mode, connect the power source and output load, and attach the voltage meter as described in the Enable, Jumper JP6 (MODE), Input Power Source, Output Load, and Input Voltage and Output Voltage Meters sections.

Enable

Each channel has its own enable pin that must be pulled high to enable that channel (see Table 5).

Table 5. Channels on the Enable Pins

Channel	Regulator	Enable Pin
1	Buck	JP1
2	LDO1	JP3
3	LDO2	JP4

Jumper JP6 (MODE)

Jumper JP6 (MODE) pulled high to VIN1 forces the buck into PWM operation. JP6 (MODE) pulled low to GND allows the buck to operate in automatic PWM/PSM operation.

Input Power Source

Connect the positive terminal of the power source to J1 (VIN1) on the evaluation board and the negative terminal of the power source to J2 (GND).

If the power source does not include a current meter, connect a current meter in series with the input source voltage. Be aware that the current meters add resistance to the input source, and this voltage reduces with high output currents.

Output Load

Connect an electronic load or a resistor to set the load current. Connect the load to one of the positive and ground output channels of the evaluation board. For example, connect the load to the buck output channel, J3 (VOUT1), and J4 (GND).

When using an external current meter, connect the current meter in series with the load.

Input Voltage and Output Voltage Meters

Measure the input and output voltages with voltage meters. Ensure that the voltage meters are connected to the appropriate evaluation board terminals and not to the load or power sources themselves.

A voltage meter that is not connected directly to the evaluation board produces an incorrect measured voltage caused by a voltage drop across the leads and/or connections between the evaluation board, the power source, and/or the load.

To measure the input voltage, connect the negative (−) and the positive (+) probes of an input voltage meter to J2 (GND) and J1 (VIN1), respectively. To measure the buck output voltage, connect the negative (−) and the positive (+) probes of a voltage meter to J4 (GND) and J3 (VOUT1), respectively. For the other channels, use either J5 (VOUT2) and J6 (AGND), or J7 (VOUT3) and J8 (AGND).

Turning On the Evaluation Board

When the power source and load are connected to the ADP5040CP-1-EVALZ or ADP5041CP-1-EVALZ board, the board can be powered for operation. Ensure that

- The power source voltage is ≥2.3 V and ≤5.5 V.
- For LDO1 and LDO2, $V_{IN} \geq V_{OUT} + 0.5$ V.
- The desired channel is enabled.

Enable the load. Check that the load is drawing the proper current and that the output voltage maintains voltage regulation.

MEASURING EVALUATION BOARD PERFORMANCE

The ADP5040CP-1-EVALZ was used for the performance evaluation. The results for the following tests also apply to the ADP5041CP-1-EVALZ.

MEASURING OUTPUT VOLTAGE RIPPLE ON THE BUCK REGULATOR

To observe the output voltage ripple of the buck regulator, place an oscilloscope probe across the output capacitor (COUT_1) with the probe ground lead at the negative (−) capacitor terminal and the probe tip at the positive (+) capacitor terminal. Set the oscilloscope to ac, 20 mV/division, and 2 µs/division time base.

MEASURING REGULATOR OUTPUT VOLTAGES

Figure 2 shows how the evaluation board connects to a voltage source and a voltage meter for basic output voltage accuracy measurements. A resistor can be used as the load for the regulator. Ensure that the resistor has a power rating adequate to handle the power expected to be dissipated across it. An electronic load can also be used as an alternative. Ensure that the voltage source can supply enough current for the expected load levels.

Note that VIN1 must always be biased to a higher or equal voltage than the other inputs to ensure correct operation of the chip (and the supervisory functions for the ADP5041).

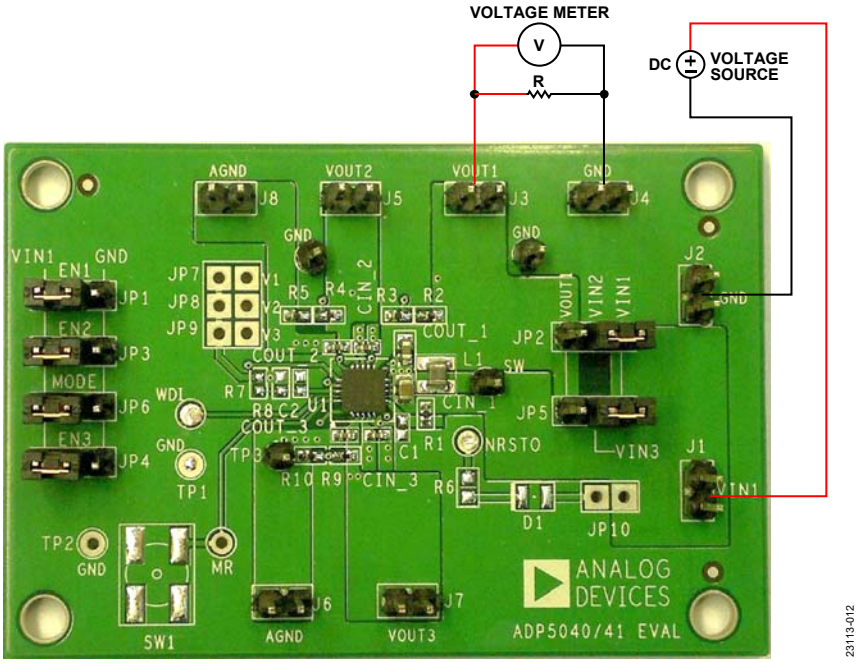

Figure 2. Output Voltage Measurement

MEASURING LDO REGULATOR BIAS CURRENT

Figure 3 shows the evaluation board connected to a voltage source and a current meter for bias current measurements. A resistor can be used as the load for the regulator. Ensure that the resistor has a power rating that is adequate to handle the power expected to be dissipated across it. An electronic load can be used as an alternative. Ensure that the voltage source can supply enough current for the expected load levels. Connect the voltage source in series with an input current (I_{IN}) measuring instrument between the respective LDO regulator input (Pin 2 of JP2 for Channel 2 and JP5 for Channel 3) and AGND. Connect the load in series with the output current (I_{OUT}) measuring instrument to the respective LDO regulator output (VOUT2 for Channel 2 and VOUT3 for Channel 3) and AGND.

Note that VIN1 must always be biased to a higher or equal voltage than the other inputs to ensure correct operation of the chip (and supervisory functions for the ADP5041).

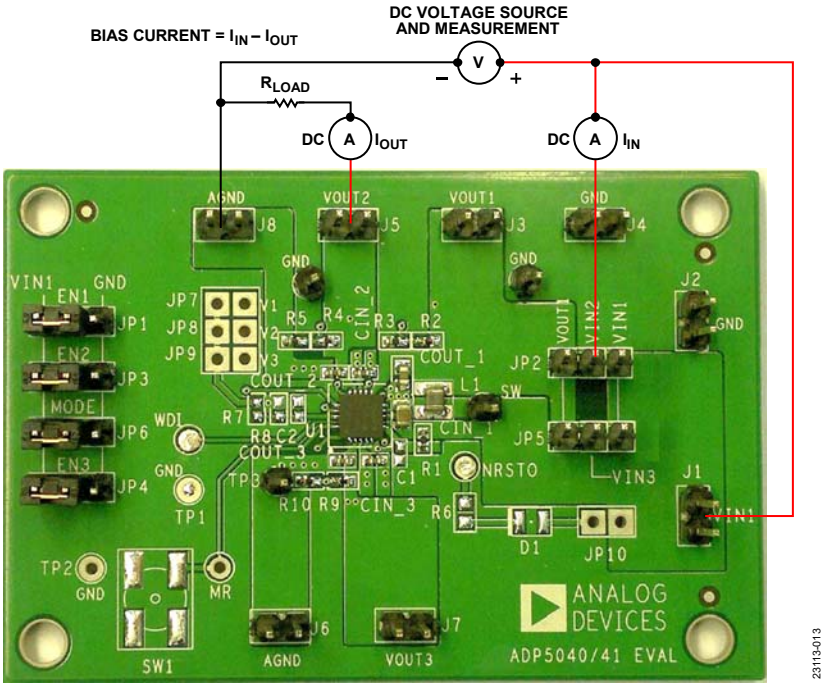

Figure 3. Bias Current Measurement

TESTING THE SUPERVISORY FUNCTIONS

The ADP5041 provides microprocessor supply voltage supervision by controlling the reset input of the microprocessor.

Reset Output

The ADP5041 has an active low, open-drain reset output. This output structure requires an external pull-up resistor to connect the reset output to a voltage rail that is no higher than 6 V. A 10 kΩ resistor is adequate in most situations.

The reset output can also be visually monitored by connecting a 2-pin connector header to JP10, which connects the reset output to the input voltage at J1 of the evaluation board through an LED and a series resistor.

The reset output is asserted when the monitored rail is below the reset threshold voltage (V_{TH}) or when the watchdog input (WDI) terminal pin on the board is not serviced within the watchdog timeout period.

Voltage Monitoring Input

The reset threshold voltage at the VTHR input pin of the chip is typically 0.5 V. To monitor a voltage greater than 0.5 V, connect a resistor divider network to the device as shown in Figure 4.

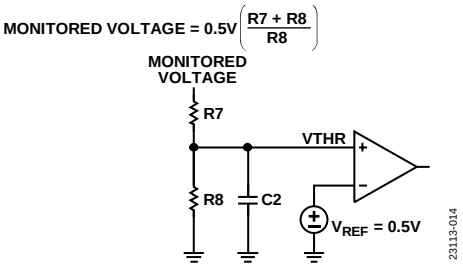

Figure 4. Voltage Monitor Threshold Programming

The combined resistance of R7 and R8 must not exceed 200 kΩ. Do not allow the VTHR input pin of the chip to float or to be grounded. Instead, connect the VTHR pin to a supply voltage greater than its specified threshold voltage. A small capacitor (C2) can be added on the VTHR node to improve the noise rejection and to prevent false reset generation.

When testing this function, refer to the schematic in Figure 13 and connect a voltage generator to Pin 1 of one of the 2-pin connector headers (JP7, JP8, or JP9), and the NRSTO test point output pin on the board can be monitored using an oscilloscope. Note that the jumpers for JP7, JP8, and JP9 must not be installed when performing this test.

Manual Reset Input

The ADP5041 features a manual reset input pin ($\overline{MR}$) that, when driven low, asserts the reset output. The manual reset feature can be activated by pushing the SW1 push-button or by connecting a pulse generator to the MR input connector pin on the evaluation board.

Watchdog Input

The ADP5041 features a watchdog timer. The timer circuit is cleared by every low to high or high to low logic transition on the WDI pin, which detects pulses as short as 80 ns.

To test the watchdog feature, connect a pulse generator to the WDI input terminal pin on the board and monitor the NRSTO output terminal pin on the board with an oscilloscope.

The watchdog function is disabled when the WDI input terminal pin on the board is left floating.

MEASURING THE SWITCHING WAVEFORM

To observe the switching waveform with an oscilloscope, place the oscilloscope probe tip at the end of the inductor, L1 (SW test point), with the probe ground at J4 (GND). Set the oscilloscope to dc, 2 V/division, and 2 µs/division time base.

MEASURING THE LOAD REGULATION

Test the load regulation by increasing the load current at the output and by monitoring the change in the output voltage. To minimize the voltage drop, use short, low resistance wires, especially for loads approaching maximum current. Figure 5 shows the buck load regulation performance of the ADP5040CP-1-EVALZ.

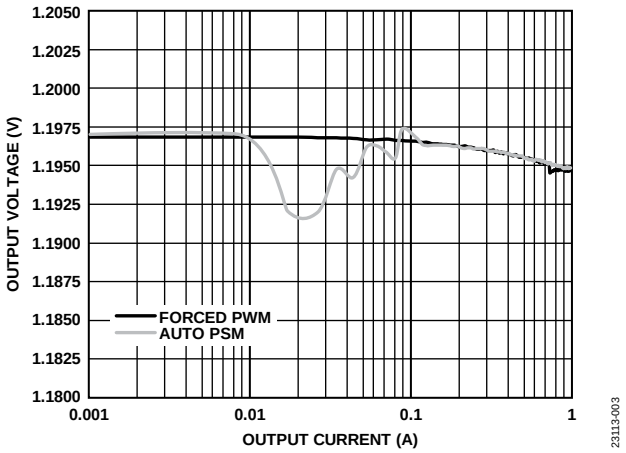

Figure 5. Buck Load Regulation

MEASURING THE LINE REGULATION

Vary the input voltage and examine the change in the output voltage. Figure 6 shows the buck line regulation performance of ADP5040CP-1-EVALZ for an output current of 500 mA.

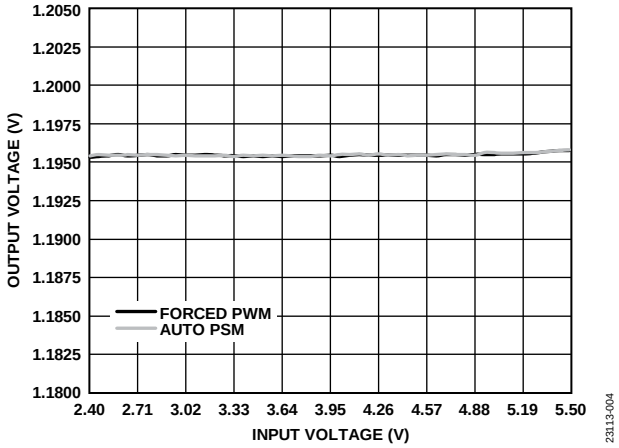

Figure 6. Buck Line Regulation

MEASURING THE EFFICIENCY

Measure the efficiency, η, by comparing the input power with the output power.

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}$$

To reduce the effect of current resistance (IR) drops, measure the input and output voltages as close as possible to the input and output capacitors.

MEASURING THE INDUCTOR CURRENT

To measure the ripple performance of the inductor current and check whether the performance meets the saturation current specification, desolder one end of Inductor L1 from its pad and connect a piece of wire in series with L1. A current probe can be connected on this wire.

LINE REGULATION OF LDO REGULATOR

For line regulation measurements, the output of the regulator is monitored while its input voltage is varied. To ensure that the LDO regulator is not in dropout mode during this measurement, the input voltage of the LDO regulator must be varied between its nominal output voltage plus 0.5 V and its maximum input voltage. For example, the input voltage of an LDO regulator with a fixed 3.3 V output must be varied between 3.8 V and 5.5 V. This measurement can be repeated under different load conditions. Figure 7 and Figure 8 show the line regulation performance of LDO1 and LDO2 with a fixed 1.8 V and 3.3 V output, respectively, for an output current of 150 mA.

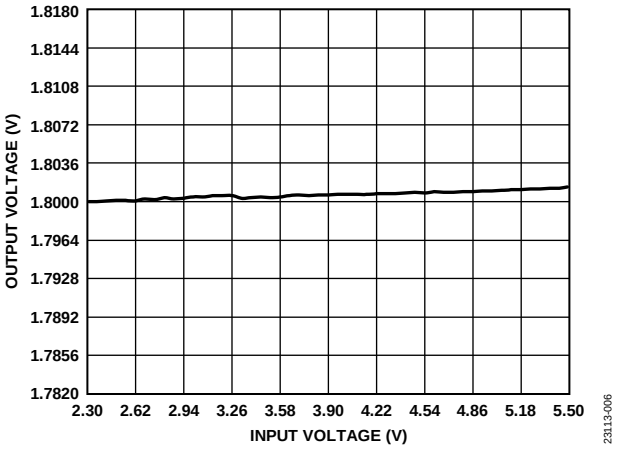

Figure 7. LDO1 Line Regulation, 1.8 V Output

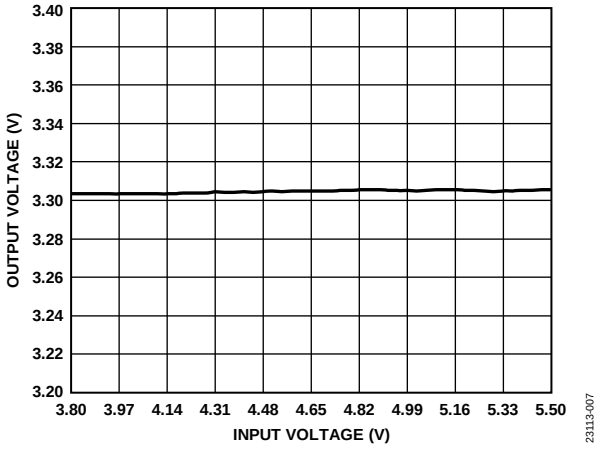

Figure 8. LDO2 Line Regulation, 3.3 V Output

LOAD REGULATION OF LDO REGULATOR

For load regulation measurements, the regulator output is monitored while the load is varied. The input voltage must remain constant during this measurement. The load current can be varied from 0 mA to 300 mA. Figure 9 and Figure 10 show the load regulation performance of LDO1 and LDO2 with a fixed 1.8 V and 3.3 V output, respectively, for an input voltage of 4.5 V.

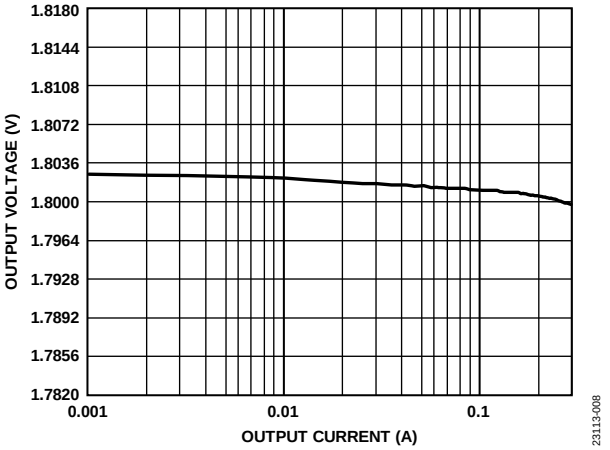

Figure 9. LDO1 Load Regulation, 1.8 V Output

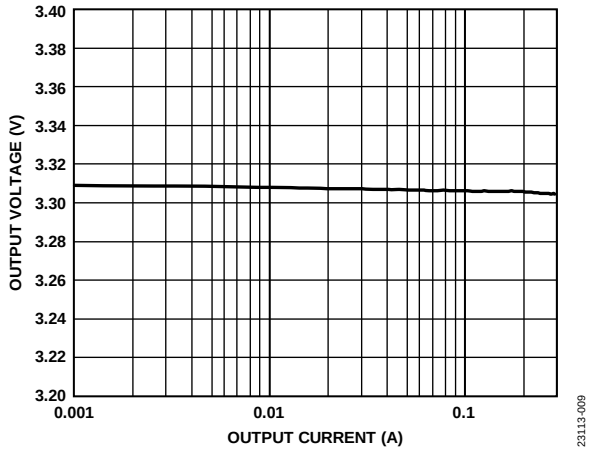

Figure 10. LDO2 Load Regulation, 3.3 V Output

OUTPUT VOLTAGE OPTIONS

The buck and LDO regulator output voltages are set through a resistor divider, as shown in Figure 11 and Figure 12, respectively. The voltage feedback of FB1, FB2, and FB3 (V_{FB1}, V_{FB2}, and V_{FB3}) are internally set to 0.5 V.

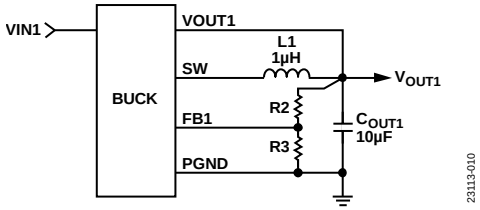

Figure 11. Buck Regulator Output Voltage Setting

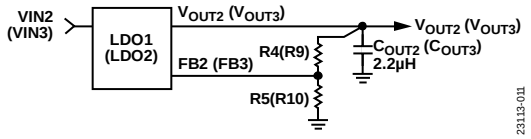

Figure 12. LDO Regulator Output Voltage Setting

To calculate the output setting for the buck regulator, calculate V_{OUT1} as follows:

$$V_{OUT1} = V_{FB1}\left(\frac{R2}{R3}+1\right)$$

To calculate the LDO output setting for LDO1, calculate V_{OUT2} as follows:

$$V_{OUT2} = V_{FB2}\left(\frac{R4}{R5}+1\right)$$

To calculate the LDO output setting for LDO2, calculate V_{OUT3} as follows:

$$V_{OUT3} = V_{FB3}\left(\frac{R9}{R10}+1\right)$$

The total resistance of R2 and R3 must not exceed 200 kΩ. The combination of other divider resistors such as R4 and R5, and R9 and R10 must also not exceed 200 kΩ.

EVALUATION BOARD SCHEMATIC AND ARTWORK

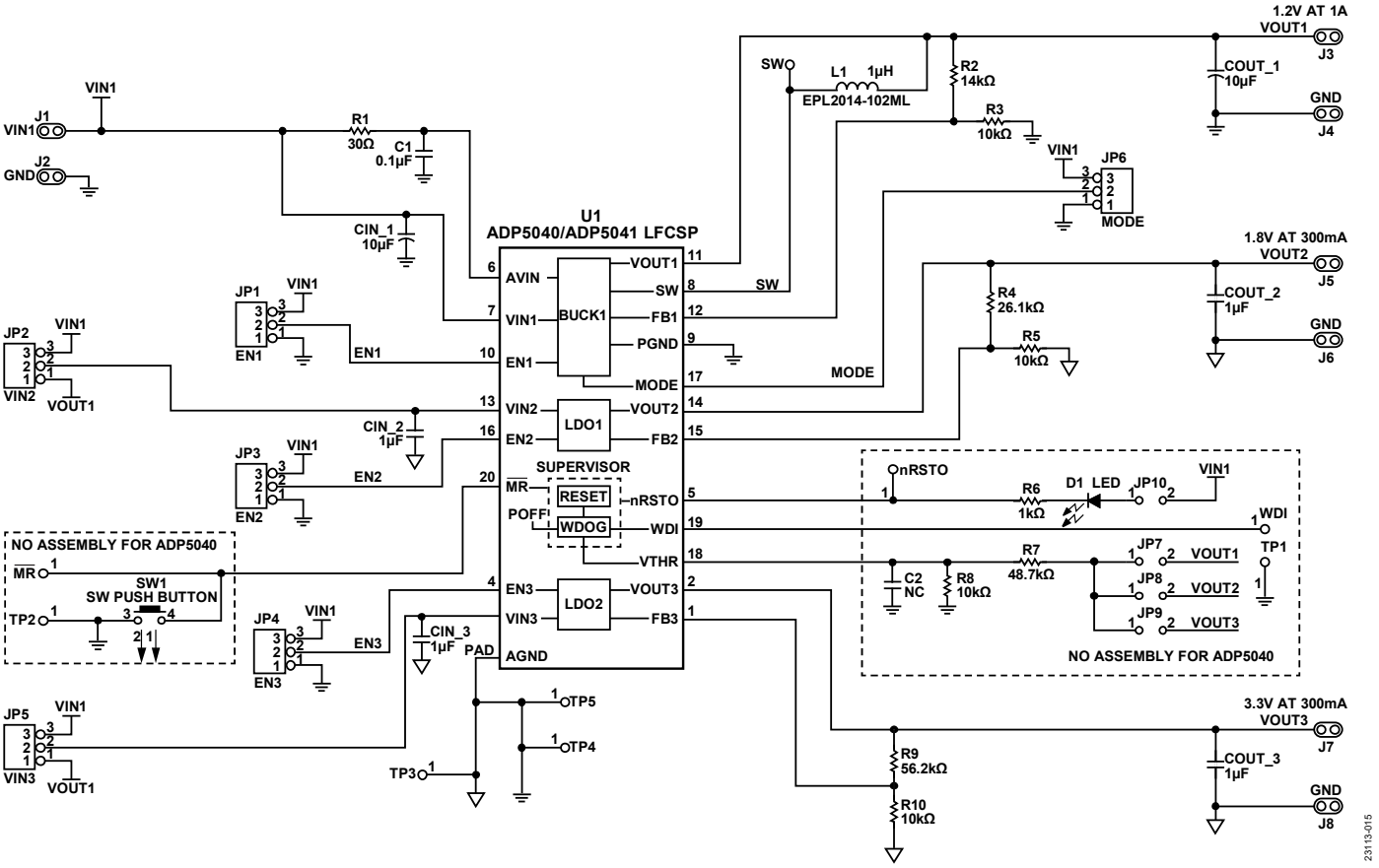

Figure 13. Evaluation Board Schematic of the ADP5040/ADP5041

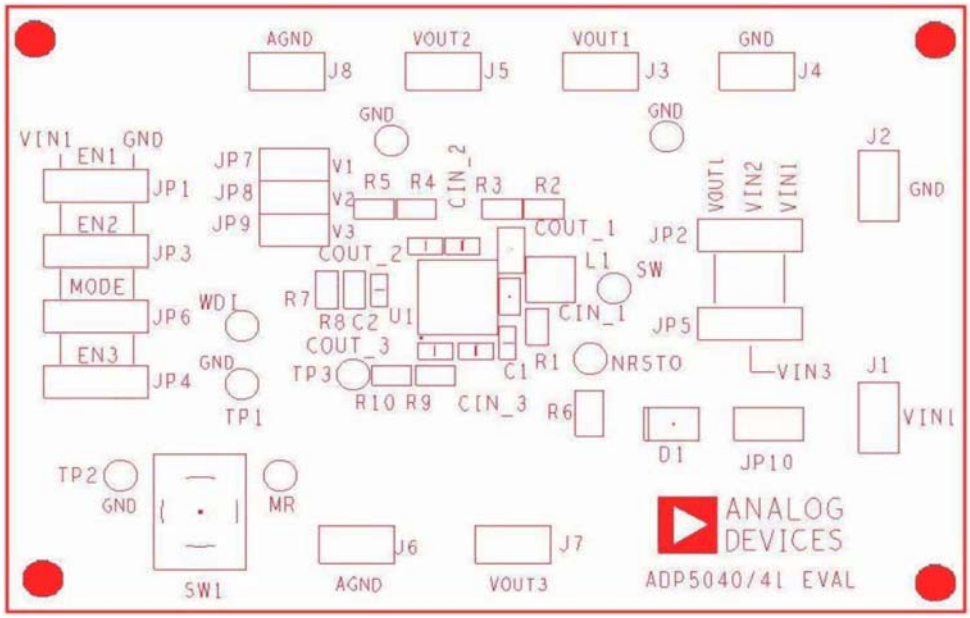

Figure 14. Recommended Layout, Top Layer

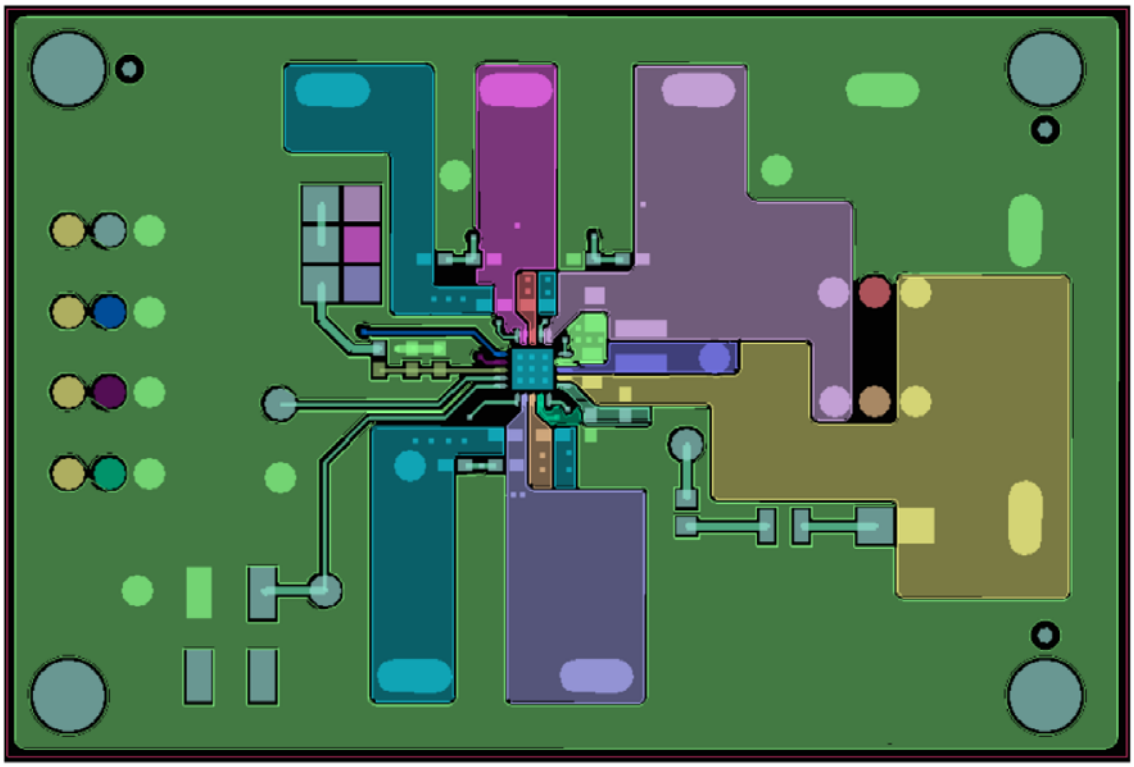

Figure 15. Recommended Layout, Layer 1

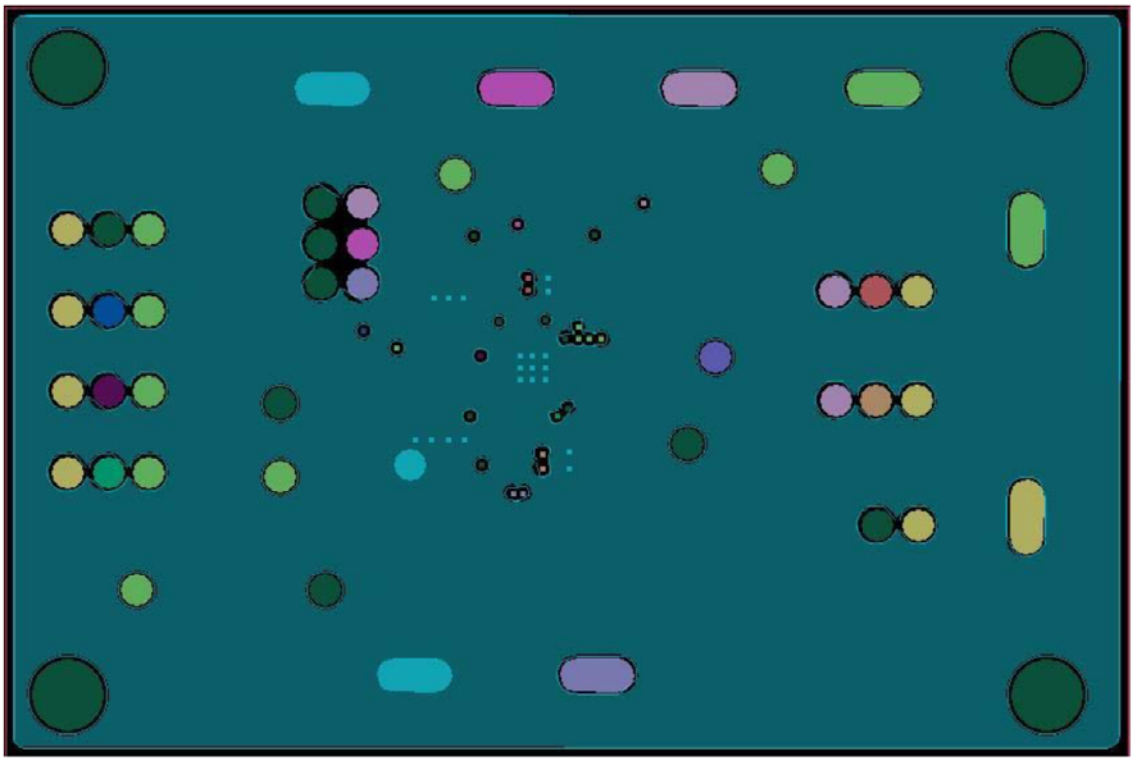

Figure 16. Recommended Layout, Layer 2, Ground Plane

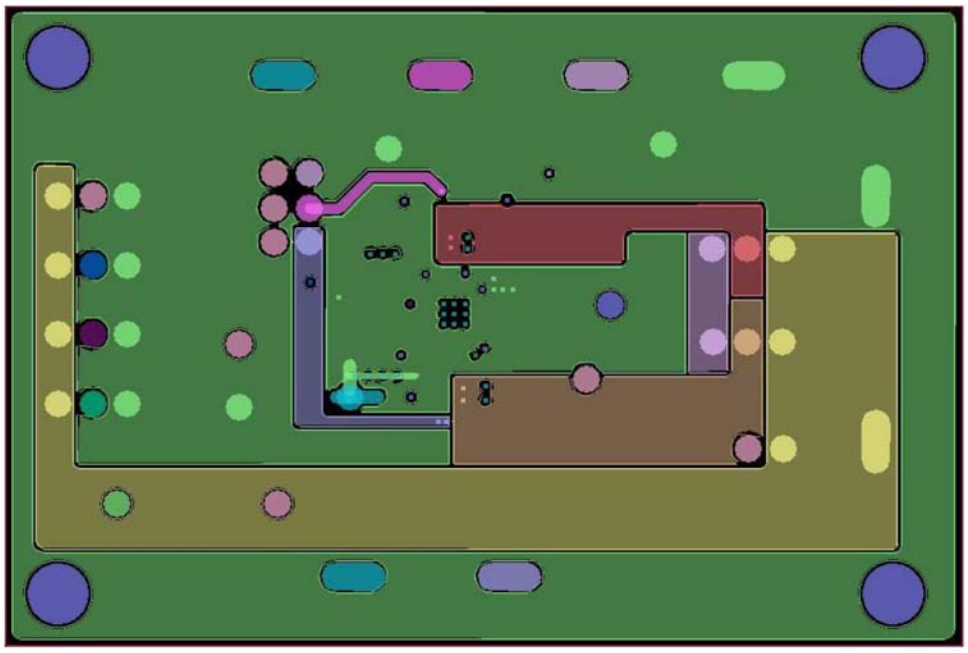

Figure 17. Recommended Layout, Layer 3

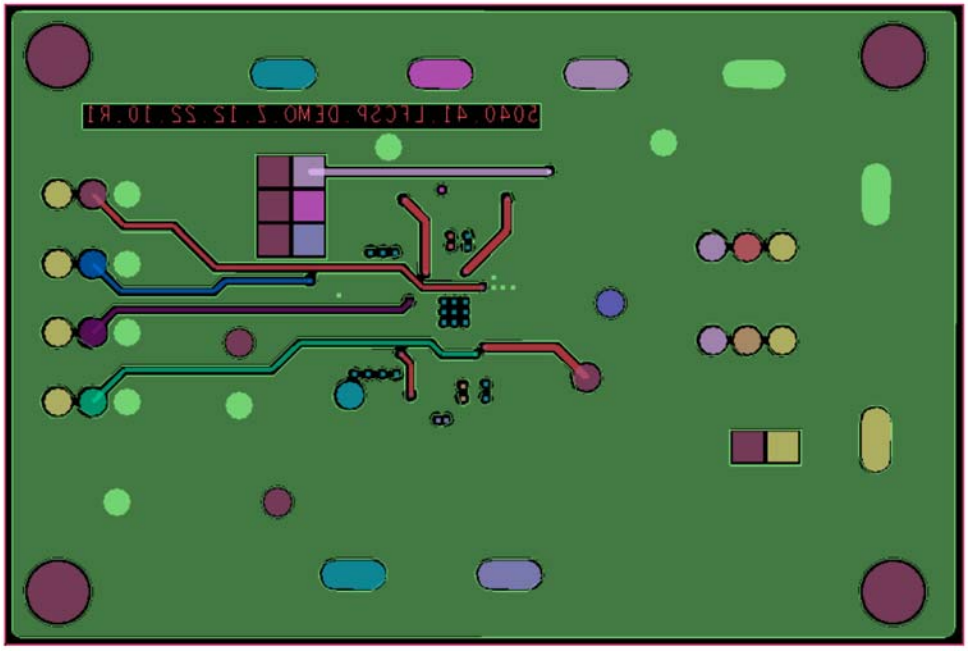

Figure 18. Recommended Layout, Layer 4

ORDERING INFORMATION

BILL OF MATERIALS

Table 6. Evaluation Board Components

Qty	Reference Designator	Description	PCB Footprint	Value	Part Number	Manufacturer
1	C1[1]	Capacitor, C0402	Not applicable	0.1 µF	JMK105B7104KV-F	Taiyo Yuden
1	C2[1]	Capacitor, C0402	Not applicable	N/A	Not applicable	Not applicable
1	CIN_1	Capacitor, C0805	Not applicable	10 µF	LMK212BJ106KG-T	Taiyo Yuden
4	CIN_2, CIN_3, COUT_2, COUT_3	Capacitor, C0402	Not applicable	1 µF	JMK105BJ105KV-F	Taiyo Yuden
1	COUT_1	Capacitor, C0603	Not applicable	10 µF	GRM188R60J106ME47D	Murata Electronics
1	D1[2]	LED, L0805	Not applicable	LED, red, 0805	SML-LXT0805IW-TR	Lumex
8	J1, J2, J3, J4, J5, J6, J7, J8	2-pin header	VIN1, GND, VOUT1, GND, VOUT2, GND, VOUT3, GND	Not applicable	TSW-102-07-S-S	Samtec
6	JP1, JP2, JP3, JP4, JP5, JP6	3-pin header	EN1, VIN2, EN2, EN3, VIN3, MODE	Not applicable	TSW-102-07-S-S	Samtec
4	JP7,[2] JP8,[2] JP9,[2] JP10[2]	2-pin header	JP7, JP8, JP9, JP10	Not applicable	TSW-102-07-S-S	Samtec
1	L1	Fixed inductor	L1	1 µH	LQM2MPN1R0	Murata
9	MR,[2] TP1,[2] TP2,[2] TP3, TP4, TP5, SW, WDI,[2] NRSTO[2]	1-pin header	MR, TP1/GND, TP2/GND, TP3, GND, SW, WDI, NRSTO	Not applicable	5-146280-1	TE Connectivity
1	R1	Resistor	R0402	30 Ω	CRCW040230R0FKED	Vishay
1	R2[3]	Resistor	R0402	14 kΩ	CRCW040214K0FKED	Vishay
1	R3[3]	Resistor	R0402	10 kΩ	CRCW040210K0FKED	Vishay
1	R4[3]	Resistor	R0402	26.1 kΩ	CRCW040226K1FKED	Vishay
1	R5[3]	Resistor	R0402	10 kΩ	CRCW040210K0FKED	Vishay
1	R6[2]	Resistor	R0402	1 kΩ	CRCW04021K00FKED	Vishay
1	R7[2, 3]	Resistor	R0402	48.7 kΩ	CRCW040248K7FKED	Vishay
1	R8[2, 3]	Resistor	R0402	10 kΩ	CRCW040210K0FKED	Vishay
1	R9[3]	Resistor	R0402	56.2 kΩ	CRCW040256K2FKED	Vishay
1	R10[3]	Resistor	R0402	10 kΩ	CRCW040210K0FKED	Vishay
1	SW1[2]	Push-button	SW1	Not applicable	KT11P3JM	C&K Components
1	U1	ADP5040 or ADP5041 LFCSP	QFN20_4X4_PAD2_6X2_6	Not applicable	ADP5040ACPZ-1-R7/ ADP5041ACPZ-1-R7	Analog Devices

[1] No assembly.
[2] No assembly for the ADP5040 only.
[3] 1% tolerance.

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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