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Electric Vehicle Warning Sound System User Guide

FEATURES

ADSP-BF706 Blackfin processor
- **88-lead QFN package**
- **24.576 MHz input clock (CLKIN) oscillator**

Quad SPI
- **256 Mb serial flash memory**

USB to UART interface bridge
Controller area network
Debug interface
- **JTAG header for use with Analog Devices, Inc., emulators**

Four LEDs
- **One power (green), one board reset (red), one hardware fault (red), and one general-purpose (yellow)**

Two push-buttons
- **One reset and one IRQ/flag**

Class A/B audio power amplifier
- **High efficiency, digital input, automotive quad power amplifier with built in diagnostics features**
- **Single, 12 V power supply with 42 V quad, monolithic, synchronous step-down regulator**

EVALUATION KIT CONTENTS

ADSP-BF706 Blackfin processor
USB Mini Connector

ADDITIONAL HARDWARE REQUIRED

ICE-1000 or ICE-2000 emulator

ADDITIONAL SOFTWARE REQUIRED

CrossCore Embedded Studio

GENERAL DESCRIPTION

The ADSP-BF706 Blackfin® processor combines a dual-MAC signal processing engine, the advantages of a clean, orthogonal microprocessor instruction set (similar to instruction sets for reduced instruction set computer (RISC) processors), and single instruction, multiple data (SIMD) multimedia capabilities into a single instruction set architecture. Enhancements to the Blackfin+™ core add 32-bit MAC and 16-bit complex MAC support, cache enhancements, branch prediction and other instruction set improvements, while simultaneously maintaining the instruction set compatibility for previous versions of Blackfin products. The electric vehicle warning sound system (EVWSS) demo system is used in conjunction with the CrossCore® Embedded Studio (CCES) development tools to test the capabilities of the ADSP-BF706 Blackfin processor.

EVALUATION BOARD PHOTO

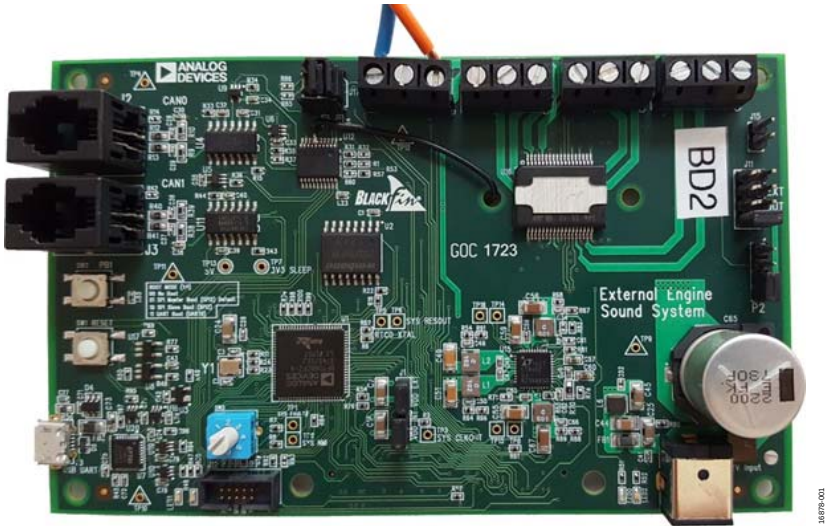

Figure 1.

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REVISION HISTORY

12/2018—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The EVWSS demo system is designed to run as a standalone unit.

When removing the EVWSS demo system from the package, handle the board carefully to avoid the discharge of static electricity, which can damage some components.

Figure 2 shows the default jumper settings and boot mode switch used in installation. Confirm that the board is in the default configuration before use.

HARDWARE INSTALLATION

Install and run the CCES software on the PC.

To connect an emulator to the EVWSS demo system, take the following steps:

1. Plug one side of the included Mini USB cable into the USB connector port of the emulator. Plug the other side of the cable into a USB port on the PC.
2. The status LED is green when the connection with the PC is working and the proper Windows® driver is installed. Refer to the ICE-1000 or ICE-2000 emulator user guide if the status LED does not illuminate.
3. Attach the emulator header (J2) on the bottom of the ICE-1000 or ICE-2000 to the J12 connector on the EVWSS demo system.
4. Attach a 12 V power supply and appropriate plug to the 12 V power adapter.
   a. Plug the jack of the assembled power adapter into the J14 power connector (12 V input) on the EVWSS demo system.
   b. Plug the other end of the power adapter into a power outlet. The power LED (LED2) is green when power is applied to the board.

POWER SUPPLIES

The EVWSS demo system uses an audio power amplifier that can draw high current. It is recommended to use a 12 V power supply, such as the GST90A12-P1M (12 V, 6.67 A, and 80 W), and a 2.5 mm × 5.5 mm plug.

SPI FLASH

The ADSP-BF706 processor has three serial peripheral interfaces (SPIs): SPI0, SPI1, and SPI2. SPI2 is connected to a Winbond W25Q256/SO16, 256 Mb, serial flash memory with dual-SPI and quad-SPI support. This flash is used for booting, sound file storage, and scratchpad space.

Quad mode is enabled by default. The processor flag signals, PB_15 ($\overline{\text{SPI2\_SEL1}}$), PB_13 (SPI2_D2), and PB_14 (SPI2_D3) are straight connected.

UART INTERFACE

The ADSP-BF706 processor has two built in universal asynchronous transmitters (UARTs). UART0 is connected to a USB to UART converter IC (FT232RQ).

The UART functionality must be enabled through the SoftConfig. Refer to the Software-Controlled (SoftConfig) Switches section for details.

The EVWSS warning sound application configures the SoftConfig switch to enable the UART interface.

CAN0 INTERFACE

The Controller Area Network 0 (CAN0) interface of the EVWSS demo system is connected to the CAN transceiver (TJA1041). The transceiver is attached to the CAN0 port of the ADSP-BF706 processor via the J2 connector.

The CAN0 transmit, receive, and error signals are connected through the SoftConfig switches and disabled by default. CAN0_EN is enabled by default and #CAN0_STB is disabled. See the Software-Controlled (SoftConfig) Switches section for details.

CAN1 INTERFACE

The Controller Area Network 1 (CAN1) interface of the EVWSS demo system is connected to the TJA1041 CAN transceiver. The transceiver is attached to the CAN1 port of the ADSP-BF706 processor via the J3 connector.

The CAN1 signals are straight connected and do not require configuration by the SoftConfig switches.

DEBUG INTERFACE

The EVWSS demo system provides a 0.05 inch pitch header JTAG/SWD/SWO connection via the J12 connector. See the JTAG/SWD/SWO Connector (J12) section for details.

EXPANSION INTERFACE

The expansion interface allows the testing of a custom design daughter board across various hardware platforms that have the same expansion interface.

The Expansion Interface 3 (EI3) is implemented on the EVWSS demo system and consists of a single connector, J4. This connector contains a majority of the signals of the processor. For details, see the Evaluation Board Schematic section.

When using the expansion interface, consider the limits to the current and interface speed. The current for the extenders that are connected to the EI3 connectors can be sourced from the EVWSS demo system. Therefore, the current must be limited to 250 mA for the 5 V planes, and 300 mA for the 3.3 V planes. If a greater current is required, a design a separate power connector and a regulator on the daughter board. Implementing additional circuitry on the daughter boards can add extra loading to signals, which decreases the maximum effective speed of these cards. Note that Analog Devices does not support and is not responsible for the effects of additional circuitry.

POWER ARCHITECTURE

The EVWSS demo system has four primary voltage levels: 12 V, 5 V, 3.3 V, and 1.1 V. The power input of the system is a 12 V wall adapter.

The Analog Devices LT8602 42 V, quad, monolithic step-down regulator provides the voltage levels for the 12 V input, the VDD_EXT signal (3.3 V) and the 3.3 V power requirements of the board, the VDD_INT signal (1.1 V), and the voltage for the CAN interface supply (5 V).

The audio power amplifier (U16) is supplied directly by the 12 V input.

Voltage levels can be measured for VDD_INT (J13), and VDD_EXT (J1). Current consumption of the power rail can be measured when the corresponding jumpers are removed.

EVWSS DEMO SYSTEM

See the EVWSS product page and request the ADSP-BF706 code. A how-to start guide is included with the software package.

REFERENCE DESIGN INFORMATION

The reference design information package is available for download from the EVWSS product page. The package provides information on the design, layout, fabrication, and assembly of the EVWSS demo system.

SYSTEM ARCHITECTURE

This section describes the EVWSS demo system configuration (see Figure 2).

The EVWSS demo system demonstrates the capabilities of the ADSP-BF706 processor. The EVWSS demo system has an audio-friendly, 24.576 MHz input clock.

The user input and output to the processor is provided in the form of one user push-button and three LEDs. The software-controlled (SoftConfig) switches facilitate the switch multifunctionality by disconnecting the push-button from the associated processor pins and reusing the processor pins elsewhere on the board. See the Evaluation Board Schematic section for details.

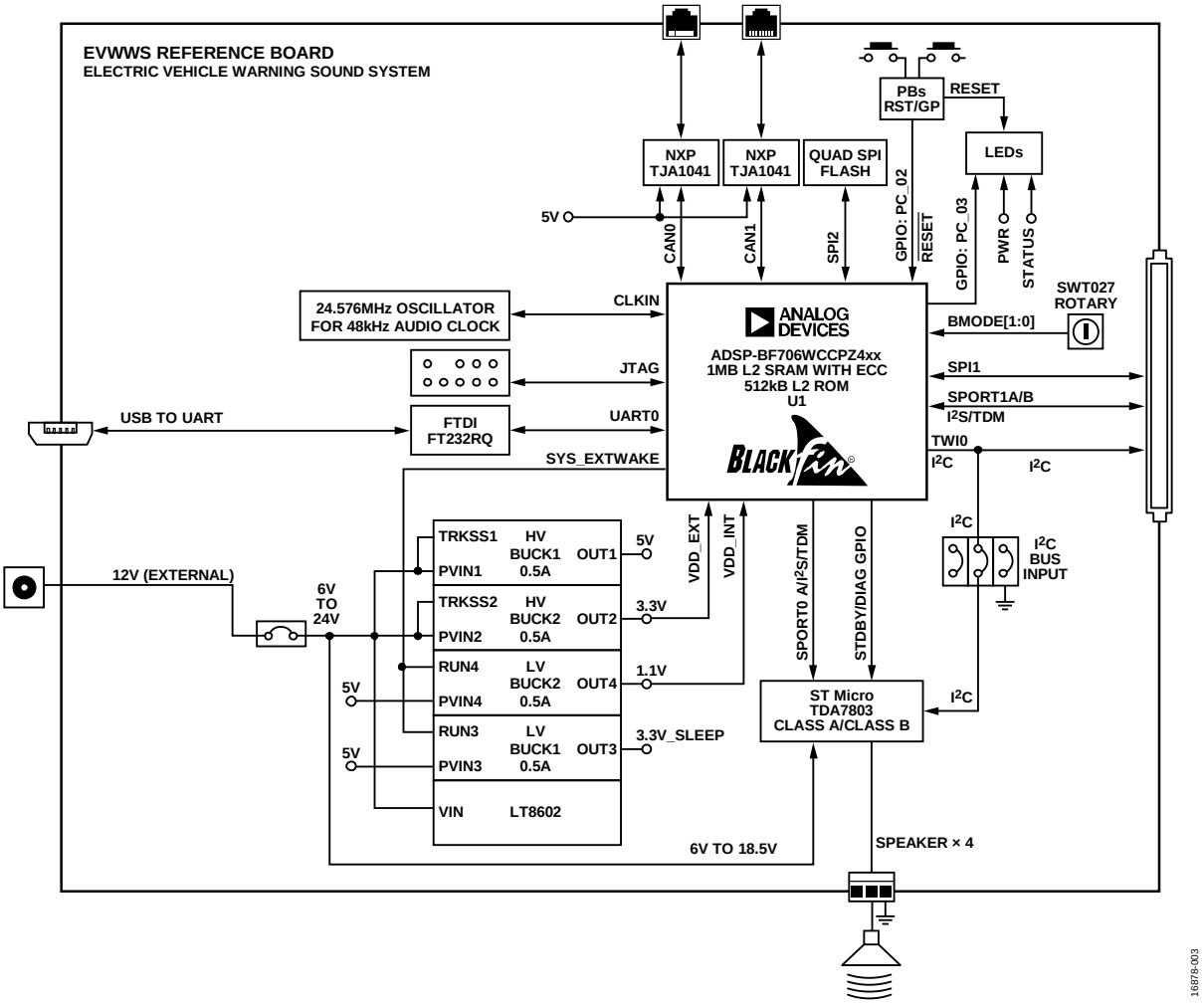

Figure 2. EVWSS Demo Block Diagram

SOFTWARE-CONTROLLED (SOFTCONFIG) SWITCHES

Most of the traditional mechanical switches on the EVWSS demo system are replaced by an I²C software-controlled switch. The remaining mechanical switches are provided for the boot mode, push-buttons, and controlling modes of the audio power amplifier.

This section of the user guide serves as a reference to modify an existing software example. If the firmware provided from Analog Devices is used, there is little need to reference this section.

Programming SoftConfig Switches

The EVWSS demo system contains an 8-bit, general-purpose, parallel input/output IC (MCP23008) with the following programming characteristics:

- A switch with one programmable general-purpose input/output (GPIO) register (Address 0x09).
- A GPIO register with control of eight signals.
- By default, the MCP23008 GPIO signals function as input signals. The signals must be programmed as output signals to override their default values. The EVWSS programs the SoftConfig switch.

PUSH-BUTTONS AND SWITCHES

This section describes operation of the push-buttons and switches (see Figure 3).

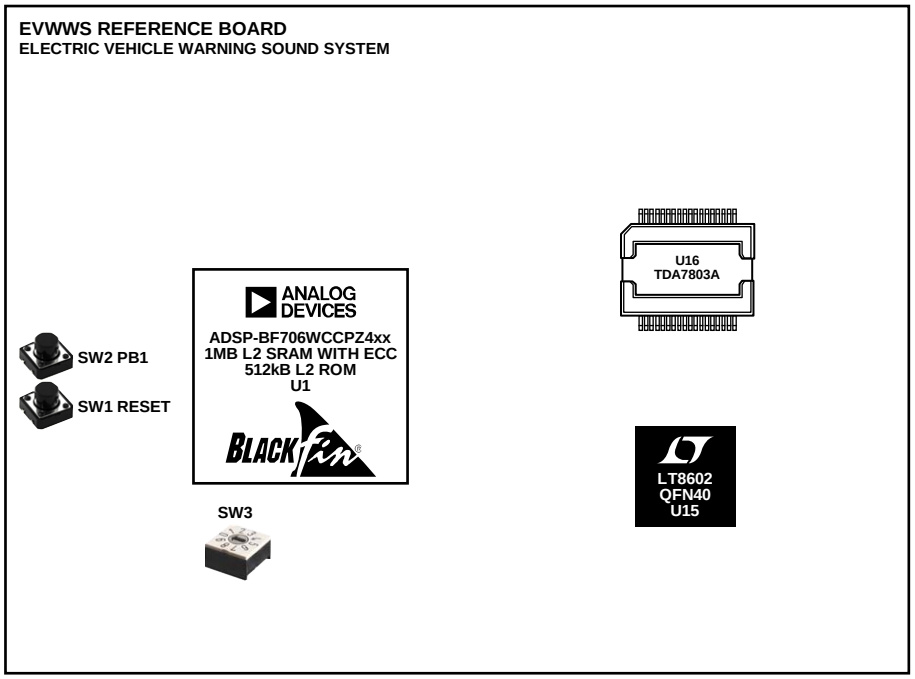

Figure 3. Push-Button and Boot Mode Switch Locations

Reset Push-Button (SW1)

The reset push button (SW1) resets the processor (U1), SoftConfig switch (U12), and SPI flash (U4) ICs. The reset push-button also is connected to the expansion interface (J4) via the SYS_HWRST signal.

GPIO Push-Button (SW2)

The GPIO push button (SW2) are connected to the PA_15/ EPPI0_FS3/SPT0_ATDV/SPT0_BTDV/SPT0_BTDV/CNT0_UD signal of the ADSP-BF706 processor, and the signal is connected by default.

Boot Mode Select Switch (SW3)

The rotary switch (SW3) determines the boot mode of the processor. Table 1 describes the available boot mode settings. By default, the ADSP-BF706 processor boots from the SPI flash memory.

Table 1. Boot Mode Select Switch (SW3)

SW3 Position	Processor Boot Mode
0	No boot, idle.
1	SPI master boot mode (SP12). Default boot mode.
2	SPI slave boot (SPI2).
3	UART boot (UART0).

JUMPERS

This section describes functionality of the configuration jumpers (see Figure 4).

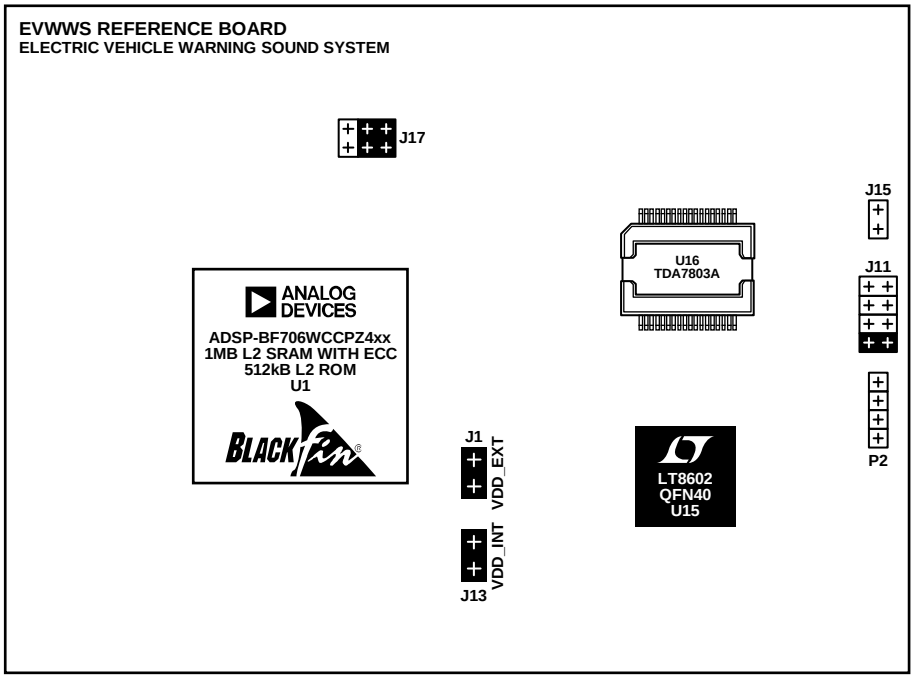

Figure 4. Jumper Locations

Table 2. Power Jumpers

Parameter	Processor Boot Mode
J1	Connects VDD_EXT signal to the processor.
J13	Connects VDD_INT signal to the processor.

Table 3. Mode Configuration Jumpers

Mode	Value
J11	Header used to configure the TDA7803A audio power amplifier.
J11.1	Insert.
J11.2	Remove.
J11.3	Remove.
J11.4	Remove.
J15	Insert to mute the power amplifier. Removed by default.
J17	Header can be used to directly program the audio power amplifier with the respective I^2C programmer device. Inserted by default.
J17.1	Connects the SCL power amplifier signal to the I^2C network or processor of the board. Inserted by default.
J17.2	Connects the SDA power amplifier to the I^2C network or processor of the board. Inserted by default.
J17.3	Ground. Removed by default.
P2	Remove.

LEDS

This section describes the on-board LEDs (see Figure 5).

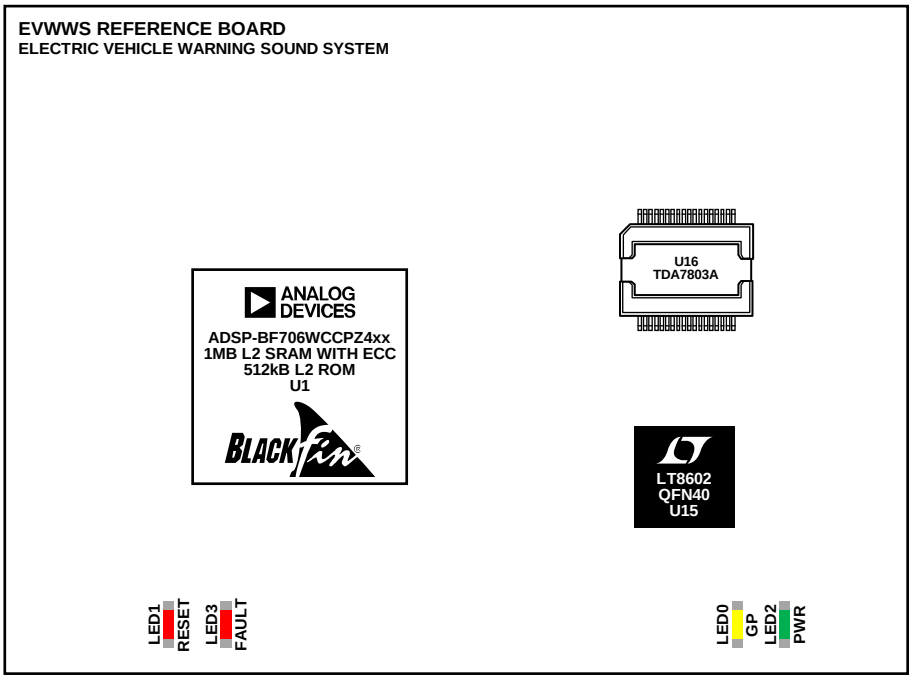

Figure 5. LED Locations

GPIO LED (LED0)

LED0 is connected to the GPIO pins of the processor. The LED is active high and can be illuminated (yellow) by writing a 1 to the correct processor signal.

Reset LED (LED1)

When LED1 illuminates red, the master reset of all the major ICs is active. LED1 is controlled by the ADM6315 supervisory reset circuit. The TARGET_RESET signal is driven from an emulator. EI3 extender cards can also drive a reset as an input to this reset circuit. Press the SW2 switch to perform a master reset and activate LED1. For more information, see the Reset Push-Button (SW1) section.

Power LED (LED2)

When LED2 illuminates green, power is being properly supplied to the board. For more information, see the Power Architecture section.

SYS_FAULT LED (LED3)

When LED3 (SYS_FAULT LED) illuminates red, a system fault has occurred. For more information, refer to the ADSP-BF70x Blackfin+ Processor Hardware Reference Manual.

CONNECTORS

This section describes connector functionality and provides information about mating connectors. The connector locations are shown in Figure 6.

Connectors located on the back of the board are noted with dotted lines in Figure 6.

EI3 Connector (J4)

One board-to-board connector (J4) provides signals from the SPI, two-wire interface (TWI), UART, SPORT, and GPIO interfaces of the processor. The connectors are located on the back of the board.

For more information, see the Expansion Interface section.

JTAG/SWD/SWO Connector (J12)

The JTAG/SWD/SWO header (J12) provides debug connectivity for the processor in the form of 0.05 inch, shrouded, through-hole connector (SHF-105-01-L-D-TH). This connector mates with the ICE-1000 and ICE-2000 emulators, or any future Analog Devices emulators. For more information, see the Expansion Interface section.

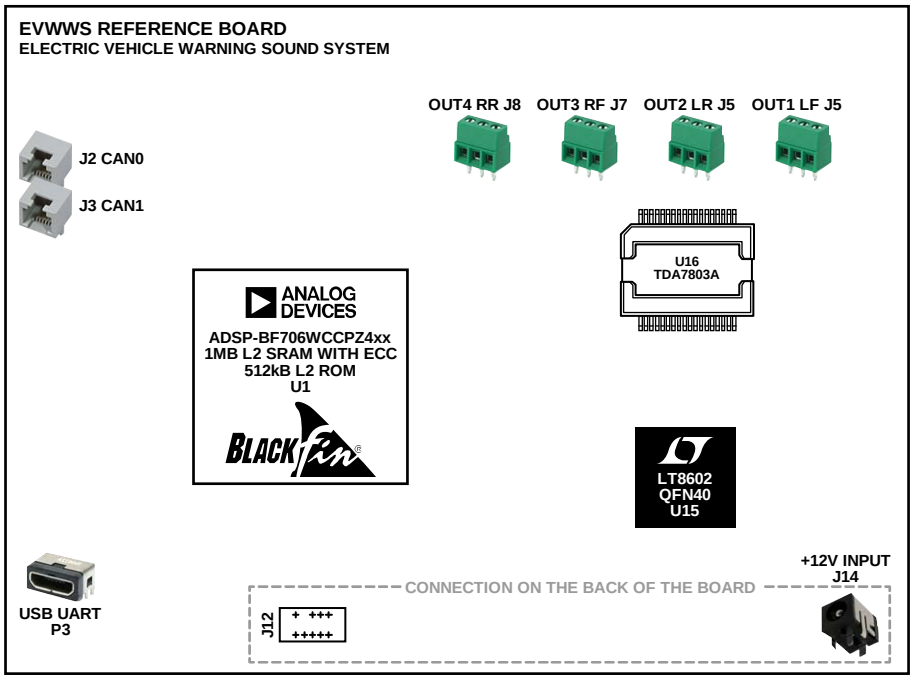

Figure 6. Connector Locations

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

For full details, refer to the *EVWSS Software Architecture Design* manual, which is included in the EVWSS software files.

Ensure that the CCES software is installed and running on the PC.

1. Navigate to the CCES software via the **Start** menu. Note that the CCES software is not connected to the board.
   a. Use the **Debug Configurations Wizard** to connect to the EVWSS demo system. If a debug configuration already exists, select the appropriate configuration and click **Debug**, and then proceed to Step 8. To create a debug configuration, click the down arrow next to the bug icon, select **Debug Configurations** > **Run** > **Debug Configurations**. The **Debug Configuration** dialog box appears.
2. Select **CrossCore Embedded Studio Application** and click **(New launch configuration)**. The **Select Processor** pane of the **Session Wizard** appears.
3. Ensure that **Blackfin** is selected in **Processor family** pane. In the **Processor type** pane, select **ADSP-BF706**, and then click **Next**. The **Select Connection Type** pane of the **Session Wizard** appears.
4. Select **Emulator** and click **Next**. The **Select Platform** pane of the **Session Wizard** appears.
5. From this pane, select the type of emulator that is connected to the EVWSS demo system, and click **Finish** to close the wizard. The new debug configuration is created and added to the **Debug Configurations** list.
6. In the **Name edit** box, users enter an appropriate name to describe the configuration, otherwise a default name is provided.
7. In the **Program(s) to load** pane, select the program to load if the appropriate program is not already populated when connecting to the board. Do not make changes if there is no need to load any program when connected to the board.

Note that when connected to the board, it is not possible to choose a program to download. To load a program when connected to the board, terminate the session and then load the new program.

To delete a configuration, navigate to the delete box, indicated by a red cross, and select the configuration to delete. Click **Close** and select **Yes** in the **Debug Configurations** dialog box when asked if the user wishes to delete the selected launch configuration, and then close the dialog box.

To disconnect from the board, click the terminate icon or choose **Run** > **Terminate**.

To delete a session, select **Target** > **Session** > **Session List**. Select the session name from the list, click **Delete**, and then click **OK**.

The default configurations that appear in the CCES **Debug Configurations Wizard** are for JTAG mode debugging only. To use SWD mode, create a new platform with the **Target Configurator**.

EVALUATION LICENSE

When running the CCES software for the first time, the user is prompted to install either a 90-day evaluation license or a permanent, full license. To automatically install an unrestricted, 90-day evaluation license, select **I do not have a serial number and would like to evaluate the product**. If the evaluation license is installed but not activated, the license allows 10 days of unrestricted use and then is disabled. The license can be re-enabled by activation. When the license is activated, the evaluation license offers 90 days of unrestricted use and then is permanently disabled.

An evaluation license can be upgraded to a full license by purchase from Analog Devices.

Note that the EVWSS demo hardware must be connected and powered up to use the CCES software with a valid evaluation license or full license.

EVALUATION BOARD SCHEMATIC

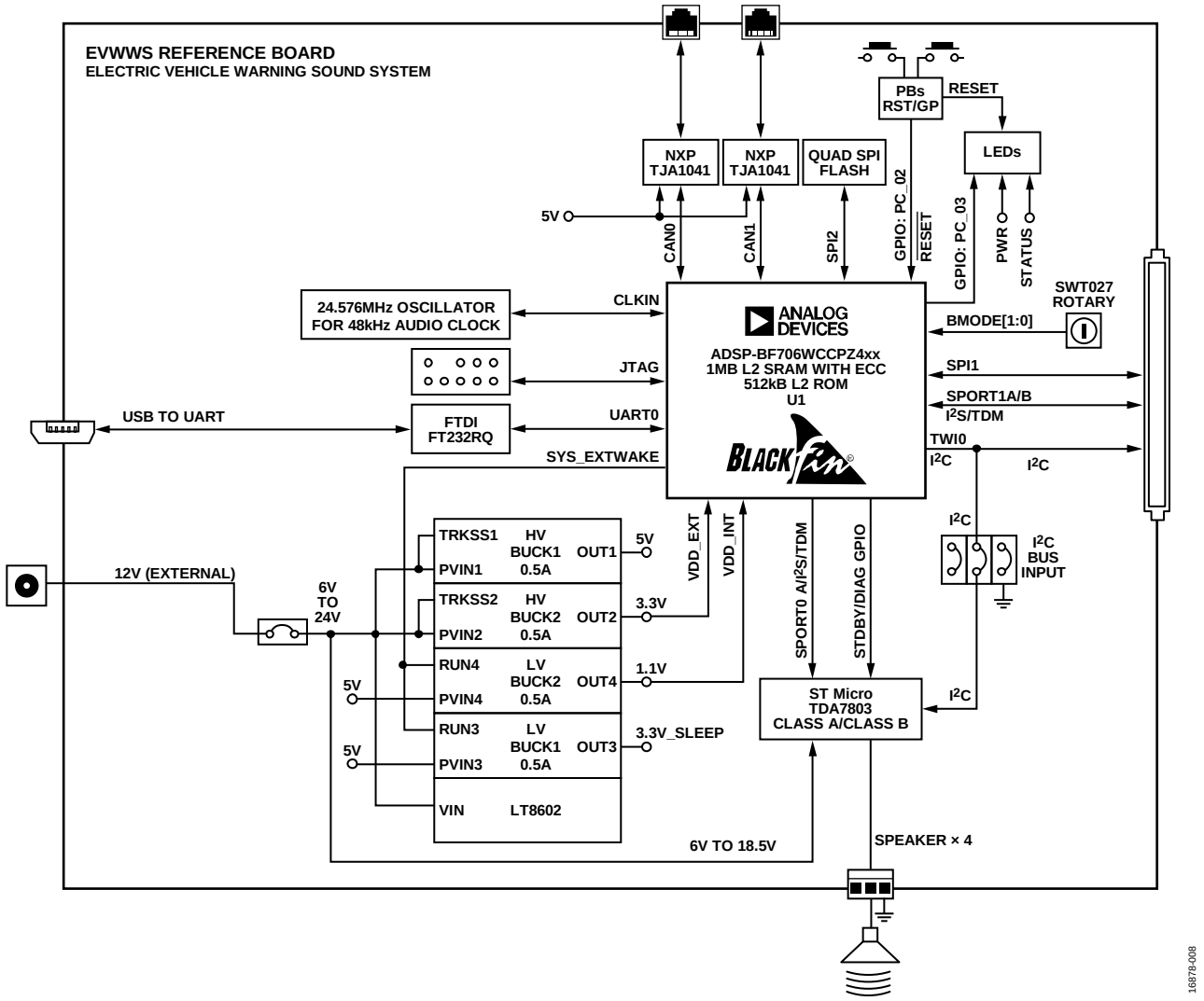

Figure 7.

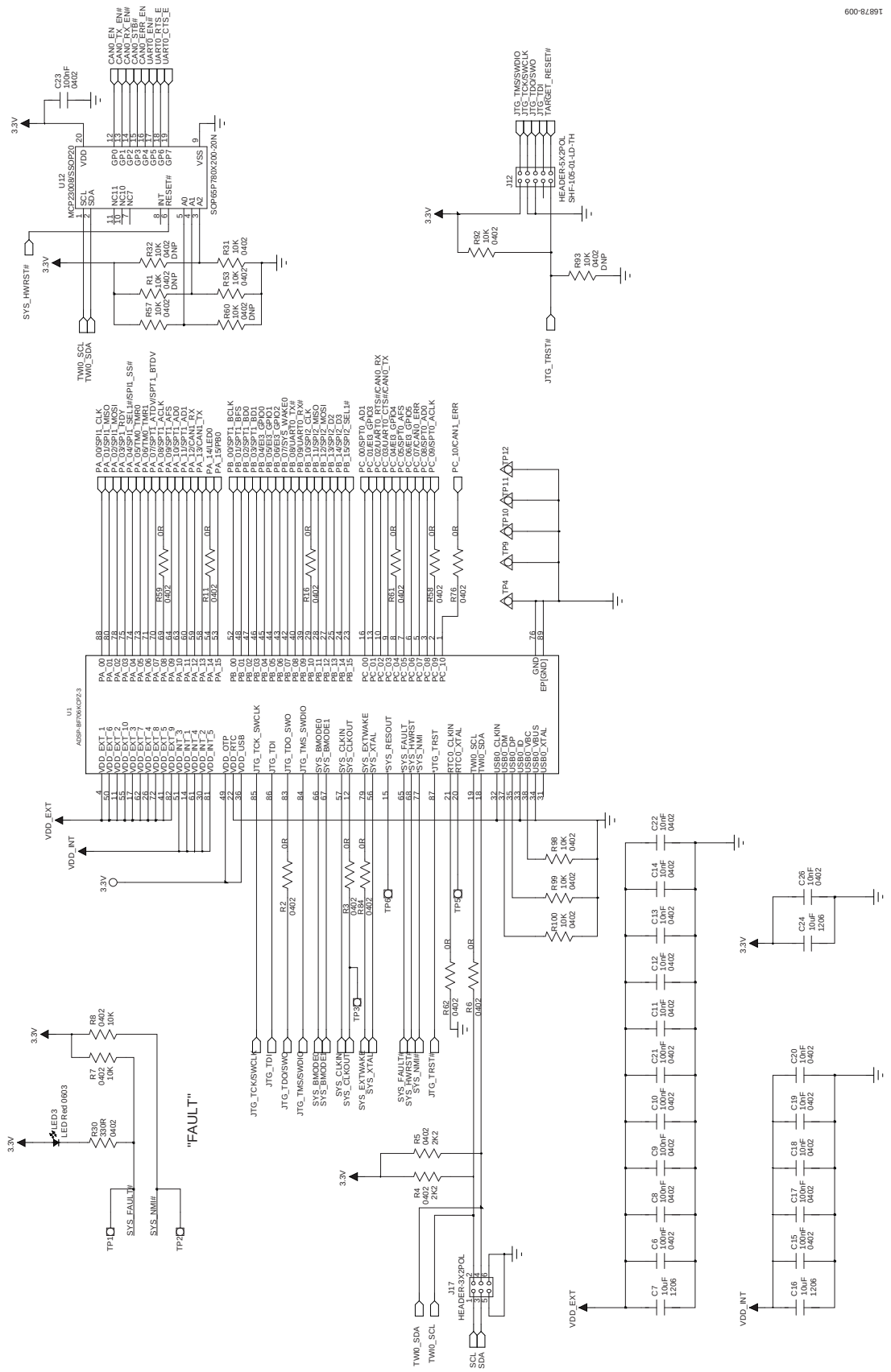

Figure 8. Processor Schematic

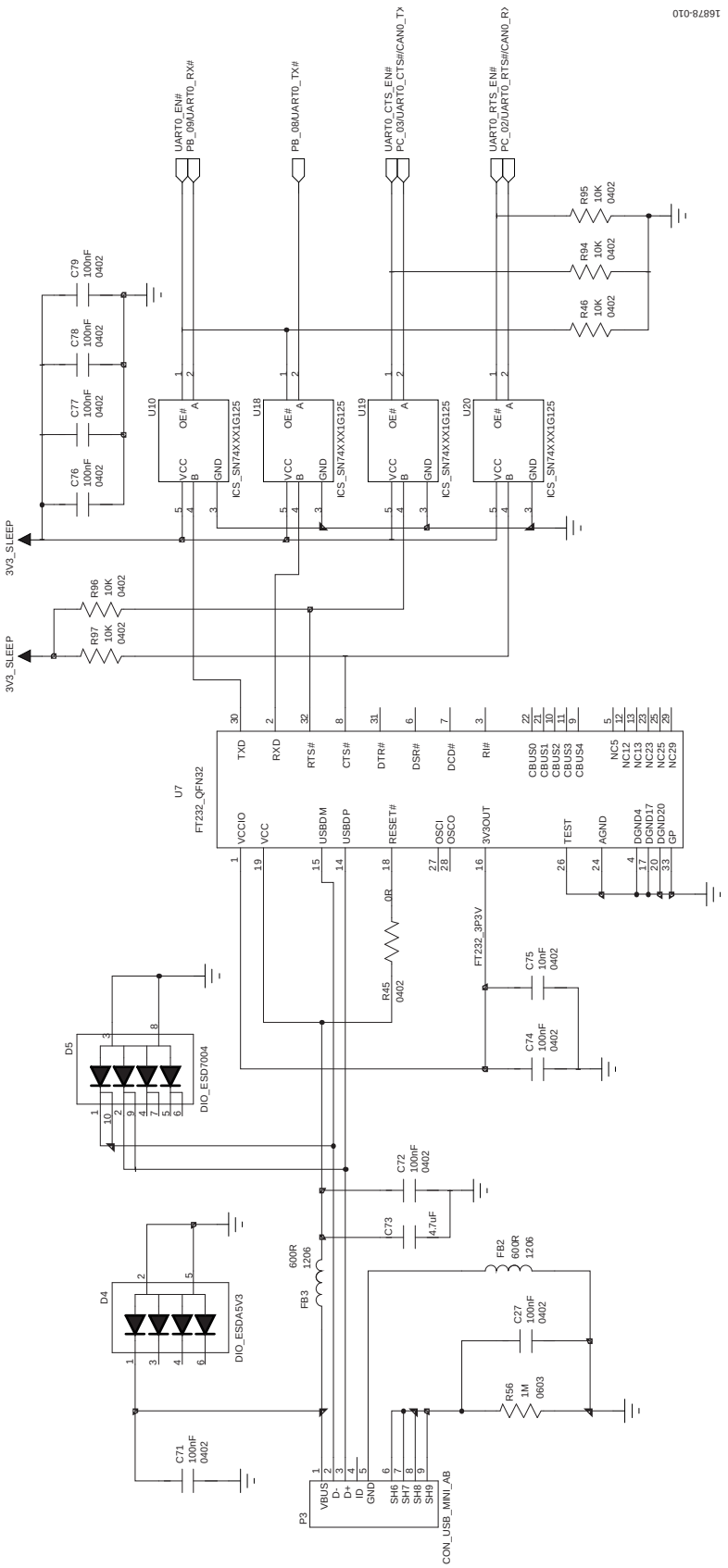

Figure 9. USB/UART Schematic

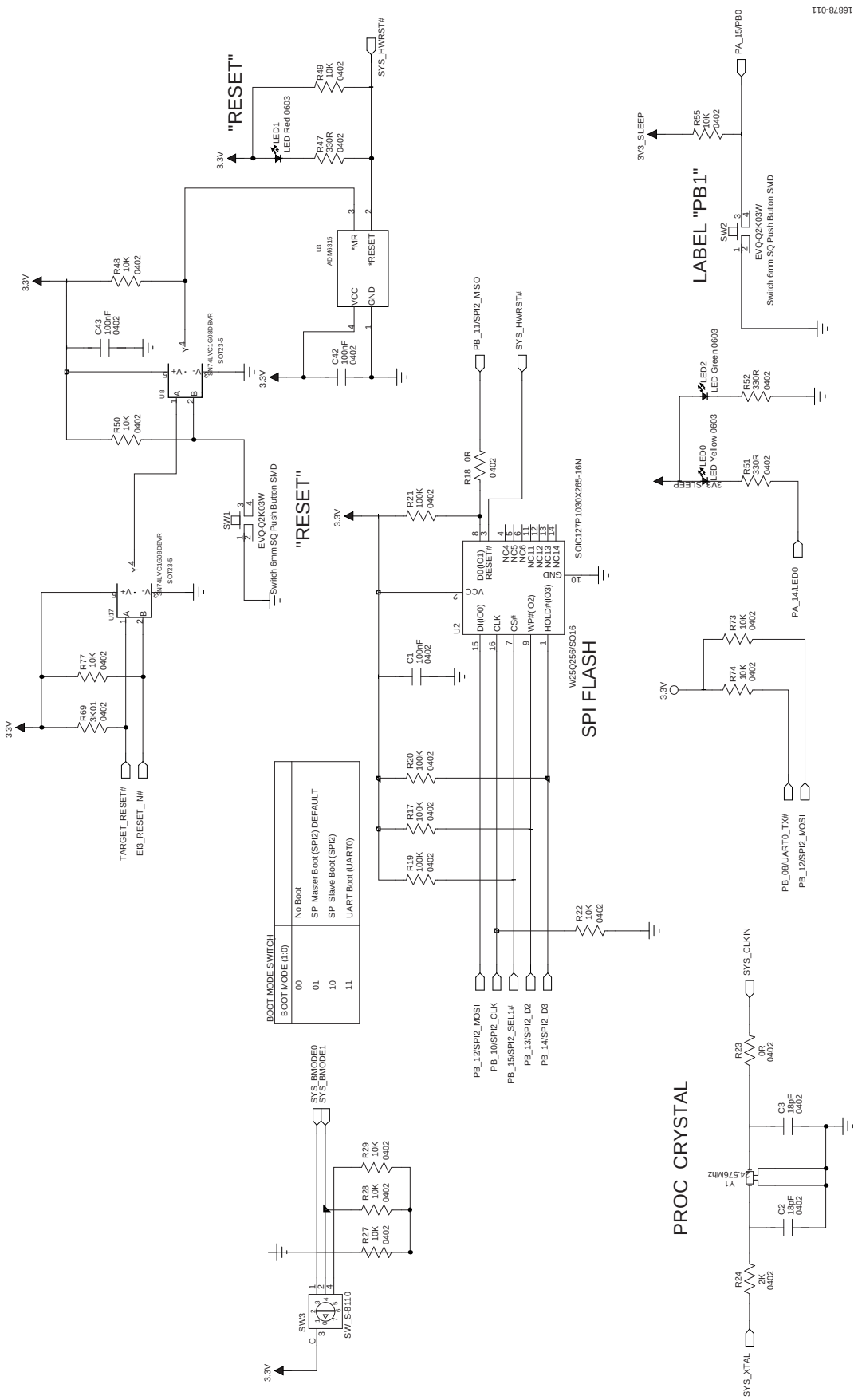

Figure 10. Clock/Reset/Memory Schematic

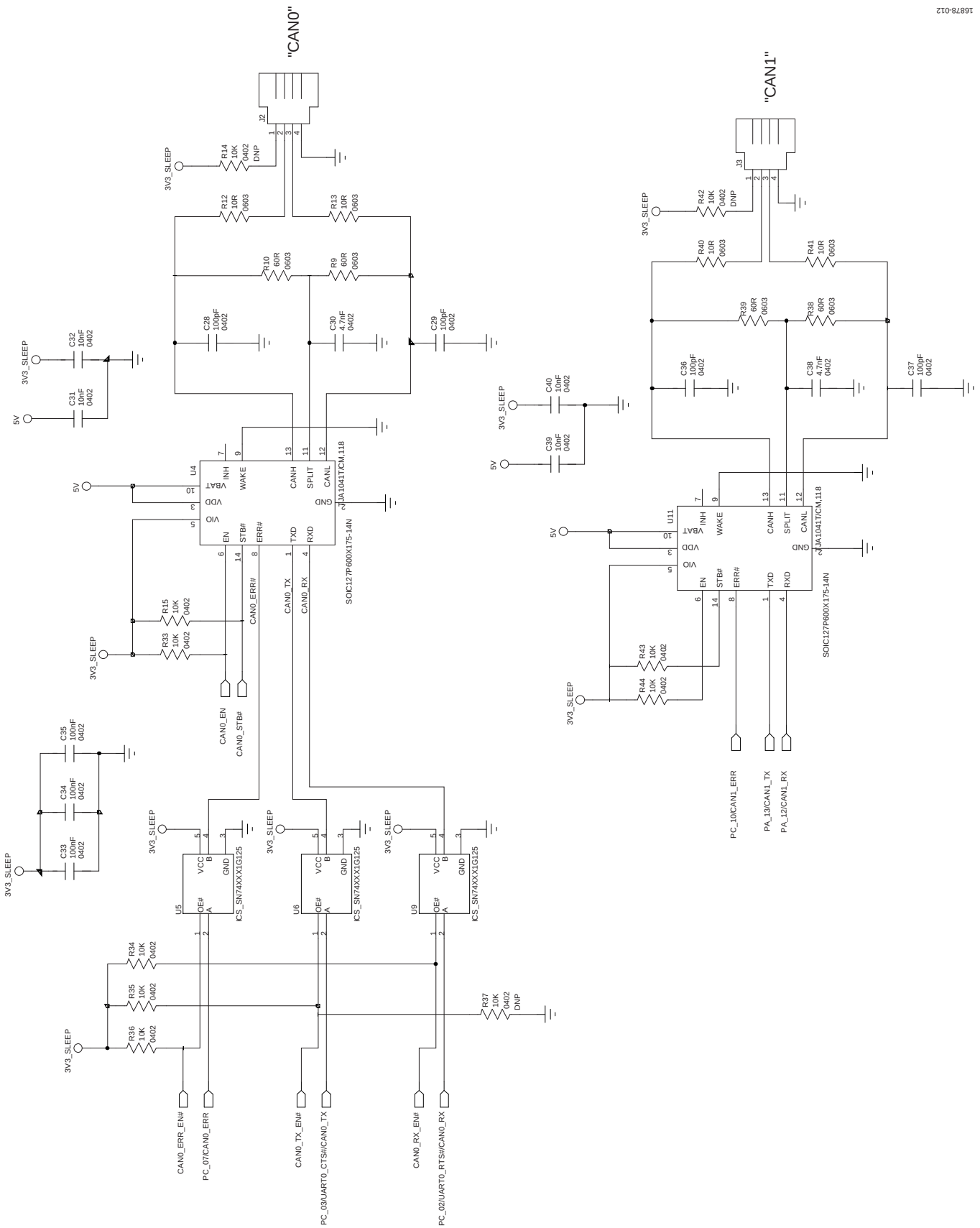

Figure 11. CAN Schematic

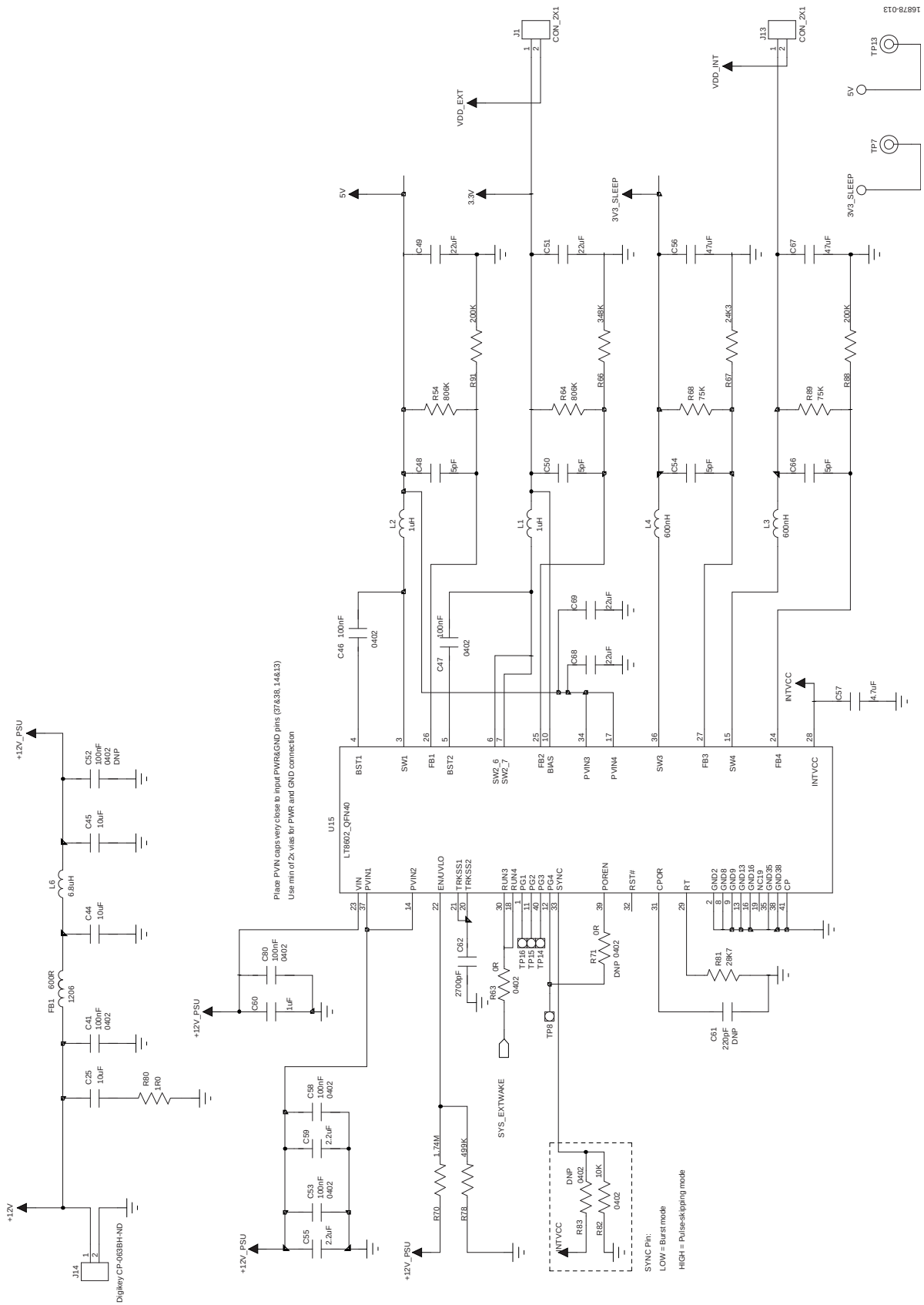

Figure 12. PSU Schematic

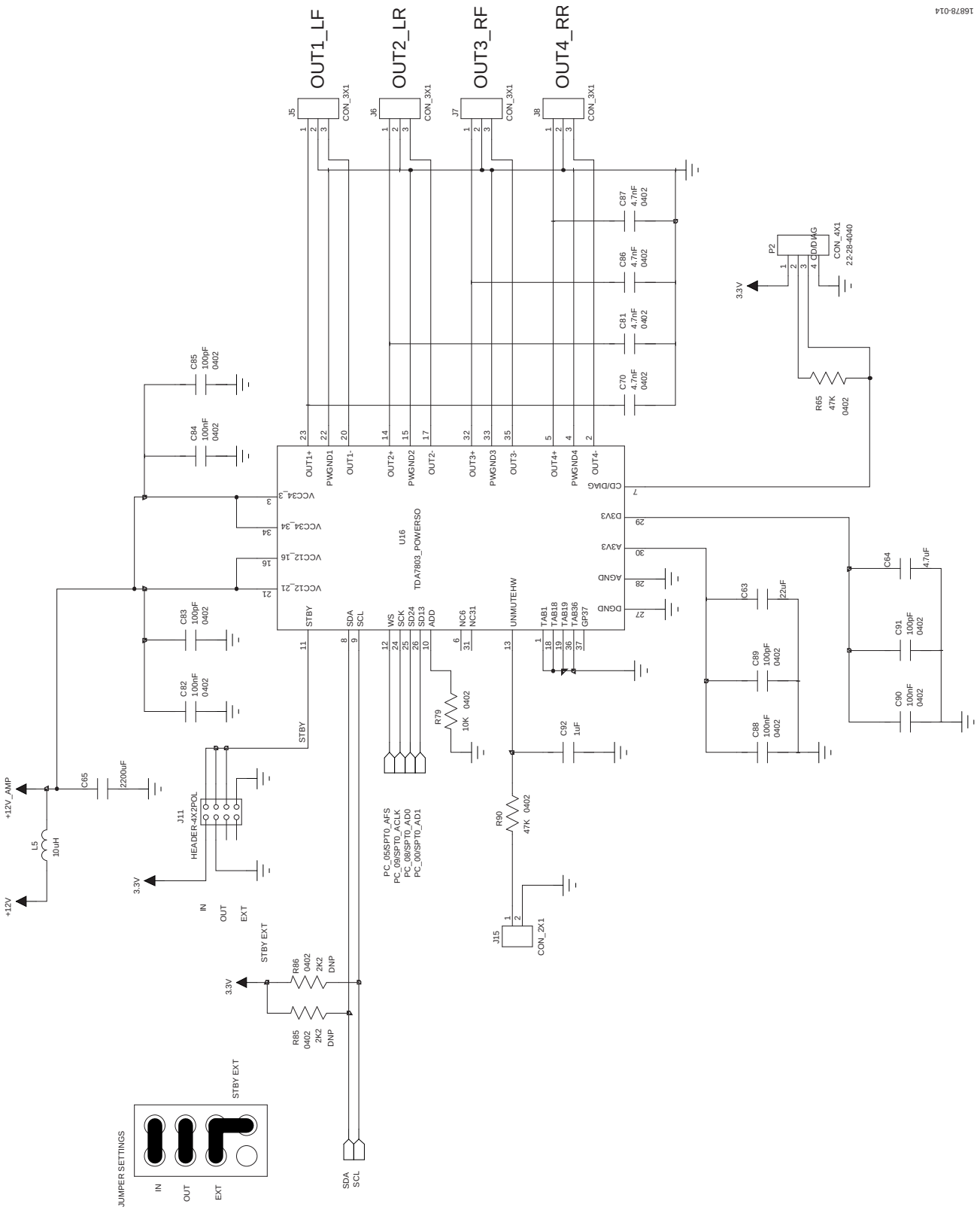

Figure 13. Power Amplifier Schematic

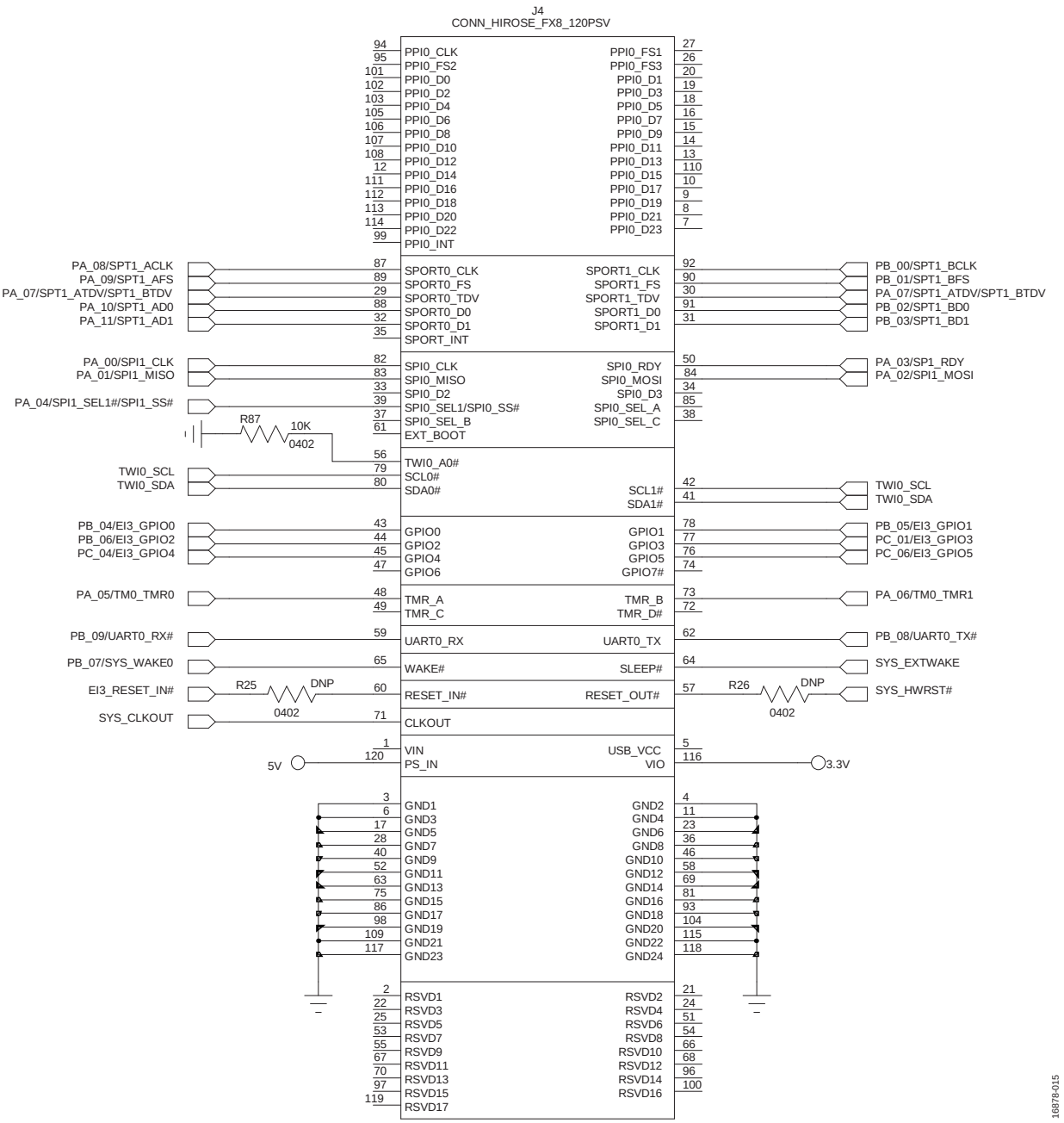

Figure 14. SDP Connector Schematic

ORDERING INFORMATION

BILL OF MATERIALS

Table 4.

Qty.	Reference Designator	Description	Part Number
33	C1, C6, C8 to C10, C15, C17, C21, C23, C27, C33 to C35, C41 to C43, C46, C47, C52, C53, C58, C71, C72, C74, C76 to C80, C82, C84, C88, C90	Capacitor, 0.1 µF, 10 V, 10%, X5R, 0402	0402ZD104KAT2A
2	C2, C3	Capacitor, 18 pF, 50 V, 5%, NP0, 0402	GRM1555C1H180JA01D
6	C7, C16, C24, C25, C44, C45	Capacitor, 1206, 10 µF, 25 V, X5R	FEC 1833825
14	C11 to C14, C18 to C20, C22, C26, C31, C32, C39, C40, C75	Capacitor, 0.01 µF, 16 V, 10%, 0402, X7R	0402YC103KAT2A
8	C28, C29, C36, C37, C83, C85, C89, C91	Capacitor, 0402 (1005 metric), 100 pF, 50 V, ±5%, C0G/NP0	FEC 2496792
6	C30, C38, C70, C81, C86, C87	Capacitor, 4700 pF, 16 V, 10%, X7R, 0402	FEC 2507329
4	C48, C50, C54, C66	Capacitor, 0402 (1005 metric), +5 pF, 50 V, ±0.25 pF, C0G/NP0, CGA series	FEC 2458210
5	C49, C51, C63, C68, C69	Capacitor, ceramic, 22 µF, 6.3 V, X7R, 10%, 1206	FEC 1845771
2	C55, C59	Capacitor, 1206, 2.2 µF, 50 V, X7R	FEC 2470443
2	C56, C67	Capacitor, ceramic, 47 µF, 6.3 V, X5R, 20%, 1206	FEC 1907351
3	C57, C64, C73	Multilayer ceramic capacitor, 0603, 6.3 V, 4.7 µF, X5R	FEC 1740638
2	C60, C92	Capacitor, low effective series resistance (ESR), 1 µF, 16 V, X7R	FEC 2112839
1	C61	Capacitor, ceramic, 220 pF, 50 V, X7R, 10%, 0402, do not populate	FEC 2210798
1	C62	Capacitor, 2700 pF, 0402	FEC 2627354
1	C65	Capacitor, aluminum electrolytic, 2200 µF, 16 mm, 25 V	FEC 2326204
1	D4	Diode, electrostatic discharge (ESD), quad array	497-6633-1-ND
1	D5	Diode, transient voltage suppressor, high speed	ESD7004MUTAG
3	FB1 to FB3	Ferrite bead, 600 Ω, 1206	HZ1206B601R-10
3	J1, J13, J15	Connector, two position header, cuttable connector, 0.100 inch (2.54 mm), through hole, gold	Digikey 952-2261-ND
2	J2, J3	Connector, RJ-11, 4-pin, 4P4C	5558872-1
1	J4	Connector, FX8, series, receptacle 0.6 mm, 120 SMD plug	Hirose FX8 120PSV
4	J5 to J8	Connector, standard terminal block, wire to board, CTB5202 series, 5 mm, printed circuit board (PCB) mount	FEC 1717002
1	J11	Connector, inline header, 8-pin, two rows, through hole, 2.54 mm pitch	FEC 1593441
1	J12	Connector, 1.27 mm, 10 contacts, header, through hole, two rows	SHF-105-01-L-D-TH
1	J14	Connector, power jack, 2.5 mm × 5.5 mm	Digikey CP-063BH-ND
1	J17	Connector, inline header, 6-pin, two rows, through hole, 2.54 mm pitch	FEC 2135961
2	L1, L2	Inductor, XFL3010, low dc resistance, 1 µH, 20%, 2.3 A	Mouser 994-XFL3010-102MEB
2	L3, L4	Inductor, XFL3010, low dc resistance, 0.6 µH, 20%, 2.5 A	Mouser 994-XFL3010-601MEB
1	L5	Inductor, MSS1260 series, 10 µH, 4 A, 6.18 A, shielded, 0.0239 Ω	FEC 2288425
1	L6	Inductor, SRN3015TA, 6.8 µH, 20%, 1 A	Digikey SRN3015TA-6R8MCT-ND
1	LED0	LED, yellow, 0603	475-2793-1-ND
2	LED1, LED3	LED, red, 0603	67-1549-2-ND
1	LED2	LED, green, 0603	67-1549-2-ND
1	P2	Connector, wire to board, 2.54 mm, four contacts, header, KK 42375 series, through hole, one row	FEC 2381172

Qty.	Reference Designator	Description	Part Number
1	P3	Connector, USB Mini A or USB Mini B	H125271TR-ND
43	R1, R7, R8, R14, R15, R22, R27 to R29, R31 to R37, R42 to R44, R46, R48 to R50, R53, R55, R57, R60, R74, R77, R79, R82, R83, R87, R92 to R100	Resistor, 10 kΩ, 5%, 0402	CRCW040210K0FKED
18	R2, R3, R6, R11, R16, R18, R23, R25, R26, R45, R58, R59, R61 to R63, R71 R76, R84	Resistor, 0 Ω, 1/10 W, 5%, 0402	ERJ-2GE0R00X
2	R4, R5	Resistor, 2.2 kΩ, 1/10 W, 5%, 0402	ERJ-2GEJ222X
4	R9, R10, R38, R39	Resistor, 60.4 kΩ, 1/10 W, 1%, 0603	ERJ-3EKF60R4V
4	R12, R13, R40, R41	Resistor, 10 Ω, 1/10 W, 5%, 0603	CRCW060310R0JNEA
4	R17, R19 to R21	Resistor, 100 kΩ, 1/16 W, 5%, 0402	541-100KJTR-ND
1	R24	Resistor, 2 kΩ, 1/10 W, 1%, 0402	ERJ-2RKF2001X
4	R30, R47, R51, R52	Resistor, 330 Ω, 1/16 W, 1%, 0402	541-330LCT-ND
2	R54, R64	Resistor, 806 kΩ, 0402, 1%	FEC 2141028
1	R56	Resistor, 1 MΩ, 1/10 W, 5%, 0603	CRCW06031M00JNEA
2	R65, R90	Resistor, 47 kΩ, 1/16 W, 5%, 0402	FEC 1358087
1	R66	Resistor, 348 kΩ, 0402, 1%	FEC 2302898
3	R67, R68, R89	Resistor, 75 kΩ, 5%, 0402	Any
1	R69	Resistor, 3.01 kΩ, 1/16 W, 1%, 0402	MCR01MRTF3011
1	R70	Resistor, 1.74 MΩ, 75 V, 100 mW, ±1%, 0603	FEC 2138635
1	R78	Resistor, 499 kΩ, 63 mW, 1%, 0402	FEC 2073089
1	R80	Resistor, 1 Ω, 50 V, 63 mW, ±5%, 0402	FEC 1739054
1	R81	Resistor, 0402, 1%, 28.7 kΩ	ERJ-2RKF2872X
2	R85, R86	Resistor, 2.2 kΩ, 1/10 W, 5%, 0402, do not populate	ERJ-2GEJ222X
2	R88, R91	Resistor, 200 kΩ, 1/10 W, 5%, 0402	Any
2	SW1, SW2	Switch, 6 mm, square push-button, SMD	EVQ-Q2K03W
1	SW3	Switch, rotary dual inline package, octal, 100 mA, 5 V	Digikey 563-1057-ND
16	TP1 to TP16	Test pad, do not populate	Not applicable
1	U1	IC, DSP, low power, 1024 kB flash, L2 SRAM, 88-lead, LFCSP	ADSP-BF706BCPZ-4
1	U2	IC, flash, SOIC-16	W25Q256FV
1	U3	IC, open drain, microprocessor supervisory circuit	ADM6315-29D2ARTZR7CT-ND
2	U4, U11	IC, CAN transceiver	TJA1041T/CM,118
7	U5, U6, U9, U10, U18, U19, U20	IC, 1-bit, field effect transistor (FET), bus switch, SC-70-5	FEC 2424774
1	U7	IC, USB, full speed serial UART, 32-QFN	FT232RQ
2	U8, U17	IC, single, two inputs, AND gate	SN74LVC1G08DBVR
1	U12	IC, 8-bit, general-purpose, parallel input/output expansion	MCP23008
1	U15	IC, dc-to-dc switching regulator, synchronous, four outputs, 3 V to 42 V input, 42 V/2.5 A output, 2 MHz	LT8602EUJ#PBF
1	U16	IC, Class D, audio power amplifier	ST Micro TDA7803A
1	Y1	Crystal, 24.576 MHz, 18 pF, 4-SMD	DigiKey 535-13393-1-ND

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG16878-0-12/18(0)

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