LT3093
–20V, 200mA, Ultralow Noise, Ultrahigh PSRR Negative Linear Regulator

DESCRIPTION

Demo circuit DC2952A features the LT®3093, an ultralow noise, ultrahigh power supply rejection ratio (PSRR) negative low dropout (LDO) regulator. DC2952A operates over an input range of –3.8V to –20V, and can deliver up to 200mA output current. It features ultralow noise (0.8µVRMS from 10Hz to 100kHz) and very high PSRR (73dB at 1MHz).

The EN/UVLO of LT3093 is bidirectional and can be switched with either a positive or a negative voltage. LT3093 also offers programmable current limit functionality by connecting a resistor from ILIM to GND. The VIOC tracking function controls an up-stream switching converter to maintain a constant voltage across the regulator and hence minimize power dissipation. The power good feedback (PGFB) pin is used to set a programmable power good threshold, and activates the fast start-up circuitry. To use the power good function, connect an external voltage source at VEXT. If power good and fast start-up functionality are not needed, tie PGFB to IN.

Built-in protection includes internal current limit with foldback and thermal limit with hysteresis.

The LT3093 datasheet gives a complete description of the part, operation and applications information. The datasheet must be read in conjunction with this Demo Manual for demonstration circuit DC2952A. The LT3093 is assembled in 12-lead MSOP and 3mm x 3mm DFN packages with an exposed pad on the bottom-side of the IC. Proper board layout is essential for maximum thermal performance.

Design files for this circuit board are available.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range (V_{IN})	I_{OUT} = 100mA, V_{OUT} = –3.3V	–20		–3.8	V
Input Voltage Range (V_{IN})	I_{OUT} = 190mA, V_{OUT} = –3.3V	–13*		–3.8	V
Output Voltage (V_{OUT})	V_{IN} = –5V, I_{OUT} = 190mA	–3.39	–3.32	–3.25	V
Shutdown Input Current (I_{IN})	V_{EN} = 0V, V_{IN} = –5V		3		µA

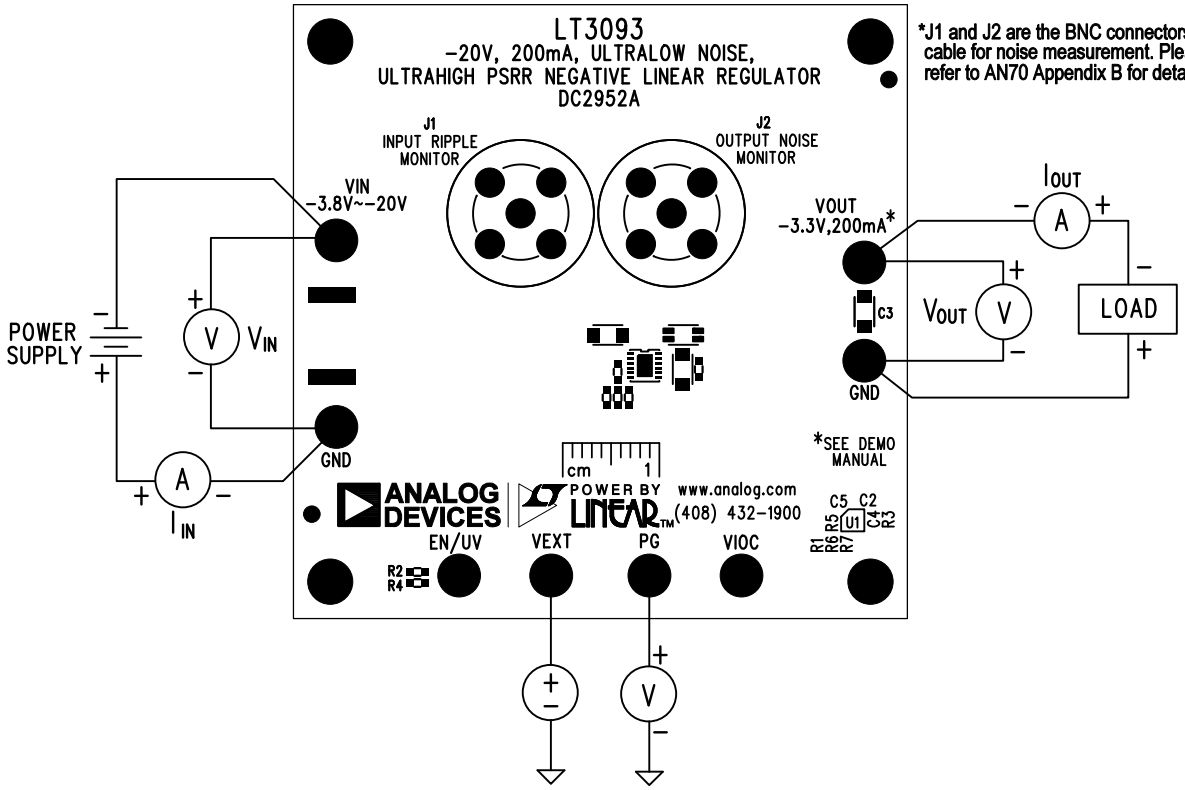
*The maximum input voltage for 100mA load current is set by a 60°C temperature rise of LT3093 on the demo circuit. Higher input voltage can be realized if larger copper area or forced-air cooling is applied. The output current is also limited by the input and output voltage differential; please refer to the datasheet for details.

QUICK START PROCEDURE

Demonstration circuit DC2952A is easy to set up to evaluate the performance of the LT3093EDD. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

1. Connect a load between the V_{OUT} and GND terminals.
2. With power off, connect the input power supply to the V_{IN} and GND terminals.
3. Apply –3.8V across V_{IN} to GND. The output voltage should be –3.32V ±3% (–3.39V to –3.25V)
4. Vary V_{IN} from –3.8V to –20V and vary the load from 0mA to 200mA.

   Note: The current limit may drop at high input-output differential voltage. Please refer to the datasheet for details. Make sure the power dissipation is below the thermal limit.
5. Apply a power source at VEXT. The PG pin voltage should be approximately equal to VEXT.
6. Refer to Application Notes AN70 and AN159 for measuring output noise and PSRR.



*The maximum output current will be limited by internal current limit based on the input and output voltage differential. Please refer to the datasheet.

Figure 1. Test procedure setup drawing for DC2952A

PCB LAYOUT

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1. Best PSRR Performance: PCB Layout for Input Trace

For applications utilizing the LT3093 for post-regulating switching converters, placing a capacitor directly at the LT3093 input results in AC current (at the switching frequency) flowing near the LT3093. Without careful attention to PCB layout, this relatively high frequency switching current generates an electromagnetic field (EMF) that couples to the LT3093 output, thereby degrading its effective PSRR. While highly dependent on the PCB, the switching pre-regulator, and the input capacitor size among other factors, the PSRR degradation can easily be 30dB at 1MHz. This degradation is present even if the LT3093 is de-soldered from the board, because it effectively degrades the PSRR of the PC board itself. While negligible for conventional low PSRR LDOs, the LT3093's ultrahigh PSRR requires careful attention to higher order parasitics in order to realize the full performance offered by the regulator.

The LT3093 demo board alleviates this degradation in PSRR by using a specialized layout technique. In Figure 2, the input trace (V_{IN}) is highlighted in red, and in Figure 3 the return path (GND) is also highlighted together with input capacitor C1. Normally when an AC voltage is applied to the input of the board, AC current flows along this path, thus generating EMF. This EMF couples to output capacitor C2 and the related traces, making the PSRR appear worse than it actually is. With the input trace directly above the return path, the EMFs are in opposite directions, and consequently cancel each other out. Make sure these traces exactly overlap each other to maximize the cancellation effect and thus provide the maximum PSRR offered by the regulator.

2. Best AC Performance: PCB Layout for Output Capacitors C2

For ultrahigh PSRR performance, the LT3093 bandwidth is quite high (~1MHz), making it very close to the output capacitor's self-resonance frequency (~1.6MHz). Therefore, it is very important to avoid adding extra impedance (ESL & ESR) outside the feedback loop. To that end, minimize the effects of PCB trace and solder inductance by Kelvin connecting OUTS and SET pin capacitor GND directly to output capacitors (C2) terminals using split capacitor techniques. With only small AC current flowing through these connections, the impact of solder joint/PCB trace inductance on stability is eliminated. While the LT3093 is robust enough not to oscillate if the recommended layout is not followed, phase/gain margin and stability will degrade.

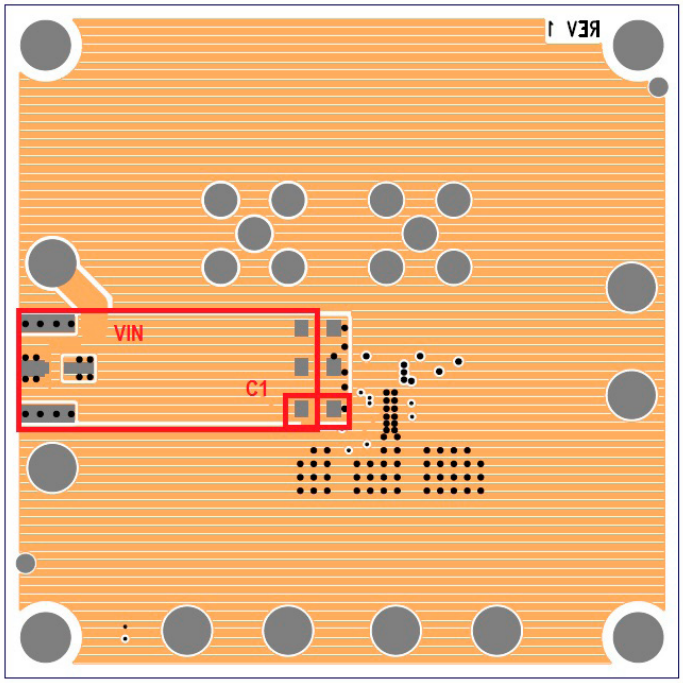


Figure 2. Bottom Layer of DC2952A

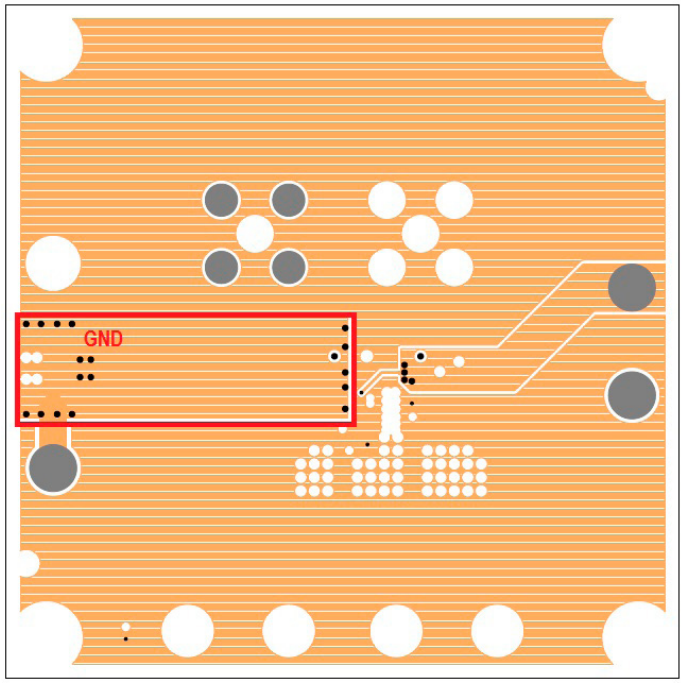


Figure 3. Layer 3 of DC2952A

PCB LAYOUT

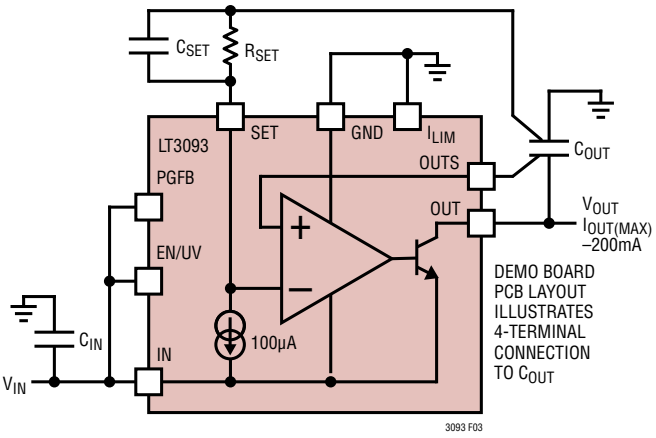


Figure 4. C2 and C_{SET} connections for best performance

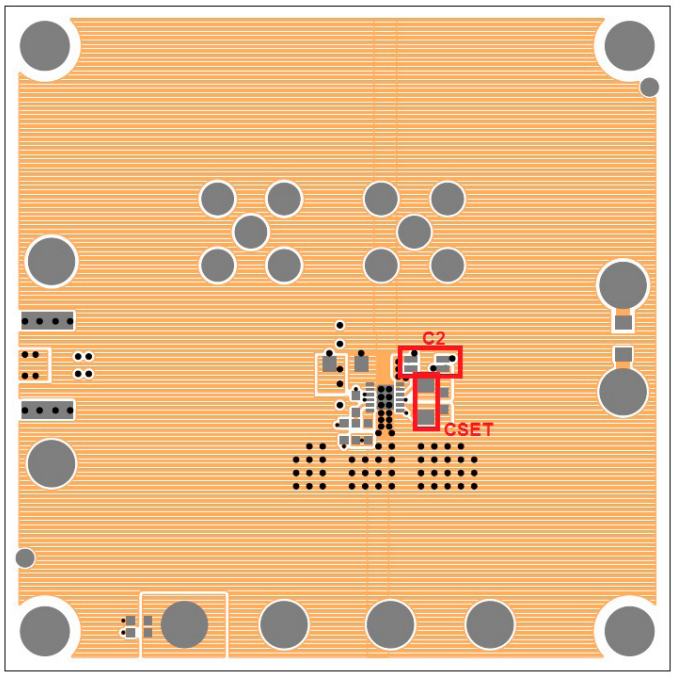
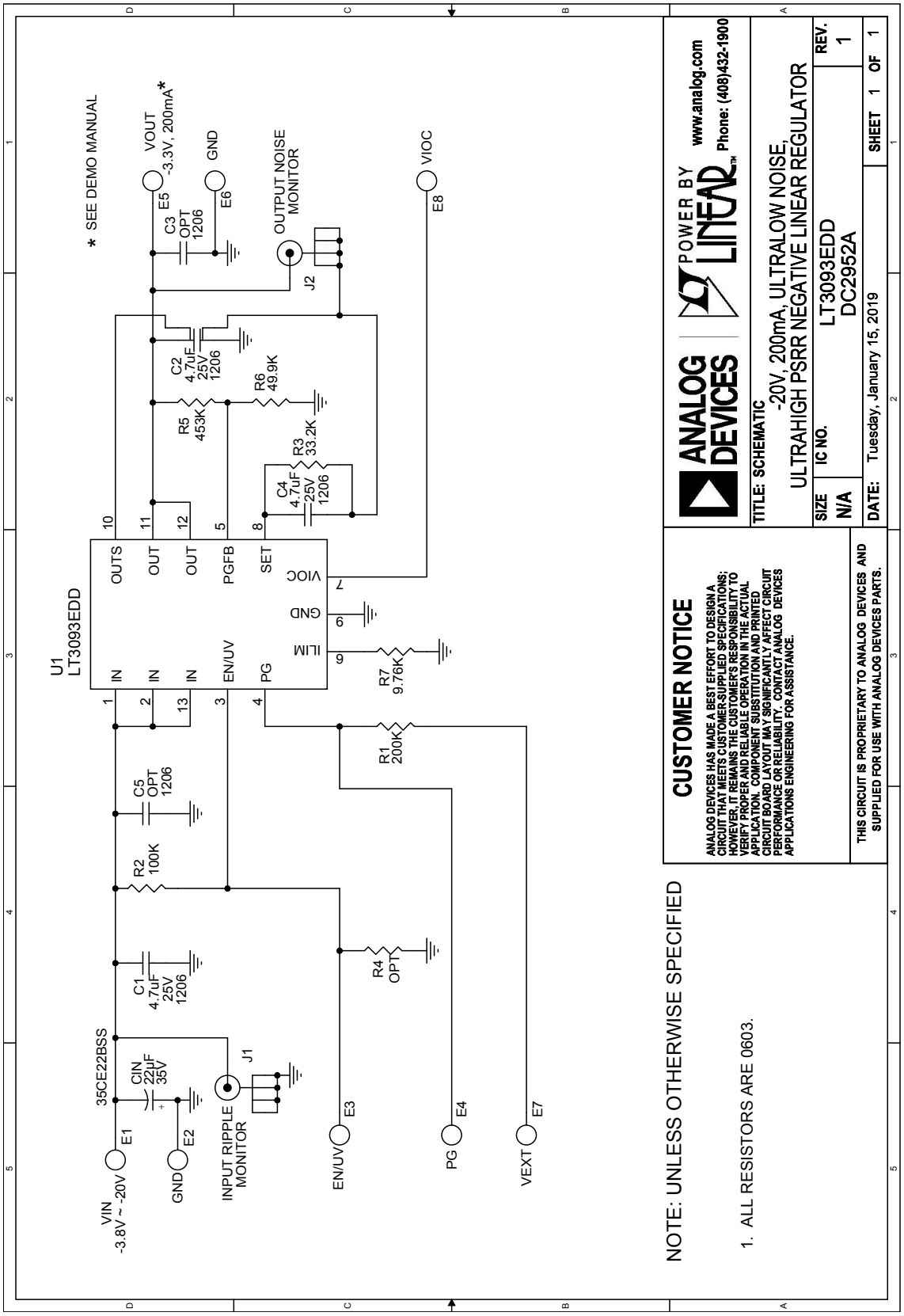


Figure 5. Split Pads for Output Capacitors on Top Layer of DC2952A

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	CIN	CAP, ALUM, 22µF, 35V, 5X5.4MM	SUN ELECTRONIC INDUSTRIES CORP, 35CE22BSS
2	3	C1,C2,C4	CAP, X7R, 4.7µF, 25V, 10% 1206	MURATA, GRM31CR71E475KA88L
3	1	R1	RES, CHIP, 200k, 1/10W, 5% 0603	VISHAY, CRCW0603200KJNEA
4	1	R2	RES, CHIP, 100k, 1/10W, 1% 0603	VISHAY, CRCW0603100KFKEA
5	1	R3	RES, CHIP, 33.2k, 1/10W, 1% 0603	VISHAY, CRCW060333K2FKEA
6	1	R5	RES, CHIP, 453k, 1/10W, 1% 0603	VISHAY, CRCW0603453KFKEA
7	1	R6	RES, CHIP, 49.9k, 1/10W, 1% 0603	VISHAY, CRCW060349K9FKEA
8	1	R7	RES., CHIP, 9.76K, 1/10W, 1% 0603	VISHAY, CRCW06039K76FKEA
9	1	U1	IC, LT3093EDD, 12DFN	ANALOG DEVICES, LT3093EDD#PBF
Additional Demo Board Circuit Components				
1	0	C3, C5 (OPT)	CAP, OPTION, 1206	
2	0	R4 (OPT)	RES, OPTION, 0603	
Hardware: For Demo Board Only				
1	8	E1 TO E8	TESTPOINT, TURRET, 0.094" pbf	MILL-MAX, 2501-2-00-80-00-00-07-0
2	2	J1, J2	CONN, BNC, 5 PINS	CONNEX, 112404
3	4	MH1 TO MH4	STAND-OFF, NYLON 6.4mm	WURTH ELEKTRONIK, 702931000

SCHEMATIC DIAGRAM



ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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