INSTRUCTION SET

Arithmetic Operations

			bytes	OSC periods
ADD	A,source	add source to A	1,2	12
ADD	A,#data		2	12
ADDC	A,source	add with carry	1,2	12
ADDC	A,#data		2	12
SUBB	A,source	subtract from A with borrow	1,2	12
SUBB	A,#data		2	12
INC	A	increment	1	12
INC	source		1,2	12
INC	DPTR		1	24
DEC	A	decrement	1	12
DEC	source		1,2	12
MUL	AB	multiply A by B	1	48
DIV	AB	divide A by B	1	48
DA	A	decimal adjust	1	12

Legend

Rn	register addressing using R0-R7
direct	8bit internal address (00h-FFh)
@Ri	indirect addressing using R0 or R1
source	any of [Rn, direct, @Ri]
dest	any of [Rn, direct, @Ri]
#data	8bit constant included in instruction
#data16	16bit constant included in instruction
bit	8bit direct address of bit
rel	signed 8bit offset
addr11	11bit address in current 2K page
addr16	16bit address

Data Transfer Operations

			bytes	OSC periods
MOV	A,source	move source to destination	1,2	12
MOV	A,#data		2	12
MOV	dest,A		1,2	12
MOV	dest,source		1,2,3	24
MOV	dest,#data		2,3	12,24
MOV	DPTR,#data16		3	24
MOVC	A,@A+DPTR	move from code memory	1	24
MOVC	A,@A+PC		1	24
MOVX	A,@Ri	move to/from data memory	1	24
MOVX	A,@DPTR		1	24
MOVX	@Ri,A		1	24
MOVX	@DPTR,A		1	24
PUSH	direct	push onto stack	2	24
POP	direct	pop from stack	2	24
XCH	A,source	exchange bytes	1,2	12
XCHD	A,@Ri	exchg low digits	1	12

Program Branching

			bytes	OSC periods
ACALL	addr11	call subroutine	2	24
LCALL	addr16		3	24
RET		return from sub.	1	24
RETI		return from int.	1	24
AJMP	addr11	jump	2	24
LJMP	addr16		3	24
SJMP	rel		2	24
JMP	@A+DPTR		1	24
JZ	rel	jump if A = 0	2	24
JNZ	rel	jump if A not 0	2	24
CJNE	A,direct,rel	compare and jump if not equal	3	24
CJNE	A,#data,rel		3	24
CJNE	Rn,#data,rel		3	24
CJNE	@Ri,#data,rel		2	24
DJNZ	Rn,rel	decrement and jump if not zero	2	24
DJNZ	direct, rel		3	24
NOP		no operation	1	12

Logical Operations

			bytes	OSC periods
ANL	A,source	logical AND	1,2	12
ANL	A,#data		2	12
ANL	direct,A		2	12
ANL	direct,#data		3	24
ORL	A,source	logical OR	1,2	12
ORL	A,#data		2	12
ORL	direct,A		2	12
ORL	direct,#data		3	24
XRL	A,source	logical XOR	1,2	12
XRL	A,#data		2	12
XRL	direct,A		2	12
XRL	direct,#data		3	24
CLR	A	clear A to zero	1	12
CPL	A	complement A	1	12
RL	A	rotate A left	1	12
RLC	A	...through C	1	12
RR	A	rotate A right	1	12
RRC	A	...through C	1	12
SWAP	A	swap nibbles	1	12

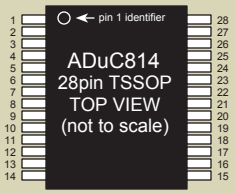
Boolean Variable Manipulation

			bytes	OSC periods
CLR	C	clear bit to zero	1	12
CLR	bit		2	12
SETB	C	set bit to one	1	12
SETB	bit		2	12
CPL	C	complement bit	1	12
CPL	bit		2	12
ANL	C,bit	AND bit with C	2	24
ANL	C,/bit	...NOTbit with C	2	24
ORL	C,bit	OR bit with C	2	24
ORL	C,/bit	...NOTbit with C	2	24
MOV	C,bit	move bit to bit	2	12
MOV	bit,C		2	24
JC	rel	jump if C set	2	24
JNC	rel	jmp if C not set	2	24
JB	bit,rel	jump if bit set	3	24
JNB	bit,rel	jmp if bit not set	3	24
JBC	bit, rel	jmp&clear if set	3	24

ASSEMBLER DIRECTIVES

EQU	define symbol	DW	store word values in program memory
DATA	define internal memory symbol	ORG	set segment location counter
IDATA	define indirect addressing symbol	END	end of assembly source file
XDATA	define external memory symbol	CSEG	select program memory space
BIT	define internal bit memory symbol	XSEG	select external data memory space
CODE	define program memory symbol	DSEG	select internal data memory space
DS	reserve bytes of data memory	ISEG	select indirectly addressed internal data memory space
DBIT	reserve bits of bit memory		
DB	store byte values in program memory	BSEG	select bit addressable memory space

PIN FUNCTIONS



G02945-1-4/02 (0)

1	DGND
2	DLOAD
3	P3.0 / RxD
4	P3.1 / TxD
5	P3.2 / $\overline{INT0}$
6	P3.3 / $\overline{INT1}$
7	P3.4 / T0 / $\overline{CONVST}$
8	P1.0 / T2
9	P1.1 / T2EX
10	RESET
11	P1.2 / ADC0
12	P1.3 / ADC1
13	AV_{DD}
14	AGND

28	DV_{DD}
27	XTAL2
26	XTAL1
25	SCLOCK / D0
24	P3.7 / MOSI / D1
23	P3.6 / MISO
22	P3.5 / T1 / $\overline{SS}$ / EXTCLK
21	P1.7 / ADC5 / DAC1
20	P1.6 / ADC4 / DAC0
19	P1.5 / ADC3
18	P1.4 / ADC2
17	C_{REF}
16	V_{REF}
15	AGND

PROGRAM MEMORY SPACE (read only)

(no parallel external memory interface)

INTERRUPT VECTOR ADDRESSES

Interrupt Bit	Interrupt Name	Vector Address	Priority within Level
PSMCON.5	Power Supply Monitor Interrupt	43h	1
PLLCON.6	PLL Lock Interrupt	4Bh	2
WDS	WatchDog Timer Interrupt	5Bh	3
IE0	External Interrupt 0	03h	4
ADCI	End of ADC Conversion Interrupt	33h	5
TF0	Timer0 Overflow Interrupt	0Bh	6
IE1	External Interrupt 1	13h	7
TF1	Timer1 Overflow Interrupt	1Bh	8
ISPI	SPI Interrupt	3Bh	9
RI/TI	UART Interrupt	23h	10
TF2/EXF2	Timer2 Interrupt	2Bh	11
TIMECON.2	Time Interval Counter Interrupt	53h	12

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ANALOG DEVICES

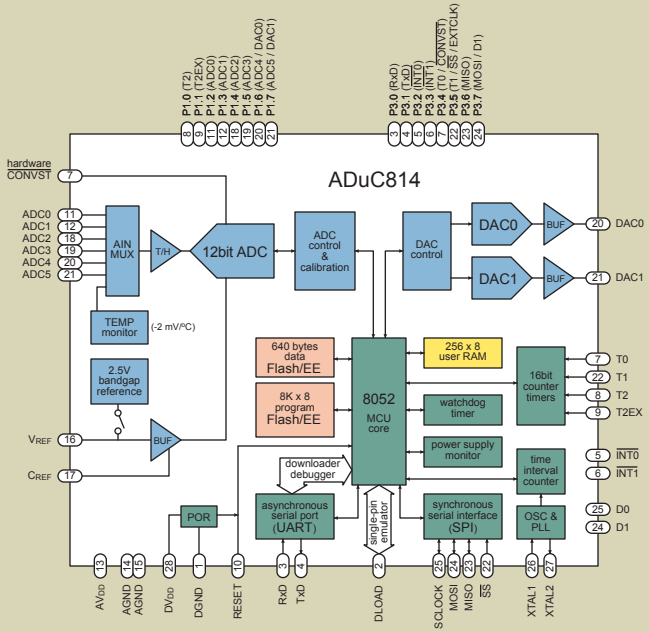
ADuC814

MicroConverter® Quick Reference Guide

a “Data Acquisition System on a Chip”

the ADuC814 is: ADC:	12bit, 5µs, 6channel, self calibrating, guaranteed no missing codes, high-speed data capture mode
DAC:	dual, 12bit, 15µs, voltage output <1LSB DNL
Flash/EEPROM:	8K bytes Flash/EE program memory 640 bytes Flash/EE data memory
microcontroller:	industry standard 8052 16 I/O lines, programmable PLL clock (131KHz to 16MHz from 32KHz crystal)
other on-chip features:	temperature monitor, power supply monitor, watchdog timer, flexible serial interface ports,

FUNCTIONAL BLOCK DIAGRAM



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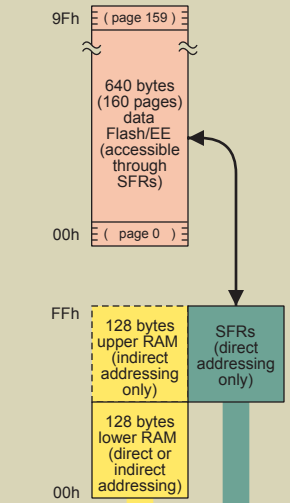
REV. 0

DATA MEMORY: RAM, SFRs, user Flash/EE (all read/write)

LOWER RAM

decimal address	HEX address		MSB address (bit addresses) LSB address							
127	7Fh	General Purpose Area								
...	...									
48	30h									
47	2Fh	Bit Addressable Area	7Fh	7Eh	7Dh	7Ch	7Bh	7Ah	79h	78h
46	2Eh		77h	76h	75h	74h	73h	72h	71h	70h
45	2Dh		6Fh	6Eh	6Dh	6Ch	6Bh	6Ah	69h	68h
44	2Ch		67h	66h	65h	64h	63h	62h	61h	60h
43	2Bh		5Fh	5Eh	5Dh	5Ch	5Bh	5Ah	59h	58h
42	2Ah		57h	56h	55h	54h	53h	52h	51h	50h
41	29h		4Fh	4Eh	4Dh	4Ch	4Bh	4Ah	49h	48h
40	28h		47h	46h	45h	44h	43h	42h	41h	40h
39	27h		3Fh	3Eh	3Dh	3Ch	3Bh	3Ah	39h	38h
38	26h		37h	36h	35h	34h	33h	32h	31h	30h
37	25h		2Fh	2Eh	2Dh	2Ch	2Bh	2Ah	29h	28h
36	24h		27h	26h	25h	24h	23h	22g	21h	20h
35	23h		1Fh	1Eh	1Dh	1Ch	1Bh	1Ah	19h	18h
34	22h		17h	16h	15h	14h	13h	12h	11g	10h
33	21h		0Fh	0Eh	0Dh	0Ch	0Bh	0Ah	09h	08h
32	20h		07h	06h	05h	04h	03h	02h	01h	00h
31	1Fh	R7	Register Bank 3							
30	1Eh	R6								
29	1Dh	R5								
28	1Ch	R4								
27	1Bh	R3								
26	1Ah	R2								
25	19h	R1								
24	18h	R0								
23	17h	R7	Register Bank 2							
22	16h	R6								
21	15h	R5								
20	14h	R4								
19	13h	R3								
18	12h	R2								
17	11h	R1								
16	10h	R0								
15	0Fh	R7	Register Bank 1							
14	0Eh	R6								
13	0Dh	R5								
12	0Ch	R4								
11	0Bh	R3								
10	0Ah	R2								
9	09h	R1								
8	08h	R0								
7	07h	R7	Register Bank 0							
6	06h	R6								
5	05h	R5								
4	04h	R4								
3	03h	R3								
2	02h	R2								
1	01h	R1								
0	00h	R0								

DATA MEMORY SPACE (read/write area)



lower RAM details

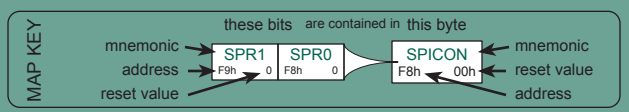
SFR details

SFR MAP & RESET VALUES

(reserved)	SPIDAT 00h F7h	ADCCON1 00h EFh	(reserved)	PSMCON DFh	PLLCON 53h D7h	(reserved)	(reserved)	EDATA4 00h BFh	(not used)	(not used)	(not used)	(not used)	(reserved)	PCON 00h 87h
(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	EADRL 00h C6h	EDATA3 00h BEh	(reserved)	INTVAL 00h A6h	(not used)	(not used)	(not used)	(reserved)	(reserved)
DACCON 04h FDh	ADCCON3 00h F5h	(reserved)	(reserved)	(reserved)	TH2 00h CDh	(reserved)	EDATA2 00h BDh	(reserved)	HOUR 00h A5h	(not used)	(not used)	TH1 00h 8Dh	(reserved)	
DAC1H 00h FCh	ADCGAINH *20h F4h	(reserved)	(reserved)	(reserved)	TL2 00h CCh	(not used)	EDATA1 00h BCh	(reserved)	MIN 00h A4h	CFG814 04h 9Ch	(not used)	TH0 00h 8Ch	(reserved)	
DAC1L 00h FBh	ADCGAINL *00h F3h	(reserved)	(reserved)	(reserved)	RCAP2H 00h CBh	(reserved)	ETIM2 10h BBh	(reserved)	SEC 00h A3h	(reserved)	(not used)	TL1 00h 8Bh	DPH 00h 83h	
DAC0H 00h FAh	ADCOFSH *20h F2h	ADCDATAH 00h DAh	(reserved)	PSW 00h D0h	RCAP2L 00h CAh	(reserved)	ETIM1 20h BAh	(reserved)	HTHSEC 00h A2h	(reserved)	(not used)	TL0 00h 8Ah	DPL 00h 82h	
DAC0L 00h F9h	ADCOFSL *00h F1h	ADCDATAL 00h D9h	(reserved)	T2CON C8h 00h	(reserved)	WDCON C0h 10h	ECON 00h B9h	(reserved)	TIMECON 00h A1h	SBUF 00h 99h	(not used)	TMOD 00h 89h	SP 07h 81h	
SPICON 04h F8h	B 00h F0h	DCON 00h E8h	ACC 00h E0h	ADCCON2 00h D8h	PSW 00h D0h	T2CON C8h 00h	WDCON C0h 10h	IP 00h B8h	P3 FFh B0h	IE 00h A8h	(not used)	SCON 00h 98h	P1 FFh 90h	TCON 00h 88h	(not used)	

SPR0 0 F8h	0 F0h	0 E8h	0 E0h	CS0 0 D8h	P 0 D0h	CAP2 0 C8h	WDWR 0 C0h	PX0 0 B8h	RXD 1 B0h	EX0 0 A8h	RI 0 98h	T2 1 90h	IT0 0 88h
SPR1 0 F9h	0 F1h	0 E9h	0 E1h	CS1 0 D9h	F1 0 D1h	CNT2 0 C9h	WDE 0 C1h	PT0 0 B9h	TXD 1 B1h	ET0 0 A9h	TI 0 99h	T2EX 1 91h	IE0 0 89h
CPHA 0 FAh	0 F2h	0 EAh	0 E2h	CS2 0 DAh	OV 0 D2h	TR2 0 CAh	WDS 0 C2h	PX1 0 BAh	INT0 1 B2h	EX1 0 AAh	RB8 0 9Ah	1 92h	IT1 0 8Ah
CPOL 0 FBh	0 F3h	D0EN 0 EBh	0 E3h	CS3 0 DBh	RS0 0 D3h	EXEN2 0 CBh	WDIR 0 C3h	PT1 0 BBh	INT1 1 B3h	ET1 0 ABh	TB8 0 9Bh	1 93h	IE1 0 8Bh
SPIM 0 FCh	0 F4h	0 ECh	0 E4h	CCONV 0 DCh	RS1 0 D4h	TCLK 0 CCh	PRE0 0 C4h	PS 0 BCh	T0 1 B4h	ES 0 ACh	REN 0 9Ch	1 94h	TR0 0 8Ch
SPE 0 FDh	0 F5h	D0 0 EDh	0 E5h	SCONV 0 DDh	F0 0 D5h	RCLK 0 CDh	PRE1 0 C5h	PT2 0 BDh	T1 1 B5h	ET2 0 ADh	SM2 0 9Dh	1 95h	TF0 0 8Dh
WCOL 0 FEh	0 F6h	D1EN 0 EEh	0 E6h	ADCSPI 0 DEh	AC 0 D6h	EXF2 0 CEh	PRE2 0 C6h	PADC 0 BEh	WR 1 B6h	EADC 0 AEh	SM1 0 9Eh	1 96h	TR1 0 8Eh
ISPI 0 FFh	0 F7h	D1 0 EFh	0 E7h	ADCI 0 DFh	CY 0 D7h	TF2 0 CFh	PRE3 0 C7h	PSI 0 BFh	RD 1 B7h	EA 0 AFh	SM0 0 9Fh	1 97h	TF1 0 8Fh

MAP KEY



* calibration coefficients are preconfigured at power-up to factory calibrated values

SFR DESCRIPTIONS

ADCCON1 ADC Control register #1

ADCCON1.7	ADC mode (0=off, 1=on)
ADCCON1.6	external Vref select bit (0=on-chip Vref)
ADCCON1.5	conversion time = 16 / ADCclk
ADCCON1.4	ADCclk = 16,777,216Hz / [8,4,16,32]
ADCCON1.3	acquisition time select bits
ADCCON1.2	acq time = [1,2,3,4] / ADCclk
ADCCON1.1	Timer2 convert enable
ADCCON1.0	external CONVST enable

ADCCON2 ADC Control register #2

ADCI	ADC interrupt flag
ADCSPI	enables ADC-to-SPI high-speed data capture mode
CCONV	continuous conversion enable bit
SCONV	single conversion start bit
CS3	input channel select bits:
CS2	0 - 5 = ADC0 - ADC5
CS1	8 = temperature sensor
CS0	9=DAC0, A=DAC1, B=AGND, C=VREF

ADCCON3 ADC Control register #3

ADCCON3.7	busy indicator flag (0=ADC not active)
ADCCON3.6	gain calibration disable bit (0=gain cal enabled)
ADCCON3.5	number of averages selection bits
ADCCON3.4	[15,1,31,63] averages
ADCCON3.3	offset calibration disable bit (0=offset cal enabled)
ADCCON3.2	(this bit must contain 1)
ADCCON3.1	calibration type (0=offset cal, 1=gain cal)
ADCCON3.0	start calibration bit, set to 1 to begin cal

ADCDATAH / ADCDATAL ADC Data registers

ADCGAINH / ADCGAINL ADC Gain calibration coefficients

ADCOFSH / ADCOFSL ADC Offset calibration coefficients

DACCON DAC Control register

DACCON.7	ModeSelect (0=12bit, 1=8bit)
DACCON.6	DAC1 RangeSelect (0=2.5V, 1=V_{DD})
DACCON.5	DAC0 RangeSelect (0=2.5V, 1=V_{DD})
DACCON.4	Clear DAC1 (0=0V, 1=normal operation)
DACCON.3	Clear DAC0 (0=0V, 1=normal operation)
DACCON.2	Synchronous Update (1=asynchronous)
DACCON.1	PowerDown DAC1 (0=off, 1=on)
DACCON.0	PowerDown DAC0 (0=off, 1=on)

DAC1H,DAC1L DAC1 data registers

DAC0H,DAC0L DAC0 data registers

PLLCON PLL Control register

PLLCON.7	oscillator powerdown control bit (0=normal)
PLLCON.6	PLL lock indicator flag (0=out of lock)
PLLCON.5	(this bit must contain zero)
PLLCON.4	(this bit must contain zero)
PLLCON.3	"fast interrupt" control bit (0=normal)
PLLCON.2	3-bit clock divider value, "CD" (default=3):
PLLCON.1	f_{CORE} = 16,777,216Hz ÷ 2^{CD}
PLLCON.0	

TIMECON Time Interval Counter Control Register

TIMECON.6	24hour select bit (0=255hour)
TIMECON.5	INTVAL timebase select bits
TIMECON.4	[128th sec, seconds, minutes, hours]
TIMECON.3	single time interval control bit (0=reload&restart)
TIMECON.2	time interval interrupt bit, "TII"
TIMECON.1	time interval enable bit (0=disable&clear)
TIMECON.0	time clock enable bit (0=disable)

INTVAL TIC Interval Register

HTHSEC TIC Elapsed 128th Second Register

SEC TIC Elapsed Seconds Register

MIN TIC Elapsed Minutes Register

HOUR TIC Elapsed Hours Register

CFG814 ADuC814 Configuration Register

CFG814.0	SPI enable (0=disabled)
CFG814.1	PLL bypas (0=XTAL+PLL, 1=P3.5)

ECON Data Flash/EE comand register

01h	READ page	05h	ERASE page
02h	PROGRAM page	06h	ERASE ALL
04h	VERIFY page	others	reserved

EADRL Data Flash/EE address register

EDATA1,EDATA2,EDATA3,EDATA4 Data Flash/EE data registers

ETIM1,ETIM2 Data Flash/EE timing registers

SPICON SPI Control register

ISPI	SPI inturrupt (set at end of SPI transfer)
WCOL	write collision error flag
SPE	SPI enable (0=DCON enable, 1=SPI enable)
SPIM	master mode select (0=slave)
CPOL	clock polarity select (0=SCLK idles low)
CPHA	clock phase select (0=leading edge latch)
SPR1	SPI bitrate select bits
SPR0	bitrate = Fcore / [2,4,8,16] (slave: SPR0=SS)

SPIDAT SPI Data register

DCON D0 & D1 Control register

(enabled if SPE=0, see SPICON register above)

D1	D1 output bit
D1EN	D1 output enable (0=disable)
D0	D0 output bit
D0EN	D0 output enable (0=disable)

WDCON Watchdog Timer control register

PRE3	watchdog timeout selection bits
PRE2	0-7=[15.6,31.2,62.5,125,250,500,1000,2000]ms
PRE1	8=0ms (immediate reset)
PRE0	>8=reserved
WDIR	watchdog interrupt response bit
WDS	watchdog status flag (1 indicates watchdog timeout)
WDE	watchdog enable control (0=disabled)
WDWR	watchdog write enable bit (set to enable write)

PSMCON Power Supply Monitor control register

PSMCON.7	(reserved)
PSMCON.6	PSM status bit (1=normal / 0=fault)
PSMCON.5	PSM interrupt bit
PSMCON.4	trip point select bits
PSMCON.3	[4.63V, 3.08V, 2.93V, 2.63V]
PSMCON.2	(reserved)
PSMCON.1	(reserved)
PSMCON.0	PSM enable control (0=off, 1=on)

SP Stack Pointer

IE Interrupt Enable register #1

EA	enable inturrupts (0=all inturrupts disabled)
EADC	enable ADCI (ADC interrupt)
ET2	enable TF2/EXF2 (Timer2 overflow interrupt)
ES	enable RI/TI (serial port interrupt)
ET1	enable TF1 (Timer1 overflow interrupt)
EX1	enable IE1 (external interrupt 1)
ET0	enable TF0 (Timer0 overflow interrupt)
EX0	enable IE0 (external interrupt 0)

IP Interrupt Priority register

IP.7	(not used)
PADC	priority of ADCI (ADC interrupt)
PT2	priority of TF2/EXF2 (Timer2 overflow interrupt)
PS	priority of RI/TI (serial port interrupt)
PT1	priority of TF1 (Timer1 overflow interrupt)
PX1	priority of IE1 (external INT1)
PT0	priority of TF0 (Timer0 overflow interrupt)
PX0	priority of IE0 (external INT0)

IEIP2 Interrupt Enable/Priority register #2

IEIP2.7	priority of LOCK interrupt (PLL lock)
IEIP2.6	priority of TII interrupt (time interval)
IEIP2.5	priority of PSMI interrupt (power supply monitor)
IEIP2.4	priority of ISPI interrupt (serial interface)
IEIP2.3	enable LOCK interrupt (PLL lock)
IEIP2.2	enable TII interrupt (time interval)
IEIP2.1	enable PSMI (power supply monitor interrupt)
IEIP2.0	enable ISPI interrupt (serial interface)

TMOD Timer Mode register

TMOD.3/.7	gate control bit (0=ignore INTx)
TMOD.2/.6	counter/timer select bit (0=timer)
TMOD.1/.5	timer mode selecton bits
TMOD.0/.4	[13bitT, 16bitT/C, 8bitT/Creload, 2x8bitT]
	(upper nibble = Timer1, lower nibble = Timer0)

TCON Timer Control register

TF1	Timer1 overflow flag (auto cleared on vector to ISR)
TR1	Timer1 run control (0=off, 1=run)
TF0	Timer0 overflow flag (auto cleared on vector to ISR)
TR0	Timer0 run control (0=off, 1=run)
IE1	external INT1 flag (auto cleared on vector to ISR)
IT1	IE1 type (0=level trig, 1=edge trig)
IE0	external INT0 flag (auto cleared on vector to ISR)
IT0	IE0 type (0=level trig, 1=edge trig)

TH0,TL0 Timer0 registers

TH1,TL1 Timer1 registers

T2CON Timer2 Control register

TF2	overflow flag
EXF2	external flag
RCLK	receive clock enable (0=Timer1 used for RxD clk)
TCLK	transmit clock enable (0=Timer1 used for TxD clk)
EXEN2	external enable (0=ignore T2EX, 1=cap/rld on T2EX)
TR2	run control (0=stop, 1=run)
CNT2	timer/counter select (0=timer, 1=counter)
CAP2	capture/reload select (0=reload, 1=capture)

TH2,TL2 Timer2 register

RCAP2H,RCAP2L Timer2 Reload/Capture

P1 Port1 register

P1.2-1.7	analog/digital pins (1=analog function, 0=digital input)
T2EX	timer/counter 2 capture/reload trigger
T2	timer/counter 2 external input

P3 Port3 register

RD	external data memory read strobe
WR	external data memory write strobe
T1	timer/counter 1 external input
T0	timer/counter 0 external input
INT1	external interrupt 1
INT0	external interrupt 0
TxD	serial port transmit data line
RxD	serial port receive data line

SCON Serial communications Control register

SM0	UART mode control bits	baud rate:
SM1	00 - 8bit shift register	- F_{OSC}/12
	01 - 8bit UART	- TimerOverflowRate/32(x2)
	10 - 9bit UART	- F_{OSC}/64(x2)
	11 - 9bit UART	- TimerOverflowRate/32(x2)
SM2	in modes 2&3, enables multiprocessor communication	
REN	receive enable control bit	
TB8	in modes 2&3, 9th bit transmitted	
RB8	in modes 2&3, 9th bit received	
TI	transmit interrupt flag	
RI	receive interrupt flag	

SBUF Serial port Buffer register

PCON Power Control register

PCON.7	double baud rate control
PCON.6	enable serial interrupt (ISI) from power-down mode
PCON.5	enable interrupt 0 (INT0) from power-down mode
PCON.4	ALE disable (0=normal, 1=forces ALE high)
PCON.3	general purpose flag
PCON.2	general purpose flag
PCON.1	power-down control bit (recoverable with hard reset)
PCON.0	idle-mode control (recoverable with enabled interrupt)

PSW Program Status Word

CY	carry flag
AC	auxiliary carry flag
F0	general purpose flag 0
RS1	register bank select control bits
RS0	active register bank = [0,1,2,3]
OV	overflow flag
F1	general purpose flag 1
P	parity of ACC

DPH,DPL (DPTR) Data Pointer

ACC Accumulator

B auxiliary math register