Using LTspice for Engineered Power and MEMS Signal Chain Simulation

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Abstract

This article provides the designer with background and guidance for simulating engineered power solutions using LTspice[®]. When an engineered power solution is optimized, the complete MEMS signal chain can then be investigated using LTspice. Some sensors have digital outputs, while some sensors include analog outputs. For those with analog outputs, the entire signal chain can be simulated using LTspice, with op amp, analog-to-digital converter (ADC), and even MEMS frequency response models available.

Doing More with Less

Several standards exist for sharing power and data on the same wires. Standards include IEEE 802.3bu for power over data lines (PoDL), and IEEE 802.3af for power over Ethernet (PoE), with dedicated power interface controllers. These defined standards offer a controlled and safe power connection with detection, connection checks, classification, and turn on/off fault monitoring. The power levels range from a few watts to tens of watts, with safe power delivery. In contrast to

Signal DC Content Can Be up to 100% Filter Design for Engineered Power More Difficult

Figure 1. Possible engineered power solutions for MEMS sensors, with trade-offs in sensor solution size and design complexity.



the standardized broad application PoE/PoDL specifications, the term engineered power (EP) refers to a customized power over data lines design, typically for a single application. For example, the Hiperface DSL specification¹ couples power and data on the same wires for motor control encoder applications. Engineered power can also be used for some modern sensor systems.

Typical shared power and data interfaces are encoded to reduce signal DC content, allowing simpler system design when transmitting AC signal content. However, many digital output sensor interfaces (for example, SPI and I²C) are not encoded, with variable signal DC content, and are not a natural fit for a shared data and power design. To encode SPI or I²C would require an additional microcontroller, which increases solution cost and size, as shown in Figure 1. To remove the need for encoding and an added microcontroller, the designer must try to do more with less—which requires careful design and simulation of the engineered power circuit. The engineered power circuit consists of inductors, capacitors, and protection circuitry, which together form a filter.



Using a Microcontroller Larger Sensor Solution Signal Encoding Possible Signal DC Content Can Be 50% with Manchester Encoding Filter Design for Engineered Power Less Constrained

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Engineered Power Background

Power and data are distributed on a wire pair using an inductor capacitor network. High frequency data is coupled to the data lines through series capacitors, which also protect the communication transceiver from DC bus voltages. A power supply is connected at the main controller via an inductor connected to a data line, and the power is then filtered out using an inductor at the subnode sensor node at the far end of the cable.

The inductor-capacitor network will create a high-pass filter, so the coupling solution must be added to a data line where DC data content is not expected. However, some interfaces are not encoded at the physical layer to remove DC content—for example, SPI. In this case, the system designer needs to consider a worst-case DC content scenario, where all bits transmitted in a data frame are logic high (100% DC content). The chosen inductor will also have a specified self-resonant frequency (SRF), above which the inductance value drops and parasitic capacitance increases. As such, the engineered power circuit will act as both a low-pass and high-pass filter (band-pass). Simulation-based modeling can greatly aid the system designer in understanding this constraint.

When porting SPI over long distances, cable and components affect system clock and data synchronization. The maximum possible SPI clock is set by the system propagation delay, which includes cable propagation delay as well as main and subnode component propagation delays. While not discussed in this article, the designer should be aware of this additional constraint, with further information available in the article "Enabling Robust Wired Condition-Based Monitoring for Industry 4.0—Part 2."²

Figure 2 presents a simplified engineered power circuit, which can be used for filter or droop voltage and droop time analysis. Due to the inductance of the power over data wires network, the communication bus voltage will droop, as described in Figure 3. Droop analysis is important, as when voltage droop exceeds 99% of peak voltage, bit errors occur in a network. A system can be designed to meet specific voltage droop and time droop specifications. For example, 1000BASE-T Ethernet assumes 27% voltage droop in 500 ns,³ as shown in Figure 3.

Equation 1 through Equation 6 provide inductance and capacitance values to achieve a target voltage droop and droop time. Assuming that the change in voltage across the DC blocking capacitors is negligible during the droop time, this yields the following expression for the voltage drop for the series LR circuit:

$$\frac{V_{DROOP}}{V_{PEAK}} = 1 - e^{\frac{RT}{L}}, \text{ which simplifies to } \ln\left(1 - \frac{V_{DROOP}}{V_{PEAK}}\right) = \frac{-RT}{L} \quad (1)$$

This provides an expression for inductance based on the target droop, droop time, and resistance: $\!\!\!^4$

$$L = \frac{-R.T_{droop}}{\ln\left(1 - \frac{V_{DROOP}}{V_{PEAK}}\right)}$$
(2)

The damping ratio for a series RLC circuit is given by:

$$\zeta = \frac{R}{2} \sqrt{\frac{C}{L}} \tag{3}$$

Assuming $\zeta = 1$ for a critically damped system provides an expression for C:

$$C = \zeta^2 \frac{4L}{R^2} = -\frac{4T_{DROOP}}{R.\ln\left(1 - \frac{V_{DROOP}}{V_{PEAK}}\right)}$$
(4)

The circuit high-pass filter cutoff frequency is given by using the previous expressions for C and L:

$$\omega_0 = \frac{1}{\sqrt{LC}} = \frac{\ln\left(1 - \frac{V_{DROOP}}{V_{PEAK}}\right)}{2T_{DROOP}} \tag{5}$$

For a critically damped system:

$$\omega_0 = 2\pi f, f = \frac{\ln\left(1 - \frac{V_{DROOP}}{V_{PEAK}}\right)}{4\pi T_{DROOP}} \tag{6}$$



Figure 2. Engineered power, simplified circuit for analysis.

Why Use LTspice for Engineered **Power Simulation?**

Compelling reasons to use LTspice for engineered power simulation include:

- ► Real inductor models, including device parasitics for closer correlation between simulation and real performance. Thousands of inductor models are available in the LTspice library from a variety of well-known manufacturers such as Würth, Murata, Coilcraft, and Bourns.
- LTspice models for Analog Devices physical layer communication transceivers are available to support a variety of interface standards (CAN, RS-485), which are not commonly provided by other semiconductor manufacturers.
- The flexible LTspice waveform viewer allows for a quick numerical evaluation ► of power over data wires designs.
- LTspice enhancements mean that simulating power devices, such as LDO regulators and switching regulators, is extremely fast compared to normal SPICE simulators, allowing the user to view waveforms for most switching regulators in just a few minutes.
- The ready to run LTspice demonstration circuits reduce schematic capture time. ►
 - VDROOF V_{PEAR} /oltage, VRX TDROOF Time

(a) $V_{DROOP} = V_{PEAK} \times 73\%$, $T_{DROOP} = 500$ ns

Figure 3. Voltage droop and droop time.

V.,

V3 Pulse Is Set to the Worst-Case Bit Rate (100% DC Content) For 250 kHz, and a 16-Bit Word, This Is Equivalent to 128 µs Period, 64 µs Half Period

There are over 1000 ADI power device models and more than 200 op amp ► models and ADC models, as well as resistors, capacitors, transistors, and MOSFET models to complete the rest of your design.

Using LTspice for Droop Analysis

A simplified power over data wires simulation circuit is provided in Figure 4. This circuit uses LTC2862 RS-485 transceiver LTspice macromodels and 1 mH inductors (Würth 74477830). LTspice includes real inductor models, which include device parasitics that enable a closer correlation between simulation and real design performance. The DC blocking capacitor values are 10 µF. In general, using larger inductor and capacitor values enables a lower data rate performance on the communication network. The simulated test case is a 250 kHz data rate, which roughly corresponds to 100 meters of cabled communication² when porting clock synchronized SPI over an RS-485 interface. The input voltage waveform used in the simulation corresponds to worst-case DC content, with a 16-bit word and all logic high bits. Simulation results are presented in Figure 5 and Figure 6. The input voltage waveform (V_{N}) matches the output at the remote powered device (no communication errors). Figure 6 presents a zoomed-in view of the bus voltage differential waveform (voltage A to voltage B) for droop analysis. The voltage at the remote sensor node, extracted from the L2 inductor (V(pout)), provides a power supply rail of 5 V \pm 1 mV.





Figure 4. Engineered power LTspice simulation circuit using an LTC2862 (RS-485) and a 1 mH Würth inductor 74477830.

Remote Sensor and Power Extraction





Figure 6. Droop analysis for point X and Y.

The V_{DROOP}, V_{PEAK}, and T_{DROOP} are measured using the Figure 5 and Figure 6 LTspice waveform. The L and C values are then calculated using Equation 2 and Equation 4. The calculated L value is 1 mH to 3 mH, as shown in Table 1, but this can change depending on where you measure the waveform. Measuring at point X is most accurate and yields the correct inductance value of approximately 1 mH. The high-pass filter frequency (Equation 6) is simply a function of the droop time and voltage, and for point X the frequency approximately equates to 250 kHz/32 for 1 bit (half clock cycle), which matches the input waveform (V3) shown in Figure 5.

When running the simulation shown in Figure 4, it is worth noting that the C8 capacitor is recommended to reduce voltage overshoot at the sensor (V_{POUT} at the power extraction node). With C8 added, the overshoot is maximum 47 mV and settles to within 1 mV of the desired 5 VDC within 1.6 ms. Simulating without a C8 capacitor results in an underdamped system, with 600 mV overshoot, and a permanent 100 mV of voltage oscillation from the 5 VDC target.

The C value is 0.4 μ F to 1 μ F, as shown in Table 1. The C value is less than the 10 μ F DC blocking capacitor value, as the circuit contains additional series capacitors (1 μ F, 100 μ F) and may be overdamped, which contradicts the calculation of Equation 1 through Equation 6.

Table 1. Droop Analysis: Using V_{DROOP}/V_{PEAK} and T_{DROOP} to Determine Circuit Inductance and Capacitance

Simulation Point	Measured on LTspice Waveform				Calculated Using Equation 1 Through Equation 6		
	V _{droop} (V)	V _{peak} (V)	V _{droop} / V _{peak}	T _{droop} (µs)	R (<u>0</u>)	L (mH)	С (µF)
Х	2.85	6.06	0.47	7.54	107	1.1	0.4
γ	5.14	6.06	0.85	63.6	107	3.6	1.2

Using LTspice to Simulate More Complex Power Delivery Circuits

Adding an LDO regulator or a DC-to-DC converter at the sensor node enables power delivery from the main node at standard industrial voltage rails such as 12 VDC and 24 VDC. The selection of LDO regulator or DC-to-DC switching regulator depends on the application requirements. If an application uses a 12 VDC rail, then an LDO regulator may be suitable for ultralow noise performance, and with tolerable power dissipation at the sensor subnode. For 24 VDC rails, a higher efficiency DC-to-DC switching regulator is recommended to reduce power losses. Analog Devices' low noise Silent Switcher[®] architecture means that higher power efficiency and low noise are achievable.

24 VDC is widely used in railway, industrial automation, and aerospace & defense applications. The EN 50155 standard⁵ for railway electronics specifies a nominal input voltage of 24 VDC, but the nominal input variation is 0.7 V_{IN} to 1.25 V_{IN}, with extended ranges of 0.6 × V_{IN} to 1.4 × V_{IN} specified. So, the DC-to-DC device used in the application needs a wide 14.4 VDC to 33.6 VDC input range.

The LTM8002 Silent Switcher µModule[®] regulator is ideally suited to space constrained vibration sensors used in railway rolling stock monitoring, with 6.25 mm × 6.25 mm BGA packaging, and a wide 3.4 VDC to 40 VDC input range.

Figure 7 repeats the Figure 4 schematic, with the LTM8002 added and a 24 VDC supply from the main to the subnode sensor. Simulation shows a 1 ms ramp time to the desired 5 VDC \pm 1% output voltage on the LTM8002. It is suggested

that the designer implement a 2 ms to 3 ms time delay at power-up, before initiating communication between the main node and subnode. This will ensure valid data at the sensor node output.



Figure 8.1 ms ramp time to the desired 5 VDC on V_{POUT} , and valid data at V_{OUT} after 2 ms to 3 ms.

Complete MEMS Signal Chain Simulation

Analog Devices has many design notes to help the designer to complete the MEMS signal chain design and simulate it using LTspice (see Figure 9). While many MEMS are digital out, there are also many high performance sensors with analog output. Simulating the op amp and ADC signal chain can provide valuable insights before completing hardware design builds.

To analyze the effects of low-pass filtering, amplifier, and ADC inputs on sensor data, the designer can refer to the LTspice reference circuit provided by Gabino Alonso and Kris Lokere.⁸ Simulation models for the AD4002 and AD4003 18-bit SAR ADCs are available, as well as the 16-bit LTC2311-16. To develop custom ADC models using LTspice, Erick Cook provides a good practical guide.⁷

Over 200 operational amplifier models are available, including the ADA4807 and ADA4805 series. Voltage reference macromodels, such as the ADR4525 and LTC6655-5 are available, as well as the ADA4807-1 reference buffer.

Simon Bramble describes how to use LTspice to analyze the frequency content of vibration data in his article on condition-based monitoring systems.⁸ Simon's article contains helpful tips to format and analyze captured sensor data.

Figure 10 shows an example LTspice model for the frequency response of the ADXL1002 low noise, ±50 g MEMS accelerometer. Using a series LRC circuit in the LTspice Laplace format is a good approximation for the frequency response of MEMS. The simulation model shows good agreement with the data sheet typical performance, with a resonant frequency of 21 kHz and 3 dB at 11 kHz. For AC analysis, it's best to use a Laplace circuit in LTspice, but for transient analysis, discrete RLC components should be used for best simulation performance.



Figure 9. A complete sensor signal chain simulation using LTspice (simplified diagram-all connections and passive components are not shown).



Figure 10. (a) A Laplace model for a MEMS frequency response, and (b) a plot showing 21 kHz resonance and 3 dB at 11 kHz.

For analog-output accelerometers, such as the ADXL1002, bandwidth is defined as the signal frequency at which the response falls to -3 dB of the response to DC (or low frequency) acceleration. Figure 11 repeats the MEMS frequency response model of Figure 10, but also includes an op amp filter circuit. Using this filter circuit, more of the MEMS frequency response can be measured within 3 dB. The plot shows that the V_{OUT} from the op amp is at 3 dB at 17 kHz, compared to an unfiltered MEMS output with 3 dB at 11 kHz.

Figure 12 includes the MEMS input model (the discrete RLC from Figure 10), op amp filtering, and a 16-bit LTC2311-16 SAR ADC model. The complete signal chain can be built and simulated using a modular approach, with wired interface and engineered power added as a distinct block.

With a transient simulation, the LTC2311-16 DIGITAL_OUT node can be probed to view the digital output corresponding to the MEMS voltage input (V_{IN}). The LTC2311-16 LTspice model can be modified to reduce to the serial clock and CNV interface timing, and the digital output reference OV_{DD} can be changed to anywhere in the 1.71 V to 2.5 V range. Some RS-485 transceivers, such as the LTC2865, include a logic interface pin, VL, which can be operated at 1.8 V or 2.5 V, providing a perfect match for wired streaming of ADC digital output data. The RS-485 interface can then be powered separately at 3.3 V or 5.0 V using the LTC2865 V_{CC} pin, providing a higher voltage cable drive.



Figure 11. (a) A MEMS frequency response and filter model, and (b) a 3 dB point pushed to 17 kHz (compared to Figure 10b at 11 kHz).



Figure 12. A MEMS input model (the discrete RLC from Figure 10), op amp filtering, and a 16-bit LTC2311-16 SAR ADC model.



Figure 13. Input voltage from the MEMS model (VIN), and the filtered, digitized output voltage (DIGITAL_OUT).

Reference MEMS and Engineered Power Evaluation Platform

Analog Devices' wired, condition-based monitoring platform provides an industrial wired link solution for the ADcmXL3021 triaxial vibration sensor. The hardware signal chain consists of the ADcmXL3021 accelerometer, with SPI and interrupt outputs attached to interface PCBs, translating SPI to an RS-485 physical layer over meters of cabling to a remote main controller board. The SPI to RS-485 physical layer translation can be achieved using isolated or nonisolated interface PCBs, which include *i*Coupler[®] isolation (ADuM5401/ADuM110N0) and RS-485/RS-422 transceivers (ADM4168E/ADM3066E). This solution combines power and data over one standard cable (engineered power), which reduces cable and connector costs at remote MEMS sensor nodes. A dedicated software GUI enables simple configuration of the ADcmXL3021 device, and vibration data capture over long cables. GUI software enables data visualization as raw time domain or FFT waveforms.



Figure 14. Wired vibration monitoring with power over data wires.

Conclusion

Modern MEMS sensor solutions are small and highly integrated, and are placed close to the vibration source to measure the vibration frequency. Changes in the frequency over time indicate issues with the vibration source (motor, generator, etc.). The frequency measurement is essential for CbM. Using an engineered power solution saves on connector count and cable costs at the MEMS sensor. LTspice is a powerful and free simulation tool that can be used to simulate engineered power designs. Thousands of power device models, including the LTM8002 Silent Switcher device, can be used to complete the rest of your design. A complete MEMS signal chain simulation is possible, with ADC, op amp, and MEMS models available.

References

¹Hiperface DSL[®]—the Digital Evolution. SICK Sensor Intelligence, October 2020.

² Richard Anslow and Dara O'Sullivan. "Enabling Robust Wired Condition-Based Monitoring for Industry 4.0—Part 2." Analog Devices, Inc., November 2019.

³"IEEE 802.3bu-2016—IEEE Standard for Ethernet—Amendment 8: Physical Layer and Management Parameters for Power over Data Lines (PoDL) of Single Balanced Twisted-Pair Ethernet." IEEE, February 2017.

⁴Andy Gardner. "PoDL: Decoupling Network Presentation." Linear Technology, May 2014.

⁵"EN 50155:2017 Railways Applications Electronic Equipment Used on Rolling Stock."

⁶Gabino Alonso and Kris Lokere. "LTspice: Simulating SAR ADC Analog Inputs." Analog Devices, Inc., November 2017.

⁷Erick Cook. "Use LTspice to Simulate Mixed Continuous and Sampled Systems." *EDN Asia*, January 2020.

⁸Simon Bramble. "Using LTspice to Analyze Vibration Data in Condition-Based Monitoring Systems." Analog Dialogue, Vol. 54, No. 2, June 2020.

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