

# Unlock Higher Data Transfer Speeds by Upgrading to the JESD204B/ JESD204C Interface

#### Nikhil Ahuja, Product Applications Engineer

# Abstract

This article provides an overview of the JESD204B/JESD204C interface on the ultrawideband direct RF sampling high speed data converters and how to implement these interfaces to enable higher data transfer speeds. It explains how high speed data converters with the JESD204B/JESD204C interface add value to the end system application. It describes the role of each implementation layer and highlights FPGA IP, tools, and platform solutions to enable a seamless upgrade as well as an optimal approach to debugging once an interface has been implemented.

### Interfacing with High Speed Data Converters

As data converters continue to support faster sample rates and higher resolutions, signal integrity concerns at higher data transfer speeds mean traditional input/ output (I/O) technologies are unable to meet today's bandwidth requirements.

Furthermore, high speed data converters have increasingly taken on more of the system workload by incorporating power-optimized digital signal processing (DSP) engines. The receive path includes highly configurable digital downconverters

(DDCs), programmable finite impulse response (FIR) filters, and automatic gain control (AGC). The transmit path features digital upconverters (DUCs), programmable delays, and transmit digital predistortion (DPD) support. This functionality can be offloaded from the FPGA or the ASIC to the converter. This results in a higher bandwidth system and a great SWaP (size, weight, and power).

The JESD204B and JESD204C standards are designed to meet the demands of next-generation data converter applications. They leverage high bandwidth serializer/deserializer (SerDes) based interfaces along with protocol-level encoding, scrambling, and synchronization techniques to enable transfer rates up to 32.5 Gbps with a reduced number of differential interconnects.

Figure 1 shows a typical high speed converter to FPGA interface, such as the one on the latest addition to Analog Devices' MxFE<sup>®</sup> family of products that can support a maximum of 24 JESD204C differential parallel lanes each for transmit and receive, each capable of moving data at a maximum of 32.5 Gbps for a net throughput of almost 800 Gbps simultaneously in each direction.



JESD204B/JESD204C Transmit and Receive Interface

Figure 1. Interfacing with high speed data converters.

# Implementing the JESD204B/JESD204C Interface on an FPGA

The flow of data over the interface between the ADC, DAC, or MxFE to an FPGA is governed by the JESD204B or JESD204C standards.

For JESD204B, the transmitter in the system assembles parallel data into frames and uses 8-bit/10-bit encoding and optional scrambling to form serial output data. The initial link establishment requires special control characters to be sent and received for synchronization. Additional control characters are embedded in the data stream to maintain synchronization.

While the JESD204B protocol lane rates are limited to 16 Gbps, the JESD204C protocol supports lane rates up to 32.75 Gbps. JESD204C uses a 64-bit/66-bit encoding scheme that provides a much higher encoding efficiency and uses an entirely feed-forward synchronization process, eliminating the need for a handshaking process for initial link synchronization.

Figure 2 shows the data path that can be broadly split into four layers, with each layer performing specific tasks within a design.

# JESD204B/JESD204C FPGA IP

To help accelerate the development of a system that requires interfacing with high speed data converter products with JESD204B/JESD204C, there is FPGA IP from ADI as well as FPGA vendors for each layer in the data path. While the eventual selection will depend on the software/hardware decisions relevant to the system, the FPGA IP modules are built to be flexible enough to allow a mix-and-match approach to arrive at the best possible solution.

#### 1. PHY Layer

The physical layer (PHY layer) enables the movement of protocol frames at the specified line rate using the SerDes. It includes transmit drivers, receiver equalizers, and clock and data recovery circuits.

The physical layer often requires hardened transceiver IP and is FPGA device dependent. Therefore, the FPGA manufacturer and the FPGA product family determine what can be used. The AMD Xilinx high speed serial transceivers (GTX, GTH, GTY, GTY-P series) and Intel<sup>®</sup> transceiver phy (L-Tile, H-Tile, E-Tile series) are options available on their FPGA devices. The transceivers become an essential metric in deciding if an FPGA device is suitable for the end applications, since they are rated for different maximum values.

#### 2. Data Link Layer

The data link layer takes care of 8-bit/10-bit or 64-bit/66-bit encoding/decoding based on the protocol selection, descrambles, lane aligns, and defames lane data. For JESD204B, it performs frame alignment character replacement. For JESD204C, it performs multiblock and extended multiblock alignment required to synchronize data over the link.

The ADI JESD204B/JESD204C transmit link layer and ADI JESD204B/JESD204C receive link layer IPs are optimized for interoperability with ADI high speed data converter products and unencrypted RTL and IP drivers are available to use in FPGA designs to interface with ADI high speed data converter products.

For the data link layer, the AMD Xilinx FPGA JESD204 or Intel FPGA JESD204 framer and deframer IPs can also be used.

#### 3. Transport Layer

The transport layer converts lane data back to ADC sample data on the transmit path or DAC pattern data into lane data on the receive path. The configuration determines the sample data format.

The ADI ADC companion transport layer RTL generator and the ADI DAC companion transport layer RTL generator are script-based tools that generate the transport layer based on an input list of desired JESD204B/JESD204C modes. They support all possible modes offered by high speed data converter products.

For designs that only need support for a single mode set at compile time, the ADI ADC transport peripheral and ADI DAC transport peripheral can be used.

#### 4. Application Layer

The application layer enables any preprocessing or postprocessing of data to facilitate a specific feature set or a more efficient way to handle data in an end application.

In most cases, the application layer code is specific to a customer application. However, ADI has FPGA IP to support certain advanced use cases, which can be made available to customers on request.

The aforementioned FPGA IPs are available as part of FPGA reference designs or as standalone IPs modules that can be used in custom designs that use ADI high speed data converter products. These reference designs are supported on multiple custom ADI FPGA platforms and commercial off-the-shelf (COTS) FPGA platforms.



Figure 2. The JESD204B/JESD204C data path layers.

The ability to evaluate features and performance of high speed ADC, DAC, and MxFE family of products is instrumental in a customer's journey towards product integration. High speed data converter evaluation boards interface with an FPGA-based data controller board, allowing users to capture samples from an ADC or transmit samples to the DAC.

For ADI high speed data converter products, the JESD204B or JESD204C data interface and other I/O control interfaces are routed over a FMC or a FMC+ connector, leveraging the VITA57.4 high pin count connector standard. The hardware components are supported by FPGA and software solution options targeted to ease customer adoption.

#### ADI FPGA Platforms

ADI's FPGA evaluation platforms (ADS7-V2 EBZ, ADS8-V1 EBZ, ADS8-V3 EBZ, and ADS9-V2 EBZ are the four active versions with an ADS10-V1 EBZ in the pipeline) are well-suited for product evaluation and building a proof of concept design based on the end customer application.

Figure 3 shows an ADS9V2-EBZ FPGA evaluation board used to interface with the MxFE family of products. It features an AMD Xilinx Kintex<sup>®</sup> UltraScale+<sup>™</sup> FPGA that supports twenty 28 Gbps transceivers connected over one FMC+ connector; HMC DRAM modules to capture the high data throughput; a power distribution network, and a scalable clocking architecture that enables deterministic link latency support.



Figure 3. An ADS9v2 FPGA platform and its components.

Each data converter product page lists the recommended FPGA evaluation boards for the product and is supported by a FPGA binary file and its corresponding software suite. The FPGA source code includes highly configurable RTL with multimode support for the JESD204B/JESD204C data path. It also provides RTL for memory controllers, embedded C drivers, and state machines to control the establishment of the link and the flow of data. The FPGA source code for high speed data converter products with JESD204B/JESD204C interfaces can be requested directly from ADI.

# **COTS FPGA Platforms**

There is also the option to use an off-the-shelf AMD Xilinx or Intel FPGA board that supports the desired line rate and memory bandwidth requirements and has adequate logic and I/O resources. ADI provides reference designs for a subset of these compatible boards suitable for product evaluations and building proof of concept designs. These designs include ADI JESD204B/JESD204C IP, drivers, and a software stack that enables the movement of data to and from these boards over Ethernet.

The FPGA reference code and software infrastructure, including drivers and detailed documentation can be downloaded as example projects on the Analog Devices Wiki.

# ADI JESD204B/JESD204C Tools

In addition to the FPGA IP offerings and evaluation boards, ADI has a variety of development tools to expedite implementation of the JESD204B/JESD204C interface.

#### **IBIS-AMI Models**

The IBIS-AMI models can be used to model the high speed serializer and deserializer links that include transmitter and receiver equalization algorithms. ADI's high speed converter product pages list IBIS-AMI models, based on the SerDes PHY IP used.

#### **JESD Mode Selector Tool**

The JESD204B/JESD204C Mode Selector Tool is a command line-based tool that can narrow down the number of modes required to support a specific end application use case. The tool guides the user through a use case description flow chart and identifies the relevant transmit and receive modes based on system design.

#### **JESD204 Frame Mapping Table Generator**

The JESD204x Frame Mapping Table Generator enables a better understanding of the way data converter samples are arranged, by allowing the user to input any valid combination of the JESD204B/JESD204C parameters (L, M, F, S, NP) and outputs to a file, the frame mapping of the mode in table format.

# Debugging the JESD204B/JESD204C Interface

In addition to debug register fields and test modes available in ADI's high speed data converters, each protocol layer IP block has features that can be enabled to help with debugging a the JESD204B/JESD204C interface once it is implemented within a system.

#### **PHY Layer Debug**

The physical interface between high speed data converters and FPGAs has high speed signals, with fast rising and falling edges moving across parallel lanes on a board. While debugging a JESD204B/JESD204C link, there are two recommended debug points for the PHY layer.

#### **Serializer Deserializer Clocking**

A phase-locked loop (PLL) synthesizer produces the high speed clock that drives the serial transmitter and receiver path on both the FPGA and high speed data converters. The PLL is a crucial block of the clock data recovery (CDR) circuit and is usually driven by a reference clock that has a defined relationship with the line rate. The ADI data converters and the FPGA IP both have the provision to check for PLL lock. In cases where this reference clock isn't set to the correct rate, the PLL will be unlocked.

#### Pseudo Random Binary Sequence (PRBS) Patterns

PRBS patterns can be used to test how the high speed parallel lanes moving data between the data converter and the FPGA affect all possible data patterns. In addition, they are a valuable tool for testing the signal integrity of the physical interface. ADI's ADC, DAC, and MxFE family of products supports PRBS modes (PRBS7, PRBS15, and PRBS31) that can be run at the maximum rate supported by the product.

The FPGA transceiver PHY IP options for FPGAs from AMD Xilinx and Intel also have built-in PRBS modes. In addition, they also have standalone signal integrity IP blocks (Xilinx iBERT) that can be used. The IPs also have preemphasis, postemphasis, and voltage swing settings that can be adjusted to offset some signal integrity issues.

# Data Link Layer Debug

The process of the JESD204B/JESD204C link establishment involves a synchronization sequence which, if not completed correctly, will lead to a failure in the link being established. For JESD204B use cases or designs, code group synchronization (CGS), initial lane synchronization (ILAS), and the physical sync signal must be monitored to ensure the link is established. In the case of JESD204C, it is the sample header (SH) lock and the extended multiblock (EMB) lock. There are two recommended debug points for the data link layer.

#### JESD204B/JESD204C Mode Mismatch

Since the selected mode (L, M, F, S, K, and other parameters) determines how the link layer encodes and decodes the data sent over the interface, the FPGA and the data converters need to be set up in the same mode. In cases where there are inconsistencies in data that are not coming from the physical link, it is helpful to verify that the JESD204B/JESD204C parameters are set up correctly.

#### JESD204B/JESD204C Lane Mapping Mismatch

Routing the high speed physical parallel lanes between the data converter and the FPGA can be challenging. A crossbar that allows routing physical lanes to logical lanes on a receiver and logical to physical lanes on a transmitter can be used to ease the restrictions on routing. If a lane mapping crossbar is used the link not being established could result from a lane mapping mismatch, and confirming mapping could be a practical debug step.

#### **Transport Layer Debug**

The transport layer is responsible for translating between lane data and sample data. In a case where there are inconsistencies in the data output from the transport layer, there is one recommended debug approach.

#### **Pattern Mode**

ADI's ADCs have built-in test modes that can generate a few different kinds of predefined digital patterns and user-defined patterns. These patterns are easier to interpret on the output and, therefore, well-suited for detecting errors in the FPGA receive transport layer.

In the case where the FPGA transmit transport layer is responsible for generating the correct lane data from sample data using a known pattern as its input can prove helpful as a debug step as well.

#### **Error Monitoring**

In addition to link establishment, the high speed data converters and the FPGA IP modules can report any errors on the link while the data is being transmitted or received. This knowledge is beneficial for link monitoring and provides an additional level of system debugging.

## Conclusion

As the next generation of wideband RF transmitters and receivers evolves to meet ever-increasing sample rate and throughput demands, ADI's high speed ADC, DAC, and MxFE family of products enabled by the JESD204B/JESD204C interface running at speeds up to 32.75 Gbps remains an integral part of the solution. With a wealth of design resources readily available such as FPGA reference designs, FPGA IP modules, cutting-edge tools, and support, designers can save significant development time and seamlessly upgrade to a high speed data converter with the JESD204B/JESD204C interface.

For a deep dive into the JESD204B or the JESD204C protocol, please refer to the JESD204B Survival Guide or the JESD204C Primer.

For more information on JESD204 and its implementation in ADI products, please visit ADI's JESD204 serial interface page. For more information on ADI's high speed converters, visit our RF converters page.

#### About the Author

Nikhil Ahuja is a product applications engineer for the Advanced Data Converters Systems Group based in North Carolina. He has worked at ADI since 2016, enabling customers to integrate ADI's high speed data converters and MxFE family of products into their systems. Nikhil earned his bachelor's degree in electrical engineering from the NorthCap University, India, and a master's degree in computer engineering from North Carolina State University.

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