Understanding and Designing Differential Filters for Communications Systems

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When it comes to communication systems, differential circuits can always provide better performance over single-ended circuits. They can provide higher linearity, immunity to common-mode interference signals, and more. However, there is often a lot of mystery around differential circuits. Some RF engineers feel they're difficult to design, test, and debug. This seems to be especially true of the differential filter. It's time to lift the veil off of differential filter design.

To do that, we'll start with a communication system receive chain IF stage filter. We'll look at some basic filter key specifications concepts, a few types of frequently used filter responses, a Chebyshev Type 1 filter application, and how to start with single-ended filter design then transfer that to a differential filter design. We'll also examine a differential filter design example as well as a few points on how to optimize differential circuit PCB design.

Differential Circuits Advantages in RF Signal Chain Applications

The user can get higher signal amplitude with a differential circuit than with a single-ended circuit. With the same power supply voltage, a differential signal can provide double the amplitude as compared to a single-ended signal. It also provides better linearity and SNR performance.

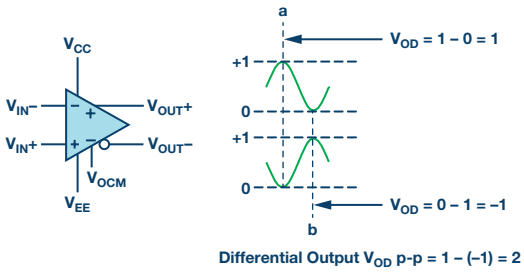

Figure 1. Differential output amplitude.

Differential circuits are fairly immune to outside EMI and crosstalk from nearby signals. This is because the received voltage is doubled—and, theoretically, the noise affects the tightly coupled traces equally, canceling each other out.

Differential signals also tend to produce less EMI. This is because the changes in signal levels (dV/dt or dI/dt) create opposing magnetic fields, again canceling each other out.

Differential signals can reject even-order harmonics. This is shown in the following example with a continuous wave (CW) passing through one gain stage. When using one single-ended amplifier, the output can be expressed, as shown in Figure 2, Equation 1, and Equation 2.

Figure 2. Single-ended amplifier.

$$V_{OUT} = \sum C_n V_{IN}^{\,n} \tag{1}$$

$$V_{OUT} = C_0 + C_1 \cos\omega t + C_2 (\cos\omega t)^2 + C_3 (\cos\omega t)^3 + \ldots \tag{2}$$

When using one differential amplifier, the input and output are shown in Figure 3 and Equations 3, Equation 4, Equation 5, and Equation 6.

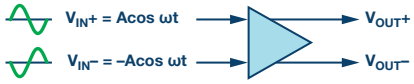

Figure 3. Differential Amplifier

$$V_{OUT} = V_{OUT}^{+} - V_{OUT}^{-} = \sum [C_n (V_{IN+})^n - C_n (V_{IN-})^n \tag{3}$$

$$V_{OUT}^{+} = C_0 + C_1 \cos\omega t + C_2 (\cos\omega t)^2 + C_3 (\cos\omega t)^3 + \ldots \tag{4}$$

$$V_{OUT}^{-} = C_0 + C_1 (-\cos\omega t) + C_2 (-\cos\omega t)^2 + C_3 (-\cos\omega t)^3 + \ldots \tag{5}$$

$$V_{OUT} = 2C_1 \cos\omega t + 2C_3 (\cos\omega t)^3 + \ldots \tag{6}$$

Ideally, the output does not have any even-order harmonics, making a differential circuit a better choice for a communication system.

Filters

Filter Specification

Cutoff frequency, corner frequency, or break frequency is a boundary in a system's frequency response at which energy flowing through the system begins to be reduced (attenuated or reflected) rather than passing through.

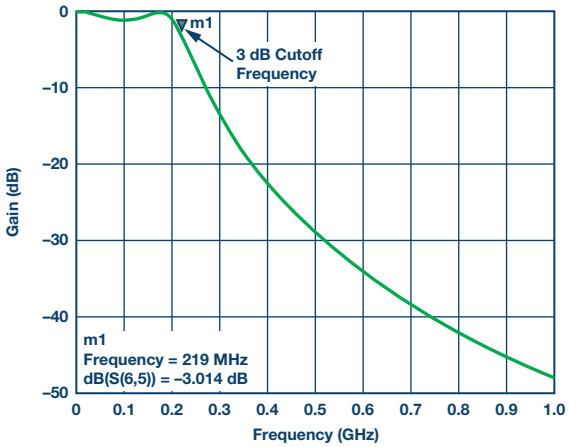

Figure 4. 3 dB cutoff frequency point.

In-band ripple is the fluctuation of insertion loss within the pass band.

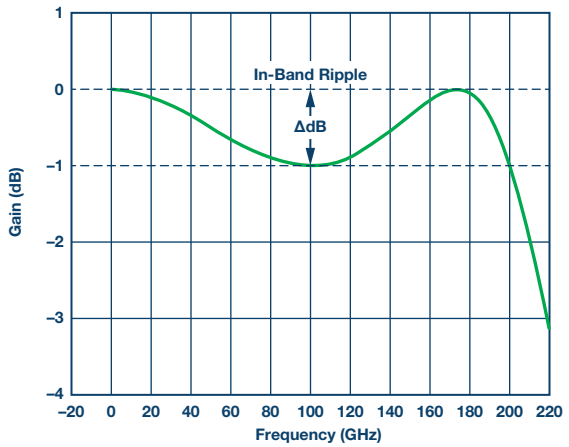

Figure 5. In-band ripple.

Phase linearity is the direct proportionality of phase shift to frequency over the frequency range of interest.

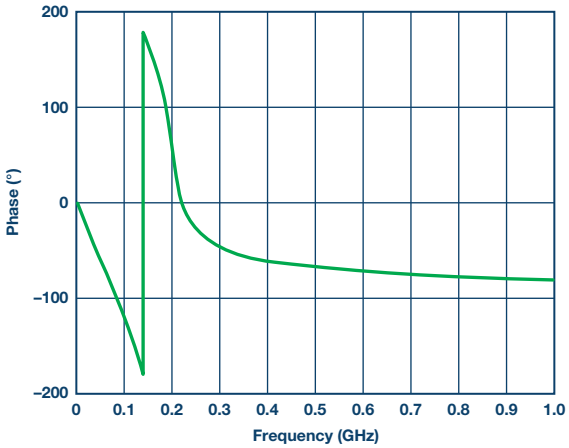

Figure 6. Phase linearity.

Group delay is a measure of the time delay of the amplitude envelopes of the various sinusoidal components of a signal through a device under test, and is a function of frequency for each component.

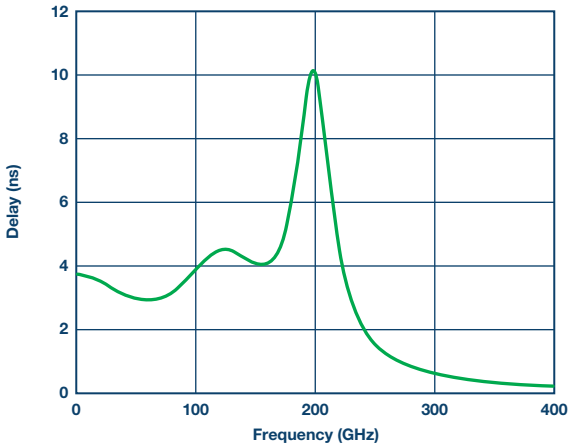

Figure 7. Group delay.

Filter Comparison

Table 1. Filters Comparison

S21 Response	Pros	Cons
Butterworth		
See Figure 8	Very good flatness in pass band	Rolls off slowly in stop band
Elliptic		
See Figure 9	Rolls off very quickly in close in stop band	Has equalized ripple in both pass band and stop band; this affects the stop band rejection performance
Bessel		
See Figure 10	Maximum flat group/phase delay	Very slow roll-off in stop band
Chebyshev Type I		
See Figure 11	Roll off quickly in stop band; no equalized ripple in stop band	Has equalized ripple in pass band
Chebyshev Type II		
See Figure 12	No ripple in pass band	Roll-off is not very fast; has equalized ripple in stop band

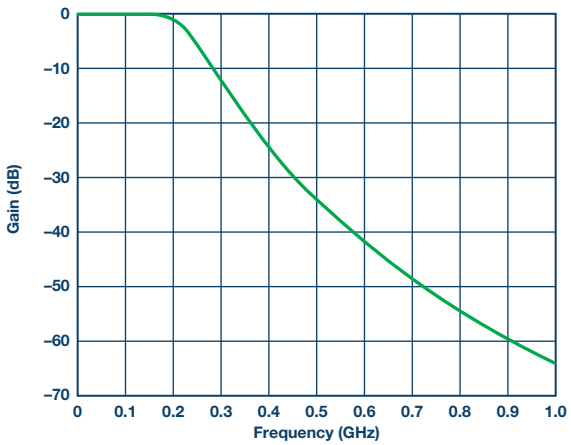

Figure 8. Butterworth filter S21 response.

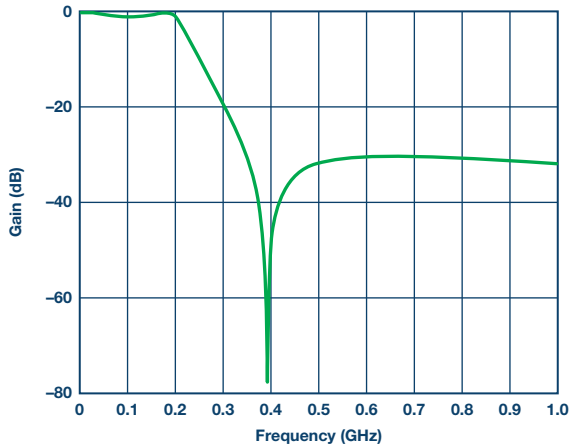

Figure 9. Elliptic filter S21 response.

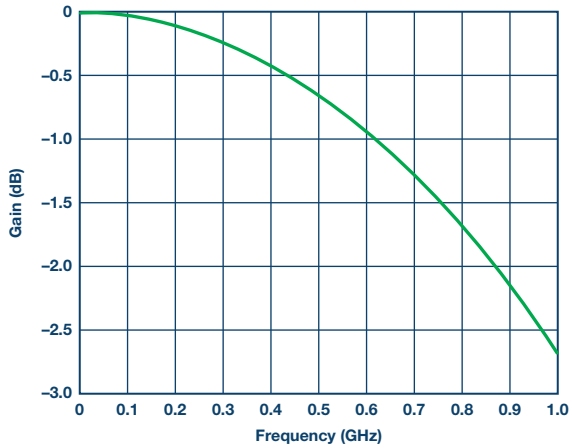

Figure 10. Besel filter S21 response.

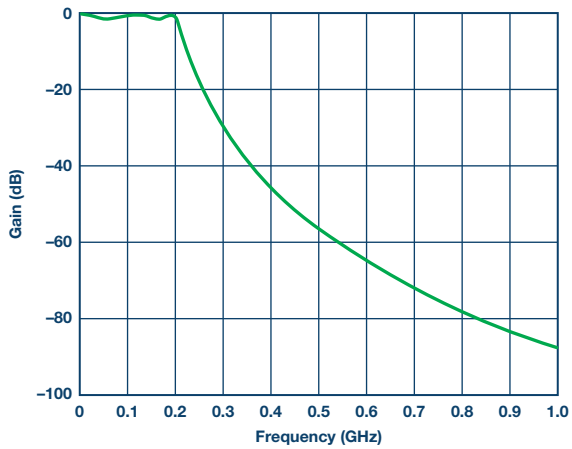

Figure 11. Chebyshev Type I filter S21 response.

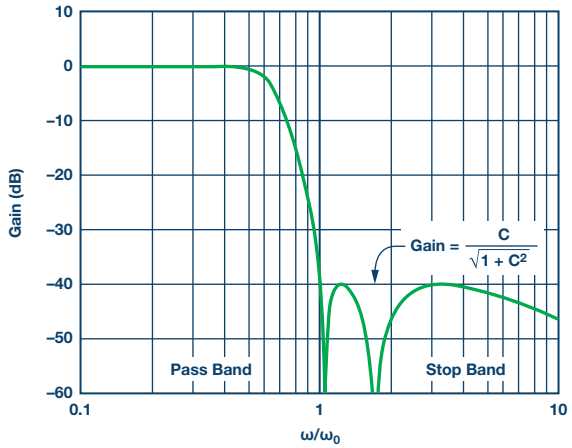

Figure 12. Chebyshev Type II filter S21 response.

The IF filter in a communications receive chain is basically a low-pass filter or band-pass filter. It is used for rejecting the aliasing signals along with the spurs generated by active components. The spurs include harmonics and IMD products, among others. With the filter, the receive chain can provide high SNR signals for the ADC to analyze.

The Chebyshev Type I filter was chosen as the topology because it has good in-band flatness, quick roll-off, and no equiripple response in the stop band.

Designing a Low-Pass Filter

Because the receiver IF filter is used to reject spurs and aliasing signals, its stop band roll-off should be as fast as possible. However, faster roll-off means higher order components, and there are a few reasons high order filtering is not recommended:

- Difficulty for tuning at design and debug stage.
- Difficulty in mass production: capacitors and inductors have part-to-part variation and it is difficult for filters on each PCB board to have the same response.
- Large PCB size.

In general, use a seventh-order or lower filter. At the same time, if bigger in-band ripple isn't a problem with the same order components, then faster roll-off in the stop band is a payout.

Then, define the response needed by specifying the required attenuation at a selected frequency point.

To determine the maximum amount of ripple in the pass band, keep the specification to the maximum limit of the system requirement. This can help get faster roll-off in the stop band.

Use filter software, such as MathCad,® MATLAB,® or ADS to design the single-ended low-pass filter.

Alternatively, design the filter manually. A useful guide is *RF Circuit Design* by Chris Bowick.

To determine the orders of the filter, normalize the frequency of interest by dividing it with the cutoff frequency of the filter.

$$Frequency\ ratio = \frac{f}{f_c}$$

For example, if the in-band ripple needs to be 0.1 dB, the 3 dB cutoff frequency is 100 MHz. At 250 MHz the rejection needs to be 28 dB so the frequency ratio is 2.5. A third-order low-pass filter can meet this requirement. If the source impedance of the filter is 200 Ω, the load impedance of the filter is also 200 Ω, RS/RL is 1—use a capacitor as the first component. Then, the user receives a normalized C1 = 1.433, L2 = 1.594, C3 = 1.433. If the fc is 100 MHz, use Equation 7 and Equation 8 to get finalized results.

$$C_{SCALED} = \frac{C_n}{2\pi f_c R_L} \quad (7)$$

$$L_{SCALED} = \frac{L_n R_L}{2\pi f_c} \quad (8)$$

Where:

C_{SCALED} is the final capacitor value.
L_{SCALED} is the final inductor value.
C_n is a low-pass prototype element value.
L_n is a low-pass prototype element value.
R_L is the final load resistor value.
f_c is the final cutoff frequency.

$C1_{SCALED} = 1.433/(2\pi \times 100 \times 10^6 \times 200) = 11.4$ pF
$L2_{SCALED} = (1.594 \times 200)/(2\pi \times 100 \times 10^6) = 507.4$ nH
$C3_{SCALED} = 11.4$ pF

The circuit is shown in Figure 13.

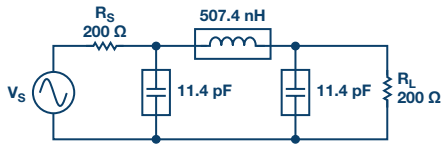

Figure 13. Single-ended filter example.

Convert the single-ended filter into a differential filter (see Figure 14).

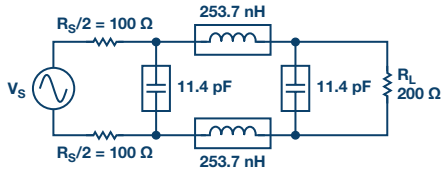

Figure 14. Converting single-ended filter into differential filter.

Using the real-world value for each component, the filter is updated as shown in Figure 15.

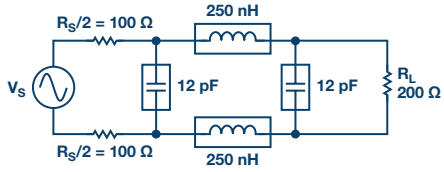

Figure 15. Final differential filter.

Note that, if the output impedance of the mixer or IF amplifier and the input impedance of ADC are capacitive, it is better to consider using a capacitor as the first component and a capacitor as the last component. Also, it is important to tune the first capacitor and last stage capacitor value at a higher rate (at least 0.5 pF) than the capacitance of the output impedance of the mixer or IF amplifier and input impedance of the ADC. Otherwise, it is very difficult to tune the filter response.

Designing a Band-Pass Filter

In communication systems, when the IF frequency is quite high, some low frequency spurs need to be filtered out, such as the half IF spur. To do this, design a band-pass filter. For a band-pass filter, it is not necessary to be symmetrical for low frequency and high frequency rejection. The easy way to design a band-pass antialiasing filter is to design a low-pass filter first, then add one shunt inductor in parallel with the shunt capacitor at the final stage of the filter to limit low frequency components (a shunt inductor is a high-pass resonance pole). If a one stage, high-pass inductor is not enough, add one more shunt inductor parallel with the first stage shunt capacitor to get more rejection for low frequency spurs. After adding the shunt inductor, tune all components again to achieve the correct out-of-band rejection specification, and then finalize the filter components value.

Note that, in general, for a band-pass filter, serial capacitors are not recommended because they increase tuning and debugging difficulty. The capacitance value is usually quite small and it is heavily affected by parasitic capacitance.

Application Example

Here is an example of filter design between the ADL5201 and AD6641. The ADL5201 is a high performance IF digitally controlled gain amplifier (DGA), which is designed for a base station real IF receiver application or a digital predistortion (DPD) observation path. It has a 30 dB gain control range, very high linearity whose OIP3 reaches 50 dBm, and a voltage gain of about 20 dB. The AD6641 is a 250 MHz bandwidth DPD observation receiver that integrates a 12-bit, 500 MSPS ADC, a 16,000 × 12 FIFO, and a multimode back end that allows users to retrieve the data through a serial port. This filter example is a DPD application.

The following are some of the band-pass filter specifications taken from a real communication system design:

- Center frequency: 368.4 MHz
- Bandwidth: 240 MHz
- Input and output impedance: 150 Ω
- In-band ripple: 0.2 dB
- Insertion loss: 1 dB
- Out-of-band rejection: 30 dB at 614.4 MHz

To build the example design:

1. Start with a single-ended, low-pass filter design (see Figure 16).

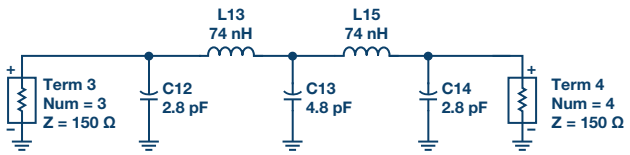

Figure 16. Single-ended, low-pass filter.

2. Change the single-ended filter into a differential filter. Keep the source and load impedance the same, shunt all capacitors, and cut all serial inductors in half and put them in the other differential path (see Figure 17).

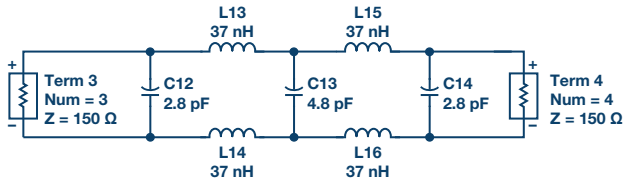

Figure 17. Differential low-pass filter with ideal components.

3. Optimize the components' ideal value with real-world value (see Figure 18).

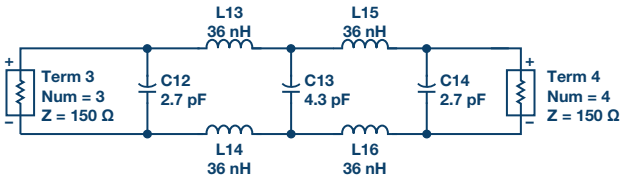

Figure 18. Differential low-pass filter with real-world value.

4. For subsystem level simulation, add the ADL5201 DGA S parameter file at the input, use the voltage control voltage source to model the AD6641 ADC at the output of the filter. To change the low-pass filter into a band-pass filter, add two shunt inductors: L7 in parallel with C9 and L8 in parallel with C11. C12 represents the AD6641 input capacitance. R3 and R4 are two load resistors put at the input of AD6641 to be the load of filter. The AD6641 input is high impedance. After tuning, see Figure 19.

5. The simulation results with ideal components are shown in Figure 20.

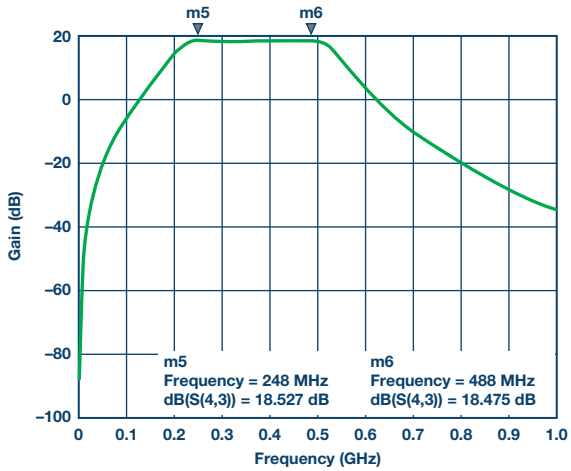

Figure 20. Filter transmission response with ideal inductors.

6. Replace all ideal inductors with the inductor S parameter files of the intended device (for example, Murata LQW18A). The insertion loss is a little bit higher than using ideal inductors. The simulation result changes slightly, as shown in Figure 21.

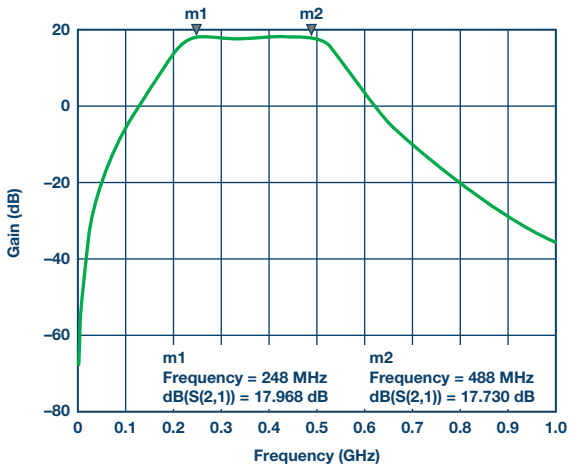

Figure 21. Filter transmission response with Murata LQW18A inductors.

Differential Filter Layout Consideration

The differential traces in a pair need to be of equal length. This rule originated from the fact that a differential receiver detects where the negative and positive signals cross each other at the same time—the crossover point. Therefore, the signals arrive at the receiver at the same time for proper operation.

The traces within a differential pair need to be routed close to each other. The coupling between the neighboring lines within a pair is small if the distance between them is >2× the dielectrical thickness. Also, this rule is based upon the fact that because the differential signals are equal and opposite, and if external noise interferes with these signals equally, the noise is nullified. Similarly, any unwanted noise induced by the differential signals into adjacent conductors is canceled if traces are routed side by side.

The trace separation within a differential pair needs to be constant over its entire length. If the differential traces are routed close together, they will impact the overall impedance. If this separation is not maintained from the driver to the receiver, there are impedance mismatches along the way, resulting in reflections.

Use a wide pair-to-pair spacing to minimize crosstalk between pairs.

If using copper fill on the same layer, increase the clearance from the differential traces to the copper fill. A minimum clearance of 3× the trace width from the trace to the copper fill, is recommended.

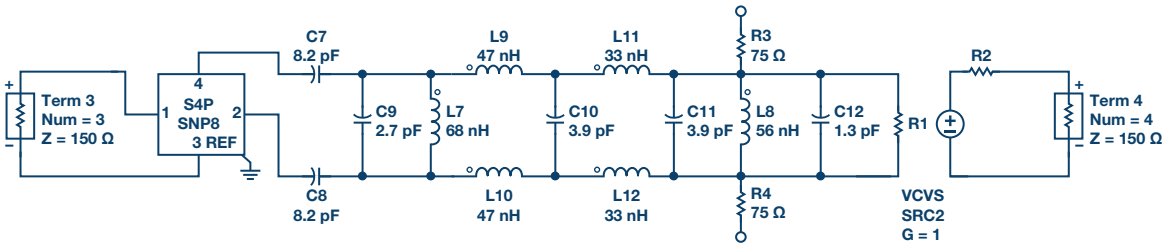

Figure 19. Differential band-pass filter.

Reduce intra pair skew in a differential pair by introducing small, meandering corrections close to the source of the skew (see Figure 22).

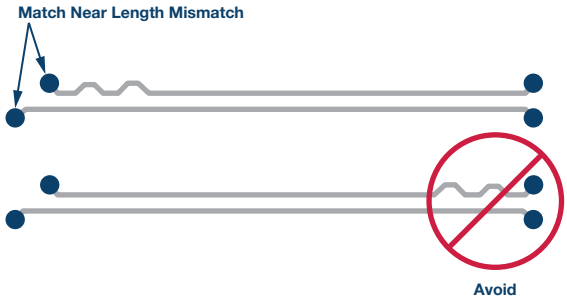

Figure 22. Using meandering corrections.

Avoid tight (90°) bends when routing differential pairs (see Figure 23).

Figure 23. Avoid 90° bends.

Use symmetric routing when routing differential pairs (see Figure 24). If test points are required avoid introducing trace stubs and place the test points symmetrically (see Figure 25).

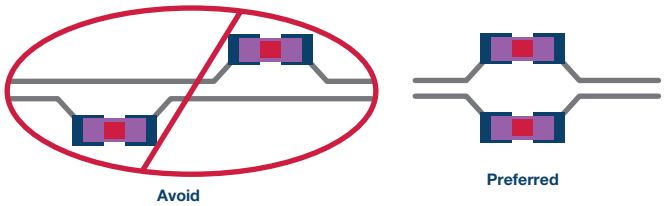

Figure 24. Symmetric routing guidelines.

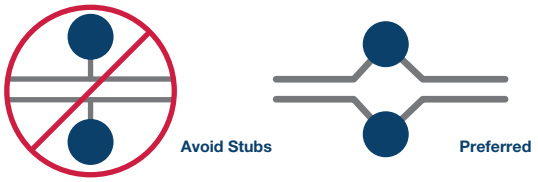

Figure 25. Avoiding trace stubs.

In terms of relaxing filter component value tuning workloads on the printed circuit board (PCB), it is important to keep the parasitic capacitance and inductance as low as possible. The parasitic inductance may not be significant compared to the design value of the inductor in the filter design. The parasitic capacitance is more critical for a differential IF filter. The capacitors in IF filter designs are only a few picofarads. If the parasitic capacitance reaches a few tenths of a picofarad, it affects the filter response significantly. To prevent parasitic capacitance, a good practice is to avoid any ground or power planes under the differential routing region and under power supply chokes.

One example of the differential filter PCB layout is the ADI receiver reference design board (see Figure 26). This shows a fifth-order filter between the ADL5201 and the AD6649. The AD6649 is a 14-bit, 250 MHz pipeline ADC with very good SNR performance.

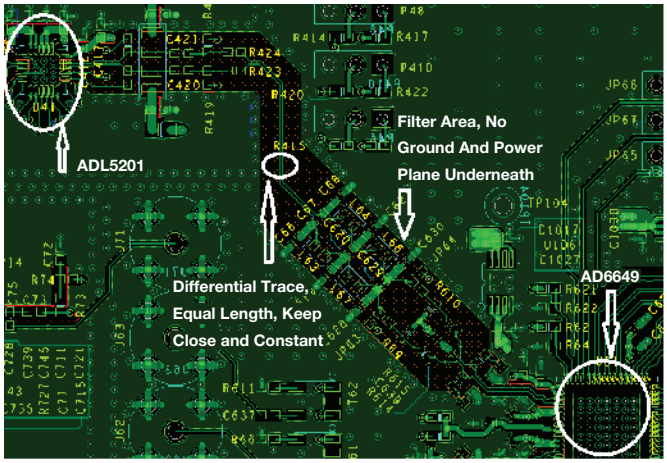

Figure 26. Example of differential circuit PCB layout design.

A Better Understanding of Differential Filter Design

Differential circuits offer some significant advantage for designers. Perhaps the greatest challenge to using them is simply moving past the idea that they're hard to design, test, and correct. Once you take a good look at how to work with differential filters, you may find yourself with a valuable new tool for RF design.

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Mercy Chen is RF applications manager at Analog Devices in Shanghai, China. She joined ADI in 2003 as a handset applications engineer and became a senior RF applications engineer in 2005. Mercy received her bachelor's and master's degree in E&E from Hefei University of Technology.

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