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µModule Data Acquisition Solution Eases Engineering Challenges for a Diverse Set of Precision Applications

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Data Acquisition System-Level Challenges

System architects and circuit-level hardware designers spend significant research and development (R&D) resources to develop high performance, discrete linear, and precision signal chain blocks for their end application (such as test and measurement, industrial automation, healthcare, or aerospace and defense) to measure and protect, condition and acquire, or synthesize and drive. This article will focus on a precision data acquisition subsystem, as shown in Figure 1.

The electronic industry's dynamics are rapidly evolving and there is less time to build and prototype analog circuits to verify their functionality as the control of R&D budgets and time to market (TTM) become challenging. Hardware designers are demanding advanced precision data conversion performance and increased robustness for complex designs in an ever-shrinking form factor amid thermal and printed circuit board (PCB) density limitations. Heterogeneous integration via system-in-package (SiP) technology continues to advance key trends within the electronics industry, including the move to higher density, increased functionality, enhanced performance, and longer mean-time-to-failure. This article will illustrate how Analog Devices is leveraging heterogeneous integration to change the precision conversion playing field and provide solutions that make a significant application impact.

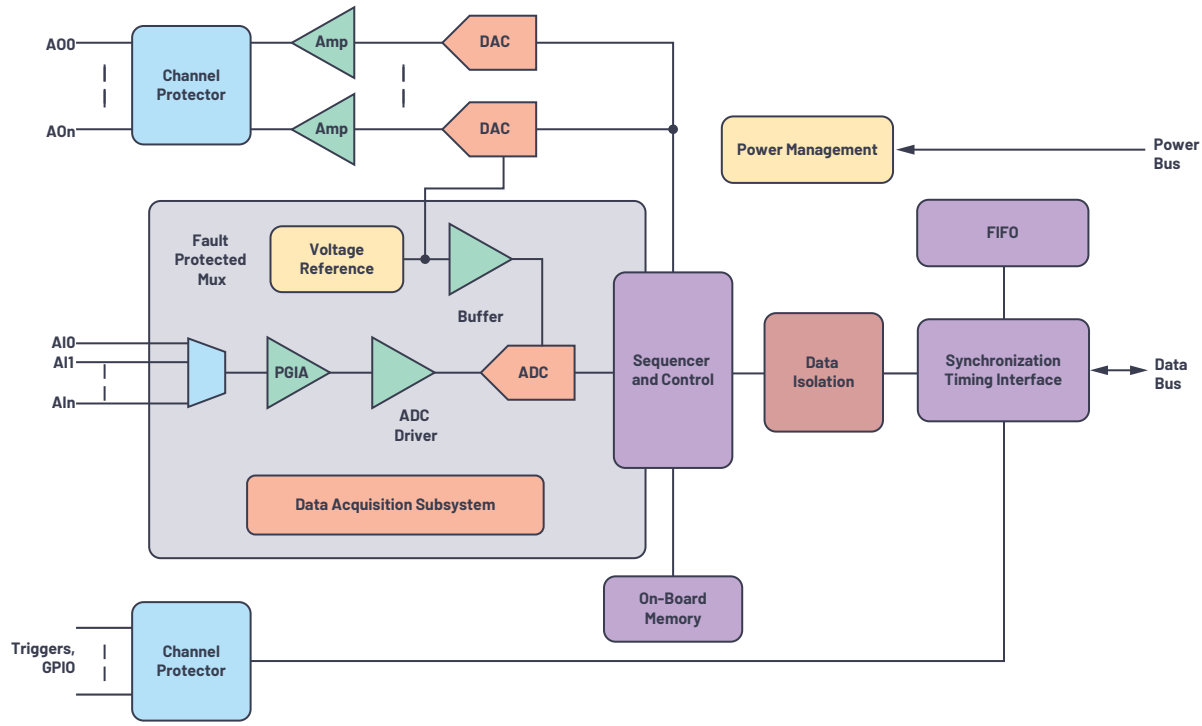

Figure 1. High level data acquisition system block diagram.

System designers face logistical challenges such as component selection and design optimization for final prototypes and technical challenges such as driving the ADC inputs, protecting ADC inputs from overvoltage events, minimizing system power, and achieving higher system throughput with low power microcontrollers and/or digital isolators. With increased focus on system software and applications to differentiate their system solution, OEMs are assigning more resources to software development instead of hardware development. This is resulting in increased pressure on hardware development to reduce design iterations.

System designers developing data acquisition signal chains typically require high input impedance to allow direct interface with a variety of sensors, which could have varying common-mode voltages and unipolar or bipolar single-ended or differential input signals present. Let's take a holistic view of the typical signal chain implemented using discrete components and understand some of the system designer's major technical pain points with the illustration in Figure 2. The key portion of the precision data acquisition subsystem is shown, where the 20 V p-p output of the instrumentation amplifier is applied to the noninverting input of a fully differential amplifier (FDA). This FDA provides necessary signal conditioning, including level shifting, attenuating the signal, and setting the output swing between 0 V and 5 V with a 2.5 V common mode, opposite in phase, resulting in a 10 V p-p differential signal to the ADC inputs to maximize its dynamic range. The in-amp is powered with dual supplies of ±15 V, whereas the FDA is powered from +5 V/–1 V and the ADC is powered from a 5 V supply. The ratio of feedback resistors (RF1 = RF2) to gain resistors (RG1 = RG2) sets the FDA gain of 0.5. The noise gain (NG) of the FDA is defined as:

$$NG = \frac{2}{(\beta 1 + \beta 2)} \quad (1)$$

Where β1 and β2 are feedback factors:

$$\beta 1 = \frac{R_{G1}}{R_{G1} + R_{F1}} \text{ and } \beta 2 = \frac{R_{G2}}{R_{G2} + R_{F2}} \quad (2)$$

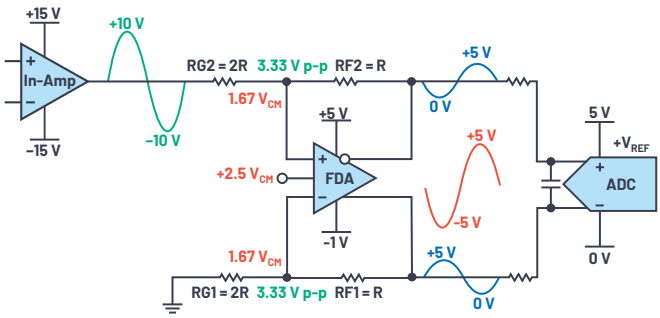

Figure 2. Simplified schematic of a typical data acquisition signal chain.

This section will present how the circuit imbalance (that is, β1 ≠ β2) or mismatch in feedback and gain resistors (R_{G1}, R_{G2}, R_{F1}, R_{F2}) around the FDA influences key specifications such as SNR, distortion, linearity, gain error, drift, and input common-mode rejection ratio. The differential output voltage of the FDA depends on V_{OCM}, so when feedback factors β1 and β2 are not equal, any imbalance in output amplitude or phase produces an undesirable common-mode component in the output, which is amplified by its noise gain and causes a redundant noise and offset in the differential output of the FDA. Therefore, it's imperative that the ratio of gain/feedback resistors matches well. In other words, the combination of input source impedance and RG2 (RG1) should match (that is, β1 = β2) to avoid the signal distortion, mismatch in the common-mode voltage of each output signal, and prevent the increase in common-mode noise coming from the FDA. One of the ways to counter-balance differential offset and avoid output distortion is to add an external resistor in series with a gain resistor (RG1). Not only that, the gain error drift is also influenced by a choice of resistor type such as a thin film, low temperature coefficient resistor, while sourcing matched resistors is challenging amid cost and board space constraints.

In addition, the generation of odd, bipolar supplies is inconvenient for many designers due to the extra cost and real estate constraints on their PCBs. Designers also need to carefully select the optimal passive components, including an RC low-pass filter (which is placed between the ADC driver output and the ADC inputs) as well as decoupling capacitor for the successive approximation register (SAR) ADC dynamic reference node. An RC filter helps limit the noise at the ADC inputs and reduces the effect of kickbacks coming from the capacitive DAC input of a SAR ADC. The COG or NPO type capacitors and reasonable value of series resistance should be chosen to keep the amplifier stable and limit its output current. Finally, the PCB layout is extremely critical for preserving signal integrity and achieving the expected performance from the signal chain.

Easing the Customer's Design Journey

Many system designers end up implementing different signal chain architecture for the same applications. However, one size does not fit all, so Analog Devices, Inc. (ADI) has focused on common sections of signal chain, signal conditioning, and digitization by providing more complete signal chain µModule® solutions with advanced performance that bridge a gap between standard discrete components and highly integrated customer specific ICs to solve their major pain points. The ADAQ4003 is a SiP solution that provides the best balance between R&D cost and form factor reduction while accelerating time to prototypes.

The ADAQ4003 µModule precision data acquisition solution incorporates multiple common signal processing and conditioning blocks as well as critical passive components laid out into a single device using ADI's advanced SiP technology (see Figure 5). The ADAQ4003 includes low noise, an FDA, a stable reference buffer, and a high resolution 18-bit, 2 MSPS SAR ADC.

The ADAQ4003 simplifies the signal chain design and the development cycle of a precision measurement system by transferring component selection, optimization, and layout from the designer to the device itself and solves all major issues discussed in the previous section. The precision resistor array around the FDA is built using ADI's proprietary *i*Passives® technology, which takes care of circuit imbalance, reduces parasitics, helps achieve superior gain matching up to 0.005%, and has optimized drift performance (1 ppm/°C). The *i*Passives technology also offers a size advantage compared with discrete passives, which minimizes temperature dependent error sources and reduces the system-level calibration burden. The fast settling and wide common-mode input range of the FDA, along with precision performance for configurable gain options (0.45, 0.52, 0.9, 1, or 1.9), allow gain or attenuation adjustments as well as fully differential or single-ended-to-differential input.

The ADAQ4003 includes a single-pole RC filter between the ADC driver and the ADC, which has been designed to maximize settling time and input signal bandwidth. All the necessary decoupling capacitors for the voltage reference node and power supplies are also included to simplify bill of materials (BOM). The ADAQ4003 also houses a reference buffer configured in unity gain to optimally drive the dynamic input impedance of the SAR ADC reference node and the corresponding decoupling capacitor. A 10 µF on the REF pin is a critical requirement to help replenish the charge of an internal capacitive DAC during the bit decision process and vital to achieving peak conversion performance. With the inclusion of the reference buffer, the user can implement a much lower power reference source than many traditional SAR ADC-based signal chains because the reference source drives a high impedance node instead of the dynamic load of the SAR capacitor array. The user has the flexibility to choose the reference buffer input voltage that matches the desired analog input range.

Small Form Factor Eases PCB Layout and Enables High Channel Density

The 7 mm × 7 mm BGA package of the ADAQ4003 offers at least a 4 times footprint reduction compared to a traditional discrete signal chain (as shown in Figure 3), enabling small form factor instruments without sacrificing performance.

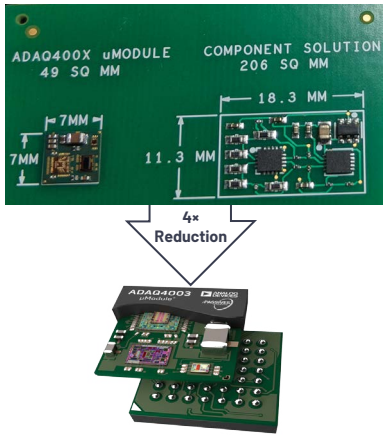

Figure 3. Size comparison of the ADAQ4003 µModule device vs. a discrete signal chain solution.

The printed circuit board layout is critical for preserving signal integrity and achieving the expected performance from the signal chain. The pinout of the ADAQ4003 eases the layout and allows its analog signals on the left side and its digital signals on the right side. In other words, this allows the designers to keep the sensitive analog and digital sections separate and confined to certain areas of the board and avoid crossover of digital and analog signals to mitigate radiating noise. The ADAQ4003 incorporates all the necessary (low equivalent series resistance (ESR) and low equivalent series inductance (ESL)) decoupling ceramic capacitors for the reference (REF) and power supply (VS+, VS–, VDD, and VIO) pins. These capacitors provide a low impedance path to ground at high frequencies to handle transient currents.

There are no external decoupling capacitors required and, in the absence of these capacitors, there is no known performance impact or any EMI issue. This performance impact was verified on the ADAQ4003 evaluation board by removing the external decoupling capacitors on the output of reference and LDO regulators that generate the on-board rails (REF, VS+, VS–, VDD, and VIO). Figure 4 shows that any spurs are buried well below −120 dB in the noise floor regardless of whether the external decoupling capacitors are used or removed. The ADAQ4003's small form factor enables the high channel density PCB layout while mitigating thermal challenges. However, the placement of individual components and routing of various signals on the PCB is crucial. The symmetrical routing of input and output signals while keeping the power supply circuitry away from the analog signal path on a separate power layer with as large of a trace as possible is especially crucial to provide low impedance paths and reduce the effects of glitches on the power supply lines and avoid the EMI type issue.

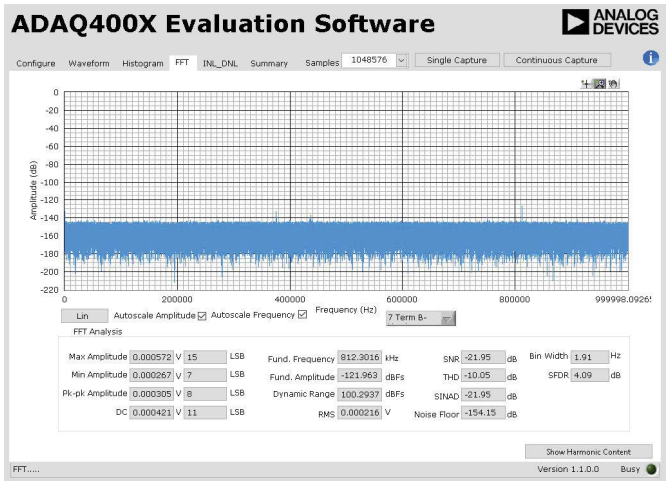

Figure 4. An ADAQ4003 FFT with shorted inputs, with the performance unchanged before and after removing the external decoupling capacitors for various rails.

Driving the ADAQ4003 Using a High Impedance PGIA

As previously discussed, high input impedance front ends are typically required to directly connect with various types of sensors. The majority of instrumentation and programmable gain instrumentation amplifiers (PGIAs) have single-ended outputs, which cannot directly drive the fully differential data acquisition signal chain. However, the LTC6373 PGIA offers fully differential outputs, low noise, low distortion, and high bandwidth, which can directly drive the ADAQ4003 without sacrificing precision performance, making it suitable to many signal chain applications. The LTC6373 is dc-coupled on the input and the output with programmable gain settings (using the A2, A1, and A0 pins).

In Figure 5, the LTC6373 is used in a differential input to differential output configuration and dual supplies of ±15 V. The LTC6373 can also be used in a single-ended input to differential output configuration if required. The LTC6373 directly drives the ADAQ4003 with its gain set as 0.454. The V_{OCM} pin of the LTC6373 is connected to ground and its outputs swing between −5.5 V and +5.5 V (opposite in phase). The FDA of the ADAQ4003 level shifts the outputs of the LTC6373 to match the desired input common mode of the ADAQ4003 and provides the signal amplitude necessary to utilize the maximum 2 × V_{REF} peak-to-peak differential signal range of the ADC inside the ADAQ4003 µModule device. Figure 6 and Figure 7 show the SNR and THD performance using various gain settings of the LTC6373, while Figure 8 shows the INL/DNL performance of ±0.65 LSB/±0.25 LSB for the circuit configuration shown in Figure 5.

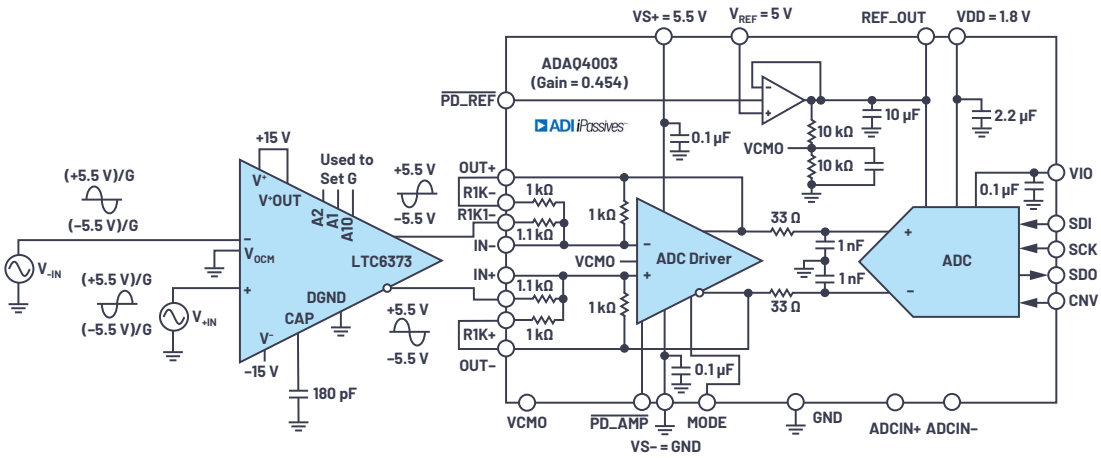

Figure 5. LTC6373 driving ADAQ4003 (gain = 0.454, 2 MSPS).

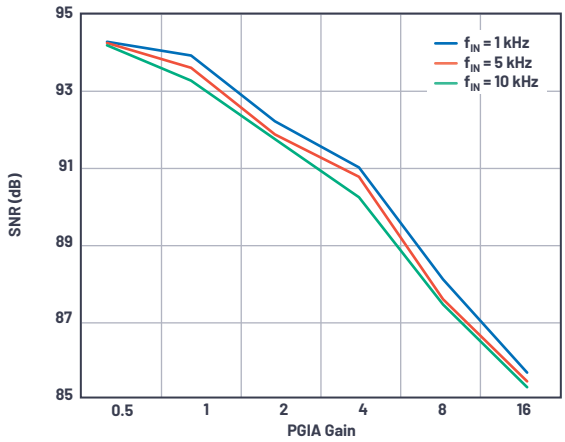

Figure 6. SNR vs. the LTC6373 gain setting, with the LTC6373 driving the ADAQ4003 (gain = 0.454, 2 MSPS).

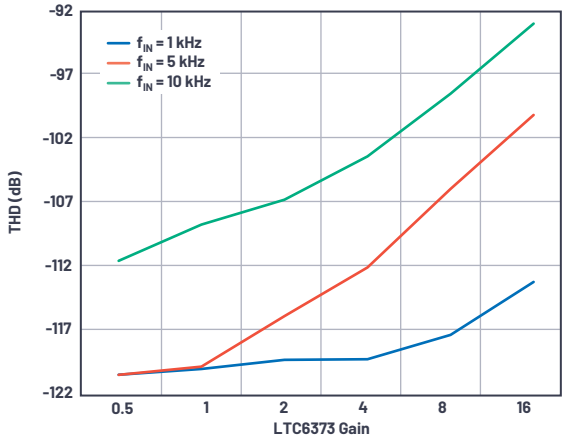

Figure 7. THD vs. the LTC6373 gain setting, with the LTC6373 driving the ADAQ4003 (gain = 0.454, 2 MSPS).

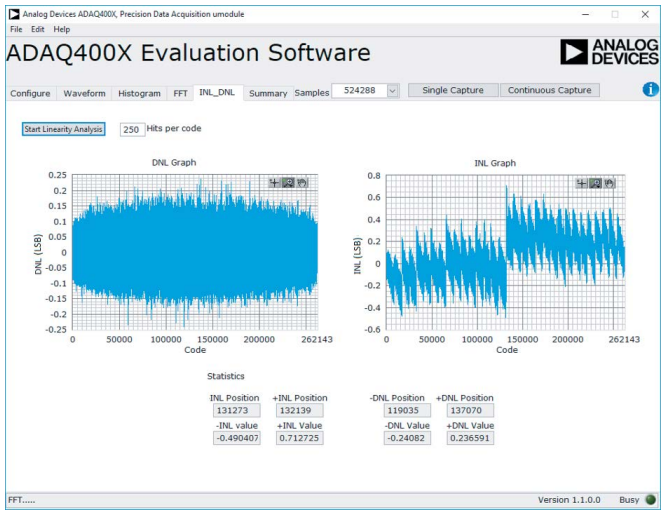

Figure 8. INL/DNL performance, with the LTC6373 (gain = 1) driving the ADAQ4003 (gain = 0.454).

ADAQ4003 µModule Application Use Case: ATE

This section will focus on how the ADAQ4003 makes a great fit for source measurement units (SMUs) and device power supplies (DPSs) for ATE. These modular instruments are used to test a wide variety of chip types for the rapidly growing smartphone, 5G, automotive, and IoT markets. These precision instruments have a sink/source capability, which requires a control loop for each channel that takes care of the programmed voltage and current regulation, and they demand high accuracy (especially fine linearity), speed, wide dynamic range (to measure µA/µV signal levels), monotonicity, and a small form factor to accommodate the increased number of channels in parallel. The ADAQ4003 offers breakthrough precision performance, reduces the end system component count, and allows for improved channel density amid board space constraints while easing their calibration burden and thermal challenges for these types of dc measurement scalable test instruments. The ADAQ4003's high precision combined with fast sampling rate reduces noise, and no latency makes it ideal for control loop applications to provide an optimal step response and fast settling to improve test efficiency. The ADAQ4003 helps ease

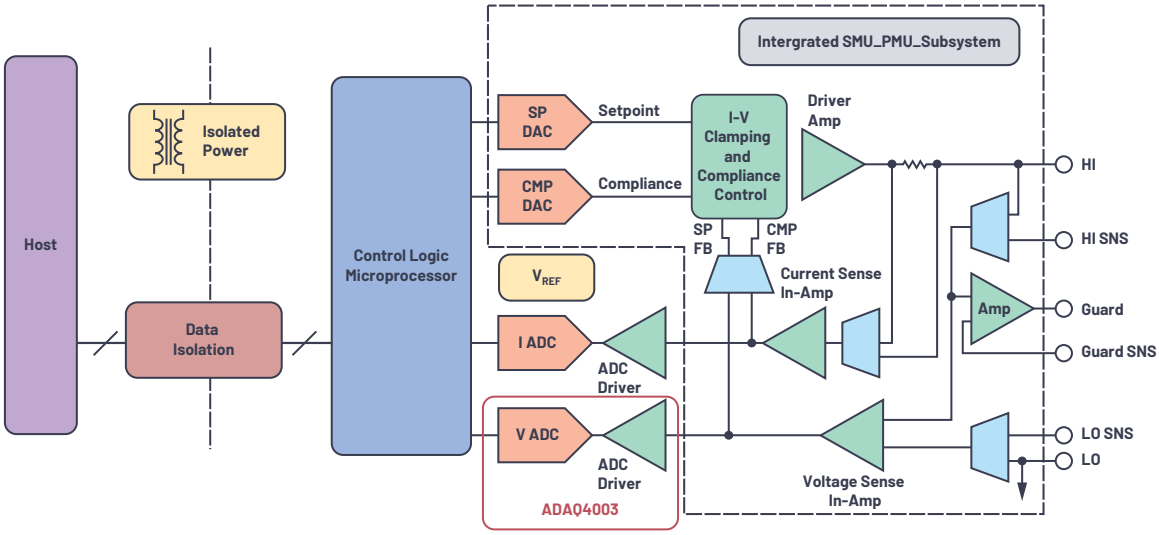

Figure 9. Source measurement unit simplified block diagram.

the design burden by eliminating buffers for distributing the reference voltage on instruments due to their own drift and for board space constraints. In addition, the drift performance and aging determine the accuracy of a test instrument, so the deterministic drift of the ADAQ4003 reduces the cost of recalibration and the instrument's downtime. The ADAQ4003 meets these requirements, pushes instruments' capability to measure lower voltage and current ranges, and helps them to optimize their control loop for a variety of load conditions, which directly translate into an improvement in operating specifications, test efficiency, throughput, and cost for the instruments. The high test throughput and shorter test times of these instruments directly translate into a lower test cost for end users. The SMU high level block diagram is shown in Figure 9 and its corresponding signal chain is shown in Figure 5.

The high throughput rate enables oversampling of the ADAQ4003 to achieve the lowest rms noise and detect small amplitude signals over the wide bandwidth. Oversampling the ADAQ4003 by a factor of four provides one additional bit of resolution (this is only possible because the ADAQ4003 provides sufficient linearity—see Figure 8) or a 6 dB increase in dynamic range—in other words, the DR improvement due to this oversampling is defined as: $\Delta DR = 10 \times \log10(OSR)$ in dB. The ADAQ4003 typical dynamic range is 100 dB at 2 MSPS for a 5 V reference with its inputs shorted to ground. Therefore, when the ADAQ4003 is oversampled by a factor of 1024× at an output data rate of 1.953 kSPS, it offers an unbeatable dynamic range of ~130 dB for a gain of 0.454 and 0.9, which can precisely detect very small amplitude µV signals. Figure 10 shows the dynamic range and SNR of ADAQ4003 for various oversampling rates and input frequencies of 1 kHz and 10 kHz.

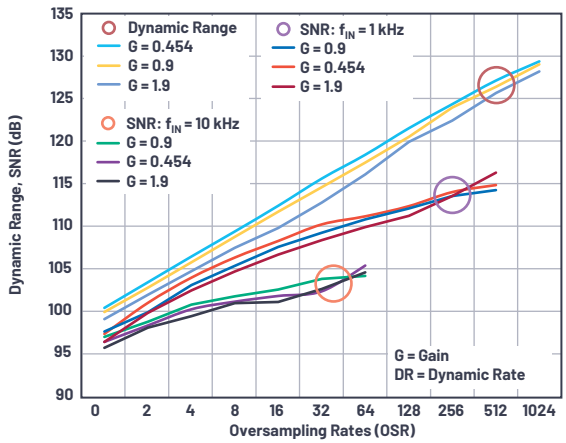

Figure 10. ADAQ4003 dynamic range, with SNR vs. the oversampling rate (OSR) for various input frequencies.

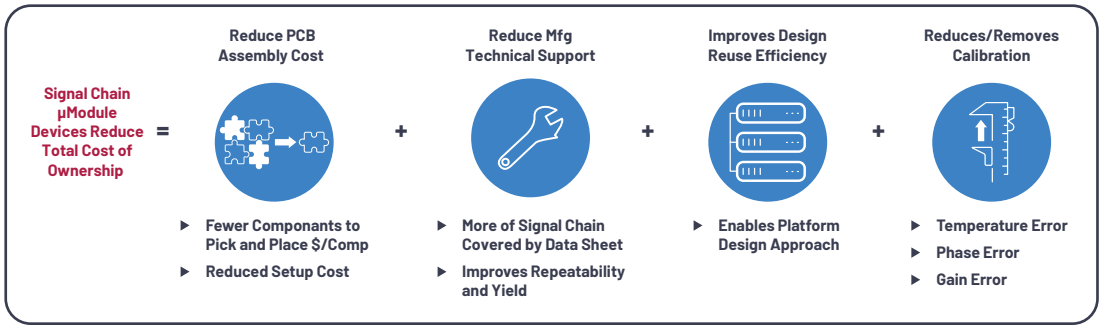

Figure 11. Reduction in total cost of ownership using signal chain µModule technology.

Conclusion

This article presented a few key aspects and technical challenges associated with designing precision data acquisition systems and how Analog Devices is leveraging its domain expertise in linear and converters to develop the highly differentiated ADAQ4003 signal chain µModule solution to solve some of the toughest engineering problems. The ADAQ4003 eases engineering burdens such as component selection and building production-ready prototypes, while enabling system designers to deliver distinguished system solutions to their end customers faster. The ADAQ4003 µModule device's breakthrough precision performance combined with a small form factor adds greater value for a wide range of applications focused on precision data conversion for applications as diverse as automated test equipment (SMU, DPS), electronic test and measurement (impedance measurement), healthcare (vital sign monitoring, diagnostics, imaging) and aerospace (aviation), as well some industrial uses (machine automation input/output modules). µModule solutions such as the ADAQ4003 significantly reduce the total cost of ownership for system designers (as illustrated in Figure 11 in each of the areas) and reduce the PCB assembly cost, increase manufacturing support by improving lot-to-lot yield, enable design reuse for scalable/modular platforms, and simplify the calibration burden in their end application, while accelerating their TTM.

About the Author

Maithil Pachchigar is a system applications engineer in the Precision Technology and Platforms Group at Analog Devices in Wilmington, Massachusetts. Since joining Analog Devices in 2010, he has been focused on the precision converters portfolio and supporting customers in the instrumentation, industrial, and healthcare segments. Having worked in the semiconductor industry since 2005, he has authored and co-authored numerous technical articles. Maithil received his B.E. in electronics engineering from S.V. National Institute of Technology, India in 2003, M.S.E.E. degree from San Jose State University in 2006, and M.B.A. from Silicon Valley University in 2010. He can be reached at maithil.pachchigar@analog.com.