The Demand for Digital: Challenges and Solutions for High Speed Analog-to-Digital Converters and Radar Systems

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Modern advanced radar systems are being challenged on a number of fronts, with additional operational requirements including a need to support multifunction processing and dynamic mode adjustment. Moreover, recent changes in frequency allocations have resulted in many radar systems potentially operating in close proximity to communications infrastructure and other spectrally demanding systems. With further spectrum congestion anticipated in the coming years, the problem is expected to be compounded to a point that radar systems will need to be run-time adaptable to suit their environmental and operational requirements, which is driving the need toward cognitive and digital radar systems.

The need for more digital signal processing is pushing the radar signal chain to transition to digital as early as possible, moving the analog-to-digital converter (ADC) closer to the antenna, which in turn introduces a number of challenging system-level considerations. To explore this further, Figure 1 illustrates a high level overview of a typical current X-band radar system. Within this system, two analog mixing stages are typically utilized. The first stage mixes the pulsed radar return to a frequency of around 1 GHz and the second to an IF in the region of 100 MHz to 200 MHz to enable sampling of the signal using a 200 MSPS or lower ADC, to a resolution of 12 bits or higher.

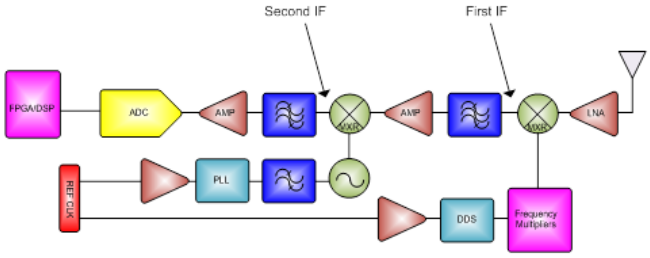

Figure 1. Example of Radar Receiver Architecture Using First and Second IFs

Within this architecture, aspects such as frequency agility and pulse compression may be implemented in the analog domain, which may require signal processing modifications and adjustments, but for the most part the system functionality is limited by the digitization rate. It should be noted that even sampling at 200 MSPS data rates has enabled a significant leap forward in radar processing, but as we move to the next stage in this evolution we are required to migrate even further toward all digital radar.

In recent years, gigasample per second (GSPS) ADCs have been pushing the transition to digital nearer to the antenna by moving the digitization point in the system to after the first mixing stage. Using a GSPS converter with an analog bandwidth in excess of 1.5 GHz already supports digitization of the first IF, but in many cases, the performance of current GSPS ADCs has limited the acceptability of this solution as the linearity and noise spectral density of the device has not met the system requirements.

Until recently, high speed ADCs predominantly used parallel low voltage differential signal (LVDS) interfaces as the means of moving data between the high speed ADC and the digital signal processing platform, typically an FPGA. However, using an LVDS data bus to output the data from the converter brings some technical challenges as a single LVDS bus would need to operate well beyond the max rate of the IEEE standard and what an FPGA can handle. To accommodate this, the output data is demultiplexed onto two or, more generally, four LVDS buses to reduce the data rate per bus. For example, 10-bit ADCs operating at sample rates in excess of 2 GSPS would typically require the output to be demultiplexed by a factor of 4, creating a 40-bit wide LVDS bus. With many radar systems, and particularly phased arrays, using multiple GSPS ADCs this soon becomes an unmanageable hardware development, with so many lanes required to be routed and matched in length—not to mention the number of FPGA pins required for the interconnect!

New GSPS ADCs provide solutions to not only overcome existing challenges but also to further optimize the system. In supporting digitization closer to the antenna, these converters provide unparalleled linearity as well as an analog bandwidth of over 3 GHz, enabling undersampling of the L and most of the S frequency bands. This enables direct RF sampling within these frequency bands, reducing component count and system size by eliminating mixer stages. For higher frequency systems, this also enables higher IFs to be used, providing options for reducing the number of mixing stages and filters, as well as increasing the frequency planning options as a wide range of IFs can be used.

The higher linearity and lower noise spectral density of these new devices further enables them to be used in next-

generation radar systems. With increasing spectral density, higher dynamic range is critical to be able to manage blockers or signals of interference which neighbor the radar return frequency. The latest GSPS ADCs are able to provide in excess of 75 dBc SFDR, which is nearly a 20 dBc improvement over devices that have been available in the last decade. This significant leap is even more critical when competing with recent communications infrastructure frequency allocations.

The improvements in analog bandwidth, linearity, and noise could possibly be anticipated as the next logical step by device manufacturers. However, two additional features of new GSPS ADCs offer more to the system designer and are likely to increase the acceptability of these components in future systems:

- JESD204B data link interfaces, and
- DSP functionality embedded within the converter, which provide system designers with options for significant benefits and possible power savings.

JESD204B data links have recently been introduced on a number of high speed ADCs but the most significant benefit is with GSPS converters where LVDS interfaces were already struggling to meet system needs. JESD204B is a high speed serial standard that enables data to be transported between the high speed ADC and FPGAs or other processors using a reduced number of differential interconnects (FPGA pins). It is a very low overhead protocol which is based upon 8b10b encoding schemes and supports baud rates as high as 12.5 Gbps.

To examine the benefits, consider Analog Devices' new AD9625, 2.0 GSPS, 12-bit converter. The output data rate for this converter is 24 Gbps. If we assume an LVDS data bus is limited to 1 Gbps and ignoring data packing issues, more than 24 LVDS pairs would be needed to support this interface, all of which would need PCB traces matched in length when routed in hardware. Using JESD204B, and with a max baud rate of only 6.25 Gbps, only six JESD204B links are required to support the output from this converter. The benefit is clearly seen in Figure 2 where only eight JESD204B lanes are routed between the AD9625 and an FPGA to support the full 2.0 GSPS data rate.

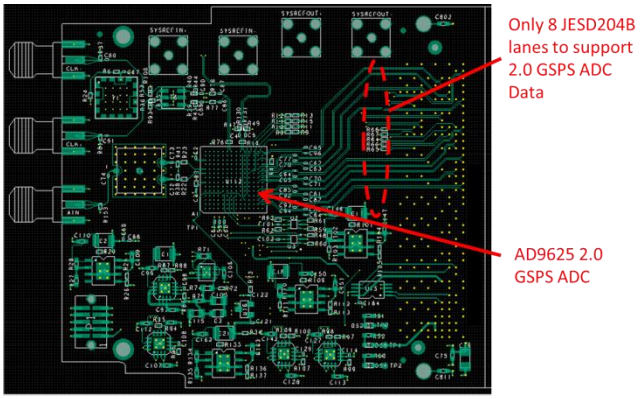

Figure 2. GSPS FPGA Mezzanine Card (FMC) PCB Routing Using JESD204B

Furthermore, when multiple JESD204B lanes are used the requirement for length matching the PCB traces is significantly relaxed as the standard only requires an alignment to 920 ps across the lanes, providing a wide variation between path delays of the individual JESD204B lanes. The latest "B" variant of the JESD204 standard also supports deterministic latency, which enables the latency between the data leaving the high speed ADC and the data arriving at the FPGA to be calculated. If the latency can be determined, this can be compensated for in digital post processing to realign and synchronize data streams, a key requirement of phased array and beamforming systems using GSPS converters.

JESD204B provides a significant benefit to the hardware designer, but possibly the most beneficial aspect of newer high speed ADCs is the addition of digital signal processing. The next generation of GSPS converters, such as the AD9625, based on 65 nm or finer CMOS process geometries, is able to support a vast array of digital signal processing at these high data rates. In the near term, high speed ADCs are being supplied with run-time selectable digital down converters (DDCs) embedded in the device as shown in Figure 3.

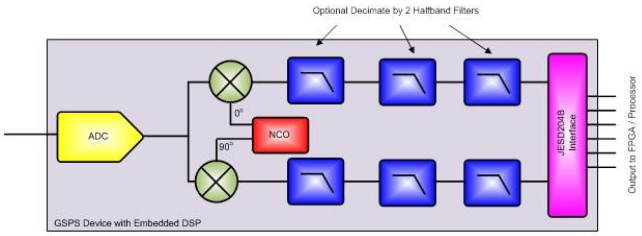

Figure 3. New GSPS ADC with Embedded DSP

Radar waveform bandwidths can vary dramatically depending on the application. For example, some synthetic aperture imaging radar waveforms require hundreds of MHz while tracking radars may use waveforms that are tens of MHz wide or even less. In the past, moving a GSPS ADC closer to the antenna would have meant that in some

instances vast amounts of unwanted bandwidth were transported to the FPGA or processor. In modern FPGAs and high speed ADCs a significant proportion, if not the majority of the power consumption, is related to the power dissipated in the interfaces to the device, thus transferring significant amounts of unwanted bandwidth needlessly increases the power of the system. In future multimode radars, the ability to dynamically enable a DDC provides a significant advantage, offloading complex processing otherwise located in the FPGA.

The DDC combines a digital numerically controlled oscillator (NCO) and decimating filters, providing the ability to select the signal bandwidth and signal location from within the high speed ADC's Nyquist band and transfer only the appropriate data needed to the signal processing devices. For example, consider radar using a 30 MHz bandwidth waveform at an IF of 800 MHz. If this is sampled using an ADC at a sample rate of 2.0 GSPS to a resolution of 12 bits, the output bandwidth of the data would be 1000 MHz, far in excess of the signal bandwidth, and the output data rate from the converter would be 3.0 GBps. If the data is decimated by a factor of 16 using a DDC, not only does the decimation provide some increased noise reduction but the output data rate is reduced to below 625 MBps, which enables data transportation using only a single JESD204B lane! This significantly reduces the overall system power required. With the ability to dynamically configure the DDCs or bypass them as needed, new high speed ADCs provide the option of switching between different modes to support power and implement optimized solutions as needed and enable the feature sets needed for cognitive radar applications.

New GSPS ADCs, such as the AD9625, are providing significant options to the radar system architect, with analog bandwidths and sample rates that enable component count reduction or direct RF sampling. With JESD204B interfaces and embedded DSP options, there is no longer a need to trade power and board complexity for these benefits. The ability to dynamically configure the high speed ADC provides multifunction support and meets the goal of creating an all digital cognitive radar system.

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