Smart Integration: Combining Analog Components with Arm Microcontroller Cores to Solve Tough Embedded System Problems

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The design of tomorrow's embedded systems presents complex challenges given the aggressive goals of improvement in areas of performance, cost, power, size, new features, and efficiency. There is, however, an emerging design option to address these complex problems—analog components smartly integrated with ARM® microcontroller cores. The difference between this and traditional analog integration is the high level of performance now being offered and the optimizations made to solve specific system level problems. While every market will have their own order ranking of these areas to improve, satisfying multiple factors simultaneously is highly desirable and can come from the integration of numerous discrete components. Logically, combining parts could solve many of these embedded system goals, but simply putting several discrete components and a processor in one package is not the answer; the solution is far more complex, requiring smart integration.

SMART INTEGRATION OF ANALOG AND DIGITAL

Smart integration of high performance analog components (amplifiers, ADCs, DACs, voltage references, temperature sensors, wireless transceivers, etc.) and 32-bit processor cores from ARM with the right digital peripherals can address goals that discrete solutions cannot. In order to create the optimum mixed-signal control processor, a strong knowledge of the overall system along with the availability of the right intellectual property (IP), and expertise in that intellectual property, is required. Needless to say, chip designers and system engineers specifying the features of these integrated devices must have an exceptional understanding of the end application requirements. This domain knowledge is critical and includes a solid understanding of board level requirements such as form factor, temperature ranges, manufacturing considerations, power consumption, cost, and complementary components in the signal chain. Figure 1 shows the analog and digital IP blocks that are often used in devices that are smartly integrated.

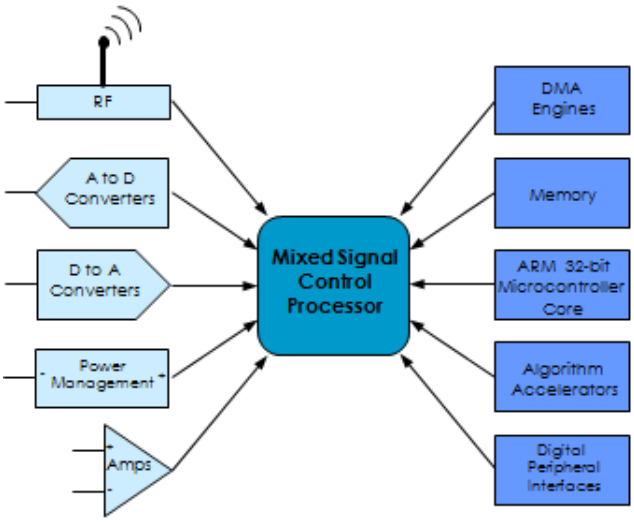

Figure 1. Smart Integration: Analog and Digital IP Combined and Optimized for Target Applications

Availability of the right IP provides a strong starting point for meeting system level goals. This starting point is needed to keep the development period of the mixed-signal control processor short. Increasingly, the acquisition/creation and implementation of the IP itself, appropriate for the application, needs to be facilitated by the semiconductor manufacturer. This IP then needs to be modified to meet two requirements in particular. The first is to maximize system level benefits by optimizing performance and operation based on the needs of the primary target application. The next is to optimize the IP to work very well and very easily with the other complementary IP blocks in the mixed-signal control processor.

And finally, there needs to be the opportunity at a business level for collaboration, combining the expertise and knowledge of the system manufacturer and semiconductor manufacturer, and resulting in an optimized, unique design.

MIXED-SIGNAL CONTROL PROCESSOR APPLICATIONS

There are many applications that can benefit from a device that integrates high performance analog with ARM

microcontroller cores, including temperature sensing, pressure sensing, gas detection, solar inverters, motor control, healthcare vital signs monitoring, automotive monitoring systems, and gas/water/electric meters. This article will look at two applications areas where integration of optimized high performance analog and ARM microcontroller cores leads to significant benefits in cost, power, size, and performance:

1. Inverters for solar photovoltaic (PV) systems with goals of increased efficiency, bill of material (BOM) cost reduction, and integration of intelligence to support interfacing to the smart grid.
2. Motor control, with the goals of improved efficiency for environmental benefits and cost reduction.

Note that while these smartly integrated mixed-signal devices are optimized for particular end applications, they can also work well for numerous adjacent applications having similar functional requirements to the primary target application.

SOLAR PHOTOVOLTAIC INVERTERS: COST REDUCTION FOR WIDER USE AND INTELLIGENCE FOR THE SMART GRID

While solar PV electricity generating systems have seen greater than 50% annualized growth over the past five years, they still only account for a very small percentage of overall electricity generation worldwide. Although in some regions solar PV generated electricity has reached cost parity with fossil fuel generated electricity, in most regions it has not and generally this parity is dependent on government subsidies.

To better compete against traditional energy sources such as natural gas, coal, and oil, cost reductions of solar PV generated electricity is best achieved by both increases in efficiency and reduction in system BOM costs. As cost and efficiency of the panels themselves trend in the right direction, new technologies also promise advancement for solar PV inverters—the interface between the power generated by a solar panel and the grid. These new technologies include NPC 3 level/5 level/multilevel, high frequency switching topologies, utilizing fast power transistors based on silicon carbide (SiC) and gallium nitrite (GaN) materials.

Figure 2 shows a two stage solar PV inverter system. Power from the panels, essentially a dc source, is converted to ac so it can be fed to the grid. The first stage is a dc-to-dc conversion that raises the voltage level so it is compatible with the peak voltage on the grid. The second stage is a dc-to-ac conversion. The area outlined in red shows the low voltage components used for control that, when combined into a single mixed-signal control processor, give benefits at a system level. Costs are saved by integration of the multiple components into a single device and by the improved efficiencies of new high speed switching topologies. The result is lowered installation costs per kW. There are also costs to be saved with the new topologies given that smaller inductors can be used. This saves BOM costs and also allows for reduction in the size of the inverter.

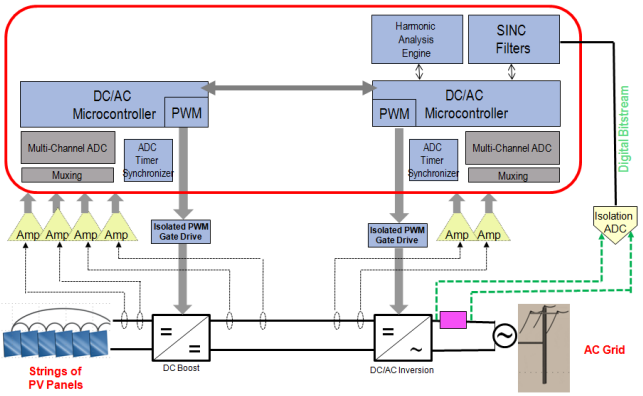

Figure 2. Block Diagram of Two Stage Solar PV Inverter System; Area in Red Shows Blocks Targeted for Smart Integration

High speed successive approximation register (SAR) ADCs are a good fit for this application as they provide the right level of accuracy (13 ENOB), fast conversion speed to support higher frequency control loops, the ability to support muxing of multiple input channels and low latency (< 1µS). This system has two ADCs for simultaneous sampling of current and voltage on the grid. A large number of input channels to the ADC are needed in order to monitor multiple points in the system—up to 24 analog channels in some cases. Special muxing with buffering was designed and interfaced with the ADCs in order to support this requirement.

For support of the multiple stages of conversion and the high speed control loops, a processor core with the right architectural performance and capability for high speed operation needs to be selected. In this case an ARM Cortex™-M4, designed for greater than 200 MHz operation over temperature, will meet the need.

The sinc filters, shown in Figure 2, are used in combination with isolation ADCs. This allows for measurement of ac on the grid and dc injection in order to avoid the saturation of transformers. The traditional method is to use a Hall effect current transducer, but this is expensive compared to the isolation ADCs. This assumes that the sinc filters are integrated into the mixed-signal control processor, avoiding

an additional chip in the BOM in the form of programmable logic. The isolation of the ADC sinc filter combination also offers an added benefit of improved linearity over Hall effect sensors, leading to a reduction in harmonic distortion.

As the grid becomes smarter, solar PV inverters will need to have more intelligence to help deal with grid imbalance. That is, occasions when more power is available from multiple sources than is needed. For this reason, there is a focus on PV system intelligence with an eye toward grid integration, where each contributor to the grid must cooperate to stabilize the grid. Grid integration requires better measurement, control, and analysis of the quality of the energy fed to the grid. A harmonic analysis engine designed specifically to monitor the quality of power injected into the grid helps address this need. With the calculation of a number of variables including harmonic distortion, power, rms voltage, rms current, VAR, VA, and power factors, the quality of power can be monitored. A dedicated engine to perform these calculations can give very high accuracy while off loading the ARM Cortex-M4 core from performing this task.

Solar inverters can benefit significantly at the system level with the use of mixed-signal control processors that are designed with this end application in mind. An understanding of market trends and solid system knowledge can lead to a smartly integrated chip capable of supporting next generation topologies with low chip counts while also adding features to support interfacing to the smart grid.

MOTOR CONTROL: IMPROVED EFFICIENCY FOR A BETTER ENVIRONMENT AND LIFETIME COST SAVINGS

In addition to environmental concerns about how energy is generated, there are also concerns about how efficiently energy is used. Given that motors account for 40% of the world's electricity usage, the question raised is how these systems can be made more green. The answer is to make them more efficient so less energy is used. Savings from broad use of more efficient motors is measured in large numbers: electricity savings in hundreds of billions of kW hours and a reduction in the CO_2 released into the atmosphere in millions of tons per year. The impact of more efficient motors is clearly very significant.

Specifically, there are a couple of key drivers for the use of more efficient motors. One impetus is government legislation driven by environmental concerns. The European Union has regulations in place and more to come in the future that mandate the use of more efficient motor systems. Another key driver is lifetime cost advantages. An approximation of motor control system costs is 15% for materials and 85% based on energy used for operation. So there is significant potential for reduction in the lifetime costs of motor systems with greater efficiency.

Higher efficiencies can be achieved by special motor design, selection of motor type, an addition of an adjustable speed drive (ASD) for systems that do not have this sort of control, and control algorithms that optimize for efficiency. In terms of special motor design and selection of a particular type of motors, permanent magnet motors have been a focus and usage has been on the rise. Efficiencies for permanent magnet motors can be as high as 96%, which exceeds Europe's premium efficiency standard (IE3).

Smartly integrated mixed-signal control processors offer potential improvements for ASDs and control algorithms. Cost effective integration of an ARM-based CPU subsystem, PWMs, ADCs, and muxing translates to system-level BOM reductions for an ASD.

Control algorithms can be improved by using highly accurate ADCs with fast conversion times. This leads to efficiency gains for the overall motor system. An ADC with greater than 12 bits of accuracy improves the precision with which the phase currents can be controlled. However, sample conversion latency cannot be traded off for higher accuracy. This eliminates the options of an ADC that averages or oversamples to improve SNR. Variables need to be measured at the rate the end machine is moving (for example, pick and place machine). Fast conversion times complemented with a fast ARM microcontroller core allows a control loop to run faster, resulting in better response and settling times. In turn this can increase the throughput and efficiency of a manufacturing production line system, resulting in lower production costs.

As with solar PV applications, SAR ADCs are a good choice for motor control. In the motor control case, high performance SAR ADCs can be designed without the need for averaging or oversampling to meet requirements.

The various IP blocks in Figure 3 were very carefully designed so that they work very well together. The desired result is a very agile instrumentation subsystem that can acquire multiple, precisely scheduled samples and deliver them efficiently to the ARM's main memory. For motor control, both of the phase winding currents and other measurements can be synchronously sampled at precisely specified points in the PWM cycle. The sampled data can then be efficiently moved, with no overhead, to the

microcontroller's memory for processing. Five different blocks in the mixed-signal control processor need to work in concert to achieve this task.

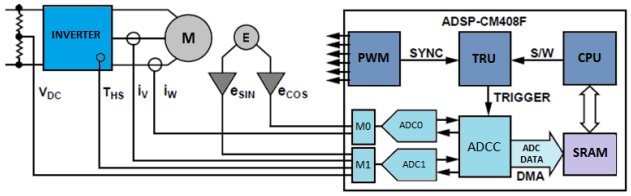

Figure 3. Block Diagram of Motor Control System

The cycle starts with a PWM pulse sent to the trigger routing unit (TRU), which has the job of connecting trigger masters to trigger slaves. In this case, the PWM is the trigger master and the ADC controller (ADCC) timer is the trigger slave. The ADCC needs to be able to manage a large number of events and uses timers (TMR0/TMR1) to track how long from the PWM trigger to initiate a particular ADC event. With a timer match to a particular event, ADC input muxing (M0 and M1) and channels (ADC0 and ADC1) are selected. The convert start signal is subsequently sent to the ADC. Sample data is moved from the ADC to ADCC and then from the ADCC to the microcontroller SRAM via DMA.

Figure 4 below shows the relative timing between PWMs pulses, PWM sync, and ADC events controlled by the ADCC.

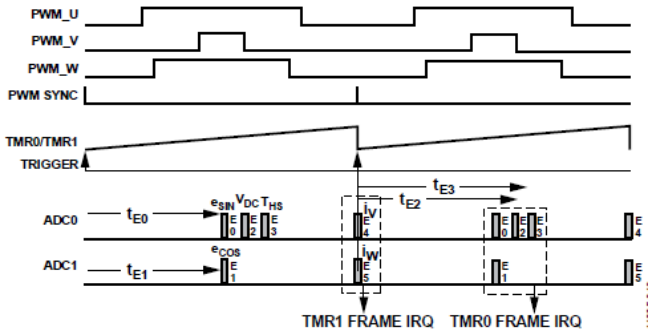

Figure 4. Timing for Sampling of Five Different Motor Control Variables Using ADC

Good base IP starting points were available for PWMs, TRU, muxing, buffering, SAR ADCs, and DMA for design of a mixed-signal control processor targeted at motor control. However, specific design modification of these blocks was necessary in order to achieve the level of coordination required for precise timing of ADC sampling within a PWM period. The need for the ADCC block is based on the fact that the other IP blocks are integrated into a single chip and require coordination. The ADCC is designed to this requirement and to fully utilize the high speed of the two ADCs engines which have a fast convert time of 380 ns.

CONCLUSION

Advanced base technology is just the starting point— chip designers must have broad knowledge of customers' systems and deep expertise in the design, application, and optimization of the precision analog and digital components. In addition, silicon manufacturers must be willing and able to directly interact and collaborate with system manufacturers to create new products. The most appropriate components are selected, optimizations are made for the targeted end application, and IP blocks are modified to work well together. It is only then that the optimized pieces can be integrated. Examples of these smart integrated products can be found from Analog Devices, including the ADuCM360, a fully integrated, 3.9 kSPS, 24-bit data acquisition system, and the ADSP-CM403F and ADSP-CM408F mixed-signal control processors that integrate dual high precision 16-bit ADCs and ARM Cortex-M4 processor cores. For more information, please visit www.analog.com.

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AUTHORS

Colin Duggan grew up in the Boston area, where he went to school, and received a Bachelor's of Science degree in electrical engineering from Northeastern University. His first job out of school was at Analog Devices and he has been with the company since, leading to a tenure of over 20 years. Colin has held a number of roles in applications engineering and marketing. Currently he is the director of marketing for the Embedded Systems Product Technology division. In this role, he is a significant contributor to the strategy, marketing, and marketing operations of Analog Devices processor-based products.

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