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Simplify Antenna Calibrations Using SDR with RF PLL Phase Synchronization Feature in Massive MIMO and Phased Array Systems

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Abstract

In this article, the radio frequency (RF) phase-locked loop (PLL) phase synchronization feature available in Analog Devices' software-defined radios (SDRs) is highlighted. This functionality helps in reducing the complexity in antenna calibrations, especially for systems that employ large antenna arrays. Control and configuration of synchronization is provided in the user guide.[1] This article emphasizes its application and benefits.

Phase Coherent Signals

Coherence is a property of waves that defines the relationships existing in the physical quantities of a single wave or between two or more waves. In electronics, physical systems deal with phase, frequency, and amplitude of continuous wave and clock signals. In general terms, two signals are phase coherent if the difference between their phases stays constant and stable over time. Figure 1a shows the phase of two signals over time. The two signals exhibit a coherent phase

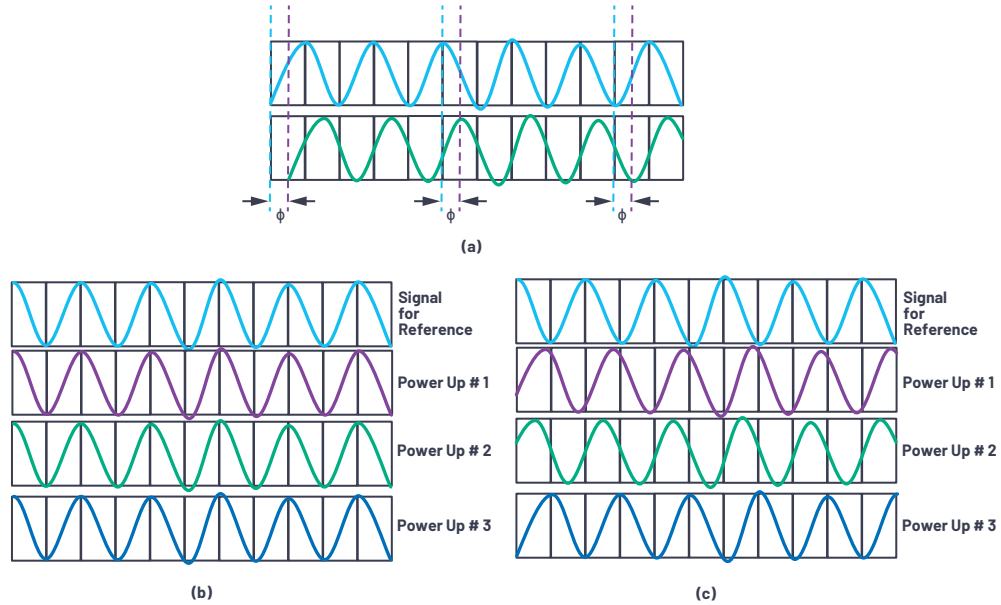

Figure 1. Examples of coherent and incoherent phase relationships over time.

relationship, as the phase between them remains constant. Figure 1b compares the starting phase of a reference signal in a system upon different power-up cycles. The coherent phase relationship over every power-up could also be observed here. However, Figure 1c presents an example where the phase is incoherent, as the signal starts with a random phase over every power-up.

Phase Imperfections and Their Mitigation in Multichannel and Multi-Antenna Systems

Phased array and massive MIMO systems have multiple antennas and multiple RF channels. From the digital back end up to the antenna array, phase coherence and timing synchronization over multiple planes are main requirements in such systems. For example, frame synchronization is needed on medium access level, coherency is required on digital interface (for example, deterministic latency), synchronization is necessary in sampling with multiple converters or chips for multiple channels, phase coherency among multiple local oscillators (LO) is essential in generating radio frequencies, and a deterministic phase relationship is needed among the elements of antenna arrays. Thus, maintaining the coherent relationship at different stages is crucial and fundamental. However, it is a challenging task simply due to real-world practical aspects such as part-to-part variation, traces on printed circuit boards, nonlinearities in the components, coupling effects, frequency divider ratios, hardware aging, clock drifts, temperature drifts, and drifts in local oscillators.

If multiple RF LOs are used in a system, LO phase drift is an additional factor that varies over multiple channels and over time. Different architecture options are available to generate coherent RF LO signals.

RF LO distribution: The LO signal is generated by a common LO and then distributed in the system. Due to radio frequencies, it is not an easy task. RF losses and RF coupling make it quite difficult.

Reference clock distribution: To avoid RF losses, LO signals are generated locally. However, due to variations in PLLs or voltage controlled oscillators (VCOs), extra efforts are needed to synchronize individually generated LO signals.

Figure 2 illustrates an example of a multichannel and multi-antenna RF subsystem architecture, which is based on integrated transceiver chips. There is an on-chip frequency synthesizer—a PLL—and a VCO for RF LO generation. The reference clock is generated externally to the transceiver chips and distributed to the device clock inputs respectively to each chip. Further scaling and distribution of the reference clock is done on the chip. In Figure 2, a breakdown of the propagation path is shown from the system reference clock to the antennas. The path could be split into different segments where each segment contributes a propagation delay. The variance in the propagation delay causes the variance in phase difference and perturbs the phase coherency in the system.

Calibration techniques are employed to mitigate the practical imperfections. By using a calibration method, the unknown factors are determined and then corrected accordingly. Due to the phase differences, the frequency response of each RF channel in phased array and massive MIMO systems differs from the other channel. Moreover, it is time variant in nature. Static factors in the system that can be measured are compensated through factory calibrations. Deployment dependent factors are mitigated using initial calibrations that could also be run upon each system startup. To mitigate dynamic and time variant factors, periodic antenna calibrations are required. In addition to temperature drifts, LO phase drift is one such dynamic factor that varies over multiple channels and over time. When these calibrations are executed during operation, they consume valuable system resources such as time frequency. Hence, an optimization problem develops that maximizes system performance with minimum resources allocated for calibration efforts.

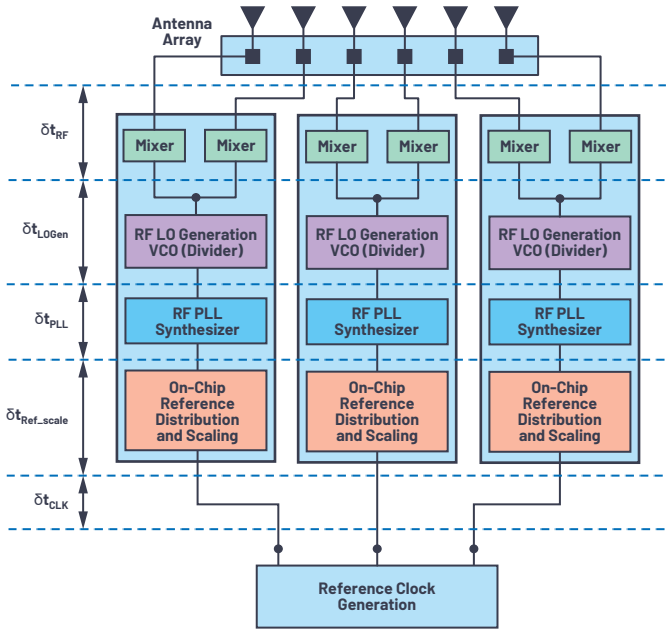

Figure 2. Sources of phase imperfections in a multichannel and multi-antenna system.

Simplifying Calibrations Using the RF PLL Phase Sync Feature

The ADRV9009 is a dual-channel, highly integrated SDR in ADI's RadioVerse® portfolio. It provides two transmit and two receive channels to convert digital IQ bits to RF and RF to digital IQ bits, respectively. It is based on zero-IF architecture, which minimizes system power consumption with exceptionally superior transmitter and receiver RF performance. The device can support complete frequency generation using on-chip functions without the need of external components. There are three on-chip frequency synthesizers, and the RF LO synthesizer is one of them. For each synthesizer, there is an integrated VCO and a loop filter. This high level of integration with superior performance provides high flexibility in frequency generation over the whole supported frequency range.

On the digital side, the ADRV9009 employs JESD204B protocol for a serial interface performing digital data transfer.[2] It provides built-in support for multichip synchronization using the JESD SYSREF signal. Therefore, it is optimum to create large scale phased array and massive MIMO systems.

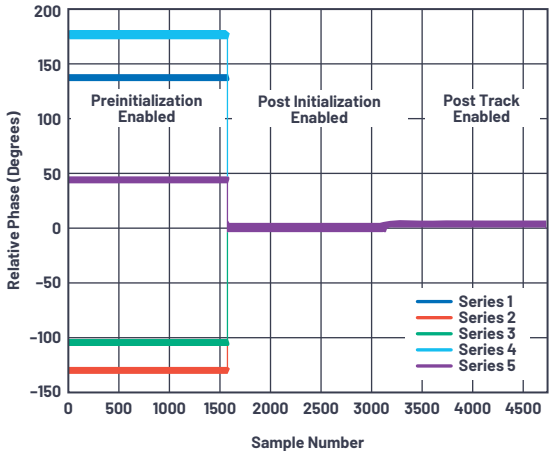

Figure 3. Transmitter output phase comparison through RF PLL phase synchronization cycle[1] (RF tune frequency = 1800 MHz).

In addition to multichip synchronization, the ADRV9009 also provides an RF PLL synchronization feature that enables the internally generated LO signals to be phase coherent and aligned with the applied reference clock. Based on this feature, the following functions could be easily achieved in large scale systems:

- Phase coherency upon power-up: constant, deterministic, and stable phase value on each power cycle
- Phase coherency during operation: tracking of the phase value after startup
- Phase coherency among multiple devices: further support to multichip synchronization

Calibration algorithms require computational and memory resources in the digital hardware. For example, the algorithms are typically implemented in the baseband processing chain and employ FPGA/DSP resources. This feature indirectly reduces power consumption and resources on system calibrations. Hence, enabling this feature optimizes the overall system performance and efficiency. Due to complex calibration algorithms, more time is required for initialization and to reach a steady system state. This time could be minimized by enabling the RF PLL synchronization feature on initialization. Calibration routines are executed periodically for tracking the drifts in LO phase, especially due to temperature. Otherwise, these drifts affect the beamforming pattern of multi-antenna systems. With the help of the RF PLL synchronization tracking feature, calibration frequency could be minimized while keeping the required beamforming performance. There are four modes of operation for controlling the phase sync feature:

- Mode 1: Disable the on-chip RF PLL sync feature.
- Mode 2: Enable RF PLL sync only for initialization.
- Mode 3: Perform RF PLL sync upon initialization and track only once.
- Mode 4: Continuous RF PLL phase tracking.

Figure 3 presents the results of measured phase difference upon multiple power-up cycles in a multichip and multichannel environment. The measurement setup has four RF channels developed using two identical evaluation boards, one of which is the ADRV9009-W/PCBZ. With the help of a vector network analyzer, the change has been measured in the phase difference between the transmitter output signals upon every power-up cycle. Please refer to the user guide[1] for further details.

The measurements are taken for five power-up cycles and compared in different modes of operation. The system started without enabling the RF PLL synchronization feature. It can be seen that, with each power-up cycle, there is a random phase relation. After enabling the RF PLL synchronization feature, all five relative phase values converge to a repeatable value within a tolerance of ±2°. When continuous tracking is enabled, it maintains the relative phase value with some delay. This delay results in a 1° to 2° increase in the relative phase. Hence, a little shift could be observed in the figure. With this feature, stable phase value can be achieved within a deterministic tolerance. This reduces the impact of dynamic factors and simplifies the overall synchronization and calibration of the system.

Conclusion

The RF PLL synchronization feature is available in advanced generations of highly integrated SDRs provided by ADI, including the ADRV9009 dual-channel transceiver. If large antenna array systems are built using this device, the RF PLL

synchronization feature could be exploited to simplify the antenna calibrations. Different modes of operations are available that can be selected according to the application requirement. Control and configuration of the feature is executed simply by using software API functions. The ADRV9009 user guide[1] provides further details on the function and usage of this feature.

References

[1] UG-1295 Hardware Reference Manual for the ADRV9008-1, ADRV9008-2, and ADRV9009.

[2] JESD204B Serial Interface and JEDEC Standard Data Converters. Analog Devices, Inc.

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About the Author

Danish Aziz is a staff field applications engineer and a subject matter expert for RF products and systems at Analog Devices. As a member of the technical sales team, he is driving growth and providing technical support to customers in the EMEA region. He is focusing on wireless connectivity applications in automotive, industrial, defense, and cellular applications. He represented ADI in the 5G Automotive Association (5GAA).

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