

# A New, Easier Way to Create Power Solutions for Signal Chain Systems

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## Abstract

Signal chain systems connect analog data from the physical world to the digital world, where the data is processed. However, powering signal chain systems can be a challenge because the power supply must not degrade the system's overall performance. Linear regulators can prevent this degradation, but at the cost of increased power loss, and thus lower efficiency. Switching regulators, on the other hand, provide a significant improvement in efficiency but can affect the signal chain system's performance by introducing noise due to their switching nature. Analog Devices' [Signal Chain Power \(SCP\) hardware evaluation platform](#) and [SCP Configurator](#) companion software tool allow signal chain hardware engineers, with or without prior power applications experience, to design a power supply for their signal chain systems in a simplified and intuitive way.

## What Is the Signal Chain Power (SCP) Platform?

The SCP platform is a combination of hardware and software that addresses the challenges when developing power for signal chain systems. It aims to guide system design engineers in providing the best and most complete power solution for their instrumentation, test and measurement, and industrial automation precision signal chain applications. The SCP hardware is a set of evaluation boards that strike a good balance of performance, size, and cost. The SCP Configurator, the platform's companion software, provides suggestions to signal chain engineers for choosing the best power tree for their application. The combination of the SCP platform hardware and the SCP Configurator provides design engineers a way to quickly develop a power solution for their signal chain.

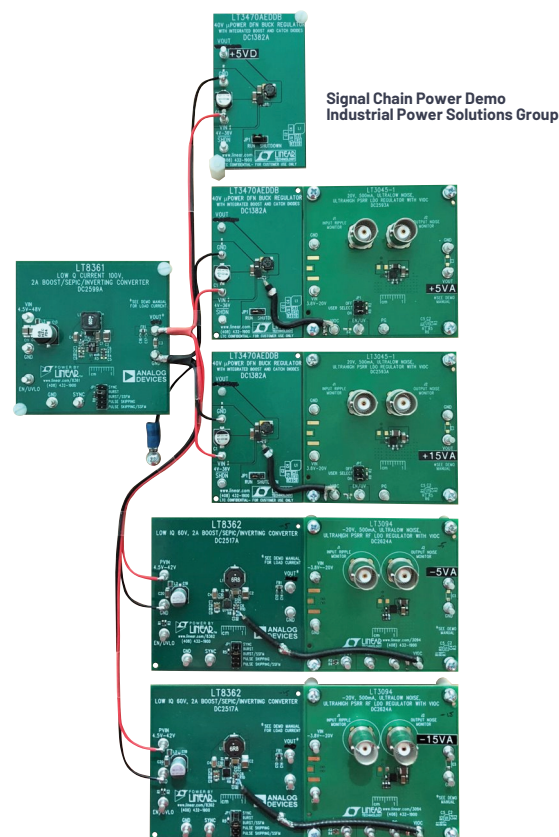


Figure 1. One of the traditional ways of developing a power solution for the signal chain is to wire up multiple demo boards. The other method is to use multiple bench power supplies. Both methods take up a lot of time, especially when optimizing the solution.

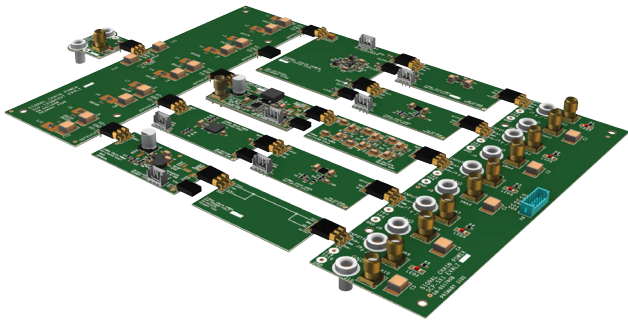


Figure 2. An example power solution using the SCP platform hardware.

## Signal Chain Power (SCP) Hardware Evaluation Platform

From the thousands of Power by Linear™ products, a small list was identified for inclusion in the hardware. These products have been used in many signal chain applications, and having this list eases the selection of power products to use. It supports multiple power configurations to meet most of the power requirements for precision signal chains, which can be in step-up, step-down, step-up or down, inverting, and dual-output boost/inverting topologies. The platform also includes a selection of positive and negative LDO regulators that can be used as postregulators for better system noise performance.

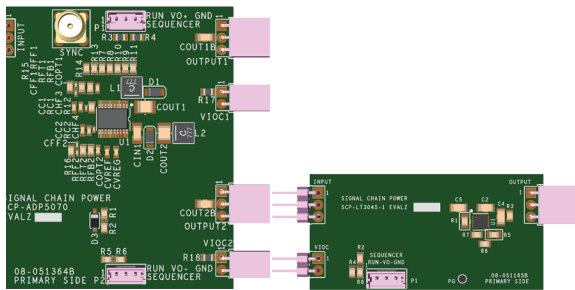


Figure 3. The SCP-ADP5070-EVALZ dual DC-to-DC converter (left) and the SCP-LT3045-1-EVALZ LDO regulator (right).

The boards in the hardware platform use a standard size with a small form factor, with input and output headers that have a predetermined polarity. The locations of these pin headers are specifically defined to enable creation of multiple board combinations. These aspects of the boards' design help in quickly testing different board configurations and their performance, all while keeping the workspace small and simple.

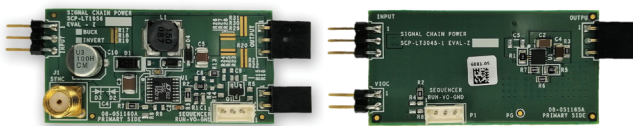


Figure 4. The LT1956 buck converter (left) and the LT3045-1 LDO regulator (right) have the same board size, despite having different topologies.

Aside from power delivery, SCP hardware also supports several functions and features. The boards are designed with oversized 0805 pads on components that may require modification. These components include the feedback, compensation, frequency setting, soft start, run, and VIOC, among others. This makes rework and design adjustments more convenient. Some SCP switching regulators support frequency synchronization. An external clock can be fed through the SCP board with an SMA connector that is available on the board. The recommended values and configuration settings can be found on each board's product page on [analog.com](http://analog.com).

The SCP hardware also incorporates a tracking function to control the switching preregulator powering the linear postregulator through the voltage for input-to-output control, or VIOC. The VIOC pin is the output of this tracking function that drives the preregulator's feedback (FB) pin to maintain the LDO regulator's input voltage at  $V_{OUT} + V_{VIOC}$ . This function can be utilized to minimize power dissipation on the LDO regulator while maintaining its PSRR performance. Overall efficiency is improved by using this function.

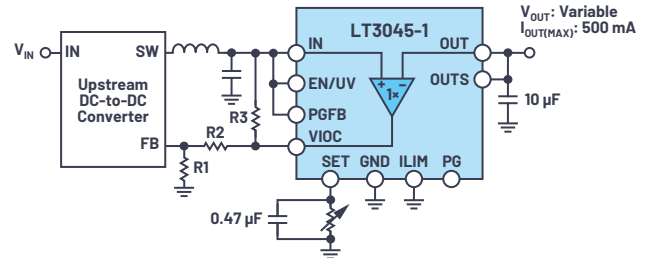


Figure 5. An example implementation of the VIOC function on the LT3045-1 LDO regulator.

All SCP switcher and LDO boards are configured so that users can properly sequence each power rail if their system requires sequential power-up and/or shutting down. The user can enable or disable individual power modules by sending a digital high or low signal from their system. Power supply sequencer and supervisors such as the LTC2928 can also be used for this function. A dedicated header is included to monitor and set the output to a desired power sequence.

The SCP hardware platform also includes board accessories, which consist of a 1×2 breakout board, 1×5 breakout board, 5×1 reintegration board, through board, filter board, single input board, and single output board.

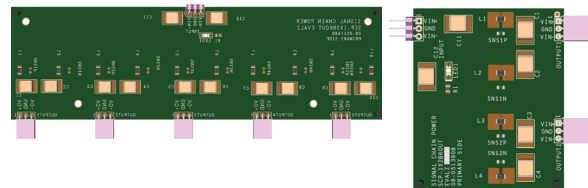


Figure 6. Breakout boards can be used for splitting the single input voltage into multiple rails.

The 1×2 and 1×5 breakout boards can be used to create multiple parallel voltage output rails. A provision for current sensing and output filtering is added on each of the output rails.

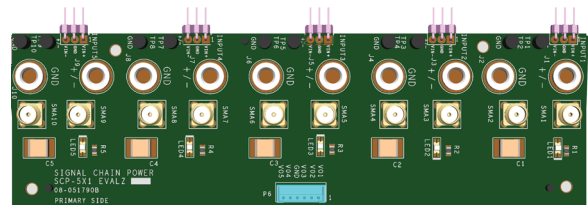


Figure 7. The 5×1 reintegration board combines multiple rails into a single connector breakout.

The 5×1 reintegration board combines a multiple output rail into a single pigtail DUT connector with the provisions of additional filtering, current sensing, power, and signal measurement through SMA connectors, and a banana jack for standard output measurement and characterizations.

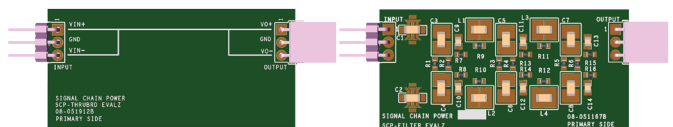


Figure 8. Through board (left) and filter board (right).

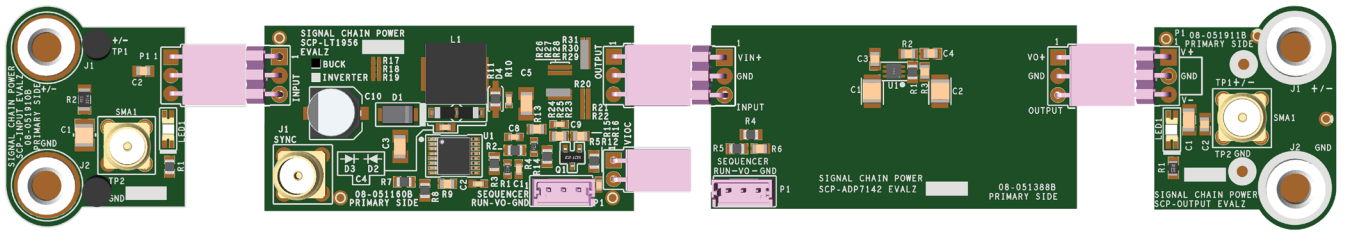


Figure 9. An example power supply configuration that uses a switcher board, an LDO board, and the input and output boards.

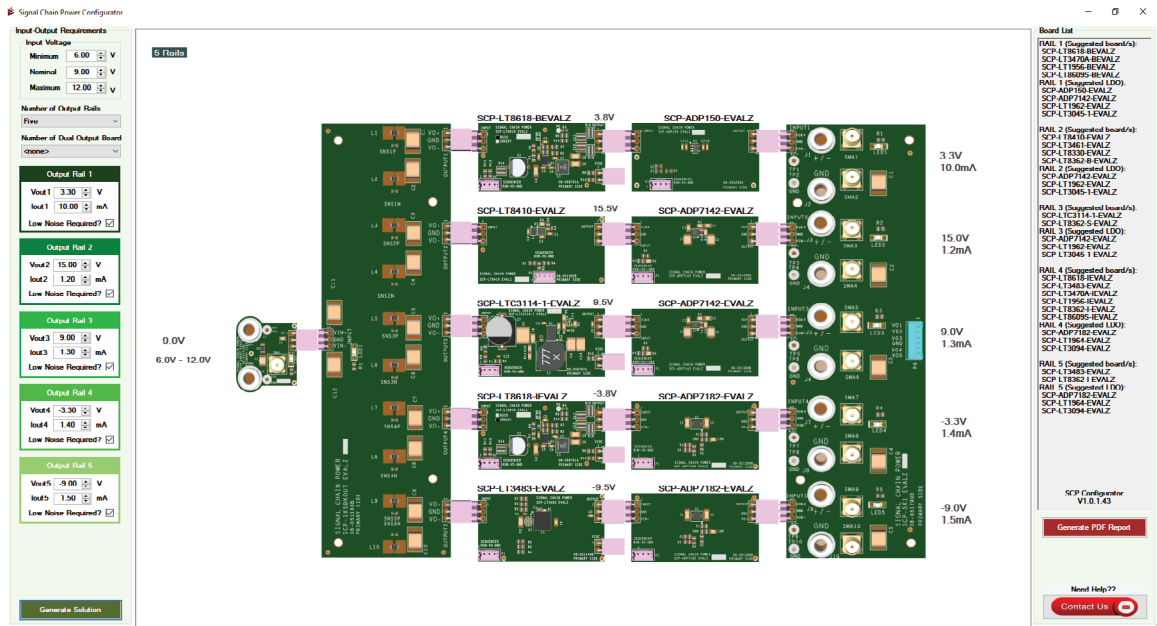


Figure 10. SCP Configurator software with a generated solution of five output rails.

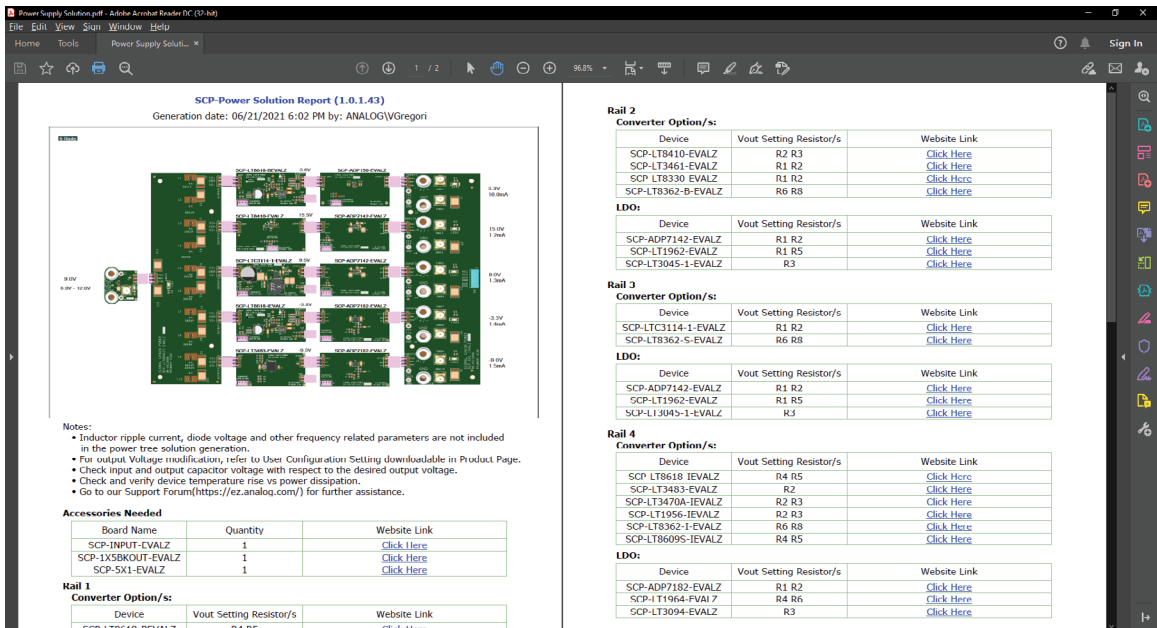


Figure 11. A generated solution report in PDF format.

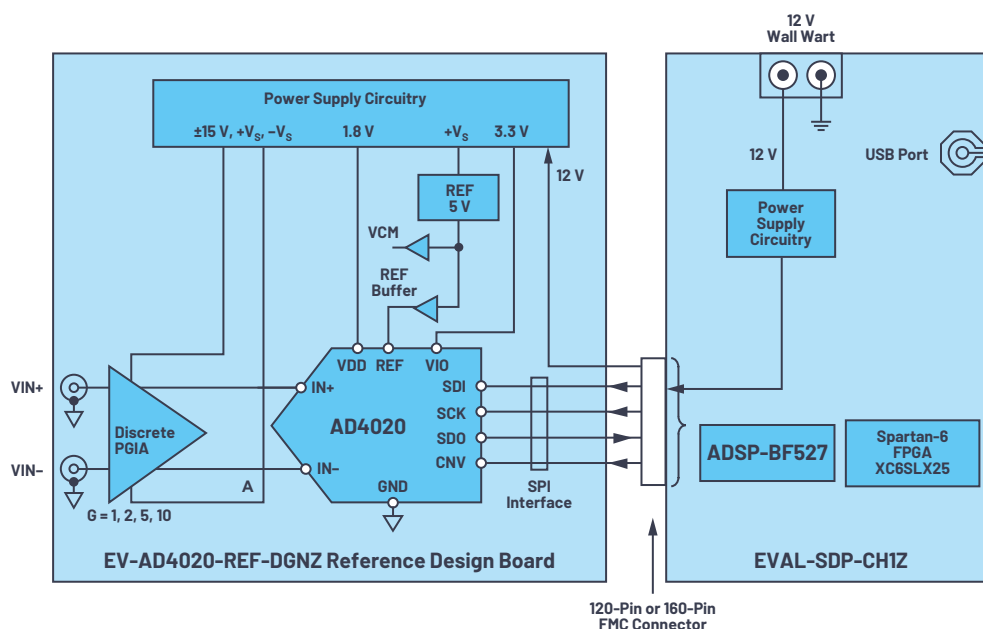


Figure 12. A system block diagram of the CN0513, which will be used in evaluating the noise performance of the SCP hardware.

The through board serves as a spacer to balance the gaps created by adjacent rails. The filter board can also be used as a spacer, in case additional passive filtering is required for better system noise performance. The filter board supports the usage of RC, LC, feedthrough capacitors, ferrite beads, and other pin network configurations.

The single input and output boards can be used for single rail evaluations. They also have multiple interface options such as a banana jack, grabber, or SMA for input and output characterizations.

By utilizing the SCP hardware platform, a system designer can easily create and design a complete power solution and quickly evaluate the performance of a signal chain system. Quick and easy power system optimization is also realized with the plug and play configuration of the SCP power boards. When the design optimization is done and ready to integrate into the final design, all engineering collaterals are available for download at [analog.com](http://analog.com).

## Signal Chain Power (SCP) Configurator

The SCP Configurator is a companion software tool for the SCP series of hardware evaluation boards. It's a simple and intuitive graphical user interface (GUI) that enables design engineers, with or without prior power supply design experience, to quickly generate a power solution for their signal chain system.

The algorithm provides the best building block of a power architecture based on the requirements the user has provided. The input voltage source, output voltages, and anticipated load current values the signal chain system requires should be determined first. If low noise is a requirement on a specific rail, a checkbox is provided to enable that. This adds an LDO postregulator to reduce noise on the rail. This brings back the most challenging question in developing a power solution for a signal chain: "How quiet is good enough?"

The GUI in Figure 10 shows the result of the generated power solution. It yields a graphical display of the generated power solution that aids the user on how

to construct the power tree and interconnect all relevant SCP hardware board series. A list of possible alternative board(s) for each rail is provided. These alternative boards are arranged by increasing output current capability.

Additionally, the GUI's generated power solution can be printed in PDF format. The report contains the same graphical representation of the output design and list of board suggestions for each rail. What is added in the report is a list of all accessories needed that will aid in interconnecting power module blocks. Also included are shortcut links that redirect the user to corresponding board documentation, such as but not limited to board layout design, bill of materials (BOM), and a schematic diagram that could be readily copied and used as a design reference.

## How It Works

Once the customized power architecture of the signal chain system is complete, the building blocks can be snapped together to create a hardware testing platform, and a performance evaluation of the whole signal chain system can be carried out. To demonstrate how the SCP platform eases the design and evaluation process of the power solution for the signal chain, the platform will be used to design a power solution for the AD4020 differential SAR ADC. In this example, the SCP platform will power the CN0513, a low drift, high accuracy data acquisition solution that uses the AD4020.

The SAR ADC requires a 1.8 V power supply (VDD) and a digital power supply for the input/output interface (VIO). The VIO rail can handle an input from 1.71 V to 5.5 V. For this demonstration, 3.3 V will be set as the VIO input voltage. The programmable gain instrumentation amplifier (PGA) uses two voltage rails for the power supply pins +V<sub>S</sub> and -V<sub>S</sub>, respectively.

To start using the platform, the SCP Configurator takes an input voltage requirement to generate a power solution for the system. A nominal input voltage of 9 V will be used.



**Input-Output Requirements**

**Input Voltage**

Minimum	9.00	V
Nominal	9.00	V
Maximum	9.00	V

Figure 13. The input voltage requirements section of the SCP Configurator.

The SCP Configurator also uses the voltage and current requirements of the system. In this demonstration, these would be the 1.8 V VDD rail, the 3.3 V VIO rail, and the +5.5 V and -1.0 V for the PGIA's dual supply rails. The current requirements of these inputs can be obtained from the component's data sheets and are shown in Table 1. The PGIA's input stage uses two [ADA4627-1](#) JFET operational amplifiers, and each takes up a maximum of 7.8 mA. This results in a maximum current of 15.6 mA. Additional current is added to consider the other parts of the PGIA, resulting in a maximum current of 20 mA for both +V<sub>s</sub> and -V<sub>s</sub> rails. These will be put in the GUI, which generates a power solution using the SCP platform hardware. There is also a checkbox to indicate if the rail has a low noise requirement. Placing a check adds an LDO regulator to improve the noise performance of the power rail. For this demonstration, the low noise requirement will be placed on all the voltage rails.

### Table 1. AD4020 Power Supply Requirements

Power Rail	Rail Voltage	Maximum Current
VDD	1.80 V	1.10 mA
VIO	3.30 V	0.30 mA
+V <sub>s</sub>	5.50 V	20.0 mA
– V <sub>s</sub>	–1.00 V	20.0 mA

**Number of Output Rails**

**Number of Dual Output Board**

**Output Rail 1**

Vout1  V  
Iout1  mA

Low Noise Required? ☒

**Output Rail 2**

Vout2  V  
Iout2  mA

Low Noise Required? ☒

**Output Rail 3**

Vout3  V  
Iout3  mA

Low Noise Required? ☒

**Output Rail 4**

Vout4  V  
Iout4  mA

Low Noise Required? ☒

Figure 14. The power rail requirements section of the SCP Configurator.

The generated power solution of the SCP Configurator is shown in Figure 15. There is also a prompt that suggests using only an LDO regulator for the 1.8 V and 3.3 V output rails. This is important, as this can be useful in optimizing the power solution. The reason behind this is while the SCP Configurator generates a complete power tree, this power tree can be easily changed due to the hardware's form factor. This makes the implementation of changes to the power solution faster.

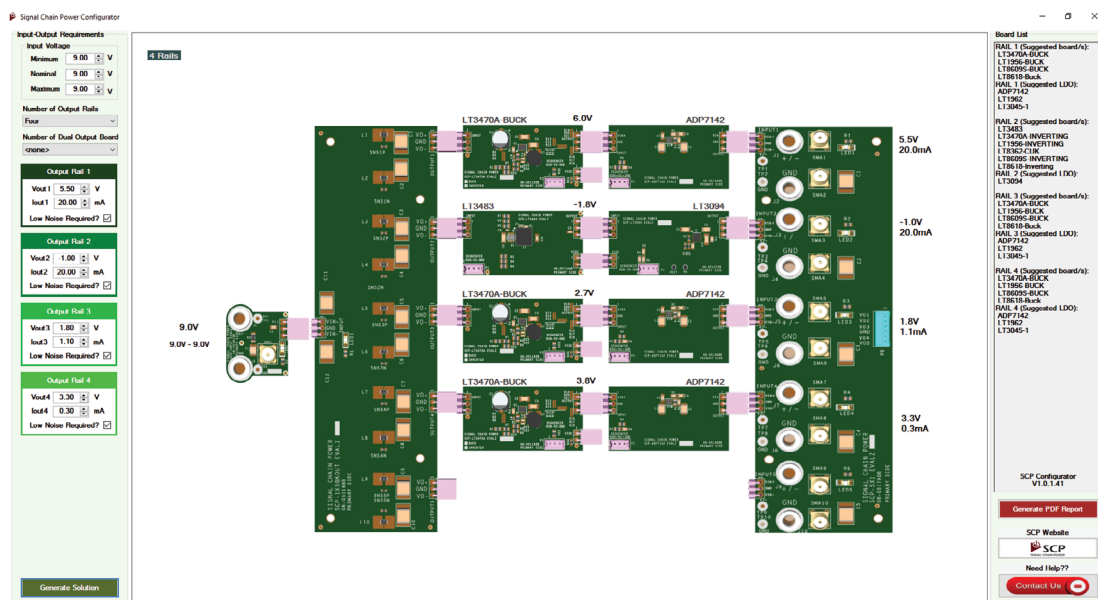


Figure 15. The power solution generated by the SCP Configurator from the requirements in figures 13 and 14.

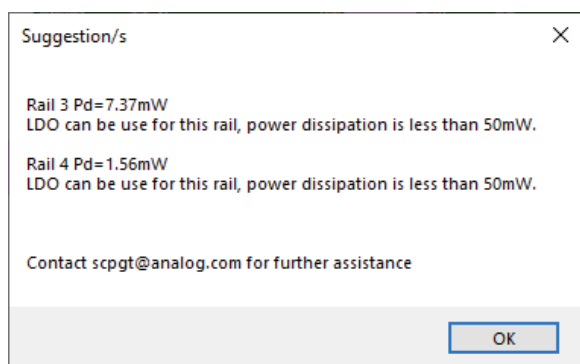


Figure 16. A prompt that suggests using only LDO regulators for rails 3 and 4 (1.80 V and 3.30 V).

There are two methods for determining how much power supply noise is tolerable. The first method is understanding and quantifying signal processing load sensitivity to power supply noise,<sup>1</sup> which is tedious and complicated. The second method is an optimal and practical approach, which is running a quick system performance evaluation, where the plug and play system of the SCP hardware platform comes into play.

To measure the performance of the hardware, the CN0513 noise metrics were obtained. A 1 kHz sine wave from a waveform generator is used as an input to the evaluation board, and the equivalent FFT of the sine wave that the ADC sampled is checked. This process was first done using the on-board power supplies for reference on the performance of the AD4020. After this, the SCP platform was connected as external supplies to the evaluation board. Each positive rail was checked three times: using the suggestion from the SCP Configurator, using only the switcher board, and using only the LDO board. The negative rail, on the other hand, was only tested using the default suggestion because the output voltage requirement is below the minimum output voltage of the negative switcher boards, and the negative LDO regulators cannot be connected to the input positive voltage.

This variety of tests demonstrates the effect of different combinations of power management ICs on the SAR ADC's performance. Tables 2, 3, and 4 show the noise parameters of the ADC for the different power rails.

## Analysis

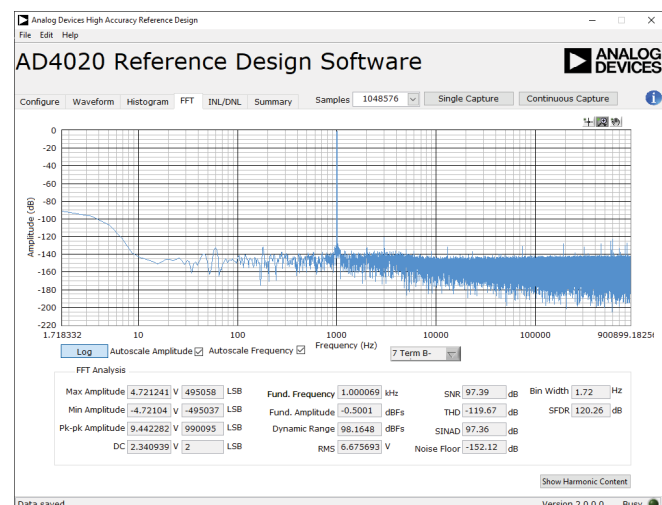


Figure 17. Noise measurements of the CN0513 with the SCP platform as external supplies.

**Table 2. Positive Supply Rail (+V<sub>s</sub> = 5.5 V)**

Parameter	Switcher + LDO	Switcher Only	LDO Only
Dynamic range	98.165 dB	98.434 dB	98.362 dB
Spurious-free dynamic range (SFDR)	120.26 dB	120.07 dB	120.4 dB
Signal-to-noise ratio (SNR)	97.39 dB	97.66 dB	97.59 dB
Total harmonic distortion (THD)	-119.67 dB	-119.5 dB	-119.76 dB
Signal-to-noise-and-distortion ratio (SINAD)	97.36 dB	97.63 dB	97.56 dB

**Table 3. AD4020 Power Supply Rail (VDD = 1.8 V)**

Parameter	Switcher + LDO	Switcher Only	LDO Only
Dynamic range	98.165 dB	98.301 dB	98.347 dB
SFDR	120.26 dB	119.46 dB	119.55 dB
SNR	97.39 dB	97.53 dB	97.57 dB
THD	-119.67 dB	-118.75 dB	-118.97 dB
SINAD	97.36 dB	97.49 dB	97.54 dB

**Table 4. Digital Power Rail (VIO = 3.3 V)**

Parameter	Switcher + LDO	Switcher Only	LDO Only
Dynamic range	98.165 dB	98.119 dB	98.152 dB
SFDR	120.26 dB	120.65 dB	120.16 dB
SNR	97.39 dB	97.34 dB	97.38 dB
THD	-119.67 dB	-120.12 dB	-119.69 dB
SINAD	97.36 dB	97.32 dB	97.35 dB

From tables 2, 3, and 4, the noise metrics between different configurations of the SCP hardware boards is comparable. For the 5.5 V positive supply rail, using only a switcher board or LDO board by itself is a possible option, as it has shown improvement over the configuration that uses both LDO and switcher boards. For the 1.8 V AD4020 supply rail, using only an LDO board yields the highest dynamic range, SNR, SINAD, and lowest THD among the three configurations. However, this comes at a lower SFDR than the combined switcher and LDO boards. The data for the 3.3 V digital power rail shows that all configurations can be used since for every metric, a different configuration had the best measurement. The data between the different rails is comparable with one another, but these differences in the measurements can have a large impact on the application's performance.

These observations on the noise metrics using different SCP configurations would take more time if done using individual demo boards. The differences in the noise metrics can have a huge impact on the signal chain that the power solution will be supplying power to, so having a platform that reduces the time and effort needed to determine the optimal power solution for the system helps. The platform also performs well when the noise metrics are considered, which can help designers look at other aspects of the power solution, such as efficiency, cost, and solution size.

## Conclusion

A lot of factors need to be considered in designing and evaluating a power solution, and time is needed to evaluate its performance. This article demonstrated the Signal Chain Power (SCP) platform by measuring noise metrics of the CN0513 with different power rail configurations, a task that can take a significant amount of time if traditional methods are used. The [SCP hardware evaluation platform](#) and [SCP Configurator tool](#) can alleviate many of the challenges in both the design and evaluation of power solutions, thus benefiting signal chain system engineers at any level of expertise.

## Reference

<sup>1</sup> Pablo Perez, Jr. and Patrick Errgy Pasaquian. "Optimizing Power Systems for the Signal Chain—Part 1: How Much Power Supply Noise Is Tolerable?" *Analog Dialogue*, Vol. 55, No. 1, March 2021.

## About the Authors

Joseph Rommel Viernes is a power applications staff engineer at Analog Devices Philippines. He joined ADI in 2018. He has more than 16 years of power supply design experience working at companies such as Emerson Network Power, Phihong Technology, Power Integrations, and now Analog Devices. His focus is on industrial and communications power system applications. He earned his bachelor's degree in electronics engineering from De La Salle University Manila, Philippines. He can be reached at [joseph.viernes@analog.com](mailto:joseph.viernes@analog.com).

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