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A New Variation of the Classic Instrumentation Amplifier (PGIA) Offers More Design Flexibility

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Introduction

As useful and versatile as instrumentation amplifiers (IAs) are when it comes to interfacing to a transducer, there are constraints that hamper the design of variable gain IAs or programmable gain instrumentation amplifiers (PGIAs), also referred to as software programmable gain amplifiers (SPGAs) in some literature. The need for such PGIAs arises because of the often-encountered case of adapting the circuit to a wide range of sensors or environmental conditions. With a fixed gain, the system designer may have to contend with suboptimal SNR, which could compromise precision. Many of the techniques that are useful in creating an accurate and stable PGIA are discussed in my colleague's *Analog Dialogue* article, "Programmable Gain Instrumentation Amplifiers: Finding One that Works for You," which points out the possible pitfalls of such a design and presents a comprehensive survey of available solutions and techniques. In this article, I will present another tool and methodology to facilitate such work and I will go through the design steps that allow one to quickly home-in on the external component values needed to create a precise PGIA using a newly released instrumentation amplifier.

A New Instrumentation Amplifier Architecture

One common instrumentation amplifier architecture is shown in Figure 1.

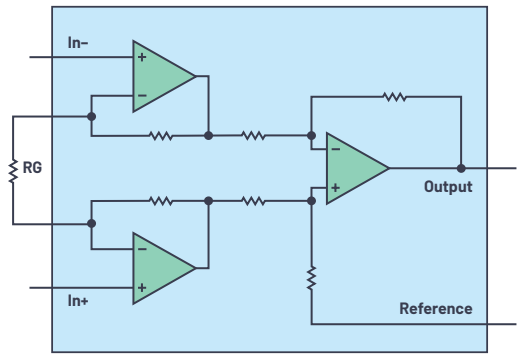

Figure 1. Classic instrumentation amplifier.

The gain is set by the value of the external resistor RG. To create a PGIA with such a device, one merely needs to switch the value of RG. This is commonly done using an analog switch or a mux. However, some of the nonideal behaviors of an analog switch complicate this task—examples being the switch on-resistance, its channel capacitance, and the variation of channel resistance with applied voltage.

One variation on the standard instrumentation amplifier architecture is shown in Figure 2. Notice how the RG pins are broken up as ±RG,S and ±RG,F and individually pinned out and accessible from the outside of the device package.

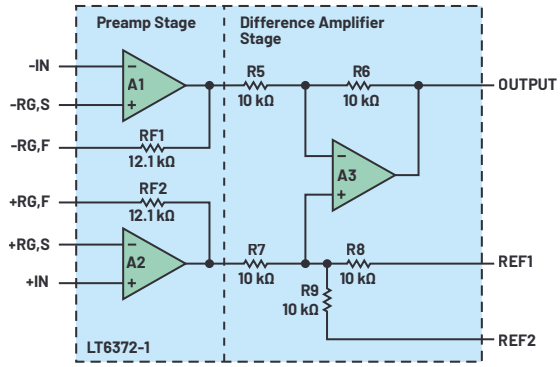

Figure 2. LT6372-1 architecture allows access to some of the IA internal nodes.

A useful and important feature of the architecture shown in Figure 2 is the ability to configure the instrumentation amplifier so that it can switch between several distinct gain values while minimizing any gain error because of the finite switch resistances. This feature can be used to create a PGIA.

As mentioned, any resistor programmable in-amp can be enabled to vary its gain by switching the value of the gain-setting resistor accordingly. However, there are significant drawbacks to this such as:

- Large gain error due to switch on-resistance (R_{ON}) nominal value and its variation.
- High gain values may be impossible to achieve due to the low switch R_{ON} values required.
- Signal distortion due to switch nonlinearity. That is because signal current flows directly through R_{ON} and thus any variation in its value as a function of voltage causes distortion.

The LT6372-1 can alleviate these concerns when configured as a PGIA, shown in Figure 3, because of how the RG,F and RG,S pins are separately pinned out. In this schematic, the signal from a Wheatstone bridge, consisting of R5 to R8, is amplified with four possible gain values selectable by the user depending on which SW1 switch position is selected. The LT6372 family pinout allows one to create a PGIA that takes advantage of varying the ratio of RF/RG to get the desired gain values.

Furthermore, the U1, U2 analog switch R_{ON} is minimized as a source of gain error because it can be placed in series with the input stage inverting terminal and its feedback resistor. Configured this way, R_{ON} is only a small fraction of the total internal 12.1 kΩ feedback resistance and thus has little impact on gain error and drift. By the same token, distortion due to the switch nonlinearity is minimized because of the R_{ON} value being a small fraction of the overall feedback resistance causing little or no effect due to variation of its value with voltage. Furthermore, the input stage of this device is comprised of a current feedback amplifier (CFA) architecture, which by its nature allows less variation in bandwidth or speed as gain is varied when compared to a traditional voltage feedback amplifier.[1] All this culminates in the ability to create a precision PGIA with accurate gain steps using low cost external analog switches.

Figure 4 shows a simplified diagram of the PGIA to demonstrate how different taps of the resistor ladder, implemented by analog switches (eight total) shorted two at a time to set the gain, configure the circuit. In this diagram, the two switch banks are depicted in one of the four possible gain values; that being with the –RG,S and +RG,S pins shorted to the RF3/RF4 junction.

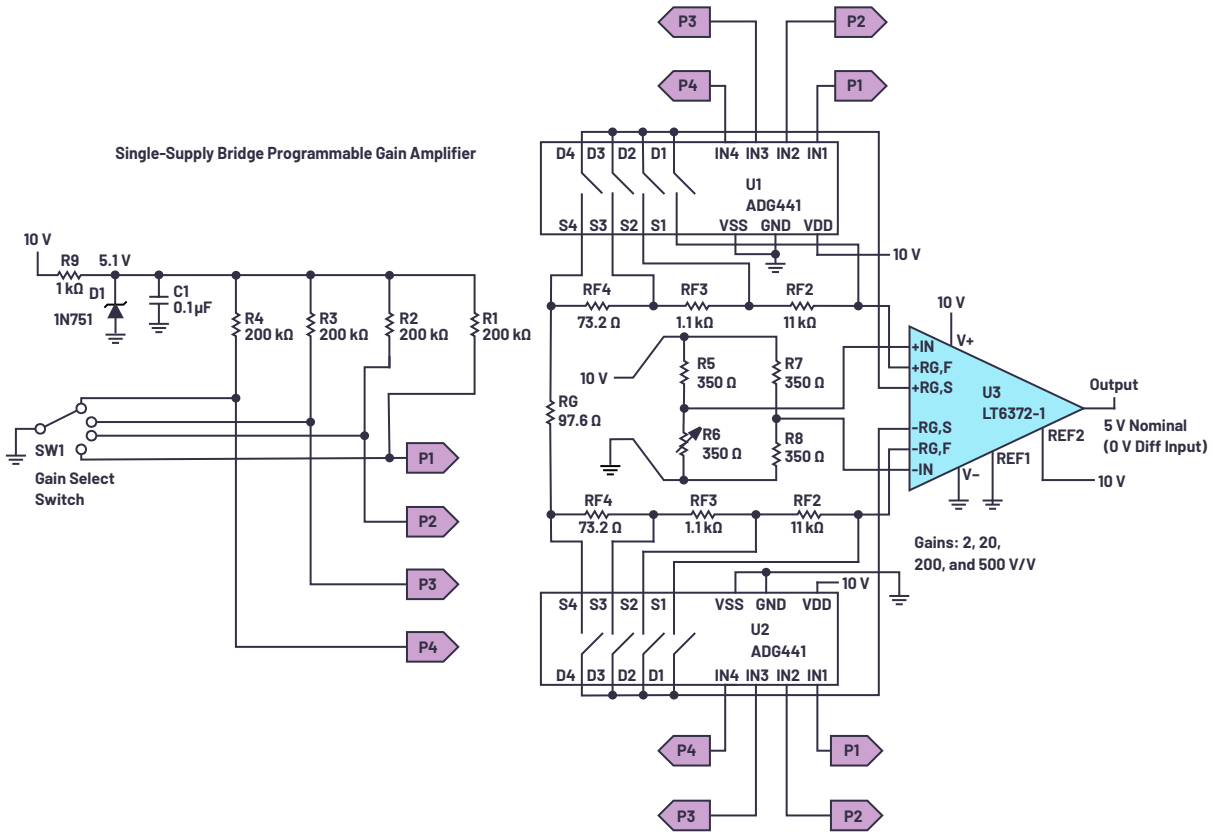

Figure 3. LT6372-1 PGIA bridge interface with four gain settings.

[1] CFA closed-loop bandwidth is inversely proportional to the value of RF, whereas a traditional voltage feedback architecture bandwidth is inversely proportional to the gain (RF/RG).

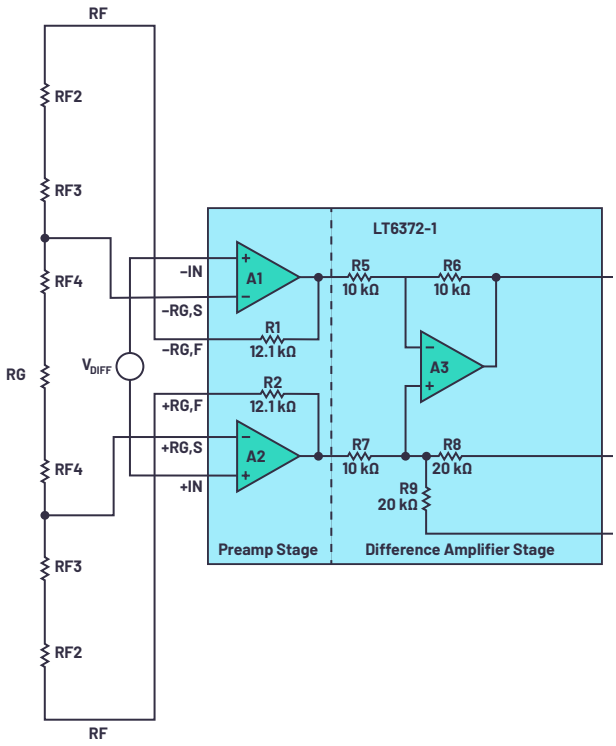

Figure 4. LT6372-1 block diagram and simplified external connection (gain switches not shown) for the PGIA.

Design Steps to Compute External Resistors for Any Gain

Figure 3 shows the complete PGIA configuration, including the switches required, which can accommodate an arbitrarily large gain range. Four possible gain values are included here, but it is possible to increase that number by adding more switches to the design. As noted earlier, the feature of allowing access to the RG,F and RG,S pins enables one to increase RF for large gains, and to reduce RG for low gains to create a versatile PGIA. For purposes of gain computation, one can consider the feedback resistor to be the internal 12.1 kΩ trimmed resistance plus other resistances in series with RG,F on its way to reach the RG,S terminal. Conversely, the gain setting resistor is the total resistance seen between +RG,S and –RG,S. This is summarized as:

RF = 12.1 kΩ + resistance between RG,F and RG,S on each of the two input amps

RG = Resistance between +RG,S and –RG,S

Gains from greater than 1 V/V up to 1000 V/V are possible with this configuration. With the switches set to short pins S3, and D3 on both U1 and U2 switches, here are the corresponding RF and RG values and the resulting gain:

RF = 12.1 kΩ + 11 kΩ + 1.1 kΩ = 24.1 kΩ

RG = 73.2 Ω + 97.6 Ω + 73.2 Ω = 244 Ω

G = 1+ 2RF/RG = 1 + 2 × 24.1 kΩ/244 Ω = 199 V/V

It is easy to see that deciding on which values to use for the external resistors is an iterative and interdependent process where the possible gain values interact and influence the choice of resistors to use. Some common gain value component values are tabulated in Table 1 for easy reference, but a multitude of other gain combinations (G) are also possible.

Table 1. Component Values for Some PGIA Gain Combinations

Case	RF2 (kΩ)	RF3 (kΩ)	RF4 (kΩ)	RG (kΩ)	G1	G2	G3	G4
1	6	4.5	1.1	0.756	2	4	16	64
2	10.9	1.1	0.0726	0.097	2	20	200	500
3	8.6	6.1	4.3	20.8	1.4 (3 dB)	2 (6 dB)	2.8 (9 dB)	4 (12 dB)

Procedure for Determining the Value of the PGIA

The individual resistors in the gain network can be calculated sequentially using the formula given in Equation 1. The equation determines the resistors as labeled in Figure 3, where Case 2 from Table 1 (gains 2, 20, 200, and 500 V/V) is used as a worked-out example. The feedback resistors and the gain setting resistors are interactive; thus, the formula must be a series where the present term is dependent on the preceding term(s). The formula is given by:

$$R_{F_{i+1}} = \left[R_T - \sum_{j=1}^{i} R_{F_j}\right] \times \left(1 - \frac{G_i}{G_{i+1}}\right) \quad (1)$$

Here are some definitions:

R_{F_1} = 12.1 kΩ (internal to the LT6372-1)

M: Number of gains (4 in this case)

G_i: The gain instance (either 2, 20, 200, or 500 V/V for G_1 – G_4 respectively of this example)

i: Varies from 1 to (M-1) to compute RF_{i+1}

$$R_T = \frac{12.1\ \text{k}\Omega \times G_1}{G_1 - 1} \quad (2)$$

Equation 1 can be used to calculate the necessary feedback resistors for any set of gains. A dummy variable (j) serves as a counter to keep a running total of the preceding feedback resistors.

- Before making any calculations, it is advised to draw a resistor network similar to the network in Figure 3. The network will have (2 × M) – 1 resistors, where M = number of gains. For this example, M = 4 and, therefore, the resistor string will have seven resistors. Equation 1 needs to be evaluated for i = 1 ⟶ (M – 1).

G1 = 2, G2 = 20, G3 = 200, G4 = 500 V/V

From Equation 2:

$$R_T = \frac{12.1\ \text{k}\Omega \times G_1}{G_1 - 1} = \frac{12.1\ \text{k}\Omega \times 2}{2 - 1} = 24.2\ \text{k}\Omega \quad (3)$$

Evaluating Equation 1 iteratively from i = 1 ⟶ (M-1)

$$\begin{aligned} &i = 1 \longrightarrow R_{F_2} = [24.2\ \text{k}\Omega - 12.1\ \text{k}\Omega]\left(1 - \frac{2}{20}\right) \longrightarrow R_{F2} = 10.89\ \text{k}\Omega \\ &i = 2 \longrightarrow R_{F_3} = [24.2\ \text{k}\Omega - (12.1\ \text{k}\Omega + 10.89\ \text{k}\Omega)]\left(1 - \frac{20}{200}\right) \longrightarrow \\ &\quad R_{F3} = 1.089\ \text{k}\Omega \\ &i = 3 \longrightarrow R_{F_4} = [24.2\ \text{k}\Omega - (12.1\ \text{k}\Omega + 10.89\ \text{k}\Omega + 1.089\ \text{k}\Omega)] \\ &\quad \left(1 - \frac{200}{500}\right) \longrightarrow R_{F4} = 72.6\ \Omega \end{aligned} \quad (4)$$

The center resistor RG can then be computed using the following:

$$R_G = \frac{2\sum_{i=1}^{M} R_{Fi}}{G_M - 1} = \frac{2(RF1 + RF2 + RF3 + RF4)}{G_4 - 1} = \frac{2(12.1\ \text{k}\Omega + 10.89\ \text{k}\Omega + 1.089\ \text{k}\Omega + 72.6\ \Omega)}{500 - 1} = 96.8\ \Omega \quad (5)$$

With this last computation, all four resistor values shown in Table 1 are computed and the design computation is finished.

Measured Performance Plots

Here are some plots showing the performance that can be achieved with this PGIA configuration:

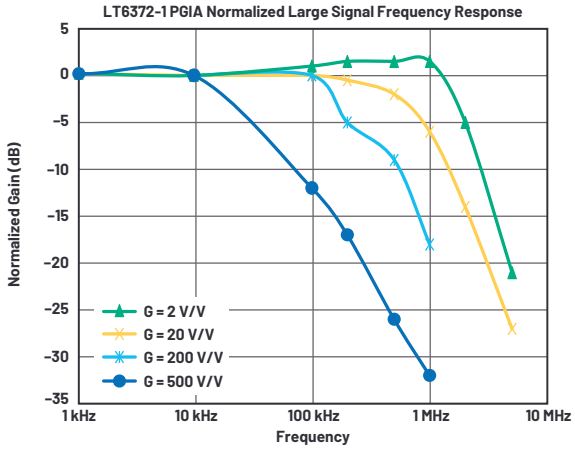

Figure 5. PGIA large signal frequency response.

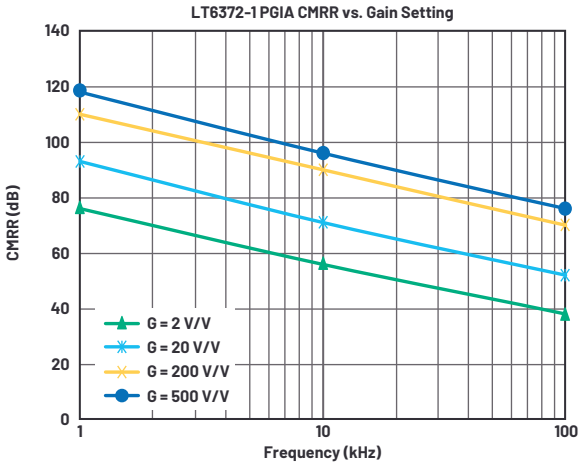

Figure 6. PGIA CMRR vs. frequency.

With the switch capacitances of ADG444, at the lowest gain setting (G1 = 2 V/V) the small signal frequency response shows some appreciable peaking (see Figure 7). This behavior only shows with the lower gain settings where the LT6372-1 bandwidth extends high enough to be affected by the pF range capacitance of the switch. Choosing a lower capacitance switch (for example, ADG611/ADG612/ADG613 with 5 pF on capacitance) or alternatively limiting the lowest gain setting of the PGIA are ways to work around this side effect.

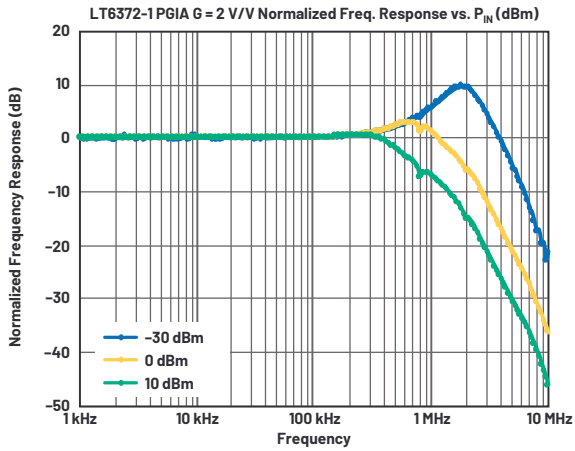

Figure 7. PGIA small signal low gain peaking.

Conclusion

A method was introduced to add gain select ability to instrumentation amplifiers by utilizing the pinout feature of a newly released set of devices, the LT6372 family. Characteristics of such a PGIA were analyzed, and the design steps were spelled out along with performance measurements. The LT6372-1 is uniquely qualified for such a solution as it is highly linear and offers precise dc specifications and performance.

About the Author

Hooman Hashemi joined Analog Devices in March 2018, where he works on characterizing new products and developing applications that showcase the products' features and uses. Hooman previously worked for Texas Instruments for 22 years as an applications engineer, concentrating on the high speed portfolio. He graduated from University of Santa Clara with an M.S.E.E. in August 1989 and San Jose State University with a B.S.E.E. in December 1983. He can be reached at hooman.hashemi@analog.com.