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The On-Chip Calibration Benefits of New Simultaneous SAR Analog-to-Digital Converters

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Abstract

This article evaluates the impact of external resistors used in front of resistive analog-to-digital converters (ADCs). These families of simultaneous sampling ADCs include a high input impedance resistive programmable gain amplifier (PGA) that drives the ADC and scales the input signal, allowing direct sensor interface. However, there are several reasons why a design would end up adding external resistors in front of the analog input. The following sections provide a theoretical explanation of the gain error expected, as a function of the resistor sizes, and different ways to minimize these errors. This article also examines resistor tolerance and the ADC's input impedance effects of the different calibration options. Beyond the theoretical study, bench measurements compare several devices to prove the excellent accuracy reached with on-chip gain calibration features. The gain calibration feature enables a system error of less than 0.05%, across a wide range of front-end resistor values, without having to perform any calibration routine, but just by writing a single register per channel.

Introduction

Simultaneous sampling successive approximation register (SAR) ADCs are traditionally defined as a response to the need expressed mainly by energy customers for protection relay applications. In transmission and distribution networks, the protection relay monitors the grid to react to any fault condition (overvoltage or overcurrent) in the minimum time possible, to avoid critical damage.

In order to monitor the power transmitted, both current and voltage need to be measured simultaneously. Current is measured through current transformers (CTs) that scale down the current, providing isolation and converting to voltages through a burden resistor. Voltage is measured through a resistor network, a voltage divider that scales the voltage down from the kV to V range. Analog Devices offers simultaneous sampling ADCs to monitor both voltages and current, simplifying the power calculations of dual, quad, or octal devices. Figure 1 shows a signal chain diagram normally used for measuring power in a single-phase, multi-phase electrical system, which would require a higher channel count data acquisition system (DAS)—that is, eight channels for three phases plus neutral.

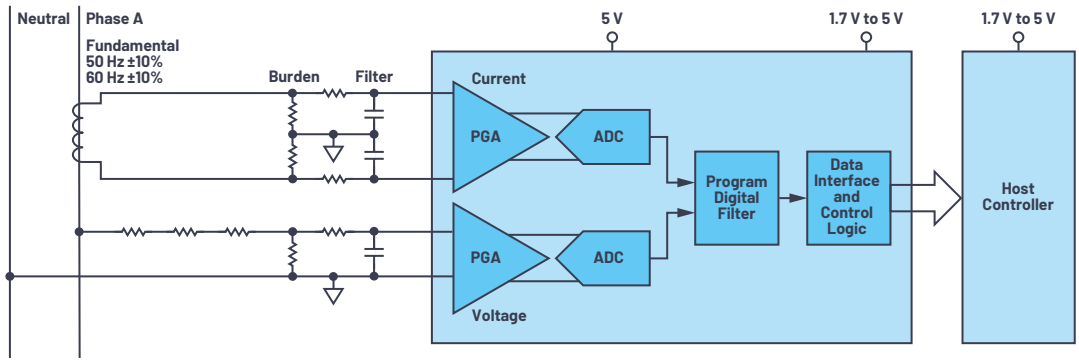

Figure 1. A typical signal chain in power monitoring applications. Only one phase is shown for simplicity.

When to Use External Front-End Resistors

Although the resistive input ADCs are designed to directly interface to most sensors, there are certain conditions where external resistors placed in front of the analog inputs may be needed. This could be the case, for example, if an application calls for extra antialiasing filtering or protecting the inputs against overcurrent fault condition.

Antialiasing Filter

Even though the resistive input ADCs normally provide an internal antialiasing filter, many applications may run at lower sampling frequencies—hence, the need for lower corner frequency.

A common requirement is to gather 256 samples per power line cycle—that is, for a 50 Hz power grid system a sampling frequency (f_S) of 12.8 kSPS.

$$f_S = 256\ samples \times 50\ second^{-1} = 12{,}800\ samples/second \quad (1)$$

Such low sampling frequency pushes the need for an external low-pass filter (LPF) in front of the resistive ADC's inputs, suppressing any frequency above about 6.4 kHz, the Nyquist frequency ($f_S/2$). This can be achieved by adding a first-order RC filter.

Input Protection

In other application examples, especially within the protection relay market, there is a possibility of overcurrent flowing into the analog input pins when a fault condition occurs. To avoid damaging the device, the absolute maximum rating (AMR) indicates to limit the input current under 10 mA. To do so, placing an external in-series resistor is recommended, limiting such potential input current.

If the sensor output accidentally increases up to ±30 V—as the input clamp protection circuitry can tolerate voltages up to ±16.5 V—the input clamp protection circuit will turn on and sink a large current that can damage the device. Placing a 1.35 kΩ R_{FILTER} in front of the analog inputs would prevent a current larger than 10 mA to flow in during the overstress; however, it's recommended to guard band the maximum limit by using a larger resistor, for example, 10 kΩ.

$$R_{FILTER} = \frac{30\ V - 16.5\ V}{10\ mA} = 1.35\ k\Omega \quad (2)$$

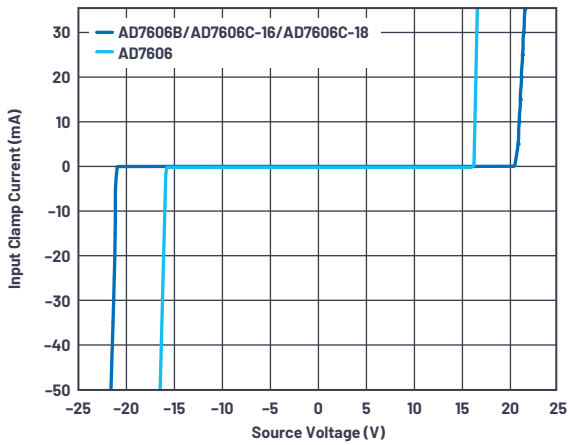

Figure 2. AD7606 input protection clamp profile.

In any case, a larger resistor among the ones calculated from Equation 2—that is, for either the antialiasing filter (AAF) or the current limit—must be used to ensure meeting both conditions. Note, however, that if the potential overstress of the analog input signal sits below ±21 V during a fault condition and there is no need for an external AAF, an external resistor may not be needed.

Errors Introduced by External Resistors

The drawback when introducing such external resistors—whether these are for extra filtering or protecting against a large current—is the impact they have on the system accuracy. The AD7606, for example, is factory trimmed to provide exceptionally low offset and gain errors—that is, 32 LSBs[1] and 6 LSBs maximum respectively—across the full temperature and supply ranges. However, by adding external passives, these specifications are no longer valid, as the system gain error (understood by the system as the resistive input ADC plus the resistor in front) becomes larger than the AD7606's gain error. Such system gain error is a concern for system designers because it means they have to perform system gain calibration themselves, such that their final product meets the accuracy target dictated by either the standards or end users. That system gain calibration can be done in two ways:

- Performing a gain calibration in production—that is, passing every manufactured system through a calibration routine, storing the calibration coefficients, and using them to remove the gain errors. This is like what the ADC does at an IC level, but at a system level.
- Applying a fixed correction factor to each ADC sample. As the systematic gain error is well understood per the analysis given in the following section, the digital host controller could multiply each sample obtained from the ADC by a factor that removes the system gain error. This is referred to later as back-end calibration.

The first solution may achieve the greatest accuracy, but requires a long production test time, which largely increases a product's cost. The second solution, although cheaper, is less accurate because it relies on the ADC's typical input impedance and implies using controller resources, which in some cases may be limited. Alternatively, so both complications are avoided, a customer may request a larger and larger input impedance, in which case the error introduced by the front-end resistors decreases and the resulting system accuracy improves. With this approach, the problem shifts from a system problem to an IC problem. However, it may not be the most efficient method because increasing the input impedance means having to develop new solutions, which takes time and causes new problems such as higher noise due to those larger on-chip resistors. The AD7606B and AD7606C include an on-chip gain calibration feature that removes the system gain error introduced by the external resistors, achieving the greatest accuracy without having to perform any calibration, and so adding no extra cost to the system solution.

Gain Error

The gain of the PGA is set by the feedback resistor (R_{FB}), which is programmable to set the analog input range, and the input impedance (R_{IN}), which is fixed and typically 1 MΩ. These resistors are trimmed to properly set the PGA gain, to scale the ±10 V or ±5 V analog input signal (AIN+/-) down to the ADC input range that is, ±4.4 V, as shown in Figure 3.

$$AD7606\ Gain = \frac{R_{FB}}{R_{IN}} = \frac{V_{OUT}}{V_{IN}} = \frac{4.4\ V}{10\ V} = 0.44\ (V/V) \quad (3)$$

[1] Least significant bit (LSB), equivalent to 305.175 µV in the ±10 V range or 152.58 µV in the ±5 V range

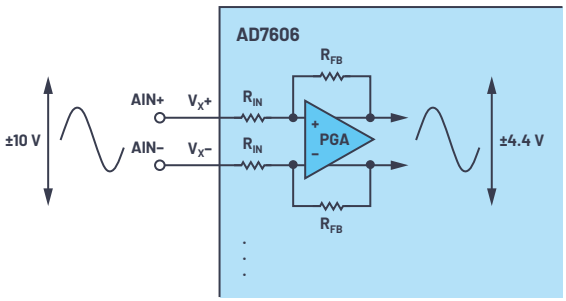

Figure 3. AD7606 internal PGA. Only the ±10 V range is shown as an example.

However, when a series resistor is placed in front of the PGA—let us call it R_{FILTER}—its gain is modified from the ideal. That resistor is indeed modifying the denominator of Equation 3; therefore, the system gain is lower than what it is trimmed for.

$$System\ Gain = \frac{R_{FB}}{R_{IN} + R_{FILTER}} = \frac{V_{OUT}}{V_{IN}}\ (\text{V/V}) \qquad (4)$$

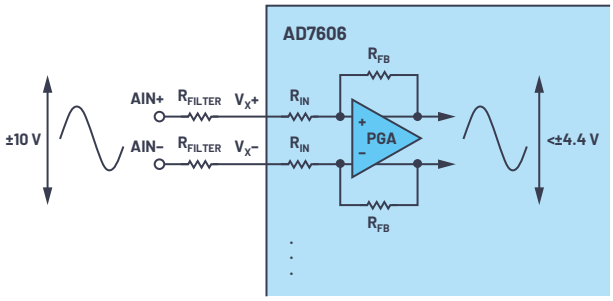

Figure 4. A series resistor in front of the AD7606's analog inputs (V_X+ and V_X-) modifies the system gain.

For example, if a 30 kΩ resistor is used in front of the AD7606, a 10 V input signal is no longer a 10 V signal at the ADC output because the AD7606's PGA output is no longer 4.4 V. The PGA output will be 4.2718 V instead, as we can see if we plot the new theoretical system gain transfer function—that is, about –3% gain error, as shown in Figure 5.

We can calculate the gain error as a function of R_{FILTER} by:

$$System\ Gain\ Error\ (\%\ of\ FS) = \frac{System\ Gain - AD7606\ Gain}{AD7606\ Gain} \times 100 = \left\{\frac{R_{IN}}{R_{IN} + R_{FILTER}} - 1\right\} \times 100 = -\frac{R_{FILTER}}{R_{IN} + R_{FILTER}} \times 100 \qquad (5)$$

For easy evaluation, Equation 5 can be presented graphically as a system gain error, in % of full scale (FS) vs. R_{FILTER}, as shown in Figure 6.

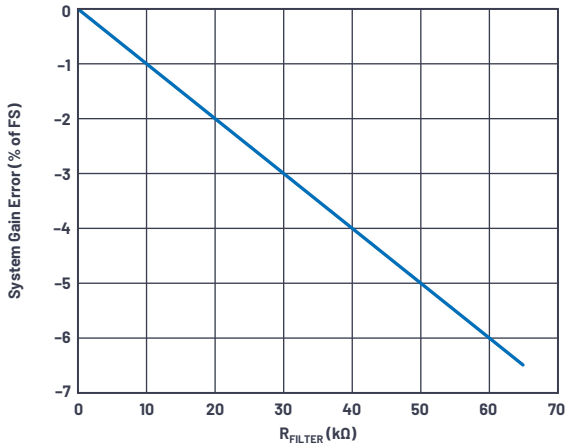

Figure 6. System gain error (% of FS) as a function of the external R_{FILTER} resistor in AD7606 (1 MΩ input impedance).

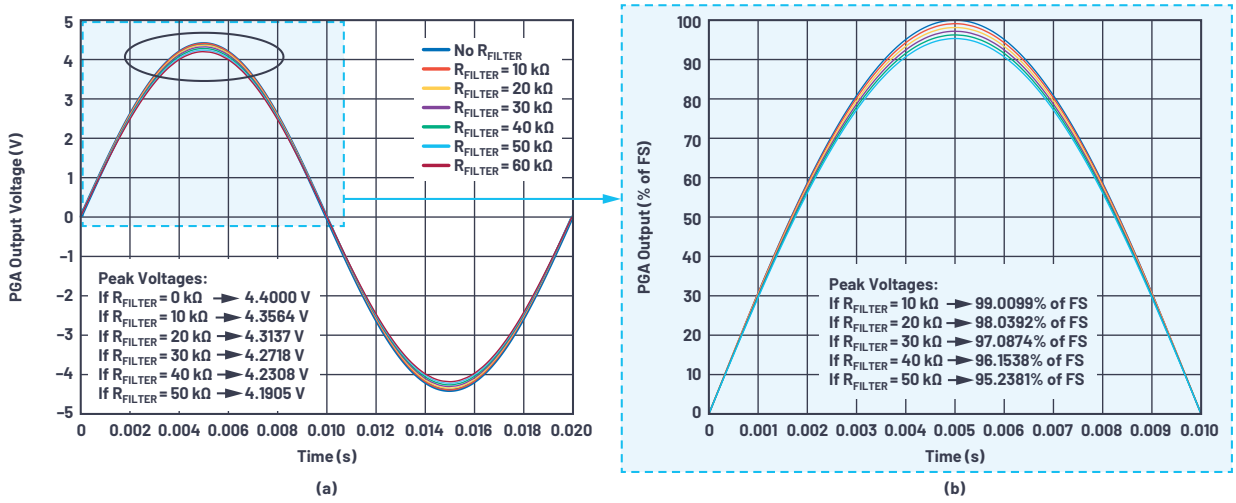

Figure 5. The PGA output's amplitude decreases with the size of the R_{FILTER}. (a) Shows the PGA output voltage in volts and (b) shows the PGA output voltage as a percentage of FS.

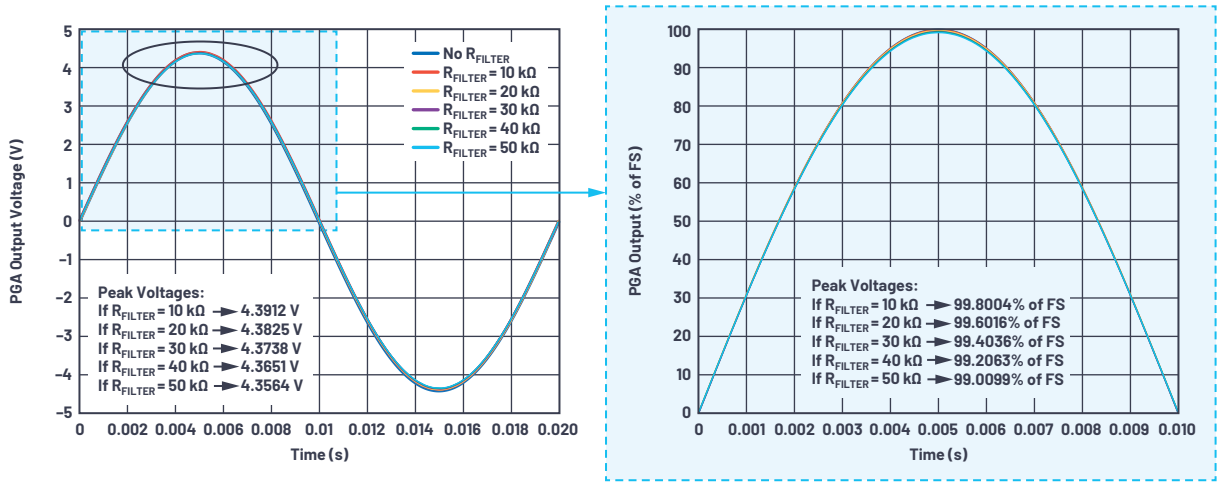

Figure 7. AD7606B's PGA output amplitude is less impacted by the external R_{FILTER}, because of the higher input impedance (5 MΩ).

The AD7606B/AD7606C Generation

Within the AD7606B project development, the three products defined have input impedances and resolutions as shown in Table 1.

Table 1. AD7606B Project Generics, Typical Input Impedances, and Resolution

Generic	Typical Input Impedance	Resolution
AD7606B	5 MΩ	16 bits
AD7606C-16	1.2 MΩ	16 bits
AD7606C-18	1.2 MΩ	18 bits

In either case, whether the R_{IN} is 5 MΩ or 1.2 MΩ, the larger the series resistor (R_{FILTER}), the lower the system gain—that is, the more the gain error increases. However, the larger the R_{IN}, the less impact the R_{FILTER} causes, as shown in Equation 5. Theoretically, for resistors as large as 50 kΩ, the system gain error reduces from almost 5% to 1%.

The comparison between both 5 MΩ and 1 MΩ input impedance devices in Figure 8 shows the impact on system gain error.

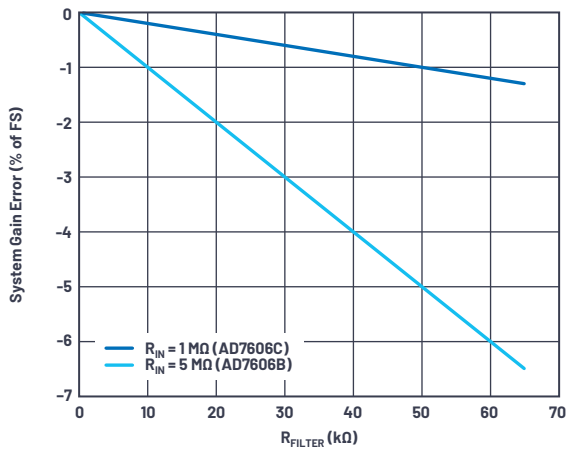

Figure 8. System gain error (% of FS) comparison depending on input impedance (R_{IN}).

In some applications, that gain error can be tolerated. Such low error removes the previous need for system calibration, which was the target when designing the PGA with higher input impedance. However, in some other applications, 1% system gain error may still exceed the requirements dictated by either the industry standard or customer, so calibration may be needed anyway.

Back-End Calibration vs. On-Chip Calibration

Traditional calibration occurs during system factory test. The process is to:

- Connect a zero-scale (ZS) input and measure the offset error.
- Remove the offset.
- Connect a full-scale (FS) input and measure the gain error.
- Remove the gain error.

However, in this case, as the system gain error is well understood through Equation 5, it could be easily removed on the controller side through postprocessing the data—that is, adding a calibration factor (K) that reverts the error introduced in Equation 4 such that the resulting system gain, after calibration, becomes similar to the ideal gain defined in Equation 3.

$$V_{OUT\_CAL} = V_{OUT} \times K = V_{OUT} \times \frac{R_{IN} + R_{FILTER}}{R_{IN}}$$

$$= V_{IN} \times \frac{R_{FB}}{R_{IN} + R_{FILTER}} \times \frac{R_{IN} + R_{FILTER}}{R_{IN}} \quad (6)$$

$$V_{OUT\_CAL} = V_{IN} \times \frac{R_{FB}}{R_{IN}}$$

But this method—let's call it back-end gain calibration—has two major drawbacks:

- It consumes resources on the controller side (microcontroller/DSP/FPGA).
- It assumes R_{IN} as its typical value, while these resistors have a 15% tolerance, so it varies from device to device.

By sweeping the R_{IN} value from its minimum to its maximum, while keeping the calibration factor (K) constant, it can be seen in Equation 6 and Figure 10 how the accuracy of the calibration depends on the internal resistor tolerance, which is unpredictable for the user.

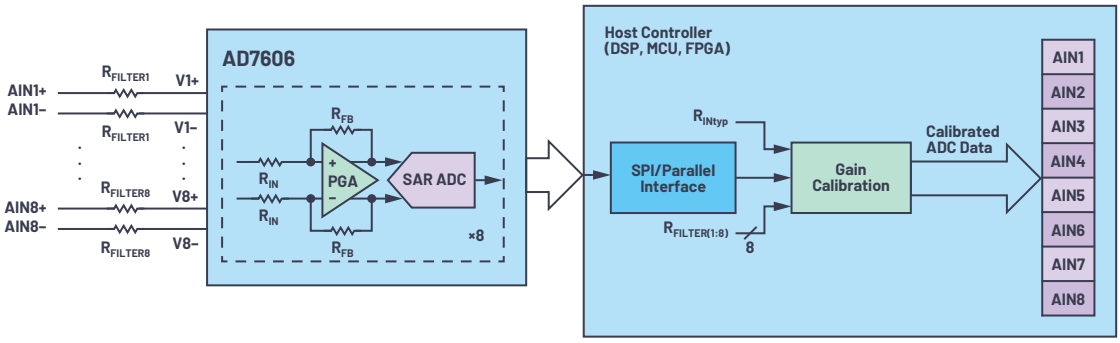

Figure 9. Back-end calibration blocks. Calibration is done on the host controller assuming typical value for R_{IN} and knowing the external resistor value R_{FILTER}.

$$V_{OUT\_CAL} = V_{OUT} \times K = V_{OUT} \times \frac{R_{INtyp} + R_{FILTER}}{R_{INtyp}}$$
$$= V_{IN} \times \frac{R_{FB}}{R_{IN} + R_{FILTER}} \times \frac{R_{INtyp} + R_{FILTER}}{R_{INtyp}} \quad (7)$$

Figure 10 shows the theoretical gain error after back-end calibration as a function of R_{FILTER}, for various input impedance values within the AD7606's 15% tolerance. If the input impedance is the same as the data sheet's typical spec (green line), the back-end calibration removes the gain error introduced by R_{FILTER} perfectly. However, if in the worst case the controller assumes R_{IN} = 1.2 MΩ (typical input impedance listed on the AD7606C-16 data sheet), but that resistor is indeed 1 MΩ (minimum value listed on the data sheet), the back-end calibration loses accuracy, reaching a gain error greater than 0.5% for a given R_{FILTER} = 30 kΩ, which does not meet the industry-standard requirements.

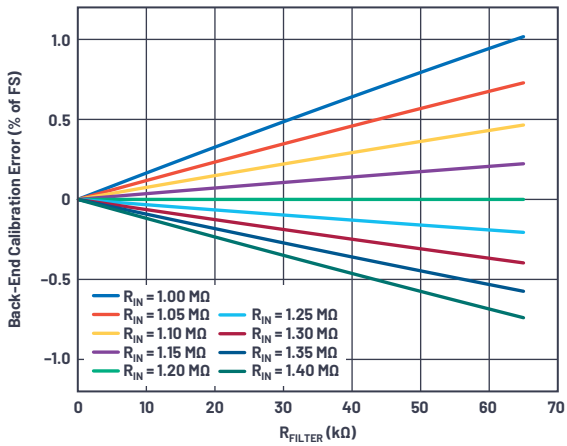

Figure 10. Back-end calibration error depending on the actual R_{IN} value.

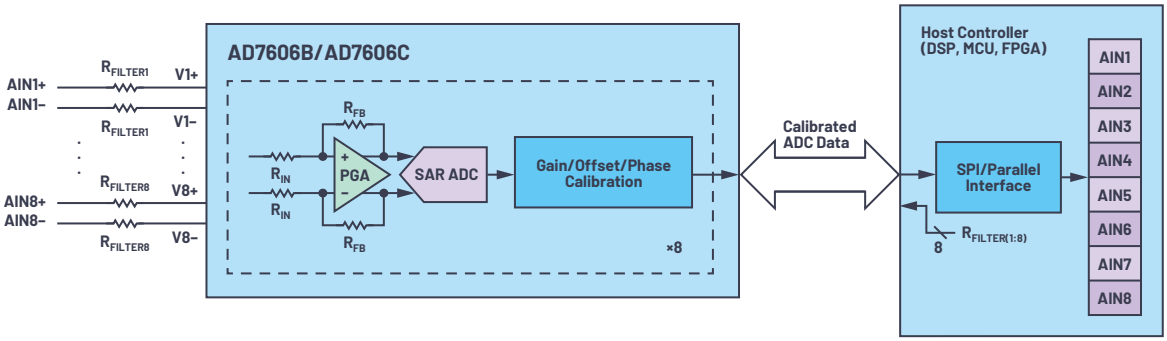

Figure 11. On-chip calibration blocks. Only one channel is shown as an example.

The AD7606B and AD7606C go a step beyond in helping create a high precision data acquisition system by offering an on-chip gain calibration feature.[1] It is very easy to use and enables minimizing the system gain error without having to spend host controller resources, nor having to perform any measurements during factory testing. There is one register per channel, where you can write the value of the R_{FILTER}, and a digital block after the ADC compensates digitally for the error this resistor adds. This user-programmable digital block compensates for gain, offset, and phase error, but only gain error is within the scope of this article. This on-chip gain calibration block knows exactly the input impedance (R_{IN}), so it will always be more accurate than the back-end calibration, independent of the actual R_{IN} and R_{FILTER} values.

This 8-bit register represents the R_{FILTER} integer variable, allowing to compensate for an up to 64 kΩ resistor, with a resolution of 1024 Ω. Because of this discrete resolution, if the R_{FILTER} is not a multiple of 1024, there will be a rounding error. The plot in Figure 12 shows how the postcalibration error stays below ±0.05%, independent of R_{FILTER} and R_{IN}, provided both of them are used in calculating the calibration coefficient (K), given there is no assumption of R_{IN} being equal to its typical specification, but the actual internally measured R_{IN} value is used instead. If compared to Figure 10, for the example of an R_{FILTER} = 30 kΩ, this would mean up to 10× error reduction. Now the error is flat independent of R_{FILTER}, and the larger the R_{FILTER} the greater the error reduction.

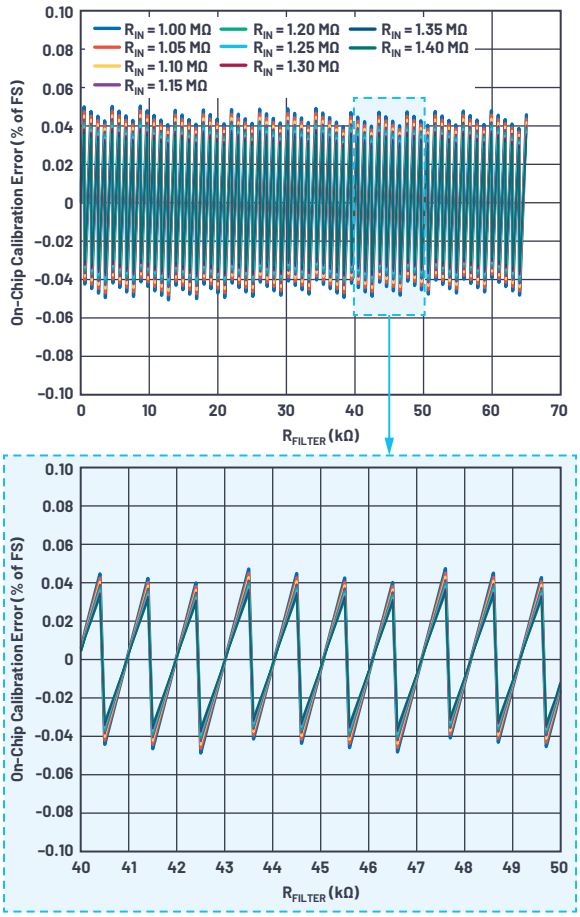

Figure 12. On-chip calibration blocks, per channel.

As the input impedance tolerance impacts the calibration accuracy, the R_{FILTER} tolerance will also impact the calibration accuracy. However, there are three points to note:

- R_{FILTER} is much smaller than R_{IN}, plus discrete resistor tolerance would normally be better than the internal 1 MΩ input impedance tolerance.
- The error introduced by the R_{FILTER} tolerance will be present in both the back end and the on-chip calibration schemes.
- The user can minimize the R_{FILTER} tolerance by using a lower tolerance discrete resistor.

A similar study can be performed, with the on-chip calibration feature enabled, assuming the R_{FILTER} is instead at the worst case of its tolerance, for different common tolerances: 5%, 1%, and 0.1%.

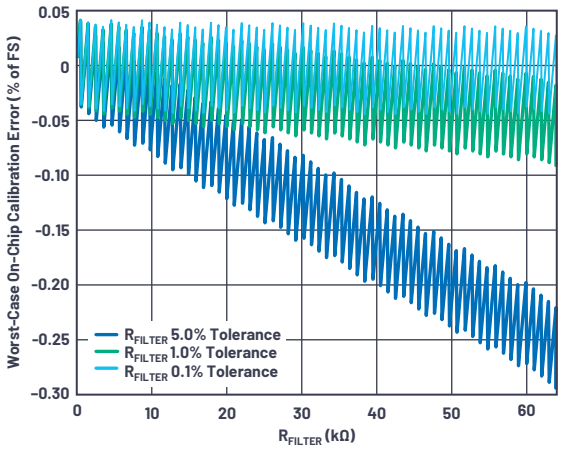

Figure 13. Impact of R_{FILTER} discrete resistor tolerance on the on-chip calibration feature accuracy (worst-case scenario).

Bench Verification

Impact of the Input Impedance

As expected from the previous theoretical analysis, the bench data in Figure 14 and Figure 15 show that the five times higher input impedance (R_{IN}) reduces approximately by five the impact the R_{FILTER} resistor has on the system gain error. For example, a 20 kΩ resistor in front of the AD7606 (R_{IN} = 1 MΩ) would cause around 1% error, whereas this same resistor in front of the AD7606B (R_{IN} = 5 MΩ) would cause around 0.2% error. However, a greater improvement can be achieved by just turning on the on-chip gain calibration feature. There is no need to perform any measurement; just write the R_{FILTER} value, rounded to the nearest multiple of 1024 Ω. By doing so, the error greatly reduces to less than 0.01%, as shown in Figure 14. Note that this error is effectively the total unadjusted error (TUE), and it includes all potential sources of error because:

- The reference and reference buffer are assumed ideal. Any deviations from the 2.5 V reference or 4.4 V reference buffer output are not removed.
- The resistor is assumed ideal at the value written despite its 1% tolerance. Any deviation from the expected resistance value is not removed.
- The offset error is not removed from the measurement—neither the AD7606x offset error nor the mismatch between the front-end resistors.

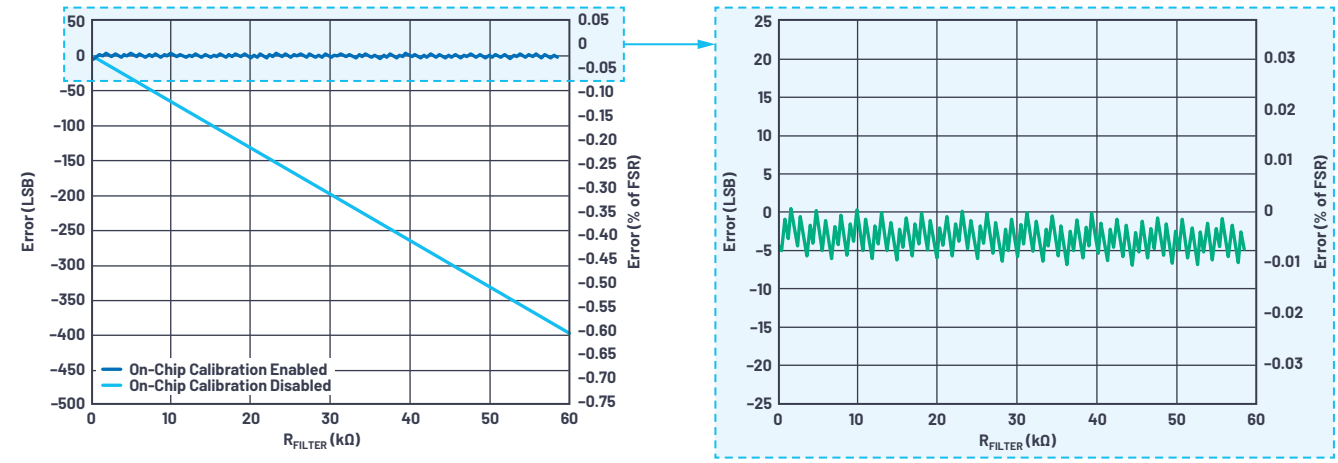

Figure 14. Total error of the AD7606B with the on-chip gain calibration enabled.

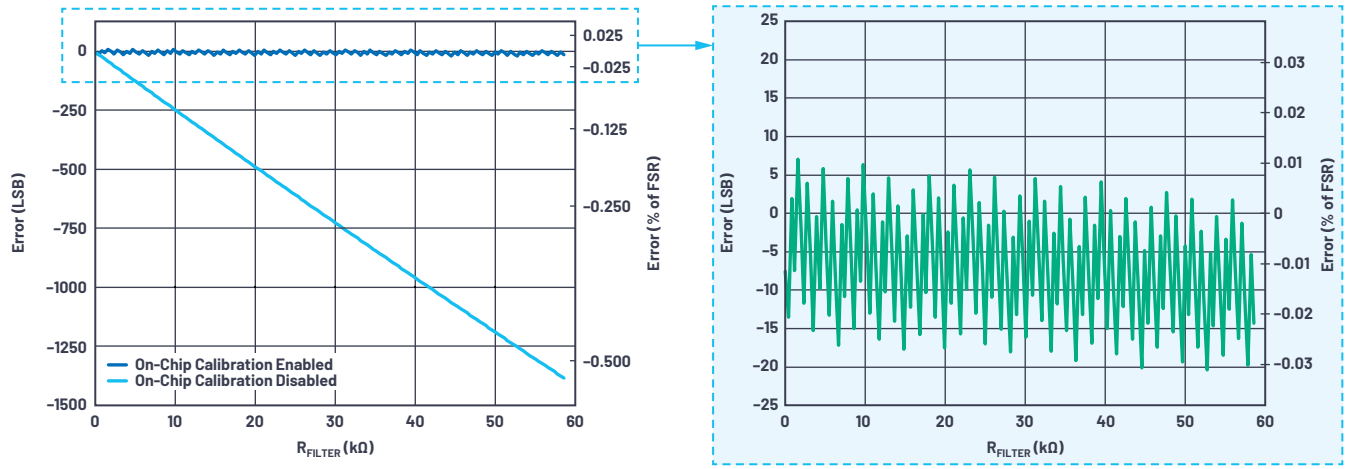

Figure 15. (a) System gain error as a function of R_{FILTER} for the AD7606C-16 with and without enabling the on-chip gain calibration and (b) close-up of the on-chip calibration plot.

Table 2. Total Error (%) for Different Generics, Both Calibrated and Uncalibrated, for a Given R_{FILTER}

R_{FILTER}	AD7606	AD7606B (5 MΩ)		AD7606C (1 MΩ)	
		Uncalibrated	On-chip calibration*	Uncalibrated	On-chip calibration*
10 kΩ	0.5%	0.1%	0.01%	0.45%	0.03%
20 kΩ	1.05%	0.2%	0.01%	0.95%	0.03%
50 kΩ	2.5%	0.5%	0.01%	2.5%	0.03%

*Worst-case error, independent of the R_{FILTER} value

The input impedance on the AD7606C-16 and AD7606C-18, unlike the AD7606B and AD7606, is typically 1.2 MΩ. These generics in the family, thanks to the lower input impedance, enable lower noise and greater SNR performance. On the other hand, they have a similar system gain error when a resistor is placed in front of the analog inputs. By enabling the on-chip gain calibration, the error can again be greatly reduced, down to less than 0.03%.

In summary, both the gain error caused by an external front-end resistor (R_{FILTER}) and the accuracy of the on-chip calibration feature will rely on the input impedance (R_{IN}), which is known in every device internally. For all three generics, the gain error scales linearly with R_{FILTER} if no calibration is performed, but Table 2 shows a comparison for just three given R_{FILTER} values and how it remains flat independent of such resistor value.

This actual data can then be compared to the theoretical data obtained in the AD7606B/AD7606C generation section. As an example, Figure 16 shows in the same graph the total error gathered on an AD7606C-16 as a function of R_{FILTER}, with on-chip calibration enabled, and the worst-case error calculated in the theoretical analysis from Figure 13. Despite that the error figures gathered on the bench are indeed the TUE—given no offset or linearity errors are removed—they're still lower than the theoretical numbers. This indicates firstly that the gain error is the main contributor to the device's TUE, and secondly that the actual resistors used in front of the resistive input ADC are well within the 1% specified tolerance.

In any case, the total DC error is confirmed to be kept less than ±0.1% FS, which is the target in many applications, with no need for calibration, only writing to the ADC the value of the resistor placed in front, independently of its value as long as it is less than 65 kΩ ±1%.

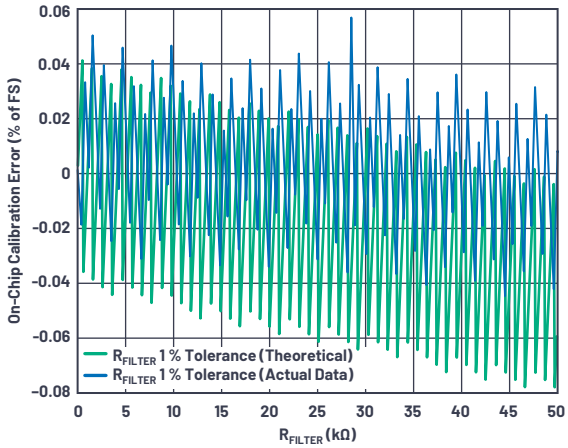

Figure 16. Actual AD7606C-16 results compared to theoretical analysis.

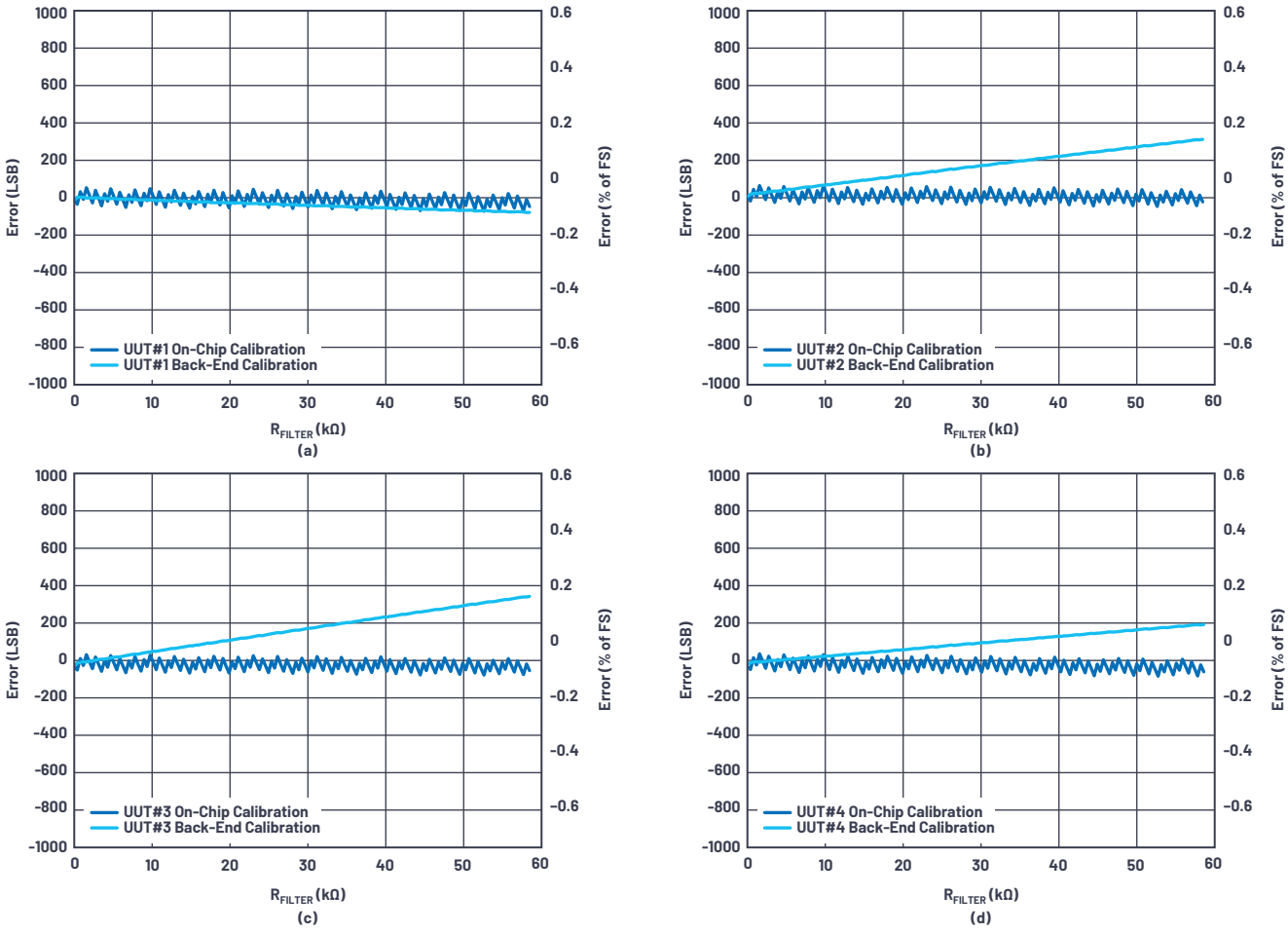

Figure 17. Comparison between on-chip calibration and back-end calibration across four AD7606C-18 units.

On-Chip Calibration vs. Back-End Calibration (Bench Results)

As described in the theoretical study, a simple calibration coefficient could be implemented on the controller side (MCU, FPGA, DSP). However, that presents two major drawbacks: the extra controller resources needed, and the error introduced by the input impedance part-to-part variation. In order to demonstrate the benefits of the on-chip calibration compared to a back-end calibration, a series of AD7606C-18 units were measured—units under test (UUT) numbered 1 to 4 in Figure 17—assuming always the input impedance is the typical value (R_{IN} = 1.2 MΩ).

- UUT #1, shown in Figure 17a, does the calibration quite well, comparable to the on-chip calibration. That means its actual input impedance (R_{IN}) is very close to the typical value.
- UUT #2 to #4 show a certain deviation, which means the actual input impedance (R_{IN}) is slightly higher than the typical value.
- On-chip calibration, displayed in dark blue in all four plots, keeps the total error lower than 0.03% across all units and R_{FILTER} values.

Using a calibration coefficient in the back-end controller does not take into account the actual input impedance of the PGA, which implies postcalibration errors due to part-to-part variation. However, on-chip calibration internally measures this input impedance, therefore achieving greater calibration results, independent of both the R_{FILTER} placed in front and the actual R_{IN} impedance. This lower postcalibration error—added to the benefit of removing the need for postprocessing every single ADC data point in the controller, which consumes resources—leads to a more efficient, easy to use, and accurate system design.

Conclusion

Resistive input simultaneous sampling ADCs are a complete solution, with all signal chain blocks on-chip, offering excellent AC and DC performance and ease of use, allowing for direct sensor interface. As noted in some applications, there is a need for external resistors in front of the analog input. These external resistors add errors to the system accuracy, which leads to longer time to market and extra calibration costs. ADI answers this problem with the AD7606B family of new resistive input ADCs. This solution includes both larger input impedance and on-chip calibration features, reducing the error introduced by external resistors to a minimum.

References

[1] Eamonn J. Byrne. U.S. Patent 10,312,930: ADC Digital Gain Error Compensation. Analog Devices Technology Unlimited Company, June 2019.

About the Author

Lluis Beltran Gil received his B.S. degree in electronics engineering in 2009 and in industrial engineering in 2012, both from the Universitat Politècnica de València, UPV (Technical University of Valencia). After graduation, Lluis joined Analog Devices in 2013 as an applications engineer in the Precision Converter Group in Limerick. Currently, Lluis is working on the SAR ADC Applications Team within the Instrumentation BU, and he is based in Valencia, Spain, where he also received his M.Sc. degree in electronics engineering from Universitat de València, UV (University of Valencia).