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#### APPLICATION NOTE 2694

# Minimizing Short-Circuit Current Amplitude and Pulse Width When Hot-Swap Controller Output is Shorted

Sep 11, 2003

*Abstract: When a hot-swap controller's output is short circuited, the internal circuit-breaker function trips to open the circuit. But initial current flow may be several hundred amps before the internal circuit breaker responds. Typical hot-swap controller circuit-breaker delay time may be 200–400ns, and gate turn-off time may be 10-50microseconds due to limited gate pull-down current. Meanwhile, a high short-circuit current flows.*

*A simple external circuit, described in the application note, can minimize the initial current spike and terminate the short circuit in 200–500ns.*

## Typical Hot-Swap Circuit

Let's look at a typical +12V 6A hot-swap control circuit using the MAX4272 (**Figure 1**). Examining the MAX4272 specifications, we see that it contains slow and fast comparators with trip thresholds of 50mV and 200mV, respectively (43.5–56mV and 180–220mV tolerances over temperature). Applying a 1.5–2.0 multiplier usually placed on operating-current to trip-current ratio, we select  $R_{SENSE} = 5m\Omega$ . Allowing for a 5% tolerance on  $R_{SENSE}$ , the trip current range would be 8.28–11.76A for the slow comparator for overload conditions, and 34–46.2A for the fast comparator when a short occurs.

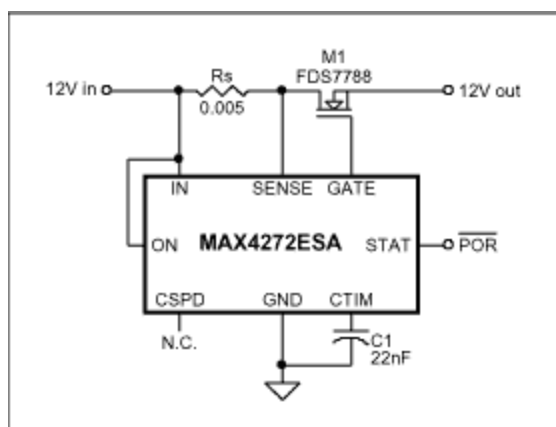


Figure 1. Typical hot-swap controller circuit.

The minimum slow-comparator trip point is 38% above normal operating current, and the fast-trip threshold is suitable for short-circuit trip at 6–8 times operating current.

The 350ns fast comparator delay means that the initial short-circuit current spike is limited only by the circuit resistances during this period. The current trails off slowly thereafter because the 3mA gate pull-down current limits MOSFET M1's 3–4nF gate capacitance discharge rate until complete interruption of the short circuit. Short-circuit current decreases slowly in the 15–40 $\mu$ s while the gate is being pulled from 19V to near ground.

## Peak Short-Circuit Current

Peak current during the initial 350ns period depends upon:

(a) source ESR, (b) short-circuit quality, (c) value of  $R_{SENSE}$ , (d) M1's  $R_{DS(ON)}$ , and (e) M1's  $I_{D(ON)}$ .

Assigning approximate best-case practical values to these, we have a total short-circuit resistance of (Source ESR  $\approx 4m\Omega$ ) + (Short Circuit  $\approx 3m\Omega$ ) + ( $R_{SENSE} = 5m\Omega$ ) + ( $R_{D(ON)} \approx 4m\Omega$ )  $\approx 16m\Omega$ .

This could produce a brief peak  $I_{SC} \approx 750A$ , depending upon the energy storage capacity of the power source (750A would discharge a low ESR backplane with 2200 $\mu$ F capacitor by only 340mV in 1 $\mu$ s). In this case, the actual peak  $I_{SC}$  would probably be limited to  $\approx 400A$  by M1's  $I_{D(ON)}$ .

$I_{D(ON)}$  is dependent upon  $V_{GS}$  so it is instructive to examine the circuit to determine the gate-source voltage during this period. The MAX4272 contains an internal charge pump that sets operating gate voltage at about 7V above  $V_{IN}$ . Thus  $V_{GS} = 7V$  when the MOS is ON.

A secondary effect of the short is that it actually increases  $V_{GS}$ . Consider that the short circuit places a voltage step - equal to a part of the full input voltage - across drain-source of M1. As M1's  $R_{D(ON)}$  is about 1/3 of the total estimated short-circuit resistance,  $\approx 1/3$  of the 12V step is applied as  $V_{DS}$ . This step is partially transferred to the gate by the voltage divider action of  $c_{dg}$  from drain to gate and  $c_{gs}$  from gate to source. Suitable calculations would indicate this additional  $\Delta V_{GS}$  to be 300–500mV, but measurements taken during short-circuit conditions indicate that it may be as high as  $\Delta V_{GS} = +3V$ .

By now it is probably clear that a good quality short circuit will cause several hundred amps to flow for several microseconds to tens of microseconds.

We may wish to limit the peak  $I_{SC}$  to perhaps 50A for  $< 1\mu$ s, but that is impractical without adding a very fast comparator and gate pull-down circuit. We can, however, consider some simple circuit modifications.

1. We can limit the period of the short circuit to  $\leq \frac{1}{2}\mu\text{s}$  by adding a simple external circuit to speed the gate discharge while current is restrained by  $I_{D(ON)}$  to several hundred Amperes for the first 350ns response time of the internal fast comparator, or
2. We can limit the peak  $I_{sc}$  to somewhere in the 100A range for a period  $\leq 200\text{ns}$  with a slightly more complex external circuit.

## Fast Gate Pull-Down Circuit Limits Duration of High Short-Circuit Current

Duration of the high-current short-circuit current can be minimized simply by adding a PNP Darlington transistor Q1 as shown in **Figure 2**. Diode D1 allows the gate to be charged normally at turn-on, but the controller's 3mA gate-discharge current is redirected to the base of Q1 at turn-off. Q1 then acts to quickly discharge the gate in  $\approx 100\text{ns}$ . The high-current portion of the short circuit is thus limited to only a bit more than the 350ns fast-comparator delay time.

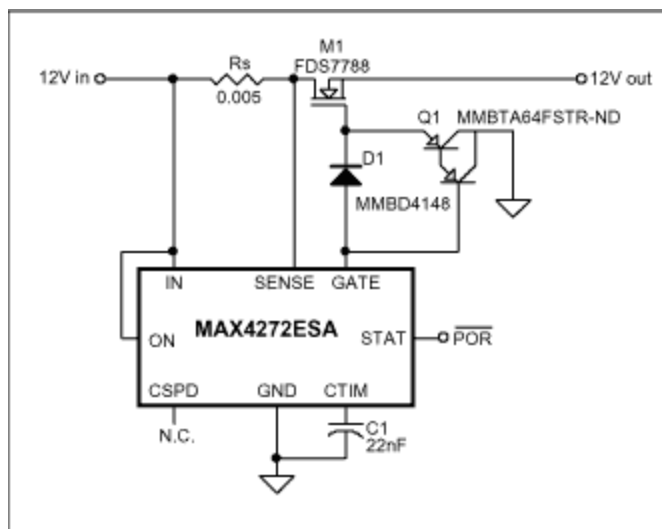


Figure 2. Hot-swap controller with fast gate pull-down.

## Fast Current-Limiting Circuit

The short-circuit current can be limited to  $\approx 100\text{A}$  for  $< 200\text{ns}$  with the circuit shown in **Figure 3**. The PNP transistor Q1a - triggered when the voltage across  $R_{sense}$  reaches  $\approx 600\text{mV}$  - drives NPN transistor Q1b to quickly discharge M1's gate capacitance.

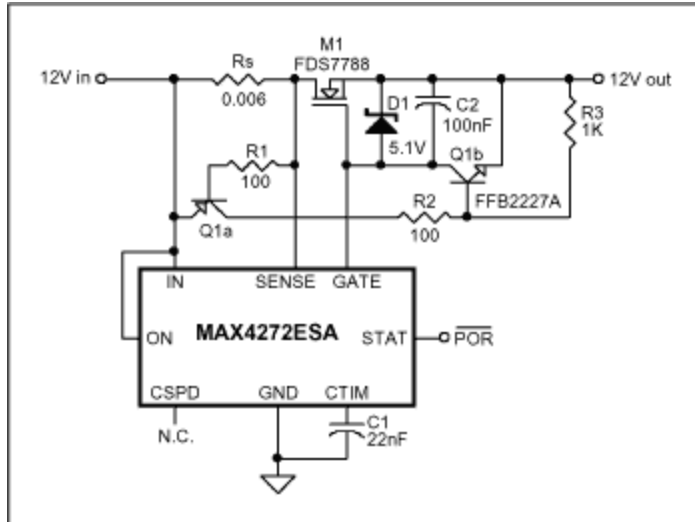


Figure 3. Hot-swap controller with fast short-circuit peak current limiting.

C2 is placed across M1 gate to source to further reduce the positive transient step voltage applied to the gate during a short circuit; its value may be anywhere from 10nF to 100nF.

Zener diode D1 is added to limit  $V_{GS}$  to something less than the 7V available from the MAX4272.

Although the Zener diode is rated 5.1V when biased at 5mA, it will limit  $V_{GS}$  to  $\approx 3.4V$  in this circuit because only 100 $\mu A$  of gate charging (Zener bias) current is available from the MAX4272. The limited  $V_{GS}$  lowers  $I_{D(ON)}$  - at some expense to  $R_{D(ON)}$ , as the data sheet shows 5m $\Omega$  at 3.4V and 3m $\Omega$  at 7V - and allows quicker turn off of M1.

Zener D1 and capacitor C2 could also be employed to some advantage in the circuit of Figures 1 & 2 to reduce  $I_{D(ON)}$  during the short circuit.

## Test Methods - Creating a Short-Circuit

What could be simpler than creating a short-circuit? There is at least one in every British roadster.

But a short-circuit of sufficient quality and repeatability for testing turns out to be a bit more challenging. Several methods of creating a short circuit were evaluated for this experiment.

- *Mechanical switches* invariably produce bouncing contact closures over a several-millisecond period. A rotary multi-leaf switch would seem to hold some promise, but one wonders about repeatability as the contacts erode, due to arcing from several high-current closures.
- *High-current relay contacts* also produce bouncing contact closure and exhibit variable contact resistance during closure.
- *Silicon controlled rectifiers* evaluated had a less-than-satisfactory current rate of rise.
- *High-current mercury-displacement relays* were expected to be the best method, but the results were not satisfactory. A 60A 600V mercury relay with specified 4m $\Omega$  resistance was found to have an initial resistance of 40m $\Omega$  at contact initiation, with leisurely relaxation to 4m $\Omega$  over a 15 $\mu s$  period as the current pulse progressed.
- *Manual manipulation of a shorting link* delivers a haphazard, intermittent, and non-repeatable contact - perhaps closest to the British roadster ideal! However, a very steep current wavefront can be achieved. In the end, this was the most effective (and economical) method, although contact erosion limited the number of closures with repeatable results.

The most promising lab-quality method is to use multiple parallel-wired low- $R_{D(ON)}$  NMOS transistors driven from multiple high-output CMOS Schmidt line drivers. This route was not pursued because of limited time and resources.

A true low-resistance short circuit with a steep current wavefront is inordinately difficult to produce consistently in the laboratory by mechanical means. And this will almost certainly be true of the inadvertent short circuit to be experienced in an operating circuit.

A typical manually-created short circuit will create capacitor-discharge current and voltage waveforms like those shown in **Figure 4**. The upper curve recording short-circuit output voltage at 5V/div. shows the capacitor to be less than half discharged over most of the time scale (25 $\mu$ s/div.). The lower curve recording short circuit current at 25A/div. clearly shows the intermittent nature of the contact.

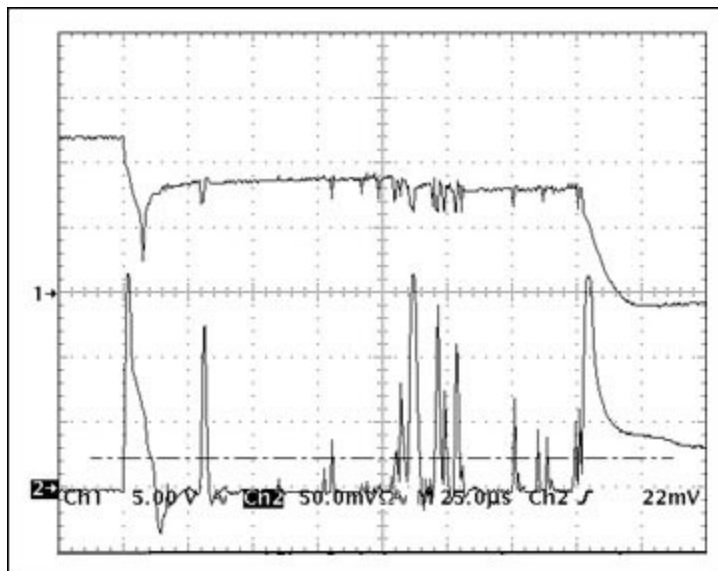


Figure 4. Ragged mechanical short-circuit waveforms.

Nor is it easy to create a power source with an ESR below 5m $\Omega$ . Nevertheless, significant effort was expended to create a low-ESR voltage source of 4–5m $\Omega$  where careful measurement showed a voltage drop of 440mV during a 100A short circuit. This voltage source utilized a 5500 $\mu$ F computer-grade electrolytic, a 3.3 $\mu$ F multi-layer ceramic, and six 100 $\mu$ F specialty polymer aluminum electrolytic capacitors in parallel mounted directly at the circuit input driven from a 10A power supply.

## Short-Circuit Current Waveforms

The unaltered circuit of Figure 1 exhibited a short-circuit current waveform as shown in **Figure 5**. The waveform appears inverted because the measurement was made of voltage across current-sense resistor  $R_S$  with the oscilloscope ground at the +12V input terminal of the test circuit.  $R_S$  was 6m $\Omega$ , and the voltage scale is 1V/div. showing a peak voltage of 2400mV or 400A. The current wavefront is not as steep as it could have been with a better contact.

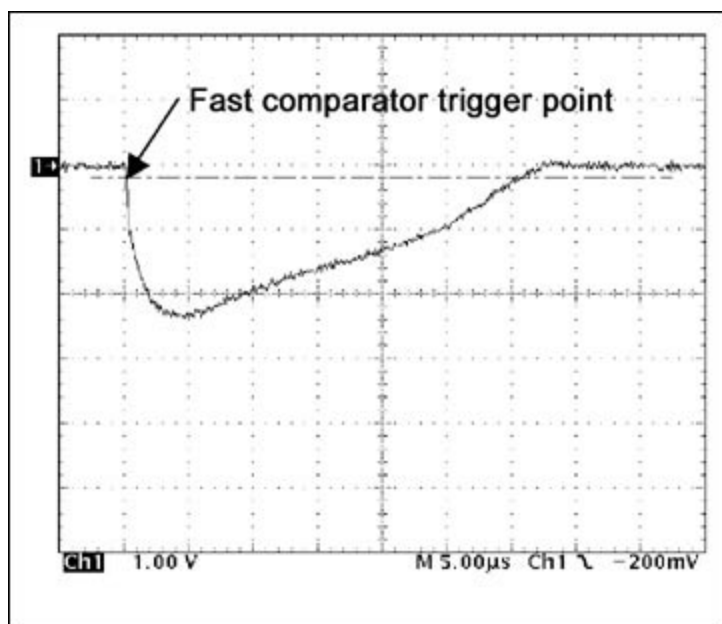


Figure 5. 400A Peak short-circuit current waveform in unaltered circuit.

It is instructive to view also the voltage waveforms of **Figure 6**, where output voltage at the short and M1 gate voltage waveforms are combined with the voltage across  $R_S$ . All voltages are referenced to the +12V input.

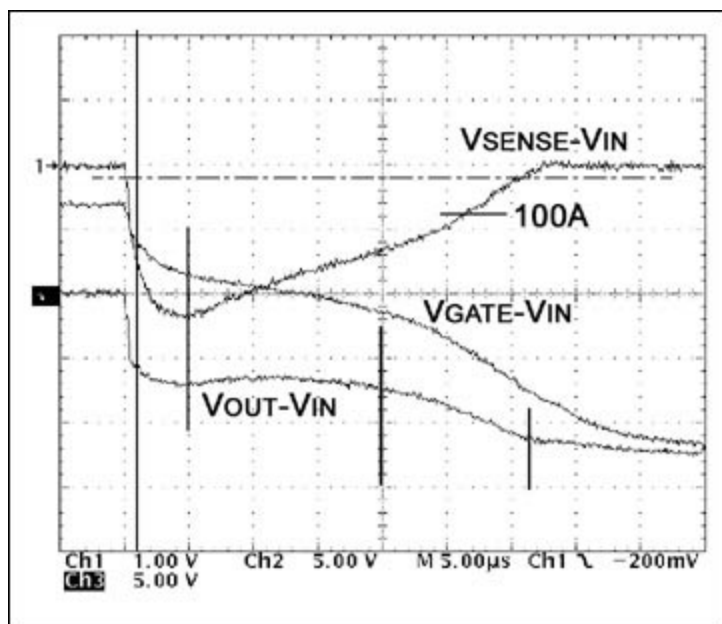


Figure 6. Short-circuit voltage and current waveforms in unaltered circuit.

The  $V_{OUT}-V_{IN}$  waveform shows that  $V_{OUT}$  drops by 7V during the short to indicate that the short-circuit resistance was only slightly less than the  $\frac{1}{2}$  the total circuit resistance. A lower-resistance short might have produced a higher than 400A peak current. The same waveform indicates that the short was not fully effective during the first 300ns; this contributes to the slowly-falling  $V_{SENSE}$  waveform.

The  $V_{GATE}$  waveform shows an initial  $V_{GS} = 7V$  with an increase to nearly  $10V$  at  $1\mu s$  due to the falling  $V_{OUT}$ .  $V_{GS}$  has only decreased to  $9V$  at  $5\mu s$ , to  $6V$  at  $20\mu s$ , and to  $4V$  at  $33\mu s$ . The slow discharge of the gate is due to only  $3mA$  being available as discharge current. As a result, the short-circuit current is still  $100A$  at  $27\mu s$  after initiation of the short.

The fast gate pull-down circuit of Figure 2 may not decrease the initial short circuit current, but the PNP Darlington pull-down will quickly terminate the current waveform. The short-circuit current waveform for this configuration shown in **Figure 7** still exhibits a  $2400mV$  or  $400A$  peak current, but the current is terminated within  $50ns$  after the fast comparator triggers at  $\approx 370ns$ . Note also, that the short-circuit current waveform is very steep, indicating an excellent mechanical short circuit initiation.

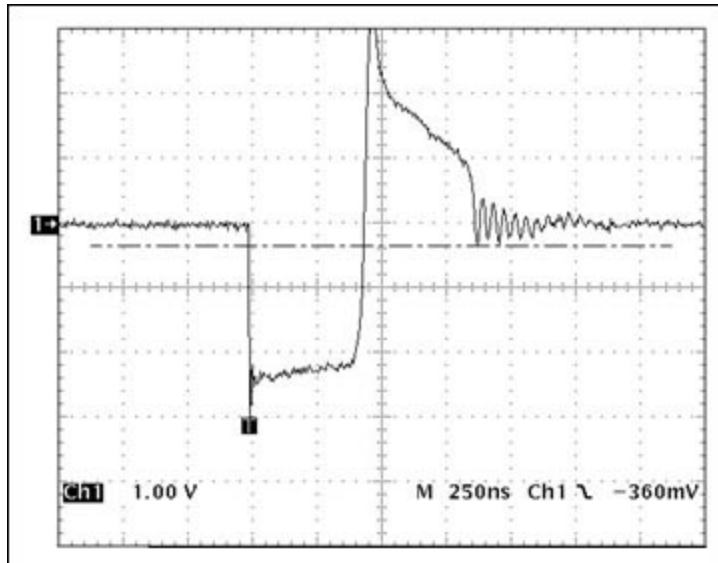


Figure 7. Short-circuit current waveform in fast-pull-down circuit.

The source current reverses as circuit capacitances recharge the input capacitance to cause a slight positive overshoot at the  $+12V$  input.

The fast short-circuit peak current limiting circuit of Figure 3 is effective in limiting both peak current and current duration due to the short circuit. The recorded voltage across  $R_S$  shown in **Figure 8** peaks at about  $600mV$  or  $100A$  in  $6m\Omega$ . Short-circuit current termination is extremely rapid, with the current pulse being completely terminated in  $< 200ns$ .

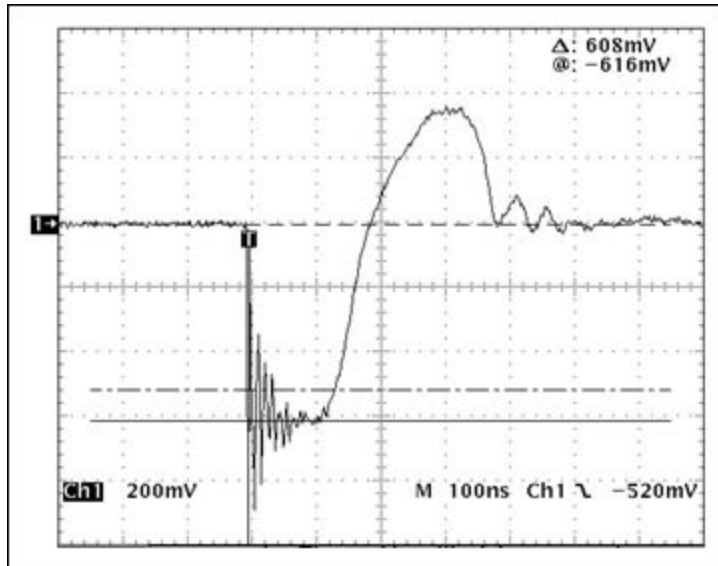


Figure 8. Short-circuit current pulse in modified hot-swap controller circuit.

The backplane power source disturbance is minimized by this technique as shown in **Figure 9** where peak voltage disturbance is  $< \pm 500\text{mV}$  on the +12V source described in the Test Methods section.

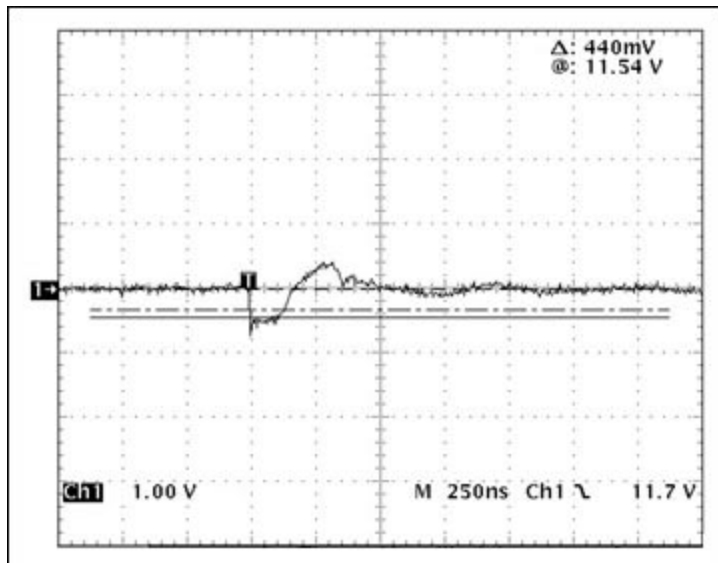


Figure 9. Backplane disturbance due to short circuit in circuit of Figure 3.

Note that the steep current wavefront again indicates a very high quality short-circuit initiation. Unfortunately, it is not easy to duplicate this steep short-circuit waveform.

## Then what happens?

The PNP-NPN detection/pulldown circuit interrupts the short-circuit current so quickly (and then disengages) that the MAX4272 fast comparator has insufficient time to trigger (response time = 350ns). **Figure 10** shows the  $V_{GS}$  waveform over a 500 $\mu\text{s}$  period (450 $\mu\text{s}$  after short-circuit initiation). The gate, having been discharged, begins to rise due to the 100 $\mu\text{A}$  gate charging current that is still active. After about 130 $\mu\text{s}$ , the gate is sufficiently enhanced (3V) that  $V_{OUT}$  rises to about 1V, and short circuit current



again begins to flow. The recharge is slow enough that the fast comparator triggers at 33A (200mV/6mΩ), and the IC performs its duty by shutting down and latching OFF.

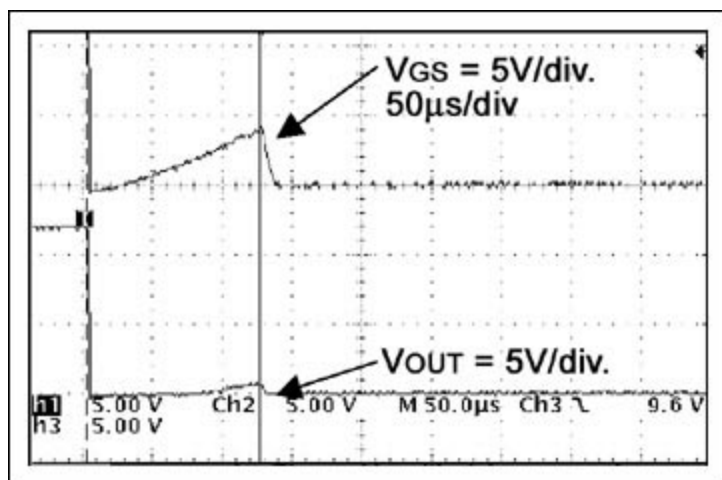


Figure 10. Compressed-time view of  $V_{GS}$  under short-circuit condition.

## Summary

Either of the two circuits discussed will protect a backplane power source by minimizing the energy dissipated when a hot-swap controlled circuit experiences a short. The simpler circuit of Figure 2 dramatically shortens the period when short-circuit current flows to somewhat less than 500ns, while the slightly more complex circuit of Figure 3 will reduce peak short circuit current to 100A as well as truncating the pulse width to less than 200ns.

Either technique can be applied to most hot-swap controller circuits.

Individual test results will vary depending upon the impedance of the power source, the impedance of the short circuit, and especially with the quality and attack time of the short circuit itself.

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