Multi-Output Clock Synthesizer with Integrated VCO Features the Low Jitter Required to Drive Modern High Speed ADC and DAC Clock Inputs

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The latest high performance ADCs cannot realize their potential without an ultralow jitter high speed clock signal. The LTC6951 satisfies the requirements of top ADCs by producing a clock signal up to 2.7GHz with an impressively low wideband noise floor. Figure 1 compares the LTC6951's measured ADC SNR results to other ADC clock sources.

The quantity and performance requirements for low jitter clocks in electronic systems continues to increase with system complexity and performance. This may result in a costly array of parts, including VCOs, PLLs, clock distribution devices and synchronization components to support the clock signals. The LTC®6951, on the other hand, *decreases* complexity and cost by integrating a high performance PLL/VCO, and distributing five ultralow jitter clock outputs. Additionally, the LTC6951 supports several software-based synchronization methods: EZSync™, ParallelSync™ and EZ204Sync™ (aka EZParallelSync™).

The latest trend in high speed converter digital interfaces is the adoption of the JESD204B standard. Previous generation clocking devices are often incompatible with the JESD204B standard due to different synchronization and output divider requirements. The LTC6951 accounts for these differences, making it capable of supporting JESD204B subclass 1. The LTC6951 introduces Linear's unique reference alignment synchronization method known as ParallelSync, which allows parallel LTC6951s to clock multiple JESD204B devices.

THE INNER WORKINGS OF THE LTC6951

Referring to Figure 2, the LTC6951 features two different configurations based on the setting of the RAO (Reference Aligned Output) register bit. The desired synchronization method determines which configuration is selected. The LTC6951 is divided into three main circuit blocks: the phase-locked loop (PLL) and voltage controlled oscillator (VCO) section, the clock distribution section and the digital control section.

The PLL section works in conjunction with the external reference and the internal 4GHz to 5.4GHz VCO to generate the desired VCO frequency (f_{VCO}) as follows:

for RAO = 0:

$$f_{VCO} = \frac{f_{REF} \bullet N}{R} \quad (1)$$

for RAO = 1:

$$f_{VCO} = \frac{f_{REF} \bullet N \bullet P \bullet M0}{R} \quad (2)$$

Figure 1. LTC6951 performance advantage

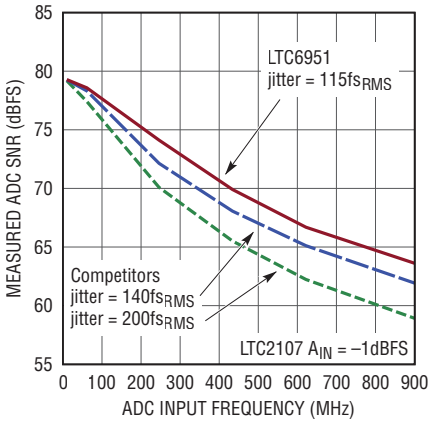
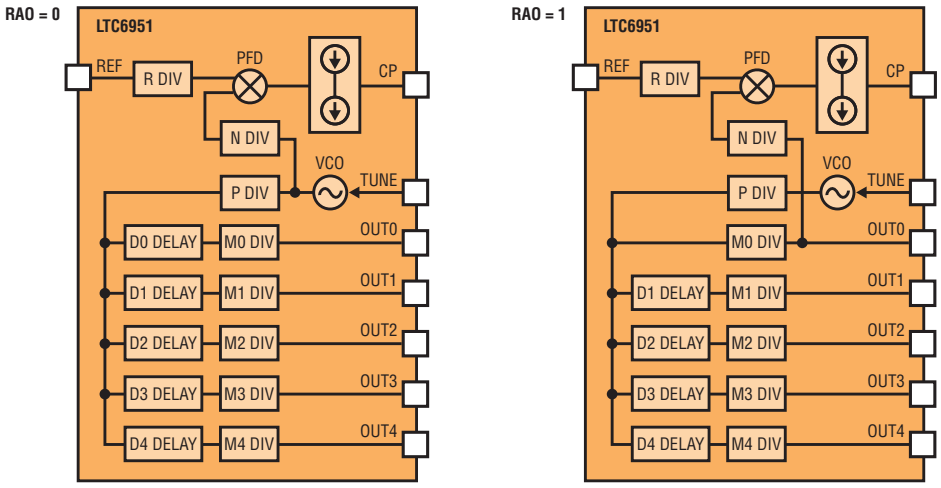


Figure 2. LTC6951 block diagram



The LTC6951 produces clock frequencies up to 2.7GHz with the lowest wideband noise floor in the industry for a clock distribution device. This allows the LTC6951 to directly clock high speed ADCs with very challenging SNR and clock-to-clock skew targets.

where f_{ref} is the reference input frequency, R is the reference input divide value, N is the PLL feedback divide value, P is the prescalar divide value, and MO is the output divider value. When RAO = 0, N is the VCO feedback divide value. When RAO = 1, the LTC6951 is in reference aligned output mode and N • P • MO is the VCO feedback divide value. Reference aligned output mode allows the user to align the outputs of one or multiple LTC6951s to the reference input.

The clock distribution section receives a signal at f_{VCO}/P, where P is the P-divider value. After the P-divider, the clock signal is distributed to five separate channels. When RAO = 0, each of the five channels can independently delay the first synchronized clock edge by any integer from 0 to 255 P-divider clock cycles. When RAO = 1, OUT0's delay option is disabled. After the delay function, each channel can independently divide the frequency from a list of divider values that range from 1 to 512. The output signal from the dividers is sent to a buffer that determines the output signal type. Four channels produce an ultralow noise differential CML clock signal capable of output frequencies up to 2.7GHz. The fifth channel creates a differential LVDS output that can produce clock frequencies up to 800MHz.

The third and final section is the digital control section, which controls the various synchronization functions and is discussed in detail in the "Synchronization Methods" section of this article. The digital control section includes a standard 4-wire serial interface and a pin to monitor the status of certain register bits.

Summary of Linear's clock generation and distribution devices

	LTC6950	LTC6951	LTC6954	LTC6957
Internal PLL	✓	✓		
Internal VCO		✓		
Output fMAX (MHz)	1400	2700	1800	300
Outputs	5	5	3	2
Max output divide ratio	63	2048	63	1
EZSync	✓	✓	✓	
ParallelSync		✓		
JESD204B Subclass 1 compatible		✓		
PC-based design, simulation and demo board control	ClockWizard™	LTC6951Wizard	LTC6954_GUI	

PERFORMANCE

There is a trade-off between using filtered ADC clocks for optimal SNR performance or unfiltered ADC clocks for optimal clock-to-clock skew performance. There are several applications with challenging clock jitter and clock-to-clock skew requirements. Examples include JESD204B converters, and multi-arrayed systems such as medical scanners and smart array antennas. Filtering multiple clocks for performance while accounting for variations in filter delays to meet skew requirements can be problematic. The LTC6951 addresses these design challenges by providing multiple CML clock outputs with 115fs_{RMS} jitter and ±20ps clock skew. For larger arrayed clock systems requiring multiple LTC6951s, ±100ps clock skew can be achieved.

To determine the jitter requirement for an ideal ADC clock input, refer to Equations 3 and 4. Equation 3 calculates the total clock jitter required to achieve a desired SNR level at a known full scale analog input frequency. Equation 4 determines the ADC clock input jitter requirement after removing the ADC aperture jitter from the total clock jitter. The ADC aperture jitter number is usually provided in the ADC data sheet. Equation 3 and Figure 1 highlight that as an ADC's analog input frequency increases, lower jitter clocks are required to achieve optimal SNR performance. For a more in-depth discussion of clock jitter requirements for ADCs refer to the LTC6951 data sheet.

$$t_{J(TOTAL)} = \frac{10^{\frac{-SNR_{dB}}{20}}}{2 \bullet \pi \bullet f_{IN}} \quad (3)$$

$$t_{J(CLK\_IN)} = \sqrt{t_{J(TOTAL)}^2 - t_{J(APERATURE)}^2} \quad (4)$$

f_{IN} = ADC analog input frequency

Table 1. Synchronization selection table

	EZSync Standalone	EZSync Multichip	ParallelSync	EZ204Sync (EZParallelSync)
Architecture	Standalone	Clock Distribution	Reference Distribution	Reference Divide and Distribution
Jitter	Ultralow	Low	Ultralow	Ultralow
Timing requirements	Easy	Easy	Moderate	Easy
Phase alignment (all outputs)	Yes, at Time 0*	Yes, at Time 0*	Yes, at Time 0*	Yes, phases aligned per LTC6951 sync

*Time 0 alignment implies all outputs requiring synchronization are phase aligned on the same sync event.

Figure 3. EZSync Standalone

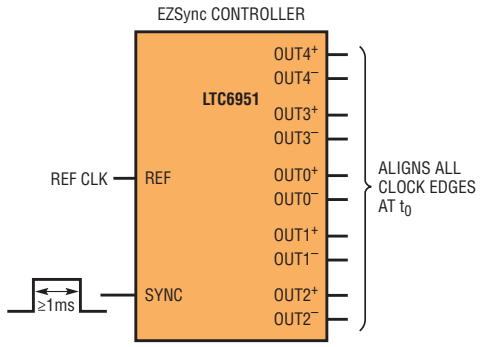
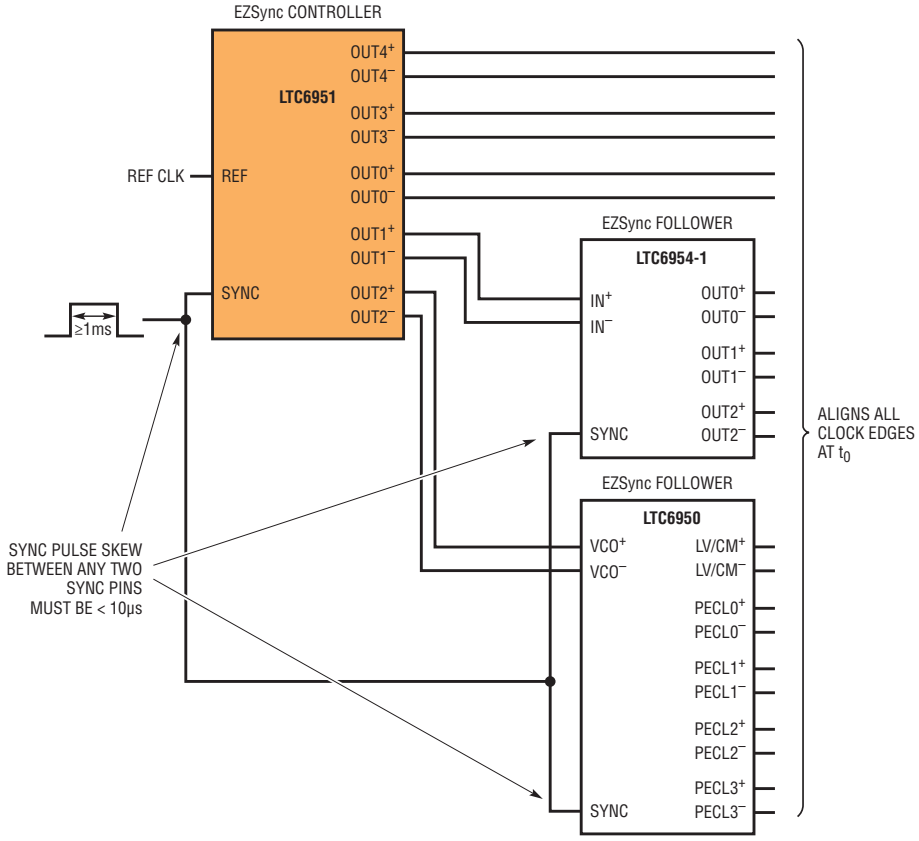


Figure 4. EZSync Multichip



SYNCHRONIZATION METHODS

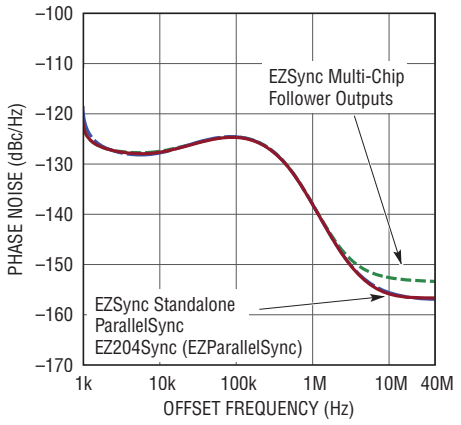
The LTC6951 provides three synchronization methods: EZSync, ParallelSync and EZ204Sync (or EZParallelSync). The advantages and disadvantages of each method are summarized in Table 1 and in the descriptions below.

EZSync Standalone (Figure 3) synchronizes the LTC6951's five outputs after toggling the LTC6951's sync pin or the SPI register SSYNC bit. This method showcases the best jitter, clock skew performance and easiest synchronization method.

EZSync Multichip (Figure 4) increases the number of synchronized clock outputs by using the LTC6951 as an EZSync CONTROLLER. This method maintains the simple EZSync synchronization timing requirements. However, for FOLLOWER devices (Figure 4), such as the LTC6950 and LTC6954, the clock jitter performance becomes additive in nature, as shown in Equation 5 and Figure 5. Clock skew performance depends on several factors, including board trace length differences between EZSync devices, FOLLOWER propagation delays, and individual EZSync device skew performance. The EZSync clock skew performance can be optimized using the LTC6951 output delay SPI bits.

$$t_{J(EZSyncTOTAL)} = \sqrt{t_{J(EZSyncCNTRLLR)}^2 + t_{J(EZSyncFLLWR)}^2} \quad (5)$$

Figure 5. Phase comparison



ParallelSync synchronization (Figure 6) increases the number of synchronized clock outputs by distributing the reference to multiple LTC6951s. This method maintains the LTC6951 jitter performance provided by the EZSync Standalone method, since the out of band reference input noise is removed by the LTC6951 loop filter, as shown in Figure 5. The synchronization timing requirements are a function of the reference frequency (refer to Figure 6 for SYNC to REF timing diagram). The clock skew performance depends on board trace length differences between the reference distribution circuit and the LTC6951, reference clock skew and individual LTC6951 output skews. The clock skew performance can be optimized using the LTC6951 output delay SPI bits.

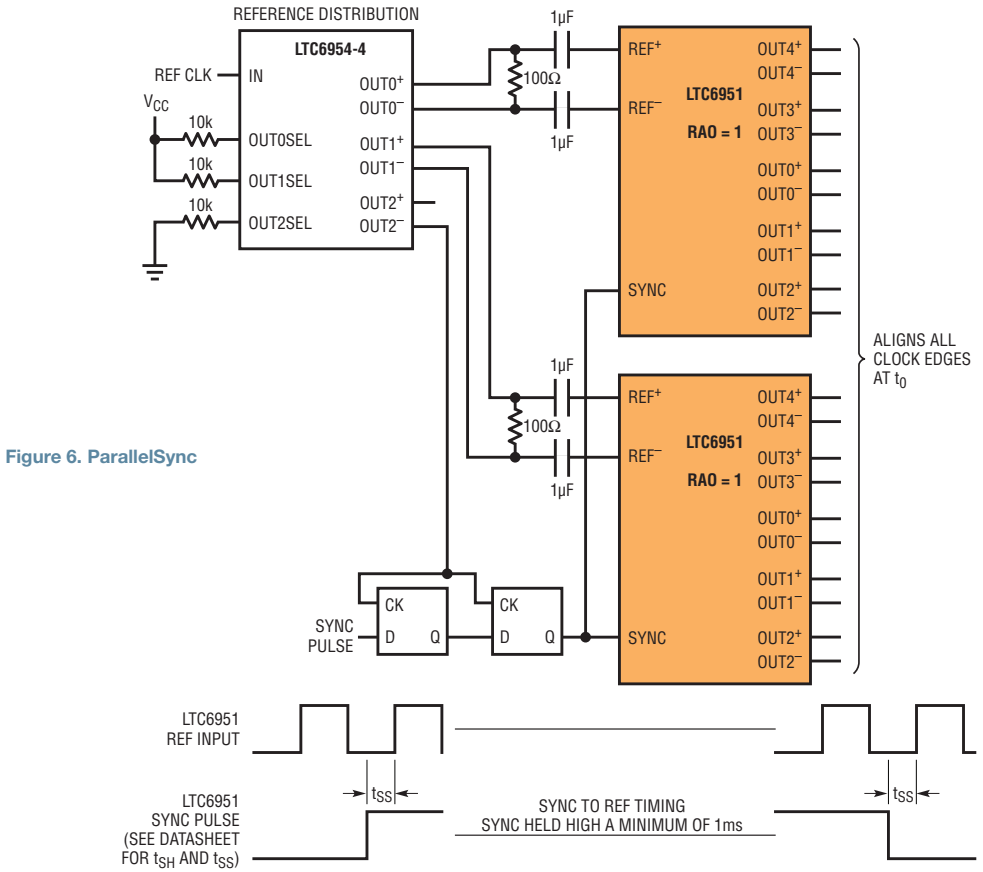


Figure 6. ParallelSync

ParallelSync synchronization uses the LTC6951's Reference Aligned Output mode (RAO = 1 in Figure 2), which provides a known latency between the falling edge of the sync input signal and the starting edge of all LTC6951 outputs. Figure 8's ParallelSync timing diagram explains how outputs from one or multiple LTC6951's can be programmed to begin at a desired point in time.

EZ204Sync (or EZParallelSync) (Figure 7) is a simple multichip synchronization method targeted at, but not limited to, JESD204B applications requiring CLOCK and SYSREF signals. EZ204Sync maintains the jitter performance of ParallelSync, but with easier implementation. This is accomplished by using an EZSync distribution device to act as an external R-divider to the PLL/VCO reference inputs, as shown in Figure 7.

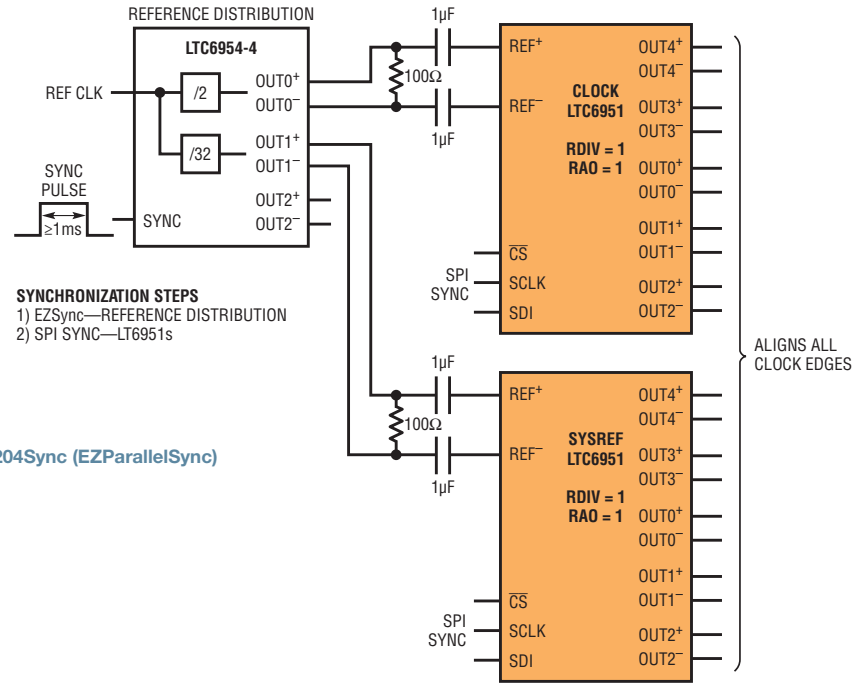
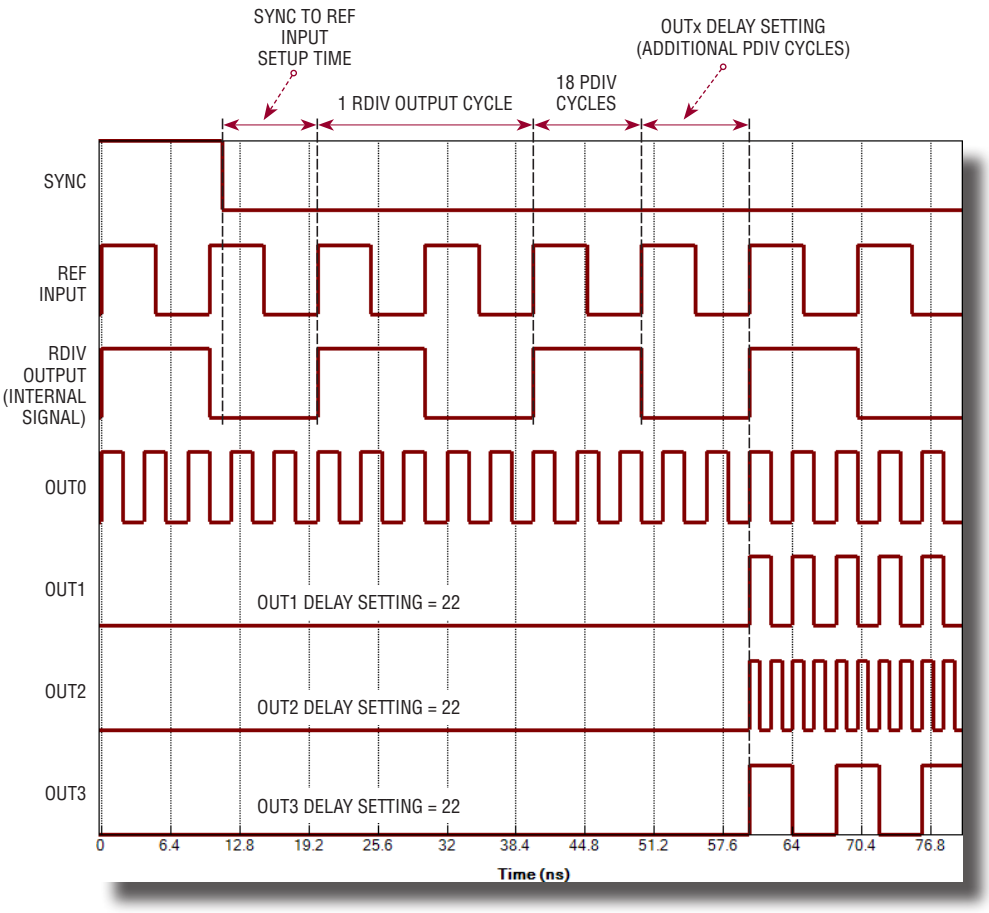


Figure 7. EZ204Sync (EZParallelSync)

The outputs of all PLL/VCOs are phase aligned. However, this architecture allows the phase alignment of the multiple PLL/VCO devices to take place on any R-divider cycle. As a result, phase alignment of each LTC6951 is performed independently, enabling the user to power on and off individual LTC6951s without requiring resynchronization of all LTC6951s. This ability to synchronize individual LTC6951s independently is ideal for JESD204B subclass 1 applications.

The LTC6951's variety of synchronization methods allows designers to optimize for ease of synchronization, clock jitter and the number of clocks required.

Figure 8. ParallelSync timing diagram



NOTES:
1. SYNC RISING EDGE (NOT SHOWN) ALIGNS RDIV OUPUT TO REF INPUT
2. RDIV = 2
3. PDIV CYCLE = 500ps (NOT SHOWN)

JESD204B INTERFACE

JESD204 is a serial data converter digital interface that has undergone two major revisions since its original 2006 specification. The original goal of JESD204 was to simplify and lower the cost of the digital interface by reducing the number of converter output pins, FGPA pins and the board area consumed by routing multiple ADCs to an FPGA. The latest revision, JESD204B, added the ability to establish deterministic latency between a logic device and the data converters. Over the past few years, a large percentage of the new converter ICs and FPGAs have adopted the JESD204B interface.

To enable deterministic latency, JESD204B added two new subclasses, subclass 1 and subclass 2. Subclass 1 is the preferred method when converter clocks are faster than 500Msps.

JESD204B subclass 1 added the alignment signal SYSREF. From the clock IC's perspective, SYSREF is phase aligned to the clock signal, and can range from a single pulse to several pulses at an integer multiple of the converter clock period. As a result, many existing clock devices did not have the divider range to support the JESD204B clock and SYSREF signals.

Over the past few years a large percentage of the new converter ICs and FPGA have adopted the JESD204B interface. The LTC6951 is JESD204B subclass 1 capable, due to the LTC6951 output divider ranging from 1 to 512.

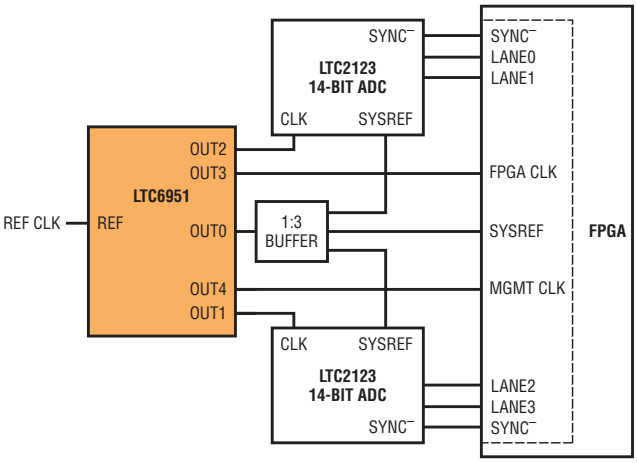


Figure 9. LTC6951 EZSync: JESD204B subclass 1 example

The LTC6951 is JESD204B subclass 1 capable, due to the LTC6951 output divider range extending from 1 to 512. In addition to Figure 7's EZ204Sync example, Figure 9 provides an EZSync Standalone example of a LTC6951 clocking two JESD204B converters. Figure 10 shows a ParallelSync example of multiple LTC6951s clocking several JESD converters.

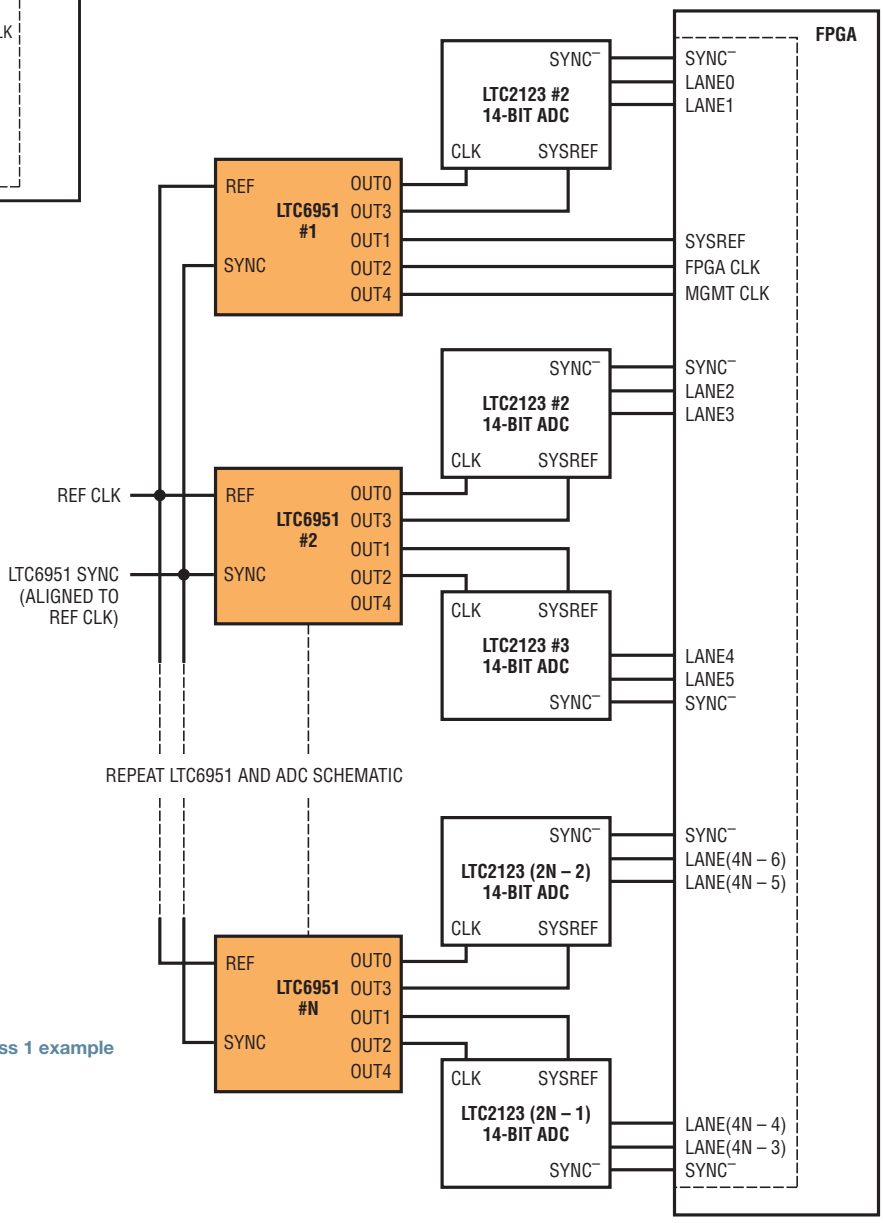


Figure 10. LTC6951 ParallelSync: JESD204B subclass 1 example

For initial evaluation, the LTC6951Wizard provides register settings files that are based off the LTC6951 data sheet examples and typical application circuits.

TOOLS

The LTC6951 demo board (www.linear.com/ product/LTC6951#demoboards) and the LTC6951Wizard™ greatly simplify evaluation and design. These tools can:

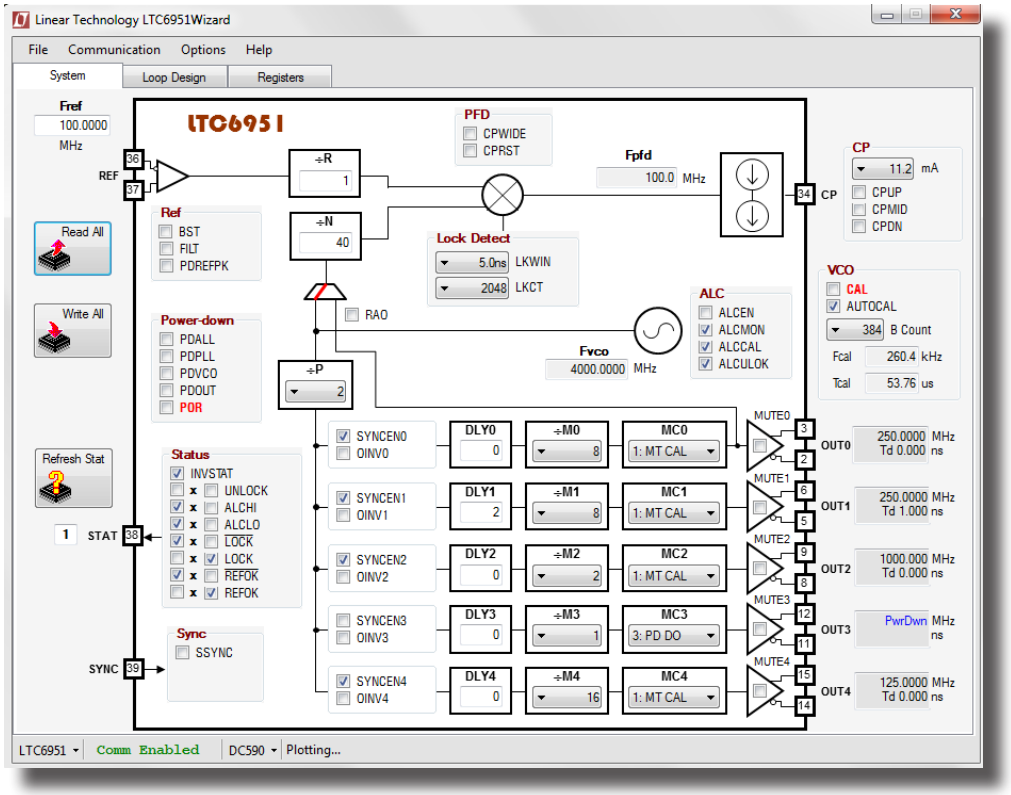
- Read/write to the LTC6951 SPI registers (Figure 11)
- Calculate registers settings and design loop filters based on a frequency plan (Figure 12)
- Simulate time and frequency domain response based on register settings and loop filter design (Figure 12)

For initial evaluation, the LTC6951Wizard provides register settings files that are based on the LTC6951 data sheet examples and typical application circuits. To evaluate a custom frequency plan, the LTC6951Wizard provides a Help file with step-by-step examples using the LTC6951Wizard to calculate register settings, design the loop filter and program the LTC6951 SPI registers. Download the LTC6951Wizard at www.linear.com/LTC6951Wizard.

CONCLUSION

The LTC6951 produces clock frequencies up to 2.7GHz with the lowest wideband noise floor in the industry for a clock distribution device. This allows the LTC6951 to directly clock high speed ADCs with very challenging SNR and clock-to-clock skew targets. The LTC6951's variety of synchronization methods allows designers to optimize for ease of synchronization, clock jitter and the number of clocks required. The LTC6951 supports JESD204B subclass 1 converter clock schemes. To further simplify design, the LTC6951Wizard is provided to guide the user through design, simulation and evaluation of the LTC6951. ■

Figure 11. LTC6951Wizard settings



To evaluate a custom frequency plan, the LTC6951Wizard provides a Help file with step-by-step examples using the LTC6951Wizard to calculate register settings, design loop filter and program the LTC6951 SPI registers.

Figure 12. LTC6951Wizard loop filter design and simulation