Bus Buffers Simplify Design of Large, Noisy I²C Systems

Rajesh Venugopal

The I²C bus and its derivatives—such as SMBus, PMBus, the DDC bus of HDMI and IPMB bus of ATCA—are used in a variety of large systems to transfer vital system information. These bus specifications have gained wide acceptance due to ease of use. The I²C bus is a digital serial 2-wire bus consisting of a single clock (SCL) and single data (SDA) line. The I²C protocol employs open drain pull-downs to drive the bus low, and resistors or current sources to pull the bus high. The maximum allowed pull-up current and bus capacitance are 4mA and 400pF, respectively.

The original I²C specification limited the maximum bus operating frequency to 100kHz; it is now 400kHz. As systems grew larger, bus buffers were introduced to buffer bus capacitance and solve several other common I²C issues. Early bus buffers degraded certain I²C specifications in a manner that can be unacceptable in large noisy systems. The LTC4313 and LTC4315 family of bus buffers offers the benefits of traditional bus buffers while maintaining compliance to all I²C voltage specifications. This makes it the preferred choice for use in large noisy systems.

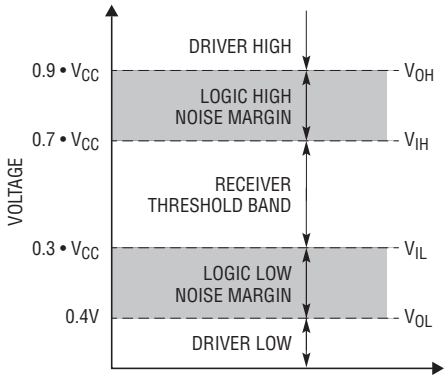

Figure 1. I²C bus voltage specifications and resulting noise margins

Figure 1 shows the I²C specification requirements for logic high and logic

Table 1. A list of LTC4313 and LTC4315 features and benefits

FEATURE	BENEFITS
I^2C Buffers	• Break up bus capacitance, which allows large I^2C compliant systems to be built, by keeping the capacitance of each section < 400pF
High V_{IL}	• High logic-low noise margin up to 0.3 • V_{CC} • Operation with noncompliant I^2C devices
Automatic Buffer Turn-Off Voltage Adjustment	• Compatible with devices whose RTA turn-on voltage is lower than 0.3 • V_{CC} • Interoperable with other LTC buffers
Level Translation	• Provides I^2C communication between buses with voltages from 1.4V to 5.5V
Rise Time Accelerators (RTAs)	• Reduce rise time • Allow larger bus pull-up resistors for better logic low noise margin • Selectable RTA pull-up current strength
Disconnection and Recovery from Stuck Bus	• Free masters to resume upstream communications • Generates up to 16 clock pulses and a stop bit on the stuck buses to get the bus to release high
Fall Time Control	• Minimizes transmission line effects in systems
Hot Swapping	• Waits for bus idle or stop bit before making a connection • Precharges bus to minimize disturbance

The LTC4315 and LTC4313 are high noise margin bus buffers that solve a number of problems associated with large I²C systems. They provide capacitance buffering, level translation for bus supplies ranging from 1.4V to 5.5V, high logic-low noise margins up to 0.3 • V_{CC} and reject noise above 0.3 • V_{CC} when the bus is a logic high.

low voltages on the bus. For I²C compliance, driven logic low signals must be below an output low level (V_{OL}) of 0.4V. Logic high signals require the bus to be pulled up above an output high level (V_{OH}) of 0.9 • V_{CC}, where V_{CC} is the bus supply voltage. I²C compliant receivers must interpret any voltage below an input low level (V_{IL}) of 0.3 • V_{CC} as a logic low and any voltage above an input high level (V_{IH}) of 0.7 • V_{CC} as a logic high. These requirements yield a logic low noise margin of 0.3 • V_{CC} – 0.4V and a logic high noise margin of 0.2 • V_{CC}.

Over time, as systems grew larger, bus capacitances increased well beyond 400pF. Bus buffers were introduced to break the large I²C bus into smaller segments and to drive the capacitance associated with each segment.

A higher operating frequency coupled with increasing bus capacitance also required a decrease in signal rise times. Rise time accelerators (RTAs) were incorporated into the bus buffers to reduce bus rise times—by sourcing strong pull-up currents into the bus during these transitions.

In addition, bus buffer products offered by Linear Technology also incorporated several additional features like SDA, SCL Hot Swap, precharge and stuck bus recovery to improve robustness of I²C systems and voltage level translation to ease communication across voltage domains.

The downside of buffer and RTA insertion into a bidirectional I²C bus is the introduction of deviations from the I²C specification. There are three reasons for this:

- First, buffers require a scheme to differentiate an externally driven logic low from their own driven low. This is required to prevent locking the bus into a permanent low state. As a result, some buffers drive V_{OL}s above the 0.4V I²C specification and require all other devices to drive below 0.4V. Others drive an output V_{OL} that is a small offset higher than the driven input V_{OL}.
- Second, to maximize RTA operating range, Linear Technology bus buffers turn off their pull-down devices and turn on their RTAs at voltages slightly higher than the I²C V_{OL}.
- Third, all buffers capacitively load the bus when they are active and need to be turned off at as low a voltage as possible in order to reduce bus rise time.

As a result, most existing bus buffers detect a logic low only if the bus voltage is < 0.6V. Most buffers turn on their RTAs at 0.8V. Some buffers drive a noncompliant V_{OL} > 0.4V. All these result in reducing the logic low noise margin from (0.3 • V_{CC} – 0.4V) to 0.2V or even lower, and slowing the bus rising edge by the capactive load of the buffers when they are active.

As systems grew, the compressed logic low noise margin of existing buffers increased the bus' susceptibility to noise. Typically larger systems require a bus buffer that restores logic low noise margin to the I²C specification, namely a fast buffer that is active until the bus voltage crosses the V_{IL} value of 0.3 • V_{CC} and does not load the bus.

An additional requirement in large systems is backward compatibility with buffer products whose RTAs turn on below 0.3 • V_{CC} or with products that drive a noncompliant V_{OL} of 0.6V. An adjustable RTA current is also advantageous, especially in large systems where multiple RTAs can be activated simultaneously. Large RTA currents result in sharp edges and raise concerns about unwanted effects like inductive ringing and EMI.

The LTC4315 (12-pin) and the LTC4313 (8-pin) parts specifically solve these problems while retaining the beneficial features of other Linear Technology bus buffer

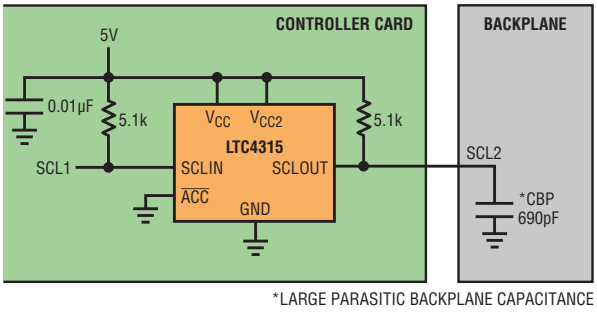

Figure 2. The LTC4315 driving the parasitic backplane capacitance in a large system. Only the SCL pathway is shown for simplicity.

In extended I²C systems, long PCB traces and large backplanes with long cables generate large parasitic bus capacitances. The LTC4315's high noise margin buffers can drive these capacitances without degrading signal integrity or reducing operating frequency.

products. Table 1 lists the key features of these products. This document references the LTC4315, but all text applies to the LTC4313 as well, unless otherwise noted. The LTC4315 has a high 0.3 • V_{CC} guaranteed minimum V_{IL}, ensuring a high logic-low noise margin. The LTC4315 is interoperable with devices that drive a high V_{OL} > 0.4V and with products whose RTAs turn on at voltages below 0.3 • V_{CC}. The LTC4315 allows user selection of the RTA current level in order to control bus rise rates. The LTC4315 retains capacitance buffering, Hot Swap, precharge, stuck bus recovery and level translation features of other Linear Technology bus buffers. Since its buffers do not load the bus, the LTC4315 is capable of operation up to 1MHz and is compatible with the I²C standard mode and fast mode, SMBus and PMBus specifications. In summary, LTC4315 provides all the benefits of the existing buffers without compromising any I²C specification.

CAPACITANCE BUFFERING AND NOISE REJECTION IN LARGE SYSTEMS

In large I²C systems, long PCB traces and large backplanes with long cables cause large parasitic bus capacitances. As shown in Figure 2, the LTC4315's high noise margin buffers can drive these large capacitances without degrading signal integrity or reducing operating frequency.

Another issue of large I²C systems, like the one in Figure 2, is noise susceptibility. Noise and signal coupling in the cable and between PCB traces can disrupt input and output clock and data signals, causing system level failures. A particularly

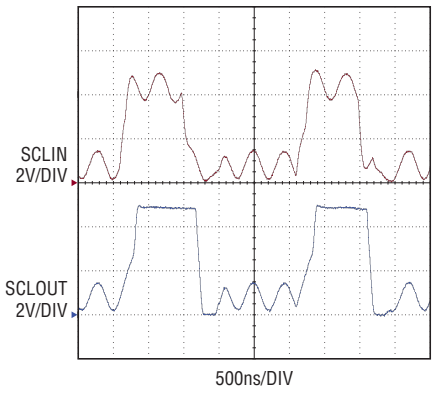

Figure 3. The LTC4315 transmits a clean logic high at SCLOUT even when a noisy 400kHz I²C signal is applied to SCLIN.

extreme example of a noisy SCL waveform is shown in Figure 3 to illustrate the robust noise rejection the LTC4315 features.

Figure 3 shows the LTC4315's handling of sinusoidal noise superimposed on a 400kHz square wave at its input. The noise applied to the logic high state is not propagated to the other side as long as that bus voltage does not drop below 0.33 • V_{MIN}. The logic high state of SCLOUT is not affected by noise on SCLIN. For the LTC4315, logic high noise margin is V_{OH} – 0.33 • V_{MIN}, where V_{MIN} is the lower of the V_{CC} and V_{CC2} voltages. For all versions of the LTC4313, V_{MIN} defaults to V_{CC}.

In Figure 3, when the SCLIN voltage drops below 0.33 • V_{MIN}, SCLOUT tracks SCLIN. No output glitches occur as the input crosses the V_{IL} level of 0.33 • V_{MIN}. Assuming a worst-case DC V_{OL} of 0.4V on the bus, the LTC4315's logic low noise margin is 0.33 • V_{MIN} – 0.4V = 1.25V. These noise suppression features make the LTC4315 a solid choice for large, noisy I²C systems. Ideally, system designers of large, noisy I²C systems should use LTC4315s on all boards for maximum noise immunity.

OPERATION WITH NON-COMPLIANT I²C DEVICES

Figure 4 shows the LTC4315's compatibility with devices that drive non-compliant V_{OL}s—in this case 0.6V. The LTC4315 passes the 0.6V to the microprocessor where it is interpreted as a logic low. The high buffer turn-off voltage of the LTC4315—1.089V in this circuit—yields a logic low noise margin of 489mV.

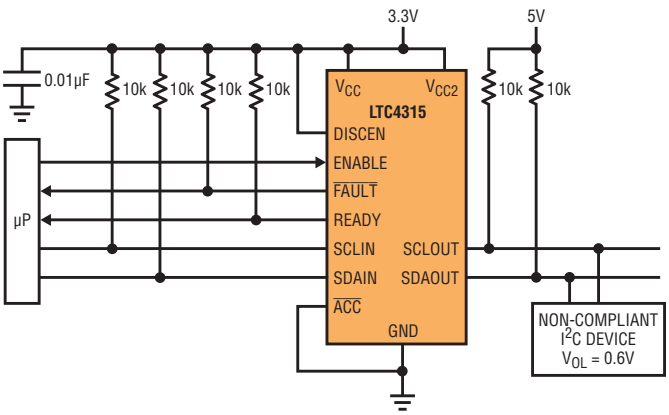

Figure 4. The LTC4315 communicating with a noncompliant I²C device.

The LTC4315 detects RTA current from other devices and turns off its buffers to prevent contention between its buffers and other RTAs. This permits the LTC4315 to be interoperable with any combination of all older Linear Technology bus buffers, whose RTAs turn on at voltages < 0.3 • V_{CC}.

INTEROPERABILITY WITH OTHER LINEAR TECHNOLOGY BUFFERS

In large systems older Linear Technology buffers might be present on the same bus with the LTC4315. These older buffers may have RTAs that turn on at voltages below the LTC4315 buffer turn-off voltage of 0.3 • V_{CC}. Glitch-free operation under these circumstances is critical for system integrity. The LTC4315 detects RTA current from other devices at bus voltages below 0.3 • V_{CC} and turns off its buffers to prevent contention between its buffers and other RTAs, to facilitate interoperability.

Figure 5 shows the LTC4315 operating in a dynamic system that changes as cards are plugged into or out of the backplane. For simplicity, a single 3.3V supply is chosen and only the SCL pathway is shown. Cards have buffers at their edges in order to shield the I²C devices on the card from the large backplane capacitance and to keep the card capacitances isolated from each other and to aid in hot swapping. The cards in the application shown have LTC4300A or LTC4307 buffers on their edges. The RTAs of these products turn on at 0.6V and 0.8V, respectively, while the LTC4315's buffers turn off at 0.3 • V_{CC} (~1V).

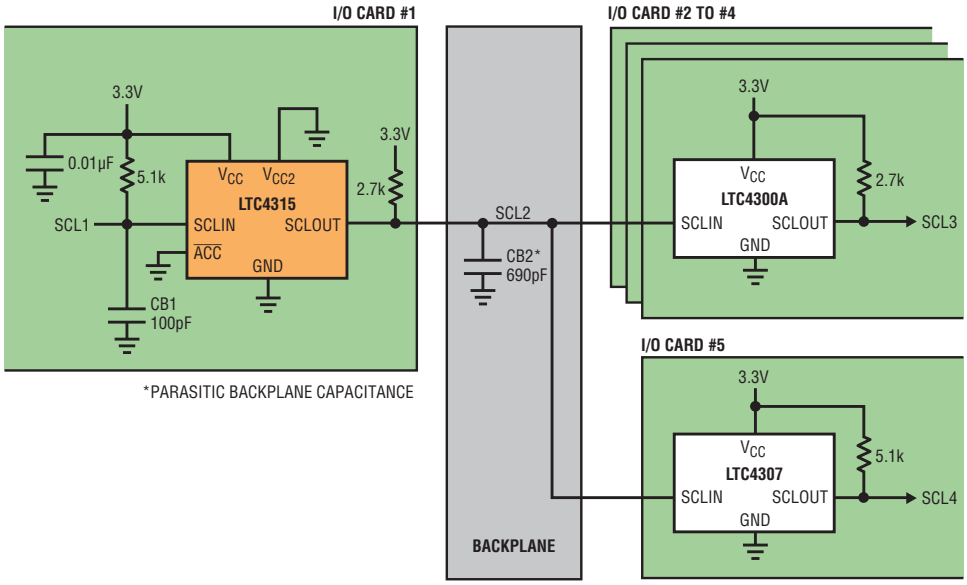

Figure 5. The LTC4315 operating with multiple LTC4300As and LTC4307s in a cascaded application.

Figures 6–9 track backplane and card SCL waveforms in this system as its configuration changes. Figure 6 shows the SCL waveforms for the system configuration shown in Figure 5, where three LTC4300As and one LTC4307 operate with one LTC4315. In Figure 7, the LTC4307 is

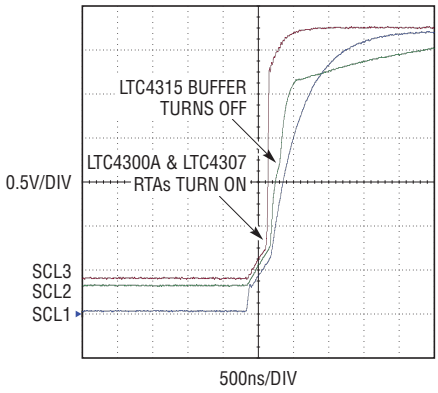

Figure 6. SCL waveforms of one LTC4315 operating with three LTC4300As and one LTC4307.

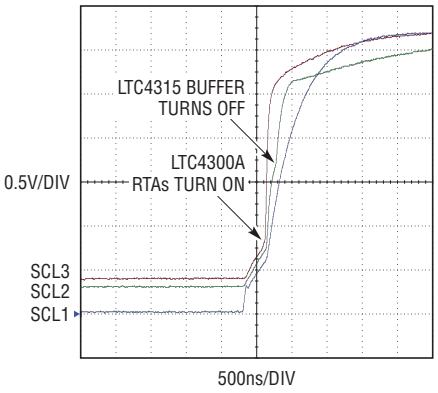

Figure 7. SCL waveforms of one LTC4315 operating with three LTC4300As.

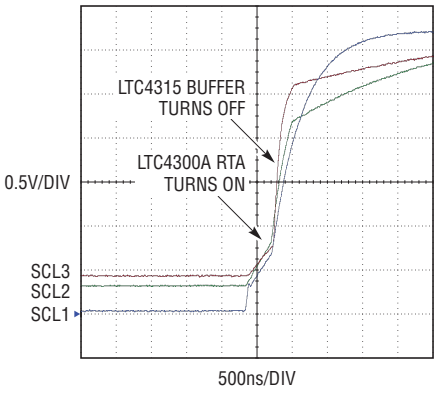

Figure 8. SCL waveforms of one LTC4315 operating with one LTC4300A.

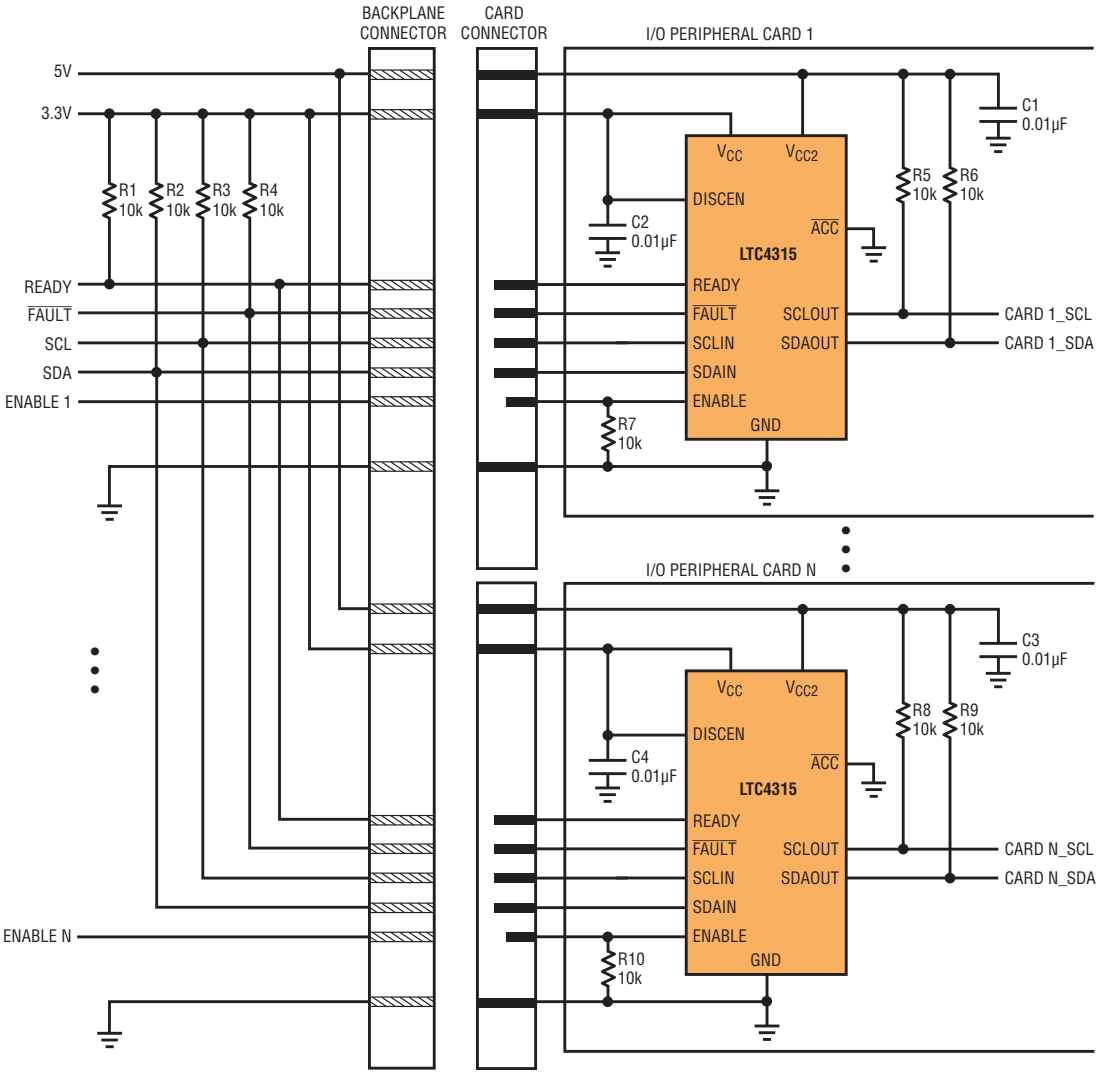

Figure 10. The LTC4315 in an I²C Hot Swap application with staggered pin lengths in the connector.

swapped out, leaving three LTC4300As and one LTC4315. In Figure 8, two more LTC4300As are swapped out, leaving one

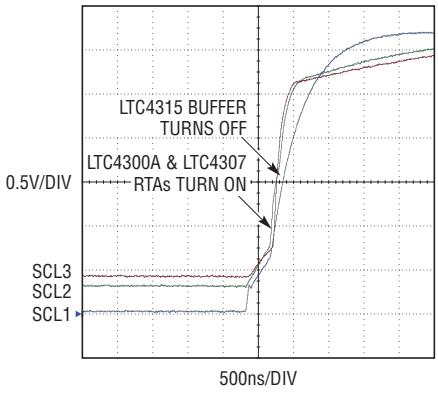

Figure 9. SCL waveforms of one LTC4315 operating with one LTC4300A and one LTC4307.

LTC4315 and one LTC4300A. Finally in Figure 9, the LTC4307 is reconnected, making the system one LTC4307, one LTC4300A and one LTC4315. The SCL waveforms remain monotonic during the entire sequence of events due to the automatic adjustment of the LTC4315 buffer turn-off voltage in response to varying amounts of LTC4300A and LTC4307 RTA current.

Figures 6–9 illustrate the interoperability of the LTC4315 with various combinations of LTC4300As and LTC4307s in a moderately complex system. As a general rule, the LTC4315 is interoperable with any number or combination of older Linear Technology buffers. Nevertheless, given the varying number and variety of buffers that can interact with each other, interoperability cannot be tested and hence guaranteed under all circumstances. Useful guidelines on card capacitances, bus pull-up resistances and buffer combinations to ensure interoperability in large systems are provided in the LTC4315 data sheet.

HOT SWAP AND CAPACITANCE BUFFERING

I/O cards with LTC4315s on their edges can be hot swapped into a live backplane as shown in Figure 10. The corresponding waveforms are shown in Figure 11. Communication at the backplane end is not disrupted during hot plug because

Circuits on a card that has an LTC4315 on its edge drive only the < 10pF input capacitance of the LTC4315. The LTC4315 drives the large combined capacitance of backplane and all the cards that plug into it. The LTC4315 can drive up to 1.2nF of capacitance on its SDA and SCL pins. This capacitance buffering feature, combined with RTAs, permits 400kHz operation in large systems.

the LTC4315's small input capacitance causes minimal disturbance during connection to the backplane. Furthermore the LTC4315 precharges its clock and data lines to 1V before they contact the backplane, minimizing the voltage step on the backplane bus. The LTC4315 waits for a stop bit or bus idle condition to enable its buffers, ensuring that a partial message is not transmitted across its buffers. When hot plugging into a live backplane, a staggered connector should be used. Make ENABLE the shortest pin with a pull-down resistor to GND on the card, V_{CC} and GND the longest pins and SCL and SDA medium length pins. This ensures that the part is powered up and SDA and SCL pins are precharged to 1V, before they connect to the backplane. Holding ENABLE low during this period ensures correct operation of the stop bit and bus idle circuitry and allows any transients associated with card insertion to settle before the LTC4315 is activated.

Figure 11 shows waveforms when the LTC4315 is hot plugged into a live backplane using a staggered connector. V_{CC} and

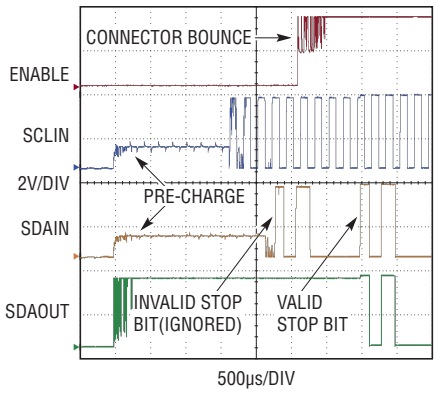

Figure 11. Waveforms during an LTC4315 Hot Swap event into a live backplane using a staggered connector.

V_{CC2}, as the longest pins, have already contacted the backplane and are powering the LTC4315 and the output buses. At this time SDAIN and SCLIN are precharged to 1V by the LTC4315. Once SDAIN and SCLIN contact the backplane, they are driven by backplane circuitry. Stop bits at the input are ignored by the LTC4315 as ENABLE is low. The outputs of the LTC4315 idle high (SCLOUT not shown), until a stop bit is detected at the input after ENABLE has been asserted high and is stable. The LTC4315 buffers turn on at this time and establish a connection between the input and output. Partial messages are not propagated across the LTC4315. If a staggered connector is not used, ENABLE should be held low until all transients associated with card insertion into a live system die out.

Circuits on a card that has an LTC4315 on its edge drive only the < 10pF input capacitance of the LTC4315. The LTC4315 drives the large combined capacitance of the backplane and all the cards that plug into it. The LTC4315 can drive up to 1.2nF of capacitance on its SDA and SCL pins. This capacitance buffering feature, combined with RTAs, permits 400kHz operation in large systems.

RISE TIME ACCELERATORS

The RTAs of the LTC4315 can be configured either in the current source mode ($\overline{ACC}$ open), slew limited switch mode ($\overline{ACC}$ grounded) or disabled ($\overline{ACC}$ high). In the current source mode the RTAs source a constant 2.5mA current into the bus. In the slew controlled switch mode, the RTAs turn on in a controlled manner and source current into the buses, making them rise at a typical rate of 40V/µs. To selectively disable RTAs only on the outputs, ground V_{CC2} and either ground $\overline{ACC}$ or leave $\overline{ACC}$ open. The LTC4313 comes with 3 different versions of RTAs. The LTC4313-1 RTAs are slew controlled switches, the LTC4313-2 RTAs are 2.5mA current sources and the LTC4313-3 has no RTAs.

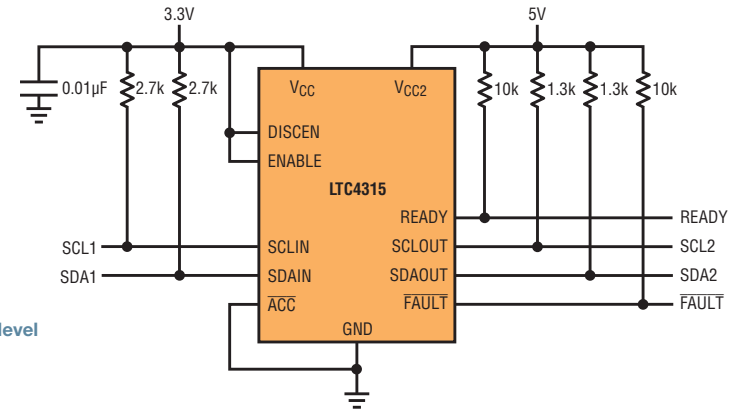

Figure 12. The LTC4315 in a level translating application.

The LTC4315 and LTC4313 disconnect stuck buses and allow I/O cards to be hot swapped into and out of live systems. They level translate signals down to 1.4V and provide user-selectable RTA current that permits operation at frequencies up to 1MHz.

LEVEL TRANSLATION

The circuit shown in Figure 12 illustrates the level translation feature of the LTC4315. The operating ranges for the LTC4315 supplies are V_{CC} from 2.9V–5.5V and V_{CC2} from 2.25V–5.5V. Tying the input bus to V_{CC} and the output bus to V_{CC2} permits level translation between 2.9V–5.5V inputs and 2.25V–5.5V outputs.

The example shown in Figure 12 translates a 3.3V input to a 5V output. Level translation to voltages lower than the minimum allowed V_{CC} and V_{CC2} values imposes other constraints. Level translation to output voltages less than 2.25V requires V_{CC2} to be tied low to disable output RTAs. Level translation to input voltages less than 2.9V requires all RTAs to be disabled by tying ACC high for the LTC4315 or using the LTC4313-3. This prevents overdriving of the input bus by the RTA. Under these conditions, level translation to a bus voltage of 1.4V is possible. The buffer turn-off voltage in both cases is 0.3 • V_{CC} and a high logic-low noise margin is maintained.

STUCK BUS DETECTION AND RECOVERY

Occasionally, slave devices get confused and get stuck in a low state. The LTC4315 monitors the output I²C bus to see if clock and data have been simultaneously high at least once in 45ms. If this condition is not detected, the LTC4315 asserts the FAULT flag low.

If DISCEN is tied high, the LTC4315 also disconnects the input and output sides and generates clock pulses on SCLOUT in an attempt to free the stuck bus. Clocking is stopped when data releases high or 16 clocks have been generated. After the final clock pulse, a stop bit is generated to reset the bus for further communication. When a stuck bus releases high, connection is reestablished when a stop bit or bus idle condition is detected on both buses. No user intervention is required.

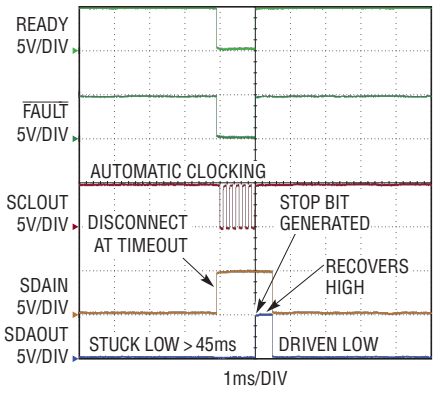

Figure 13. Bus waveforms during an SDAOUT stuck low and recovery event.

Figure 13 shows the waveforms during an SDAOUT stuck low and recovery event with DISCEN tied high. In Figure 13, the FAULT flag is asserted low after the 45ms timeout period and the input and output sides are disconnected. This causes SDAIN to release high. Clock pulses are generated on SCLOUT. SDAOUT releases high before 16 clock pulses have been generated. Clock pulsing is stopped and a stop bit is generated. As SDAOUT recovers and a stop bit is detected, connection is reestablished and signals propagate from the input to the output. If SDAOUT stays low, an input to output connection can be forced by toggling ENABLE low, then high.

If automatic stuck bus disconnection is not desired, this feature can be disabled in the LTC4315 by tying DISCEN low. In this case, during a stuck bus event, the FAULT flag is asserted low, but no stop bit or clock generation occurs and the input and output sides stay connected. Stuck bus disconnection and output clocking cannot be disabled in the LTC4313.

CONCLUSION

The LTC4315 and LTC4313 are high noise margin bus buffers that solve a number of problems associated with large I²C systems. They provide capacitance buffering, level translation for bus supplies ranging from 1.4V to 5.5V, high logic-low noise margins up to 0.3 • V_{CC} and reject noise above 0.3 • V_{CC} when the bus is a logic high. Their high bandwidth buffers and integrated RTAs enable operation at frequencies up to 1MHz. The buffers can drive noncompliant buses with parasitic capacitance as large as 1.2nF. They disconnect stuck buses and allow I/O cards to be hot swapped into and out of live systems. These buffers are interoperable with noncompliant I²C devices that drive a high V_{OL} and with legacy buffers whose RTAs turn on at low voltages. The LTC4315 and LTC4313 ease practical design issues associated with large I²C bus systems. ■