Versatile 80V Hot Swap Controllers Drive Large MOSFETs; Improve Accuracy and Foldback Current Limiting

by Mark Belch

Introduction

Routine maintenance and upgrades to high reliability computing, networking and telecommunications systems require that new or replacement circuit boards be inserted into a powered 48V(typical) bus. When a circuit board is inserted into a live backplane, the input capacitors on the board can draw high inrush currents from the backplane power bus as they charge. The inrush current can permanently damage the connector pins and board components as well as glitch the system supply, causing other boards in the system to reset. The new LT4256 family (LT4256-1 and LT4256-2) provides a compact and robust solution to eliminate these hot plugging issues.

The LT4256 is designed to turn on a board's supply voltage in a controlled manner, allowing the board to be safely inserted or removed from a live backplane having a supply voltage from 10.8V to 80V. The device features programmable inrush current control, current foldback, programmable undervoltage threshold with a 1% tolerance, overcurrent protection, and a power good output signal that indicates when the output supply voltage is ready.

The LT4256-1 and LT4256-2 are offered in an 8-pin SO package and are pin compatible with the LT1641-1 and LT1641-2. The LT4256 family upgrades the LT1641 and offers several superior electrical specifications (see Table 1), requiring only a few minor component modifications.

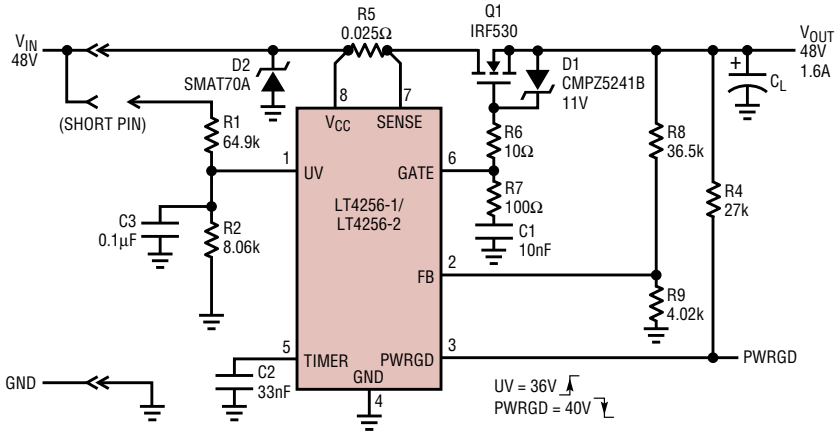

Figure 1. Typical application

Power-Up Sequence

Figure 1 shows a typical LT4256 application. An external N-channel MOSFET pass transistor (Q1) is placed in the power path to control the turn-on and turn-off characteristics of the supply voltage. Capacitor C1 controls the GATE slew rate, R7 provides compensation for the current control loop and R6 prevents high frequency oscillations in Q1. When the power pins first make contact, transistor Q1 is

Table 1. Differences between LT1641 and LT4256

SPECIFICATION	LT1641	LT4256	COMMENTS
UV Threshold	1.233V	4V	Higher 1% Reference for Better Noise Immunity and System Accuracy
FB Threshold	1.233V	3.99V	Higher 1% Reference for Better Noise Immunity and System Accuracy
TIMER Current	±70%	±26%	More Accurate TIMEOUT
TIMER Shutdown V	1.233V	4.65V	Higher Trip Voltage for Better Noise Immunity
GATE I_{PULLUP}	10µA	30µA	Higher Current to Accommodate Higher Leakage MOSFETs or Parallel Devices
GATE Resistor	1kΩ	100Ω	Different Compensation for Current Limit Loop
Foldback I_{LIM}	12mV	14mV	Slightly Different Current Limit Trip Point
I_{LIM} Threshold	47mV	55mV	Slightly Different Current Limit Trip Point

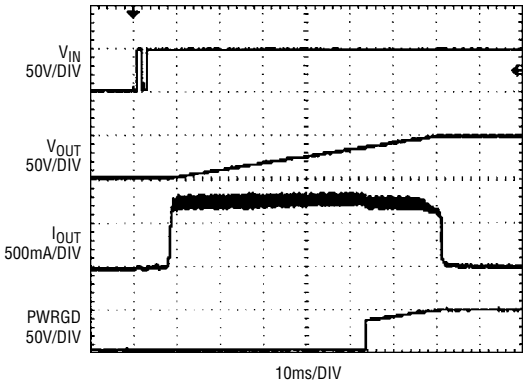

Figure 2. Startup waveforms

held off. The V_{CC} and GND connector pins should be longer than the pin that goes to R1 so they connect first and keep the LT4256 off until the board is completely seated in its connector. When the voltage on the V_{CC} pin is above the externally programmed undervoltage threshold, transistor Q1 is turned on (Figure 2). The voltage at the GATE pin rises with a slope equal to 30µA/C1 and the supply inrush current is:

$$I_{INRUSH} = C_L \bullet \frac{30\mu A}{C1}$$

where C_L is the total load capacitance. If the voltage across the sense resistor reaches 55mV (typical), the inrush current is limited by the internal current limit circuitry. When the FB pin voltage goes above 4.45V, the PWRGD pin goes high.

Short-Circuit Protection

The LT4256 features a programmable foldback current limit with an electronic circuit breaker that protects against short circuits or excessive load currents. The current limit is set by placing a sense resistor (R5) between V_{CC} and SENSE. To limit excessive power dissipation in the pass transistor and to reduce voltage spikes on the input supply during short-circuit conditions at the output, the current folds back as a function of the output voltage, which is sensed internally on the FB pin. When the voltage at the FB pin is 0V, if the part goes into current limit, the current limit circuitry drives the GATE pin to force a constant 14mV drop across the sense resistor.

Under high current (but not short-circuit) conditions, as the FB voltage increases linearly from 0V to 2V, the controlled voltage across the sense resistor increases linearly from 14mV to 55mV (see Figure 3). With FB above 2V, a constant 55mV is maintained across the sense resistor.

During startup, a large output capacitance can cause the LT4256 to go into current limit. The current limit level when V_{OUT} is low is only one quarter of the current limit level under normal operation, and it is time limited, so careful attention is needed to insure proper start up. The maximum time the LT4256 is allowed to stay in current limit is defined by the TIMER pin capacitor.

The current limit threshold (during normal operation) is:

$$I_{LIMIT} = \frac{55mV}{R5}$$

where R5 is the sense resistor. For a 0.02Ω sense resistor, the current limit is set at 2.75A and folds back to 700mA if the output is shorted to ground.

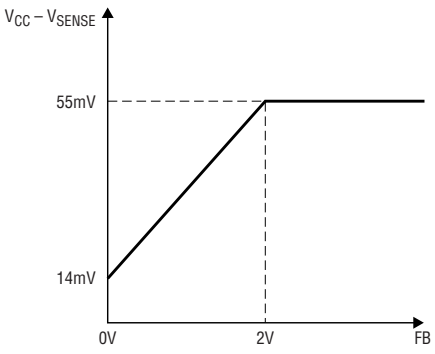

Figure 3. Current limit sense voltage vs FB pin voltage

For a 48V application, MOSFET peak power dissipation under short circuit conditions is reduced from 132W to 33.6W.

The LT4256 also features a variable overcurrent response time. The time required for the part to regulate the GATE pin voltage is proportional to the voltage across the sense resistor, R5. This helps to eliminate sensitivity to current spikes and transients that might otherwise unnecessarily trigger a current limit response and increase MOSFET dissipation.

Current Limit TIMER

The TIMER pin provides a method for programming the maximum time the part is allowed to operate in current limit. When the current limit circuitry is not active, the TIMER pin is pulled to GND by a 3µA current source. When the current limit circuitry becomes active, a 118µA pull-up current source is connected to the TIMER pin and the voltage rises with a slope equal to 115µA/C2. Once the desired maximum current limit time is chosen, the capacitor value is:

$$C(nF) = 25 \bullet t(ms)$$

If the TIMER pin reaches 4.65V (typ), the internal fault latch is set causing the GATE to be pulled low and the TIMER pin to be discharged to GND by the 3µA current source. The LT4256-1 latches off after a current limit fault. The LT4256-2 does not turn on again until the voltage at the TIMER pin falls below 0.65V (typ).

Undervoltage Detection

The LT4256 uses the UV (undervoltage) pin to monitor V_{IN} and allow the user the greatest flexibility for setting the operational threshold. Figure 1 also shows the UV level programming via a resistor divider (R1 and R2). If the UV pin goes below 3.6V, the GATE pin is immediately pulled low until the UV pin voltage goes above 4V. The UV pin is also used to reset the current limit fault latch after the LT4256-1 has latched off. This is accomplished by grounding the UV pin for a minimum of 5µs.

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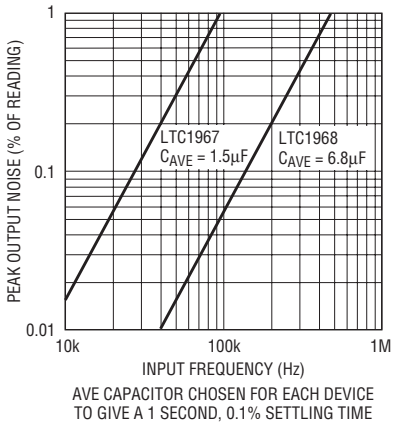

Figure 3. Output noise vs input frequency

noise in the DC output increases because the noise increases with frequency in the ΔΣ modulator. This noise aliases to low frequencies in the DC output. The increased averaging from a larger averaging capacitor lowers this noise. Figure 3 shows the output noise versus input frequency for the LTC1967 and LTC1968. The LTC1968 has lower noise than the LTC1967 at higher frequencies.

Finally, one must consider the settling time of the device. With larger averaging capacitors, the settling time increases. Since accuracy at low and high frequencies both increase with a larger averaging capacitor, *one should use the largest averaging capacitor possible while still meeting settling time requirements.* The data sheet has a graph of the settling time versus averaging capacitor.

Conclusion

The LTC1967 and LTC1968 simplify AC measurement by providing calibration-free accuracy, flexible input/output connections, and temperature stability. They maintain their accuracy over a large input frequency range. Both are available in a tiny 8-pin MSOP package.

LT4256-1/-2, continued from page 8

Automatic Restart and Latch Off Operation

Following a current fault, the LT4256-2 provides automatic restart by allowing Q1 to turn on when voltage on the TIMER pin has ramped down to 650mV. If the overcurrent condition at the output persists, the cycle repeats itself until the overcurrent condition is relieved. The duty cycle under short-circuit conditions is 3%, which prevents Q1 from overheating (see Figure 4).

The LT4256-1 latches off after a current fault (see Figure 5). After the LT4256-1 latches off, it can be commanded to restart by cycling UV to ground and then above 4V. This command can only be accepted after the TIMER pin discharges below the 0.65V (typ) threshold (to prevent overheating transistor Q1).

Power Good Detection

The LT4256 includes a comparator for monitoring the output voltage. The output voltage is sensed through the FB pin via an external resistor string. If the FB pin goes above 4.45V, the comparator's output releases the PWRGD pin so it can be externally pulled up. The comparator's output (PWRGD pin) is an open collector capable of operating from a pull-up voltage as high as 80V, independent of V_{CC}.

GATE Pin

The GATE pin is clamped to a maximum of 12.8V above the V_{CC} voltage. This clamp is designed to sink the internal charge pump current. An external Zener diode must be used from V_{OUT} to GATE. When the input supply voltage is between 12V and 15V, the minimum gate drive voltage is 4.5V, and a logic level MOSFET must be used. When the input supply voltage is higher than 20V, the gate drive voltage is at least 10V, and a MOSFET with a standard threshold voltage can be used.

Conclusion

The LT4256's comprehensive set of advanced protection and monitoring features make it applicable in a wide variety of Hot Swap™ solutions. It can be programmed to control the output voltage slew rate and inrush current. It has a programmable undervoltage threshold, and monitors the output voltage via the PWRGD pin. The LT4256 provides a simple and flexible Hot Swap solution with the addition of only a few external components.

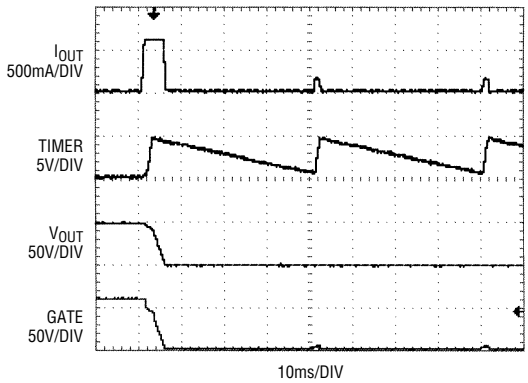

Figure 4. LT4256-2 current limit waveforms

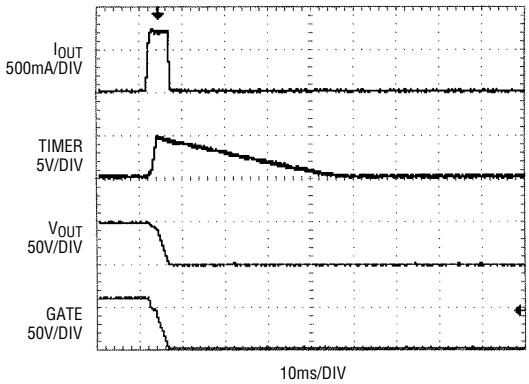

Figure 5. LT4256-1 current limit waveforms