Infinite Sample-and-Hold Outperforms Many Legacy Sample-and-Hold Amplifiers

by Derek Redmayne

Many applications requiring sample-and-hold amplifiers have been left high and dry by the dearth of these devices in today's catalogs. The use of an ADC followed by a DAC can provide this function, as well as producing characteristics not possible with a conventional sample-and-hold. The circuit shown in Figure 1 is a simple and compact implementation of a topology referred to as an "infinite sample-and-hold." It does not, in fact, hold for an infinite length of time but will do so until the power is turned off or until a new sample is required. The reason it is termed "infinite" is that it does not droop. It is formed from an ADC feeding a DAC. There is no droop because the sample is held as a digital code in the registers of the DAC.

The overall accuracy of the infinite sample-and-hold is determined by the error contributions of both the ADC and the DAC but is comparable to or better in most aspects than many of the older, and now obsolete, integrated sample-and-hold amplifiers. The disappearance of sample-and-hold amplifiers from the market is largely due to the fact that most ADCs now incorporate internal sampling circuits. Why not use these devices as the sampler? The alternative is building sample-and-hold amplifiers out of analog switches or diode bridges, and FET amplifiers. Most design engineers do not find this to be a very attractive alternative.

The infinite sample-and-hold in Figure 1 uses an LTC1417 serial 14-bit ADC interfaced to an LTC1658 serial 14-bit DAC. The short acquisition time of the ADC, coupled with external trigger circuitry, can produce a variety of useful functions, such as peak detection, a means for sampling dwell in a waveform such as the black reference level in video, phase measurement schemes, capacitance measurement or time division multiplexing, all without processor intervention. Such functions can, of course, be implemented by a microprocessor reading the output of an ADC, optionally modifying the result and sending it to one or more DACs. The advantage of a scheme that does not require a processor is, of course, low power and cost; in addition, the sample rate can be much higher than practical with a low powered processor. The uses of this type of function are almost endless, as are the possible variations.

Circuit Operation

The circuit in Figure 1 passes the serial output from the LTC1417 directly to the LTC1658, without requiring glue logic. If the reference voltages of the two parts are essentially the same, the function is very similar

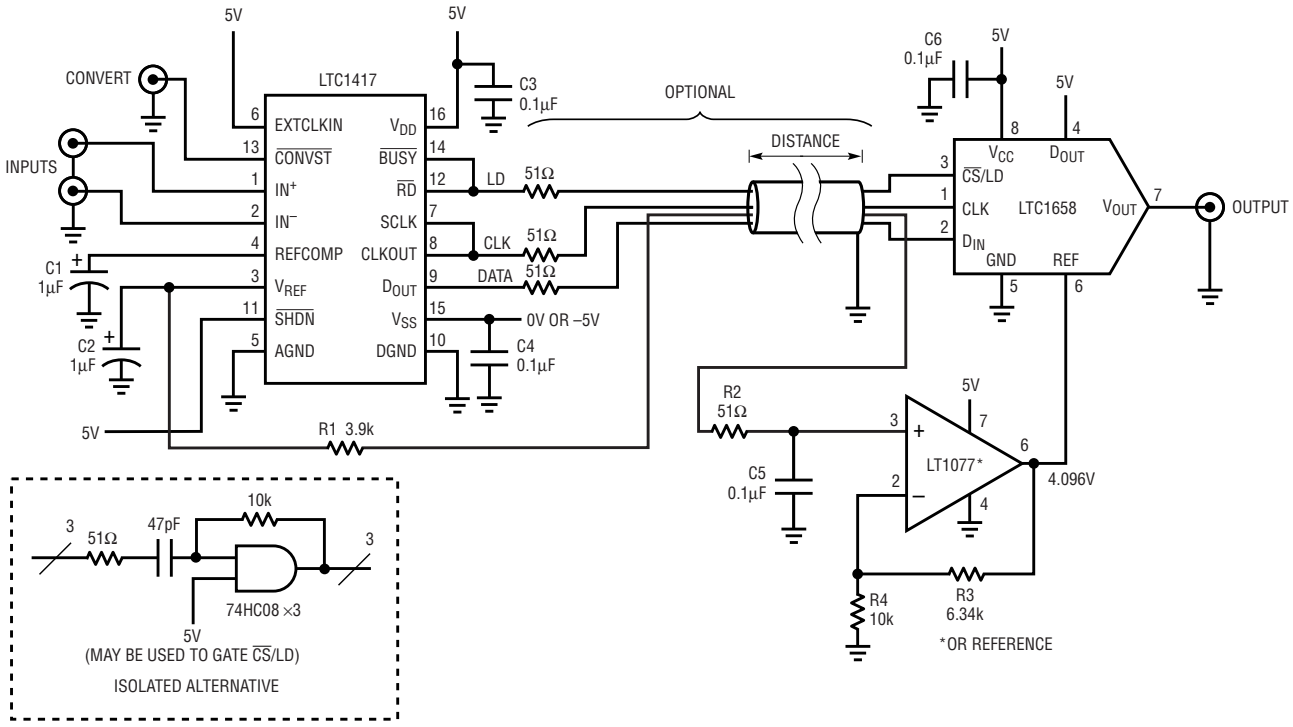

Figure 1. Infinite sample-and-hold schematic diagram

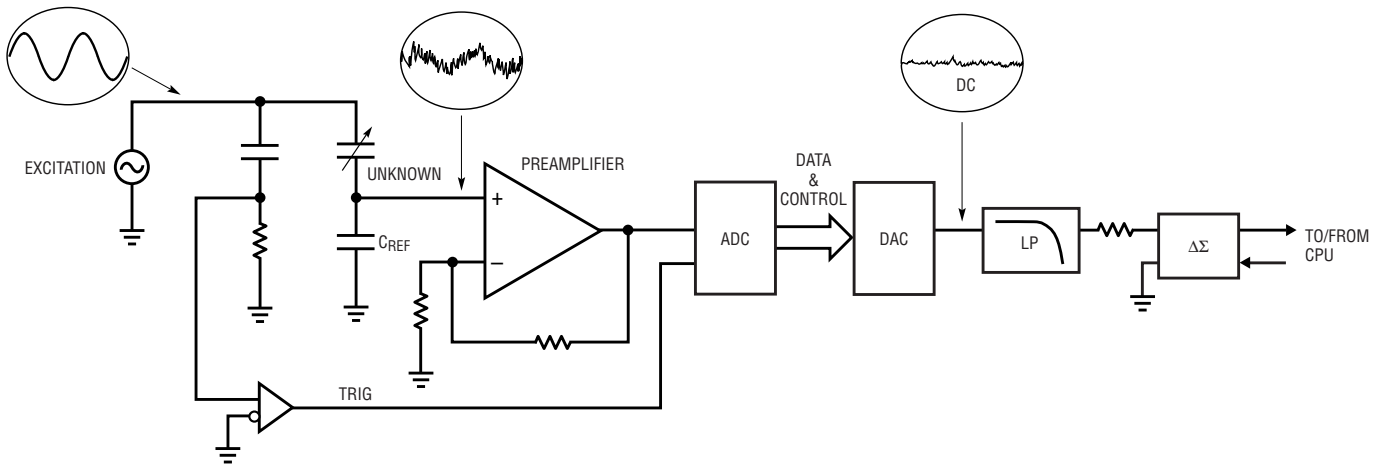

Figure 2. Block diagram of sample-rate conversion scheme

to an instrumentation amplifier followed by a sample-and-hold amplifier. In the case of the LTC1417, the internal 2.5V reference is stable but high impedance, but the REFCOMP terminal, which is labeled 4.096V and determines the full scale of the ADC, is only nominally at 4.096V. The LT1077 buffers the 2.5V output and provides a gain of 1.634 to produce the appropriate 4.096V reference for the LTC1658. If the output section is located at a distance or across a potential barrier, it needs a separate 4.096V reference at the LTC1658.

The LTC1417 is used in "internal conversion clock mode," where conversion and data transfer occur simultaneously. There is a one-conversion delay between the data sampled and the data output. If the waveform is sampled infrequently and an update is required as soon as possible, a first conversion must be performed at the time of the required sample, followed by a dummy conversion to transfer the data. The CS/$\overline{LD}$ line to the DAC can be gated to allow only the desired conversion to be passed to the DAC. Alternately, the fastest update will occur with parallel devices.

The use of a field-programmable gate array (FPGA) between the ADC and DAC allows the digital data to be modified prior to sending it to the DAC. If parallel I/O converters are used, some simple and useful operations, such as conversion of signed to absolute valued data, are possible even in a simple programmable-array-like device (PAL). The resulting output is a full-wave-rectified version of the original AC signal.

Sample-Rate Converter

There are cases where the infinite sample-and-hold can be useful as a sample-rate conversion scheme (see Figure 2). The LTC1417 can synchronously sample some recurring feature in the input waveform, possibly at a fairly high conversion rate or, alternatively, perform undersampling. Undersampling involves sampling a frequency that is above (possibly far above) Nyquist ($f_S/2$). The resulting output frequency is then the difference between the sample frequency or one of its harmonics and the input frequency. This type of sampling usually requires the bandwidth of the signal being sampled to be less than Nyquist ($1/2\ f_S$) or multiple signal components will fold into the same signal band and interfere with each other. The output of the DAC can then be bandpass filtered and resampled at a lower and potentially unrelated rate by a slower ADC associated with a low power processor. This circuit can be used in capacitive sensing schemes with repetition rates up to 400kHz, using a lowpass filter after the DAC to reduce the noise for subsequent resampling with a slower ADC. This effectively reduces the bandwidth of the system to 2× that of the lowpass filter. If the noise present at the original ADC is greater than several LSB, the filtering effects following the DAC and the use of a higher resolution ADC for resampling can reveal details below the quantization floor of the original ADC and DAC. The integral linearity is limited by the infinite sample-and-hold, but resolution can be greater. If a recurring waveform is noisy, the use of the infinite sample-and-hold at a high sample rate, followed by a lowpass filter and resampling at a lower rate can provide a $\sqrt{N}$ improvement (where N = the number of samples) in noise level relative to what would be achieved by sampling directly at the lower rate. This approach makes sense if the power or budget restrictions do not allow the use of a DSP. The total current consumption of this circuit is less than 5mA.

Other advantages of using this topology are in the area of aperture uncertainty. Where a low powered processor may have limitations on how fast and how consistently it can respond to interrupts, sampling a signal in response to an external timebase or trigger can eliminate the uncertainty associated with nondeterministic behavior in the processor. If a direct control voltage is also required from the sampled waveform, the DAC may be the best way to produce it, even if the digital output is subsequently used by the processor.

The acquisition time of the LTC1417 is typically 150ns, and aperture jitter is only 5ps. The pedestal error common with classic

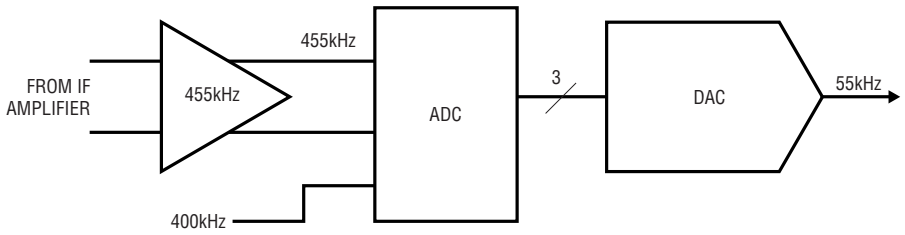

Figure 3. Down converter samples in Nyquist zone 3 (zone 3 extends from f_S to $f_S \times 1.5$).

sample-and-hold amplifiers and caused by charge injection is not an issue with this infinite sample-and-hold. There are, however, other error sources, such as offset voltage, quantization error and differential and integral nonlinearity contribution in both the ADC and the DAC. In this particular example, the DAC has more significant nonlinearity and offset error than the ADC. If higher linearity and offset performance are required, a 16-bit multiplying DAC, such as the LTC1595 could be used, because the 14-bit ADC (LTC1417) delivers 16-bit words.

As this serial scheme only requires three interface lines, the use of optoisolators or some other isolation scheme is practical, allowing the output to be at different potential or distant from the input and, of course, with the variable gain offered by the multiplying feature of the DAC.

The inset in Figure 1 shows a very inexpensive scheme by which the output of the ADC can be level shifted hundreds of volts, provided that there is minimal high frequency noise between the ADC and the DAC. This would often be the case where a high voltage power supply has a common ground with lower voltage circuitry. This means of capacitively coupling digital data uses the high frequency content in the waveform only. It should not be used in situations where transients will be seen between the two subsystems. The voltage rating of the capacitors must be adequate and agency-accepted creepage distances should be observed.

Down Converter

If the conversion clock of the ADC is driven with a fixed frequency and the incoming signal is undersampled, the circuit in Figure 3 can down-convert frequencies up to the full linear bandwidth of the LTC1417. For example, if a band-limited 455kHz IF signal is being received at the input of the LTC1417 and a conversion clock of 400kHz is used, a 55kHz difference frequency appears at the output of the DAC. This output could be used in a variety of ways after active low-pass or bandpass filtering. For example, in conjunction with a frequency synthesizer, a mixer, and precision rectifier, a spectrum analyzer could be built using an LTC2420 20-bit micropower No Latency™ ΔΣ converter and a PIC. The subsequent filtering and resampling of this signal with a lower speed ADC permits a low power processor to characterize a high frequency signal and gain the benefit of a sample rate that far exceeds its processing capability. The use of an active filter after the DAC produces a narrow-band response that is not possible if the filtering is done at the IF frequency.

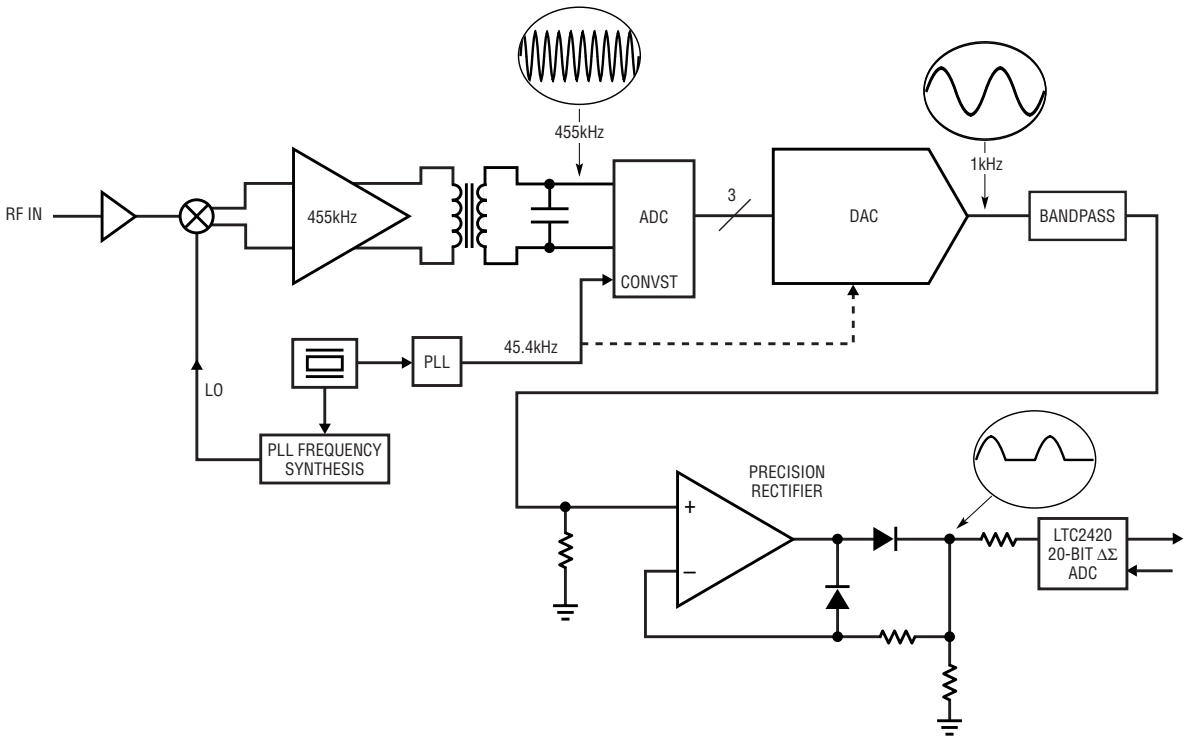

Figure 4. Block diagram of spectrum analyzer based on infinite sample-and-hold and LTC2420 20-bit ΔΣ ADC

In cases where the infinite sample-and-hold is used to undersample a higher frequency, the down conversion that is performed exaggerates the effects of phase jitter. This can be both a blessing and a curse. The blessed effect is that frequency stability and jitter effects are much easier to measure. The curse is that the use of a phase-locked loop as a tunable sample clock for spectrum analysis applications may simply expose the phase jitter of the phase-locked loop, rather than the incoming signal. Note also that undersampling a signal requires that the frequencies correspondingly below the sampling clock must be suppressed or they will fold into the baseband and become inseparable from the signal of interest.

An alternate down-conversion scheme in a single stage can use undersampling at a submultiple of an offset frequency (see Figure 4). If, for example, it is necessary to produce a 1kHz tone directly from a 455kHz IF signal, sampling at 454kHz is beyond the capability of the both the LTC1417 and the LTC1658. At the above mentioned 55kHz output rate, the output does not actually settle, but because each step is well within the slew limits of the DAC, the results are reasonable. On the other hand, if the ADC were sampling at 454kHz/10 (45.4kHz), the difference frequency would be 1kHz but the DAC update rate would allow plenty of time for settling, and distortion would be lower than would result from running at or near the full rate of the ADC. If the DAC update rate is 45kHz, the low-pass filter following the DAC should suppress the 45kHz update rate by 50dB or more.

Conclusion

The use of the infinite sample-and-hold as a sample-and-hold is straightforward and provides hold times not possible with a capacitor-based sample-and-hold amplifier. The characteristics can be tailored to suit many different applications by addition of circuitry before or after the ADC/DAC combination. Other Linear Technology ADCs and DACs can be used and multiple outputs derived from a single waveform can be provided by many DACs driven by a single ADC, as can multiple inputs be sampled via a multiplexer.

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