Maximize the Performance of 16-Bit, 105Msps ADC with Careful IF Signal Chain Design

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Introduction

Modern communication systems require an ADC to receive an analog signal and then convert it into a digital signal that can be processed with an FPGA. The job of a mixed signal engineer is to optimize the signal at the input of the ADC to maximize overall system performance. This usually requires a signal chain comprised of multiple gain and filtering sections. An ADC is only as good as the signal it is measuring.

For instance, the LTC2274 provides excellent AC performance with an appropriate IF signal chain. The LTC2274 is a 16-bit, 105Msps ADC that serially transmits 8B/10B encoded output data compliant with the JESD204 specification. It uses a single differential transmission line pair to reduce the number of IO lines

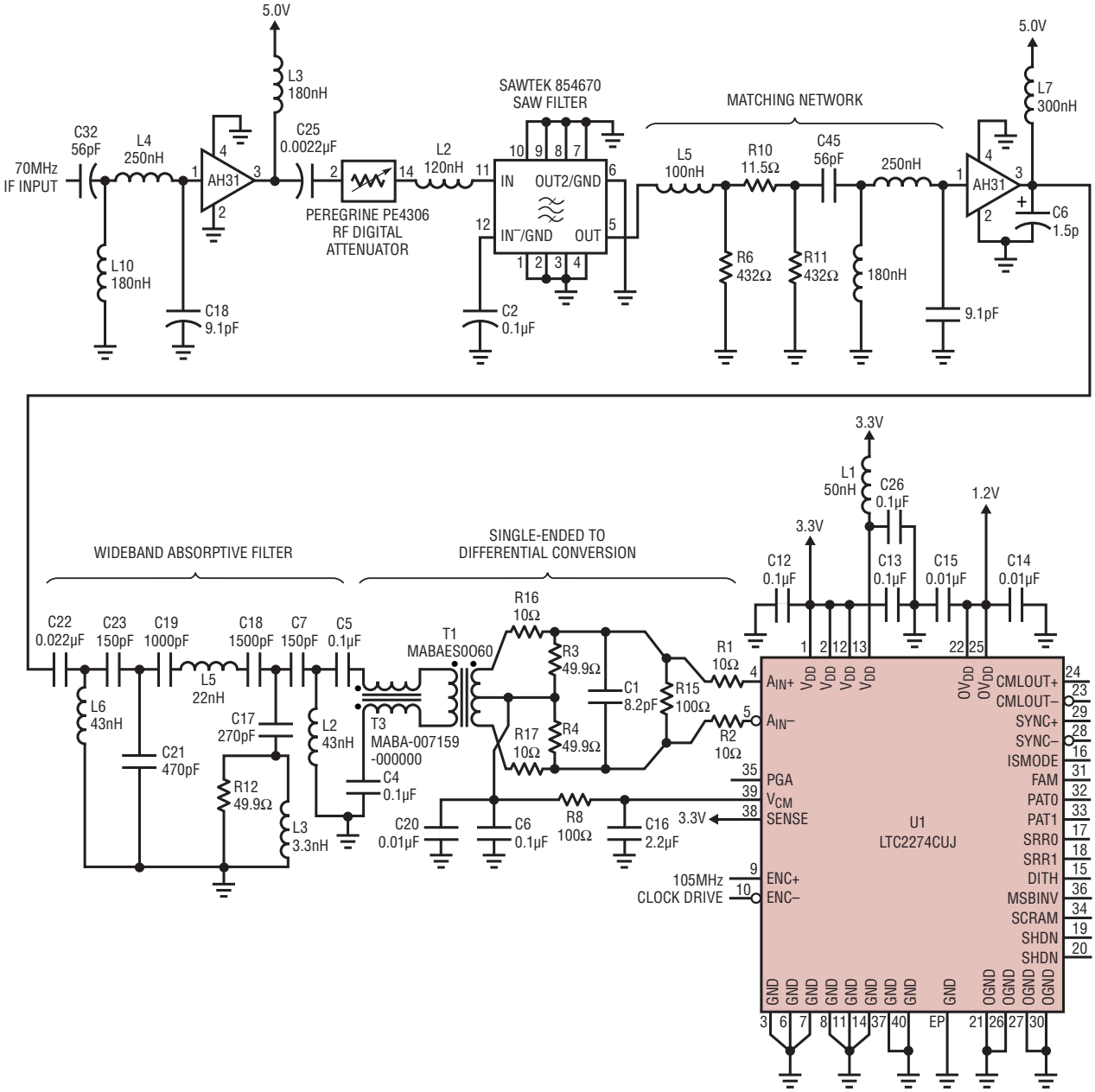

Figure 1. IF receiver chain

required to transmit output data. The LTC2274 has 77dB of SNR, and 100dB of spurious free dynamic range.

Signal Chain Topology

Figure 1 details a signal chain optimized for a 70MHz center frequency and a 20MHz bandwidth driving the LTC2274. The final filter and circuitry around the ADC are shown in detail. The earlier stages of the chain can be changed to suit a target application.

The first stage of amplification in the chain uses an AH31 from TriQuint Semiconductor. This GaAs FET amplifier offers a low noise figure and high IP3 point, which minimizes distortion caused by the amplifier stage. It provides 14dB of gain over a wide frequency region. The high IP3 prevents intermodulation distortion between frequencies outside the passband of the surface acoustic wave (SAW) filter.

A SAW filter follows the amplification stage for band selection. The SAW filter offers excellent selectivity and a flat passband if matched correctly. Gain before the SAW must not be higher than the maximum input power rating of the SAW; otherwise it leads to distortion. A digitally controlled step attenuator may be required in the signal path to control the power going into the SAW filter.

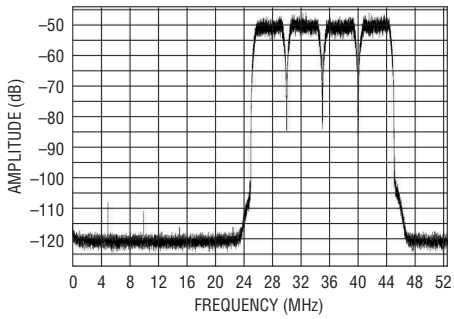

Figure 2. Typical spread spectrum performance

The second stage of amplification is used to recover the loss in the SAW filter. The insertion loss of the SAW filter is about –15dB, so the final amplifier should have at least this much gain, plus enough gain to accommodate the final filter. By splitting the gain between two amplifiers, the noise and distortion can be optimized without overdriving the SAW filter. It also allows for a final filter with better suppression of noise from the final amplifier, improving SNR and selectivity.

The output stage of the final filter needs to be absorptive to accommodate the ADC front end. This suppresses glitches reflected back from the direct sampling process.

This signal chain will not degrade the performance of the LTC2274. When receiving a 4-channel WCDMA signal with a 20MHz bandwidth, centered at 70MHz, the ACPR is 71.5dB (see Figure 2).

Conclusion

The LTC2274 can be used to receive high IF frequencies, but getting the most out of this high performance ADC requires a carefully designed analog front end. The performance of the LTC2274 is such that it is possible to dispense with the automatic gain control and build a receiver with a low fixed gain. The LTC2274 is a part of a family of 16-bit converters that range in sample rate from 65Msps to 105Msps. For complete schematics of this receiver network, visit www.linear.com.

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a 100mV V_{OCM} shift. This illustrates the fact that single-ended feedback around a fully differential amplifier introduces a noise gain of two from the V_{OCM} pin to the "open" output. In order to avoid this noise, simply do not use that output, resulting in a fully single-ended application. Or, you can take the slight noise penalty and use both outputs.

A Single-Ended Transimpedance Amplifier

Figure 3 shows the LTC6406 connected as a single-ended transimpedance amplifier with 20kΩ of transimpedance gain. The BF862 JFET buffers the LTC6406 input, drastically reducing the effects of its bipolar input transistor current noise. The V_{GS} of the JFET is now included as an offset, but this is typically 0.6V so the circuit still functions well on a 3V single supply and the offset can be dialed out with the 10k potentiometer. The time domain response is shown in Figure 4. Total output noise on 20MHz bandwidth measurements shows 0.8mV$_{RMS}$ on V_{OUT}^+ and 1.1mV$_{RMS}$ on V_{OUT}^-. Taken differentially, the transimpedance gain is 40kΩ.

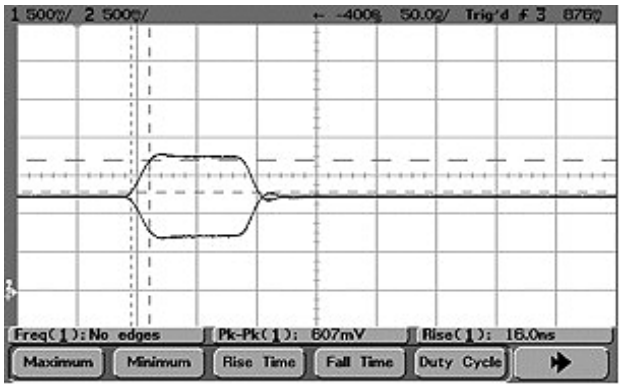

Figure 4. Time domain response of circuit of Figure 3, showing both outputs each with 20kΩ of TIA gain. Rise time is 16ns, indicating a 20MHz bandwidth.

Conclusion

New families of fully differential op amps like the LTC6406 offer unprecedented bandwidths. Fortunately, these op amps can also function well in single-ended and 100% feedback applications.