New Generation of 14-Bit 150Msps ADCs Dissipates a Third the Power of the Previous Generation without Sacrificing AC Performance

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Introduction

The LTC2262 family of ultralow power, high speed analog-to-digital converters dissipates less than one third the power of comparable earlier-generation ADCs while maintaining excellent AC performance. Ultralow power makes it possible to add features to and improve the performance of power-limited applications while remaining within the power budget. Of course, improved operating efficiency also reduces recurring operating costs in applications found in 3G/4G LTE and WiMAX basestation equipment.

In addition to offering considerably lower power, the ADCs in the LTC2262 family incorporate a unique set of digital output features that help to simplify layout and reduce digital feedback. The low power core of the LTC2262 is also integrated into multichannel parts, including 4-channel ADCs and 2-channel ADCs. For a complete list of the ultralow-power ADC family, see Table 1.

Low Power, High Performance

The LTC2262 family includes 14- and 12-bit ADCs that span sampling rates from 25Msps (which can sample down to 1Msps) to 150Msps, while consuming approximately 1mW for every megasample-per-second. For instance, the LTC2262-14 is a 14-bit, 150Msps ADC that consumes only 149mW of power from a 1.8V supply.

It is important to note that the ultralow power dissipation for this pipelined ADC architecture comes without sacrificing performance. The LTC2262-14 has a typical signal-to-noise ratio (SNR) of 72.8dB and SFDR of 88dB at baseband. Figure 1 shows the typical AC performance of the LTC2262-14 sampling a 30MHz sine wave at 150Msps (data from the circuit of Figure 2). The exceptional low power operation improves thermal performance in compact enclosures, where high temperatures can degrade SNR.

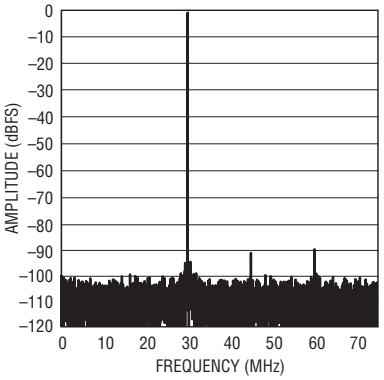

Figure 1. Typical performance of the LTC2262-14

Digital Outputs

The LTC2262 family also offers some unique digital features to simplify overall design in a wide variety of applications. The LTC2262 can be configured to run in one of three data output modes: full rate CMOS, double data rate (known as DDR) CMOS, and DDR LVDS.

Full rate CMOS presents the data on all 14 lines and consumes the lowest power. This mode is identical across Linear's parallel CMOS output ADCs so designers can use a much lower power ADC without changing FPGA code or ASIC design.

Table 1. The new generation of ultralow-power ADCs

Sample Rate	Resolution	Single Channel	Two Channel	Four Channel
25Msps	12-Bit	LTC2256-12	LTC2263-12	LTC2170-12
	14-Bit	LTC2256-14	LTC2263-14	LTC2170-14
40Msps	12-Bit	LTC2257-12	LTC2264-12	LTC2171-12
	14-Bit	LTC2257-14	LTC2264-14	LTC2171-14
65Msps	12-Bit	LTC2258-12	LTC2265-12	LTC2172-12
	14-Bit	LTC2258-14	LTC2265-14	LTC2172-14
80Msps	12-Bit	LTC2259-12	LTC2266-12	LTC2173-12
	14-Bit	LTC2259-14	LTC2266-14	LTC2173-14
105Msps	12-Bit	LTC2260-12	LTC2267-12	LTC2174-12
	14-Bit	LTC2260-14	LTC2267-14	LTC2174-14
125Msps	12-Bit	LTC2261-12	LTC2268-12	LTC2175-12
	14-Bit	LTC2261-14	LTC2268-14	LTC2175-14
150Msps	12-Bit	LTC2262-12	N/A	N/A
	14-Bit	LTC2262-14	N/A	N/A

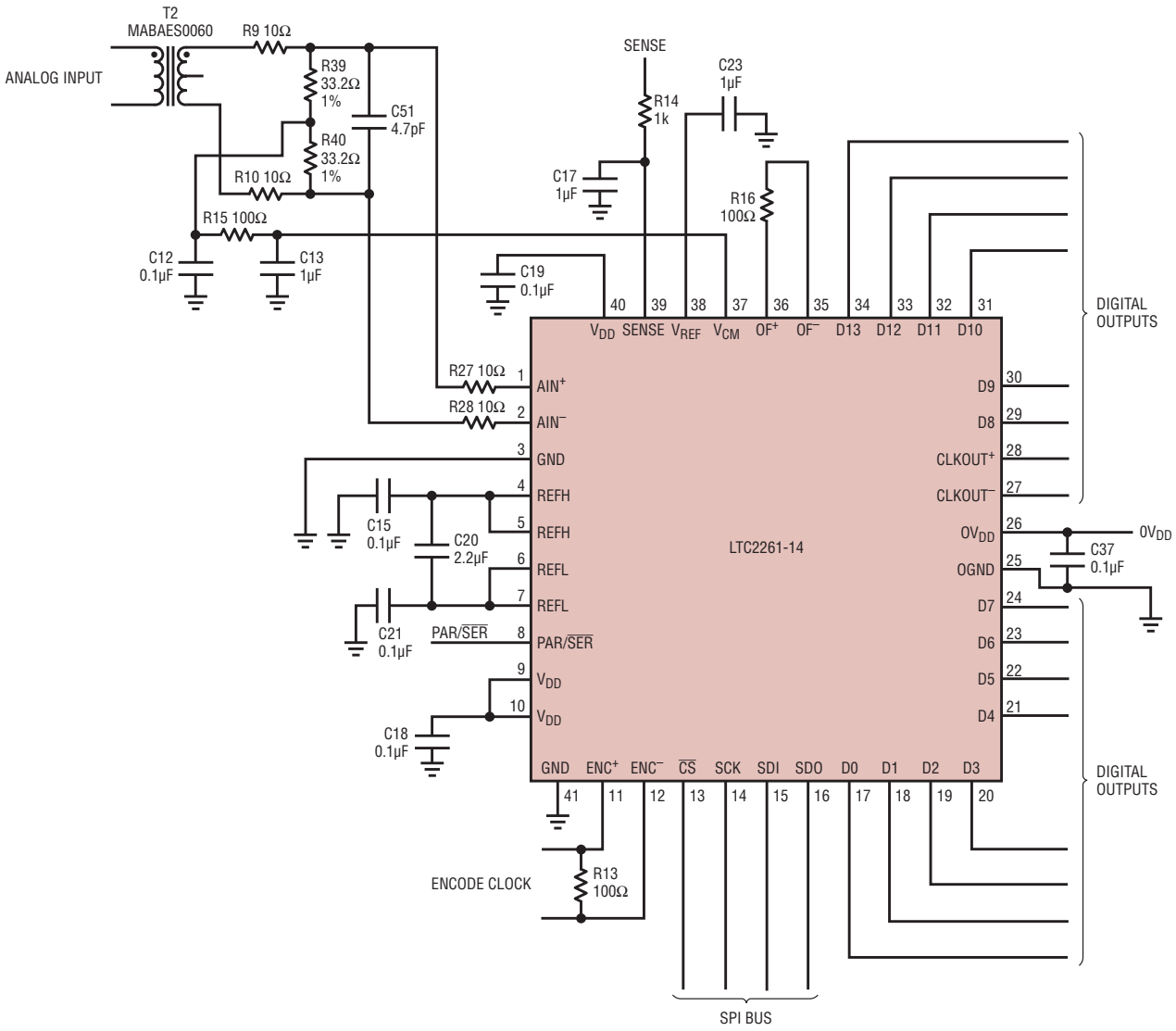

Figure 2.Typical application of the LTC2261-14

If board space or FPGA GPIO is limited, then the DDR CMOS mode can be used reduce the number of data lines. In double data rate LVDS mode, two data bits are multiplexed and output on each differential output pair, one valid on the rising edge of the clock, the other on the falling edge. This allows the data to be clocked out on half the data lines, which reduces the number of lines to seven for the 14-bit ADCs, and six for the 12-bit ADCs.

DDR LVDS mode functions in a similar fashion, with two bits clocked out on each data line on each clock cycle, but because it is a differential signal it uses 14 data lines, versus the 28 lines required for standard LVDS signaling. DDR LVDS uses an additional 10mW but the differential signaling provides some rejection of digital noise, also known as digital feedback.

Digital Feedback

Digital feedback occurs when energy from ADC outputs couples back into the analog section, causing interaction that appears as odd shaping in the noise floor and spurs in the ADC output spectrum. The worst situation is at midscale, where all outputs are changing from ones to zeroes, or vice versa, generating large ground currents that couple back into the input.

Digital feedback at both the device level and the system level can be made worse by poor layout choices. Long output busses, routing at low characteristic impedance and heavy capacitive loading at the receiving device all conspire to produce higher pulse currents in the output stages.

The use of the maximum digital output supply voltage (OV_{DD}) similarly maximizes digital currents. Placement of OV_{DD} bypass on the bottom of the board, with added lead inductance, large bodied capacitors, small diameter vias, thick boards, and thermal relief all raise the impedance of the supply rails to the output section, increasing the potential for noise sources. Returning OGND to a poorly grounded paddle makes things worse. These layout conditions together conspire to increase ground bounce on the substrate, which leads to digital feedback.

Digital feedback manifests itself in the ADC output spectrum. Figure 3 shows the noise floor of the LTC2261-14, a 14-bit 125Msps ADC. To produce this result, a demo board was modified to maximize digital feedback. In this case the digital feedback causes peaks in the noise floor of about 8dB.

The layout techniques used on the LTC2261-14 demo board are designed to help minimize digital feedback, but some is still unavoidable. The layout of the demo board area around the LTC2261 is shown in Figure 4. The use of barriers around the analog input, and clock help to reduce digital feedback effects. Also proper grounding of the reference bypass and OV_{DD} bypass help to mitigate digital feedback. A proper layout helps reduce the digital feedback seen in the output spectrum.

With a poor layout, and with low signal levels, digital feedback can appear as an exaggeration of odd harmonics, as shaping of the noise floor related to the delayed feedback and as some exaggeration of the noise floor. In severe cases, localized regions of the noise floor may be elevated by 20dB. If a narrow band application happens to collide with the elevated region of the noise floor, the result is a real loss of SNR on the order of 20dB. While good layout can help reduce the effects of digital feedback, it may not be enough to eliminate the problem.

The LTC2262 includes a unique digital feedback mitigation feature called "alternate bit polarity mode." Digital feedback is likely to occur when sampling a small input signal that is exercising a few codes around midscale. On each sample, all of the high order data bits are swinging from zero to one, which generates large ground currents that can couple back into the analog inputs, maximizing digital feedback. When alternate bit polarity mode is used, every odd data line is inverted. So, instead of 14 data lines simultaneously switching between 0 and 1, half are switching in one direction, half in the other direction. This produces a cancellation of fields, significantly reducing the resulting ground currents, and minimizing digital feedback. To decode this data, simply apply an inverter on each odd data line in the receiver.

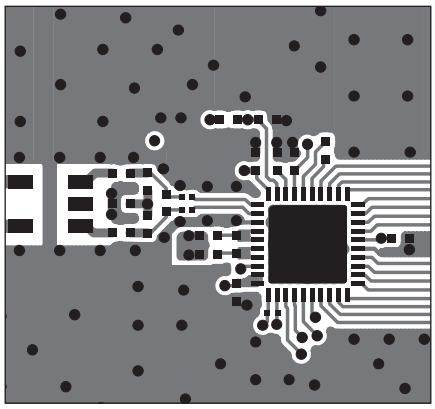

Figure 4. Layout of the LTC2261-14 application shown in Figure 2

The LTC2262 ultralow power core is also available in 2- and 4-channel ADCs. The LTC2175-14 is a quad, 14-bit ADC that samples at 125Msps. The LTC2175 dissipates only 558mW of total power—only 139.5mW per ADC. At 125Msps, each channel outputs two bits at a time, using only two lines per ADC. This reduces the number of data lines used by the LTC2175, and allows it to be packaged in a space-saving 7mm × 8mm QFN package.

In addition to the alternate bit polarity mode, an optional data output randomizer is available to further reduce interference from the digital outputs. The least significant bit (LSB) is combined using an exclusive-OR function with the other outputs before transmission. The received digital output bus can then be easily decoded by performing the reverse operation in the FPGA. Using this data encode scheme reduces the residual tone caused by digital feedback by 10dB to 15dB. Using the output randomizer and alternate bit polarity together can significantly decrease the effects of digital feedback.

For comparison, Figure 5 shows an image of the noise floor of the LTC2261-14 taken using the same board and on the same scale as before, but with alternate bit polarity and the data output randomizer enabled. The shaping of the noise floor is reduced, which improves SNR and SFDR. Using alternate bit polarity mode helps to reduce digital feedback on boards with poor layout, and can improve results in designs with low level input signal.

Multiple Channel Versions

The LTC2262 ultralow power core is also available in 2- and 4-channel ADCs. The LTC2175-14 is a quad, 14-bit ADC that samples at 125Msps. The LTC2175 dissipates only 558mW of total power—only 139.5mW per ADC. At 125Msps, each channel outputs two bits at a time, using only two lines per ADC. This reduces the number of data

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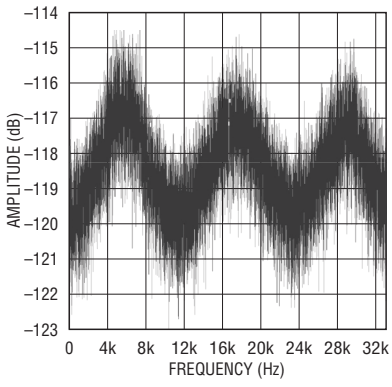

Figure 3. LTC2261 noise floor in normal operation

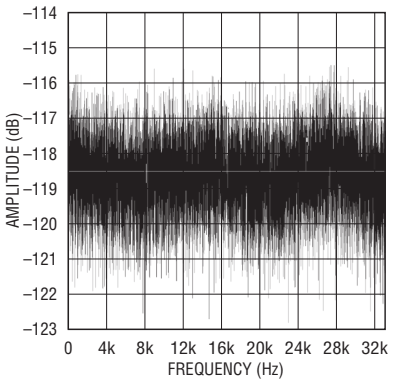

Figure 5. Noise floor with alternate bit polarity and data output randomizer enabled

activation energy can come from heat or the terminal voltage. The more activation energy available from these two sources the greater the chemical reaction rate and the faster the aging.

Li-Ion batteries that are used in the automotive environment must last 10 to 15 years. So, suppliers of automotive Li-Ion batteries do not recommend charging the batteries above 3.8V. This does not allow the use of the full capacity of the battery, but is low enough on the activation energy PDF to keep corrosion to a minimum. The iron phosphate battery anode has a shallower discharge curve, thus retaining more capacity at 3.8V.

Battery manufacturers typically store batteries at 15°C (59°F) and a 40% state of charge (SoC), to minimize aging. Ideally, storage would take place at 4% or 5% SoC, but it must never reach 0%, or the battery may be damaged. Typically, a battery pack protection IC prevents a battery from reaching 0% SoC. But pack protection cannot prevent self-discharge and the pack protection IC itself consumes some current. Although Li-Ion batteries have less self-discharge than most other secondary batteries, the storage time is somewhat open-ended. So, 40% SoC represents a compromise between minimizing aging and preventing damage while in storage (see Figure 2).

In portable applications, the reduction in capacity from such a reduced SoC strategy is viewed negatively in marketing specifications. But it is sufficient to detect the combination of high ambient heat and high battery SoC to implement an algorithm that minimizes aging while ensuring maximum capacity availability to the user.

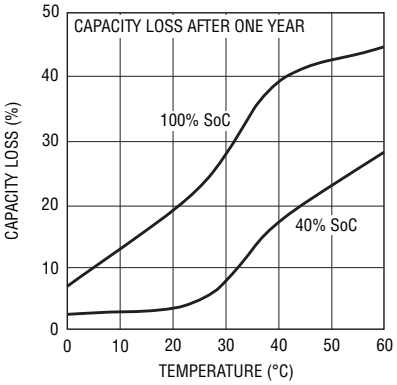

Figure 2. Yearly capacity loss vs temperature and SoC for Li-Ion batteries

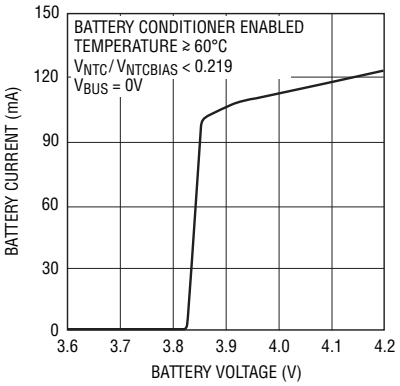

Figure 3. Battery discharge current vs voltage for the LTC4099 battery conditioning function

Battery Conditioner Avoids Conditions that Accelerate Aging

The LTC4099 has a built-in battery conditioner that can be enabled or disabled (default) via the I^2C interface. If the battery conditioner is enabled and the LTC4099 detects that the battery temperature is higher than ~60°C, it gently discharges the battery to minimize the effects of aging. The LTC4099 NTC temperature measurement is always on and available to monitor the battery temperature. This circuit is a micropower circuit, drawing only 50nA while still providing full functionality.

The amount of current used to discharge the battery follows the curve shown in Figure 3, reaching zero when the battery terminal voltage is ~3.85V. If the temperature of the battery pack drops below ~40°C and a source of energy is available, the LTC4099 once again charges the battery. Thus, the battery is protected from the worst-case battery aging conditions.

Conclusion

Although the aging of Li-Ion batteries cannot be stopped, the LTC4099's battery conditioner ensures maximum battery life by preventing the battery-killing conditions of simultaneous high voltage and high temperature. Further, the micropower, always on NTC monitoring circuit ensures that the battery is protected from life-threatening conditions at all times.

LTC2262, continued from page 25

lines used by the LTC2175, and allows it to be packaged in a space saving 7mm × 8mm QFN package.

The dual version of the LTC2262 is the LTC2268. It dissipates 299mW of total power, or 150mW per ADC. It also has LVDS serial output lines that reduce space, and allow the LTC2268 to be in a 6mm × 6mm QFN package.

The dual and quad versions of LTC2262 are available in 12- and 14-bit versions, in speed grades from 25Msps up to 125Msps. A complete list of the variant is shown in Table 1. Each device shares the excellent AC performance of the LTC2262, and features better than 90dB of channel-to-channel isolation. The serial outputs of the multiple channel parts mitigate the effect of digital feedback, producing a clean output spectrum. In sum, the performance of LTC2262 is not sacrificed when migrating into multiple channel parts.

Conclusion

The LTC2262 ultralow-power ADC simplifies design with a unique combination of features. Digital noise can be reduced by using DDR LVDS signaling, alternate bit polarity mode, or the data randomizer. The number of data lines needed to transmit 14 bits of data can be reduced to seven with DDR CMOS signaling, which simplifies layout. The LTC2262 is part of a pin-compatible family of 12-bit and 14-bit ADCs with sample rates from 25Msps to 150Msps, with power consumption ranging from 35mW at 25Msps up to 149mW at 150Msps while maintaining excellent AC performance characteristics.