Dual Hot Swap Controller in 3mm × 2mm DFN is Perfect for Backplane or Card Resident 1V-6V Applications

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Introduction

High availability electronics, such as those used in telecom, real-time transaction processing, hospitals and air traffic control systems, cannot afford any down time. These systems must continue to operate even as components are added or removed (hot swapped) for expansion, upgrades or maintenance. The Hot Swap[™] systems must be carefully designed to avoid burned PCB traces and power brownouts, which can result in system resets and data loss. The LTC4224 ensures dependable Hot Swap design while simplifying and shrinking total solution size. It does this by combining two feature-rich and independent Hot Swap controllers for 1V–6V applications in a 3mm × 2mm DFN package.

Figure 1 shows a functional block diagram of the LTC4224. The \overline{ON} pin is used to turn an external N-channel MOSFET on or off via the GATE pin. When commanded on, an internal charge pump pulls the GATE above the supply rail to fully enhance the MOSFET, reducing its series resistance to several m Ω . The LTC4224's ability to derive power from the higher

SENSE1 5.5V CHARGE PUMP Vcc **ψ**10μΑ ACL1 GATE1 25mV Vcci (\pm) GATE PULLDOWN 🕁 10μA ON1 ON. Д FCB1 Д 0.8V 0.81 V_{CC1} UV Vcc FAULT Vcc LOGIC CONTROL 🕁 10μA 2.4V V_{CC2} UV ON2 ON2 ECB2 Д \square 0.8V 0.8V CHARGE PUMP GATE PULLDOWN 🕁 10µA 25m\ V_{CC2} ACL2 GATE2 5.5V SENSE2

Figure 1. Functional block diagram of the LTC4224

of its two supplies allows it to control load voltages as low as 1V. Active current limiting (ACL) acts on the GATE when the load current causes more than 25mV of voltage drop across the sense resistor. An electronic circuit breaker (ECB) performs the role of a timekeeper, latching off the MOSFET in the event of a prolonged current overload.

Operation

Figure 2 shows the LTC4224 together with two N-channel MOSFETs and two sense resistors in a 5V backplane resident Hot Swap application. Initially, the \overline{ON} pin is pulled high in the absence of an add-in card and the GATE is held low, shutting off the MOSFET. When an add-in card is fully inserted into the backplane connector, the \overline{ON} pin is pulled low through the ground connections on the card connector. Spurious ON transitions can occur as the connectors mate. To prevent the MOSFET from turning on prematurely, the LTC4224 waits out these short term transitions with an internal 10ms debounce delay that restarts every time \overline{ON} transitions high.

To turn on the MOSFET, an internal charge pump sources 10µA to soft-start the GATE with a slew rate of 10µA/C_{ISS}, where C_{ISS} is the external MOSFET's gate capacitance. The start-up inrush current flowing into the load capacitor C_{OUT} is limited to $(C_{OUT}/C_{ISS}) \cdot 10\mu$ A. However, if the sense resistor voltage drop becomes too large, the inrush current is limited at 25mV/R_{SENSE} by the ACL. The ECB monitors the ACL, and if it detects that the current limit is still active 5ms after the GATE began ramping, the MOSFET latches off and FAULT pulls low. If



Figure 2. Hot Swap application for two add-in cards

 C_{OUT} cannot be sufficiently charged within this period, connect a capacitor from GATE to ground to lower the inrush current, as shown in Figure 3. With C_{GATE} , the inrush current is reduced to $(C_{OUT}/(C_{GATE} + C_{ISS})) \cdot 10\mu A.$ Adjusting C_{GATE} so that the inrush current stays below the ECB threshold prevents ECB faults with large load capacitors.

Overcurrent Protection

An important feature of the LTC4224 is its 25mV electronic circuit breaker (ECB) threshold with a 10% tolerance. This low ECB threshold allows the use of sense resistors with lower power ratings and hence smaller packages. In addition, the ECB threshold must not cut excessively into the supply voltage tolerance of downstream circuits. For instance, if the downstream circuits can tolerate at most a 5% variation on the 1V supply, the ECB threshold of an upstream Hot Swap controller must be significantly lower than 50mV.

To guard against damage to the external MOSFET from excessive power dissipation, active current limiting (ACL) regulates the gate to limit the sense resistor's voltage drop to about 25mV. To minimize external components, the current limit loop is compensated by the parasitic gate capacitance C_{ISS} of the MOSFET and remains stable for C_{ISS} values as low as 600pF. During ACL, the ECB activates and initiates an internal time-out period of 5ms. The waveform in Figure 4 shows the LTC4224 limiting the

current and subsequently latching off the MOSFET due to a mild current overload at the output lasting longer than 5ms. FAULT is pulled low; this could either instruct the microprocessor to take actions or light an LED to attract operator's attention.

In the event of a severe short-circuit, the current typically overshoots the current limit level significantly as the gate overdrive of the external MOSFET is large initially. The LTC4224 responds in less than 0.1µs to swiftly discharge the gate with a 100mA current sink. Figure 5 shows the LTC4224 bringing the current under control in less than 0.5µs when a 3.3V rail is shorted into a $10m\Omega$ load without any load capacitance. Also due to the fast ACL is the absence of gate undershoot, despite the speed at which the gate is discharged. The potential peak current is dictated by DC resistances along the power path (trace resistance + R_{DSON} of the MOSFET + R_{SENSE} + 10m Ω), while the path's parasitic inductance limits the current slew rate.

After the MOSFET latches off, the \overline{ON} pin must be pulled above 0.8V to reset the internal fault latch. Alternatively, recycle the supply below its UV level. The LTC4224-1 latches off after a fault, while the LTC4224-2 automatically tries to apply power four seconds after latching off.

Optical Transceiver Hot Swap Application

Optical transceivers such as those specified for the popular XENPAK/X2



Figure 3. A method to adjust inrush current by gate capacitor. R_G prevents parasitic self-oscillation in Q1



Figure 4. Active current limiting latches off the external MOSFET following a mild overcurrent



Figure 5. Fast current limit isolates severe short circuit fault in less than 0.5µs

Multi- Source Agreements (MSA) are employed in high speed networking routers as an interface between optical and electrical signals. The MSA mandates hot plug capability for transceiver modules, which are supplied with 5V, 3.3V and 1.xV.

A Hot Swap application based on the LTC4224 for the 5V and 3.3V rails is shown in Figure 6. Typically, a dedicated DC/DC converter controls the 1.xV rail and limits the inrush current for each module. As the optical module consumes relatively little power, a dual FET such as the FDS6911 is a good candidate for the power switches, saving cost and minimizing area. For the tiniest solution, sense resistors in a 0603 case size are selected. Figure 7 shows the full solution, which fits in the footprint of an SO8 package. In an application where all the three supply rails need to be hot swapped, three LTC4224s can be used to control the power to two modules, all in a solution no larger than the footprint of three SO8 packages.

5V/5A, 3.3V/5A Hot Swap Application

The LTC4224 can also reside on an add-in card as shown in Figure 8. There are no bulk capacitors on the inputs as these could draw large inrush current. In their place are the Transient Voltage Suppressors (Z1 and Z2) and RC Snubber networks. During current transients, inductive kickback can cause the input supply to swing beyond the absolute maximum (ABSMAX) rating of LTC4224's input pins without the TVS. By clamping the voltage, the TVS protects the LTC4224 from damage and an ABSMAX rating of 9V provides margin for the selection of the TVS. Snubbers damp the parasitic LC tanks to eliminate ringing on the input supplies. The Si7336ADP has been chosen for its SOA, 20V Gate-Source breakdown voltage and low R_{DSON}.

Conclusion

The LTC4224 simplifies the design of low voltage Hot Swap applications by integrating two Hot Swap controller and timing delay circuits in a tiny $3\text{mm} \times 2\text{mm}$ DFN package. Fast current limiting ensures that system disturbances are minimized during a severe overload and that faults are

quickly isolated. The LTC4224 offers a complete and robust Hot Swap solution for XENPAK/X2 optical modules that can be implemented in an SO8 footprint.



Figure 6. XENPAK/X2 optical module Hot Swap application



Figure 7. A compact PCB layout of the sense resistors, MOSFET and the LTC4224



Figure 8. A 5V and 3.3V card resident Hot Swap application