Low Offset 2-Wire Bus Buffer Provides Capacitance Buffering, Stuck Bus Recovery, and Tolerates High V_{OL}

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Introduction

High availability computing, networking and data storage systems employ system management buses such as I^2C or SMBus to monitor system health. These simple serial buses allow system controllers to monitor parameters such as temperature and voltage, read vital product information from individual cards, and make changes to the system, such as controlling fan speed. As these systems increase in complexity, several implementation issues arise with the system management bus.

First, each additional device on the bus adds a capacitive load. The bus capacitance of a large system makes meeting rise time specifications very difficult. While a strong pull-up resistor can reduce the rise time, the penalty is increased V_{OL} and decreased noise margin. Second, some devices that can communicate via I^2C or SMBus have a V_{OL} that is near or above the maximum allowed by the standards. Third, power cannot be cycled whenever a new card is added to the system. Finally, since any device can hold the bus low, each additional device increases the chance of a stuck bus caused by a single confused device.

The LTC4309 solves all of these problems by acting as a buffer between two physically separate 2-wire buses. The input side of the LTC4309, SDAIN and SCLIN, connects to one 2-wire bus (backplane), while the output side, SDAOUT and SCLOUT, connects to the other bus (I/O card). The LTC4309 provides bidirectional buffering, keeping the backplane and card capacitances isolated from each other.

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A large system can be broken into many smaller buses by inserting LTC4309s throughout the system, reducing the capacitance of each electrically isolated bus. The LTC4309's rise time accelerators help to further reduce the rise time.

The LTC4309 has connection circuitry that connects and passes a logic low even if the input voltage is above the bus specification V_{OL}. The low, pull-up independent offset reduces the impact to the V_{OL} of buffering the bus.

Since the LTC4309's SDA and SCL pins are high impedance when inactive or powered down, the LTC4309 can be inserted into a live bus without corrupting the bus. The LTC4309's capacitance buffering feature also isolates the capacitance of the card from the live bus during, and after, insertion.

Finally, the LTC4309's stuck bus detection circuitry can detect when a bus is stuck in a low condition and disconnect the stuck portion of the system while attempting to recover the stuck bus.

Circuit Operation

Start Up

A block diagram of the LTC4309 is shown in Figure 1. When the LTC4309 first receives power on its V_{CC} pin, either during power up or live insertion, it starts in an undervoltage lockout (UVLO) state, ignoring any activity on the SDA or SCL pins until V_{CC} rises above 2.0V (typ). This is to ensure that the LTC4309 does not try to function until it has enough voltage to do so. During this time, the 1V precharge circuitry is active and forces 1V through 100k nominal resistors to minimize the worst-case voltage differential these pins see at the moment of connection, thus minimizing the disturbance caused by the I/O card.

Once the LTC4309 comes out of UVLO and the ENABLE input is high, it monitors both the input and output sides for either a stop bit or bus idle condition to indicate the completion of data transactions. When transactions on both sides of the LTC4309 are complete, the back-to-back buffers shown in Figure 1 (referred to below as "connection circuitry") are activated, joining the SDA and SCL buses on the input side with those on the output. Once the connection is made, the READY pin is released, allowing it to pull up and signal that the connection is complete. READY remains high as long as the connection circuitry is active. If the ENABLE pin is grounded, the LTC4309 does not connect and I/Os remain in a high impedance state until ENABLE is pulled high.

Connection Circuitry

When the connection circuitry is activated, the functionality of the SDAIN and SDAOUT pins, as well as SCLIN and SCLOUT, are identical. When an external device pulls any SDA or SCL pin below a threshold of 1.65V (for $V_{CC} > 2.9V$) or 1.35V (for $V_{CC} < 2.9V$) the LTC4309 detects a low and pulls the other side down to a voltage that is 60mV above the forced voltage. This low offset is practically independent of bus voltage level and pull-up resistance. The LTC4309 remains connected until the input and output are above 0.6V and it senses a rising edge on both the input and output or until one side is above the $0.45 \cdot V_{CC}$ connection threshold. The LTC4309's connection circuitry ensures that the input and output enter a logic high state only when all devices on both sides of the LTC4309 have released the bus and the pull-ups have pulled the bus high. This important feature ensures that clock stretching, clock arbitration and the acknowledge protocol always work, regardless of how the devices in the system are connected to the LTC4309.

Another key feature of the connection circuitry is that, while it joins the two buses together, it still maintains electrical isolation between them, thus providing capacitance buffering for both sides. With the LTC4309's low offset and tolerance to devices having high V_{OL}, multiple devices can be cascaded on a single bus. This allows larger systems to be divided into many smaller, less capacitive and therefore faster buses. The LTC4309 is capable of driving capacitive loads ranging from 0pF to more than 1000pF on all of its data and clock pins.

Stuck Bus Detection and Recovery

Slave devices on a bus use the clock signal to sample the data. Occasionally, devices become confused and get stuck in a low state, causing a "stuck"
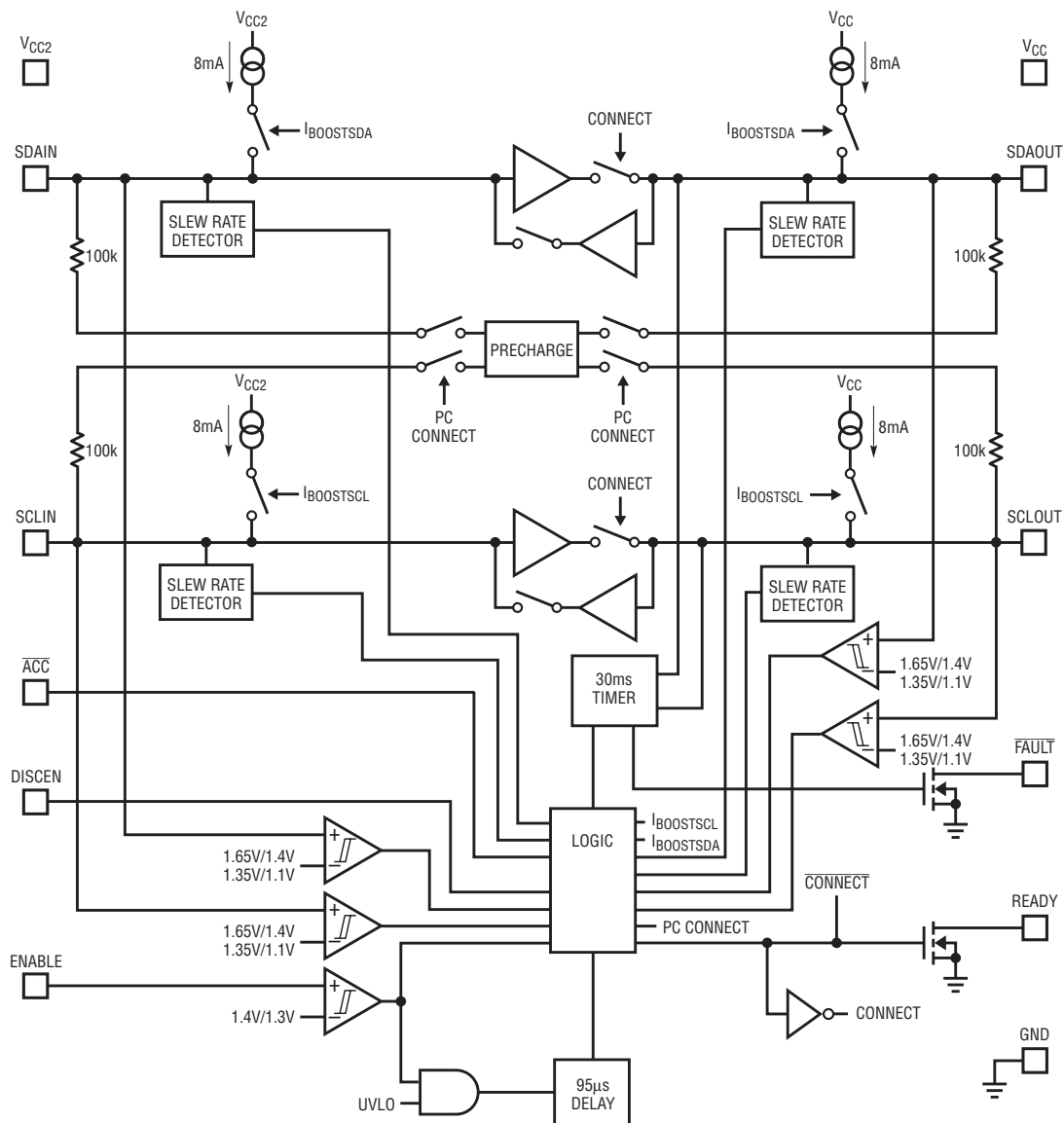

Figure 1. Block diagram of LTC4309. The input side of the LTC4309, SDAIN and SCLIN, connects to one 2-wire bus (backplane), while the output side, SDAOUT and SCLOUT, connects to the other bus (I/O card). The LTC4309 provides bidirectional buffering, keeping the backplane and card capacitances isolated from each other.

bus. The LTC4309 monitors both the data and clock buses independently for a stuck bus condition. If either data or clock is in a low state for more than 30ms, the LTC4309 determines that the bus is "stuck." The LTC4309 signals a fault condition by pulling the FAULT and READY pins low and disables the connection circuitry, disconnecting the stuck bus and freeing the portion of the bus that is not stuck. At this time, the LTC4309 attempts to free the stuck bus by generating up to 16 clock pulses on SCLOUT. Once the 16 pulses are completed, or the clock pulses terminate due to the bus becoming unstuck, a stop bit is generated to clear the bus for further communication. If a master wants to force reconnection of the bus after the LTC4309 has disconnected the bus due to a fault condition, the master can pull the ENABLE pin low and immediately high again. This resets the 30ms timer and forces the LTC4309 to reconnect.

The LTC4309's stuck bus recovery feature is illustrated in Figure 2. After SDAOUT has been held low for 30ms,

Figure 2. The stuck bus recovery feature of the LTC4309 disconnects stuck buses and uses auto clocking to recover the stuck bus.

the LTC4309 detects the stuck bus. The LTC4309 pulls the FAULT pin low, and releases the SDAIN bus. The SCLOUT pin is then toggled at 8.5kHz in an attempt to free the bus. In this example, after 11 clock edges the bus becomes unstuck and the FAULT pin is released. Note that SDAOUT temporarily goes high at the same time that FAULT goes high, but this is not visible in the figure due to the time scale and due to the LTC4309 quickly pulling SDAOUT back low so that it can generate a Stop Bit on the

bus. The LTC4309 holds SDAOUT low for 125µs, then releases SDAOUT to generate the Stop Bit.

If automatic disconnection is not desired, this feature can be disabled by connecting the DISCEN pin to GND. The LTC4309 still monitors both sides for a stuck bus condition and pulls FAULT low if a fault occurs, but does not disconnect the bus or attempt to free the stuck bus. A master can disconnect the stuck bus manually by pulling the LTC4309's ENABLE pin low. This forces the connection
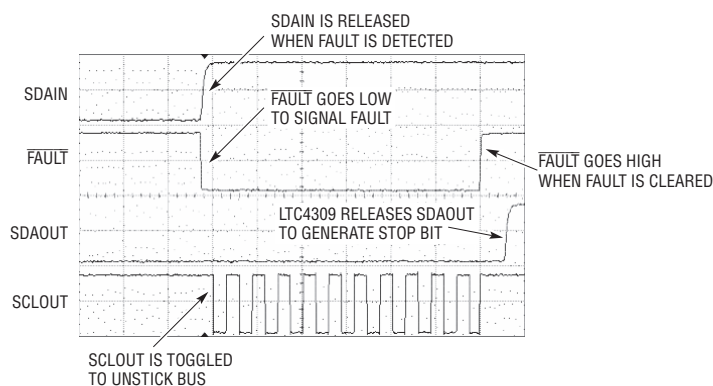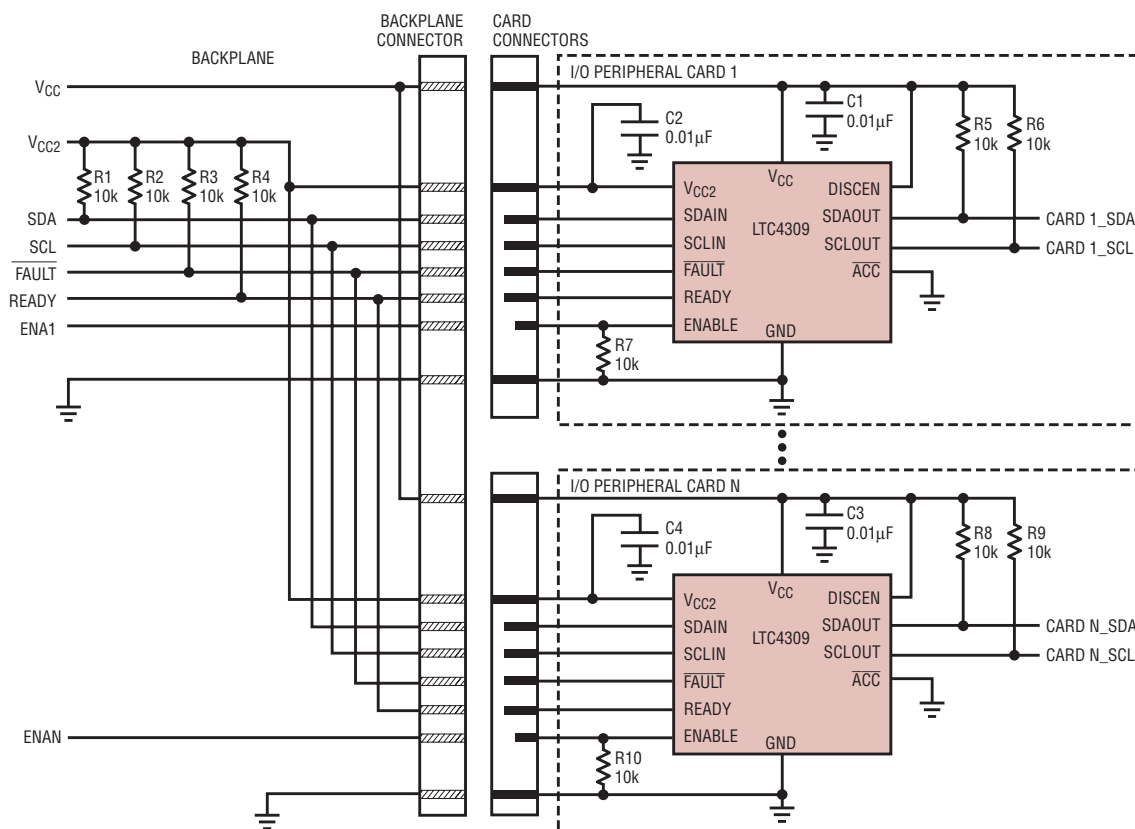

Figure 3. The LTC4309 in a live insertion and capacitance buffering application
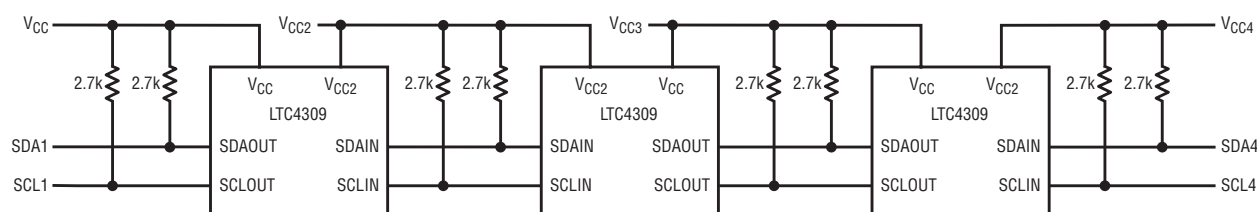
Figure 4. The LTC4309 provides level translating, and allows cascading of multiple buffers while meeting system V_{OL} requirements.

circuitry to disconnect the inputs from the outputs, and put the I/O pins in a high impedance state. Once the master has cleared the stuck bus, the LTC4309 ENABLE pin can be pulled high. When the bus is idle, the LTC4309 reconnects the input to the output as described previously.

Rise Time Accelerators

The $\overline{ACC}$ pin controls the state of the rise time accelerators. If the $\overline{ACC}$ pin is tied to GND, all four accelerators are activated. To disable the input side accelerators only, tie the $\overline{ACC}$ and V_{CC2} pins to GND. Connect the $\overline{ACC}$ pin to V_{CC} to disable all four rise time accelerators. When activated, the rise time accelerators switch in 8mA of slew limited pull-up current at V_{CC} = 3.3V during bus rising edges to quickly slew the SDA and SCL lines once their DC voltages exceed 0.8V and the initial rise rate on the pin exceeds 0.8V/μs. The slew limiting is achieved by monitoring the rising edge; if the edge is rising faster than 1V/10ns, the pull-up current is reduced. This helps prevent signal integrity issues in lightly loaded systems where a strong pull-up could make the rising edge fast enough to create transmission line reflections on the bus.

Live Insertion and Removal, and Capacitance Buffering Application

The application shown in Figure 3 highlights the live insertion/removal and the capacitance buffering features of the LTC4309. Assuming that a staggered connector is available, make ground, V_{CC} and V_{CC2} the longest pins to guarantee that SDAIN and SCLIN receive the 1V pre-charge voltage before they connect. Make SDAIN and SCLIN medium length pins to ensure that they are firmly connected

while ENABLE is low. Make ENABLE the shortest pin and connect a weak resistor from ENABLE to ground on the I/O card. This ensures that the LTC4309 remains in a high impedance state while SDAIN and SCLIN are making connection during live insertion. During live removal, having ENABLE disconnect first ensures that the LTC4309 enters a high impedance state in a controlled manner before SDAIN and SCLIN disconnect.

Note that if an I/O card were plugged directly into the backplane, the card capacitance would add directly to the backplane capacitance, making rise and fall time requirements difficult to meet. Inserting a LTC4309 on the edge of the card, however, isolates the card capacitance from the backplane. The LTC4309 drives the capacitance of everything on the card, and the backplane must drive only the capacitance of the LTC4309. As more I/O cards are added and the system grows, placing a LTC4309 on the edge of each card breaks what would be one large, unmanageable bus into several manageable segments, while still allowing all segments to be active at the same time. If breaking the bus up further is desired, the LTC4309's low offset and high V_{OL} tolerance allows cascading of multiple devices. Moreover, the LTC4309's rise time accelerators provide strong pull-up currents during bus rising edges, so that even heavily loaded bus lines meet system rise time requirements with ease.

Level Translator and Cascading Applications

The LTC4309's very low offset, typically 60mV, allows cascading of multiple devices while still meeting V_{OL} specifications. Figure 4 illustrates an application where three LTC4309s

have been used to break a bus into four isolated buses. The total offset of the cascaded devices is approximately 180mV. This feature can be used in conjunction with the level translating feature of the LTC4309 and each isolated section of the bus can operate off a different supply voltage. The LTC4309 functions for voltages ranging from 2.3V to 5.5V on V_{CC} and 1.8V to 5.5V on V_{CC2}.

Simplified 8-Pin Option in the LTC4307

The LTC4307 is a simplified 8-pin version of the LTC4309. For the LTC4307, the DISCEN, $\overline{ACC}$, $\overline{FAULT}$ and V_{CC2} pins are removed. The rise time accelerators and stuck bus recovery are always enabled. Since there is no $\overline{FAULT}$ pin, the READY pin should be monitored to determine if a fault condition occurs.

Conclusion

The LTC4309 low offset buffer allows I/O cards to be hot-plugged into live systems and breaks one large capacitive bus into several smaller ones, while still passing the SDA and SCL signals to every device in the system. The low, pull-up independent offset allows cascading of multiple devices, breaking the bus into smaller, less capacitive sections. Slew limited rise time accelerators further decrease the rise time and allow the bus to operate at higher frequencies, or with better data integrity. Stuck bus recovery helps maintain system integrity by detecting and clearing stuck buses. The LTC4309's tolerance to high V_{OL} allows capacitance buffering on buses with other devices that may not meet V_{OL} specifications. With these features, the LTC4309 simplifies the design process of complex 2-wire bus systems. ⌐