Negative Voltage Hot Swap Controller with 10-Bit ADC and I^{2}C Monitoring

by Zhizhong Hou

Introduction

High availability –48V power systems, such as telecom and AdvancedTCA systems, allow for circuit board upgrade and replacement on a live powered backplane. The primary role of a Hot Swap controller is to make this possible by limiting potentially large inrush currents, which can cause damage to the hot swapped board or create disturbances on the backplane. Traditionally, –48V Hot Swap controllers operate autonomously—the Hot Swap controller shuts down an abnormally operating board before the host processor knows why. This simplifies system design, but gives little in the way of diagnostic support to the host.

A far more robust system would use the Hot Swap controller to communicate the conditions of the board to the host processor, and let the host processor take action. To this end, the LTC4261 integrates a –48V Hot Swap controller, 10-bit ADC monitoring and I^{2}C/SMBus communication. It monitors the real-time board parameters such as current and voltages and communicates the data to the host.

Features

Figure 1 shows a simplified block diagram of the LTC4261. Power is derived from the –48V RTN using an external dropping resistor connected to the V_{IN} pin. An internal shunt regulator clamps the voltage at V_{IN} to 11.2V above V_{EE} (chip ground). This floating architecture allows a wide operating voltage range. The device also provides a 5V linear-regulated voltage at the $INTV_{CC}$ pin that can source current up to 20mA for driving external circuits.

Using an external N-channel pass transistor, the negative Hot Swap circuit of the LTC4261 allows a board to be safely inserted and removed from a live –48V backplane. The device features a new inrush control technique

Figure 1. Simplified block diagram of LTC4261

that minimizes stresses on the pass transistor in all operating conditions. Turning the device on or off can be either autonomous or controlled by a host processor through the I^{2}C interface. Auto-retry following a fault is programmable and fully controlled by the host. Configurations of the device are stored in the internal registers as shown in Table 1.

The LTC4261 continuously monitors and registers board status and fault conditions. With an onboard 10-bit ADC and 3-channel multiplexer, it accurately measures real-time board current (through the voltage across the sense resistor) and two external voltages. The data are stored in the ADC registers (see Table 1). When polled by a host processor, the LTC4261 reports the ADC data along with the status and fault information using the I^{2}C interface. The real-time board current and voltages provides a means for the host to detect any early warn-

ing signal and to flag the board for maintenance before it fails. With the $\overline{ALERT}$ pin, the LTC4261 interrupts the host for specific fault conditions, when configured to do so.

One unique feature of the LTC4261 is that the I^{2}C interface can be easily configured using the address pins (ADR1 and ADR0) into a single-wire broadcast mode that only uses a single I^{2}C signal, SDAO, to report the ADC data and fault information. This mode simplifies the interface and saves component cost by eliminating two optoisolators.

The LTC4261 has additional features to sequence two power good outputs, detect insertion of a board and turn off the pass transistor if an external supply monitor fails to indicate power good within a timeout period. Using the PGIO and $\overline{FLTIN}$ pins along with the ADC, the device can detect a specific fuse that is open for up to four fuses.
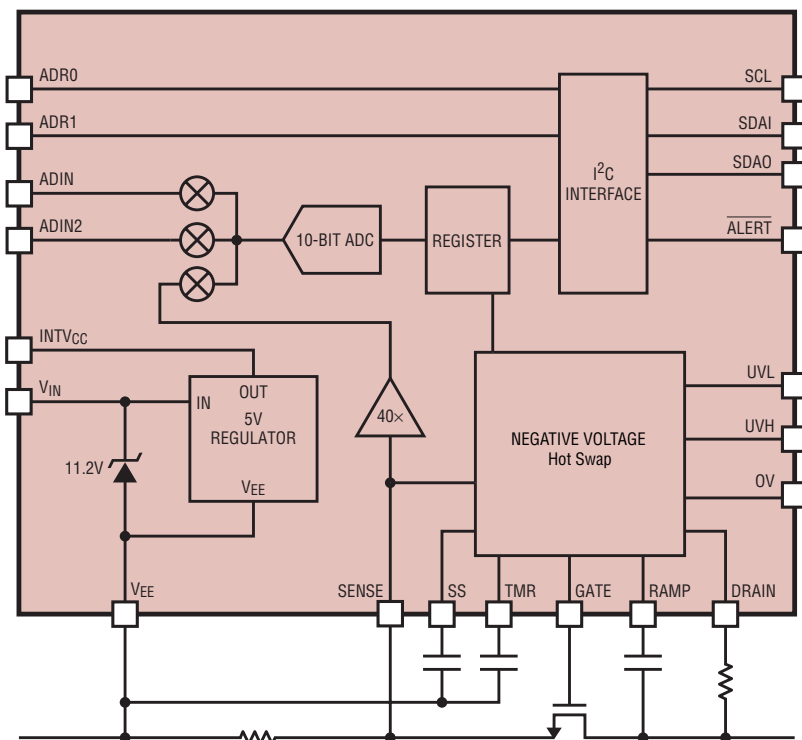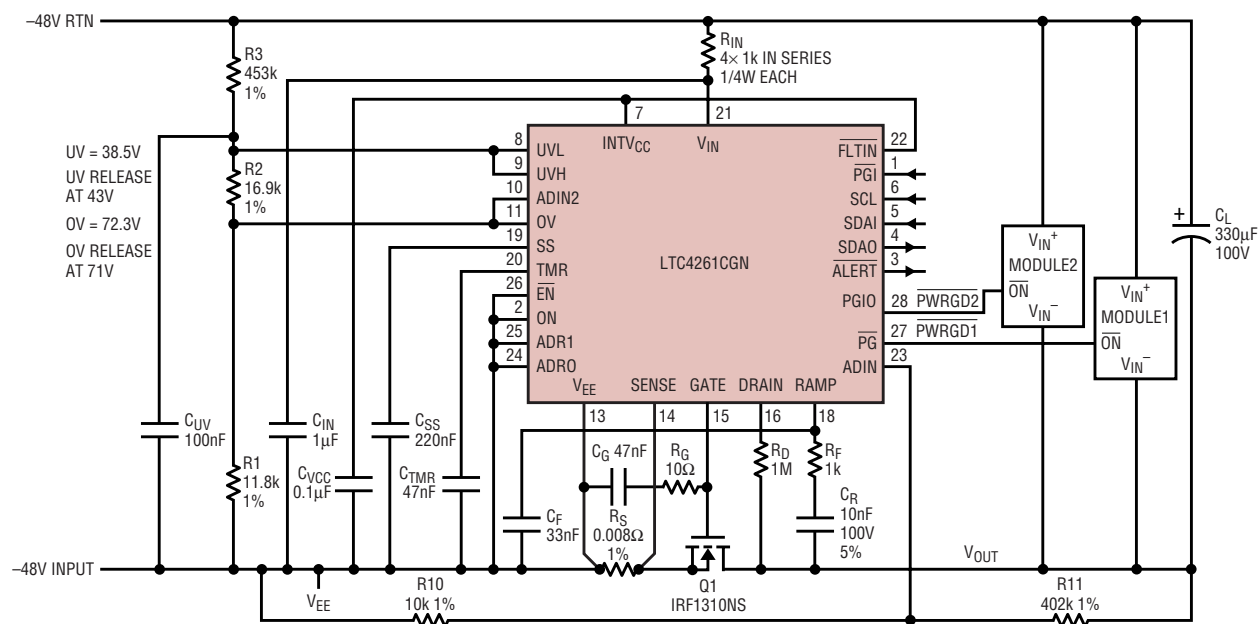
Figure 2. A –48V/200W Hot Swap controller (5.6A current limit, 0.66A inrush) using LTC4261 with current, input voltage and V_{DS} monitoring

10-Bit ADC Provides Accurate Measurement of Real-Time Board Current and Voltages

Quantitative monitoring of real-time board level voltage and current (and thus power) provides significant benefits in high availability systems. Real time operating data can be compared to budgeted or historical data to detect whether a circuit board is using its allotted power or if is operating abnormally. By issuing early warning to system management, an abnormally operating board can be flagged for service even before it fails. This feature greatly improves the reliability of high availability systems.

The LTC4261 includes a 10-bit ADC that accurately measure voltages at the SENSE, ADIN2 and ADIN pins, all referred to chip ground (V_{EE}). With a 2.56V full scale and 2.5mV resolution, the ADIN and ADIN2 pins are uncommitted inputs that allow monitoring of any external voltages. With the sense resistor, the SENSE pin voltage is used to measure current flowing through the pass transistor. This voltage is internally amplified by 40 times resulting in a 64mV full scale and 62.5µV resolution. The digital codes of the three voltages after each conversion are stored in corresponding ADC registers (see Table 1) and updated at a frequency of 7.3Hz. Setting the test mode bit in the CONTROL register halts the updating so that software testing can be performed by writing to and reading from the registers.

An example of using the ADC monitoring is shown in Figure 2, where current, input voltage and V_{DS} of the pass transistor are measured at the SENSE, ADIN2 and ADIN pins, respectively. The latter two voltages can be used to derive the output voltage referred to RTN. Another application of the ADC monitoring is to detect an open fuse in a multi-feed system, which is detailed later in this article.

Independently Adjustable Inrush and Overcurrent Limits Minimize Stress on Pass Transistor

A typical –48V/200W Hot Swap application using the LTC4261 is shown in Figure 2. Initial turn-on of pass transistor Q1 is autonomous but I²C can take over the control after power-up. To protect the pass transistor from overstress, the LTC4261 independently controls inrush current

Table 1. LTC4261 registers

Register	Read/ Write	Description
STATUS	R	Provides pass transistor (on/off), $\overline{EN}$ (high/low) and PGIO input conditions. Also lists five fault present conditions.
FAULT	R/W	Latches overcurrent, overvoltage, undervoltage, power bad, FETshort faults and $\overline{EN}$ changed state. Also logs $\overline{FLTIN}$ and PGIO inputs.
ALERT	R/W	Enables which faults interrupt the host using the $\overline{ALERT}$ pin. Defaults not to alert on faults at power-up.
CONTROL	R/W	Controls on or off of the pass transistor and whether the part auto-retries or latches off after a fault. Also configures the PGIO pin and enables ADC register test mode.
SENSE	R/W	ADC data for the SENSE voltage measurement
ADIN2/OV	R/W	ADC data for the ADIN2 (on TSSOP) or OV (on QFN) pin voltage measurement
ADIN	R/W	ADC data for the ADIN pin voltage measurement
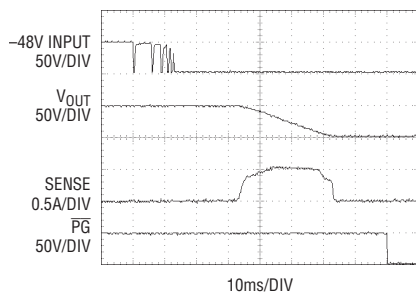
Figure 3. The LTC4261 start-up behavior

during power-up and overcurrent upon a short circuit. As indicated in Figure 2, the current limit and circuit breaker threshold is set to 5.6A by the sense resistor R_S, while the inrush is set to a much lower level (0.66A) by controlling the ramp rate of V_{OUT} with an external capacitor C_R connected between V_{OUT} and the RAMP pin. The operation theory and the benefits of this inrush and overcurrent control technique are demonstrated below.

Following a start-up debounce delay, the turn-on sequence of the LTC4261 starts with charging the SS pin up with a 10µA current. The SS voltage (V_{SS}) is converted to a GATE pull-up current. When the GATE voltage reaches the threshold voltage of the pass transistor Q1, the inrush starts to flow through Q1. The output voltage (V_{OUT}) begins to move and C_R begins to

charge. This draws a current from the RAMP pin that flows through C_R and causes the GATE current to drop to 0. The RAMP pin is regulated at 1.1V so the inrush is set by the ramp rate of V_{OUT}, which leads to:

$$I_{INRUSH} = 20µA \frac{C_L}{C_R}$$

The slew rate of V_{SS} determines dI/dt of the inrush current. Figure 3 shows the start-up behavior of the LTC4261.

The LTC4261 provides 2-level overcurrent protection: an active current limit (ACL) amplifier that also serves as a circuit breaker comparator with a threshold of 50mV±10%, and a fast pull down comparator with a threshold of 150mV. In the event of an output short or a fast input step, when V_{SENSE} exceeds 150mV, the fast pull down comparator immediately brings the GATE down with a 110mA current. Once V_{SENSE} falls back below 150mV, the ACL starts to servo the GATE and maintains a constant output current of 50mV/R_S. If the short-circuit condition lasts longer than the circuit breaker delay of 530µs, the pass transistor is turned off and an overcurrent fault is registered. The device defaults to latch off upon an overcurrent fault but can

be configured to automatically re-try after a cooling delay. Figure 4 illustrates the response of the LTC4261 to the short-circuit condition. In the case of an input step, the inrush control circuit takes over following the fast GATE pull-down and the current limit loop is disengaged before the circuit breaker timer expires. The device then operates similarly to the start-up, only with a difference that the current through the pass transistor is now a sum of inrush and load current.

By decoupling start-up inrush from the current limit/circuit breaker threshold, the LTC4261 makes it possible to optimize the safe operating area (SOA) of the pass transistor in all operating conditions. The short circuit breaker timer substantially reduces the stress on the pass transistor in a short-circuit condition. Startup and input step typically impose the greatest stress on the pass transistor. Setting the inrush current much smaller than the current limit relieves the SOA requirement during start-up and input step. This allows using smaller pass transistors for large load applications, making selection of pass transistors much easier. Using the dedicated RAMP pin that is regulated separately from GATE
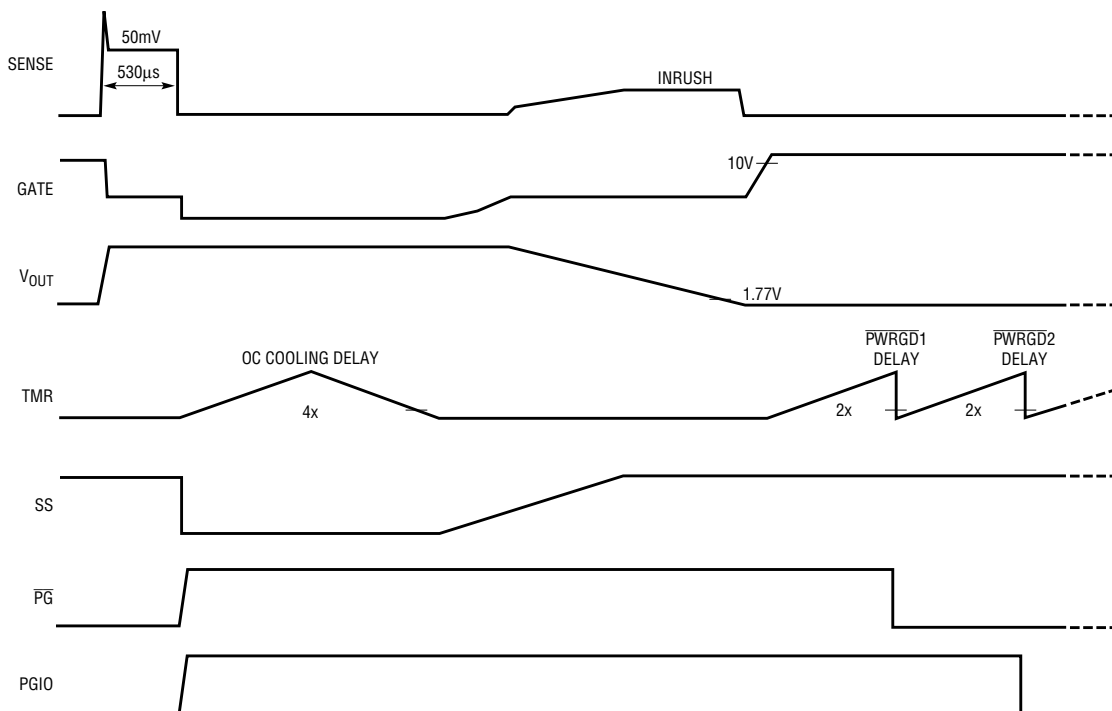
Figure 4. Response of the LTC4261 to overcurrent fault in auto-retry mode

for inrush control, the LTC4261 does not require a large capacitor between GATE and V_{EE} that relates to C_R, so the turn-off of the pass transistor upon short-circuit can be fast even for large load applications.

Adjustable Undervoltage Comparator Offers Both Precision and Flexibility

The LTC4261 provides two UV pins (UVH and UVL) that can be used to precisely set the undervoltage threshold and hysteresis. Each of the two pins has an accurate threshold: 2.56V for UVH rising (turn-on) and 2.291V for UVL falling (turn-off), and both pins have a small, built-in hysteresis of 15mV. With either a rising or falling input voltage, both the UVH and UVL pins have to cross their thresholds for the comparator output to change state. If both pins fall below their thresholds, an undervoltage fault is registered.

The ratio between the UVH and the UVL thresholds is designed to precisely set 43V turn-on and 38.5V turn-off UV thresholds popular in telecom applications with minimum external components, by tying UVH and UVL together. Along with the OV pin (with a threshold of 1.77V and a hysteresis of 37.5mV), the 3-resistor divider shown in Figure 5a sets an accurate operating range of 43V to

71V with UV turn-off at 38.5V and OV turn-off at 72.3V.

The UV levels can be adjusted by connecting a resistor R_H between the UVH and UVL pins, as illustrated in Figure 5b (UVL tap above UVH tap for a larger hysteresis) and Figure 5c (UVL tap below UVH tap for a smaller hysteresis). In the latter case, the LTC4261 does not allow hysteresis to drop to zero or negative values if a larger R_H is used. Instead, hysteresis reaches a guaranteed minimum (15mV typical) and increases with increasing R_H, preventing comparator oscillation.
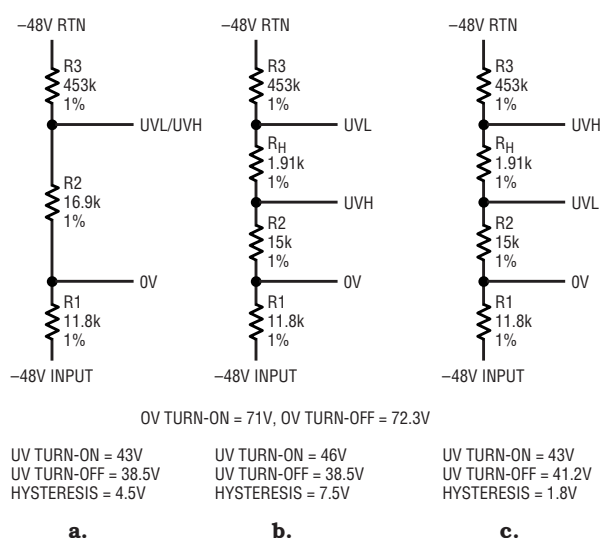

Figure 5. Adjustment of undervoltage thresholds and hysteresis

OV TURN-ON = 71V, OV TURN-OFF = 72.3V

a.	b.	c.
UV TURN-ON = 43V	UV TURN-ON = 46V	UV TURN-ON = 43V
UV TURN-OFF = 38.5V	UV TURN-OFF = 38.5V	UV TURN-OFF = 41.2V
HYSTERESIS = 4.5V	HYSTERESIS = 7.5V	HYSTERESIS = 1.8V

Versatile On/Off Control

The LTC4261 provides various methods of on/off control using the ON, $\overline{EN}$, UVH/UVL/OV, PGIO or $\overline{FLTIN}$ pins along with the I²C interface. Turning on or off the pass transistor can be either autonomous or controlled by the system host through the I²C interface. Furthermore, the LTC4261 may reside on either the removable board or on the backplane.

Even when operating autonomously, the host can exercise control over the GATE output through I²C, although $\overline{EN}$ and ON could subsequently override conditions set by I²C

a. Optoisolator control

b. Logic control

c. Contact debounce delay upon insertion for use with an ejector switch or loop-through style connection sense

d. Short pin connection sense to RTN

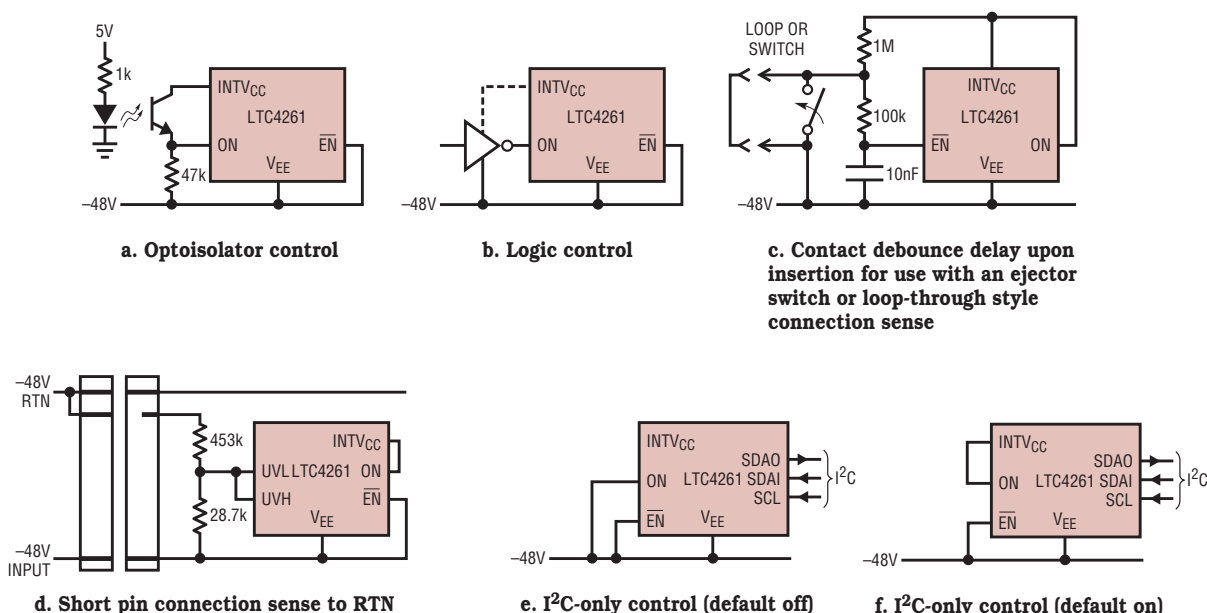**e. I²C-only control (default off)**

f. I²C-only control (default on)

Figure 6. The LTC4261 provides versatile on/off control

command. Card insertion/extraction can be conveniently detected with the $\overline{EN}$-changes-state bit in the FAULT register. After power-up, UV, OV and other fault conditions seize control as needed to turn off the GATE output, regardless of the state of $\overline{EN}$, ON or the I²C port.

Auto-retry following the faults can be enabled or disabled by the host at any time and the configurations are stored in the CONTROL register (Table 1). Although PGIO (when configured as an input) and $\overline{FLTIN}$ control nothing directly, they are useful for I²C monitoring of connection sense or other important signals. The host can then use the information detected by these two pins to take action.

Figure 6 shows some examples for on/off control using the LTC4261. The circuits in Figures 6a to 6d work equally well in both backplane and board resident applications. Circuits in Figures 6e and 6f are for I²C-only control.

Broadcast Mode Saves Cost and Space

To facilitate I²C communication between the LTC4261 and a system host that are isolated from each other, the SDA signal is split into SDAI and SDAO. Separate pins allow the device to drive optoisolators with a minimum number of external components. Still, three optoisolators (two for inputs on SCL and SDAI, and one for output on SDAO) are needed for typical I²C operations. To further reduce component count, the LTC4261 provides a special single-wire mode that only uses the SDAO pin to continuously transmit ADC data and fault information (Figure 7). This simple communication mode saves component cost and board space by eliminating two optoisolators and is useful for applications where only monitoring is needed.

The single-wire broadcast mode is simply enabled by tying the ADR1 pin to INTV$_{CC}$ and the ADR0 pin to V$_{EE}$ (Figure 7). At the end of conversion of each ADC channel, a serial data stream is sent out to SDAO with a fixed data rate of 15.3kHz ±20% in the format shown in Figure 8. The data stream

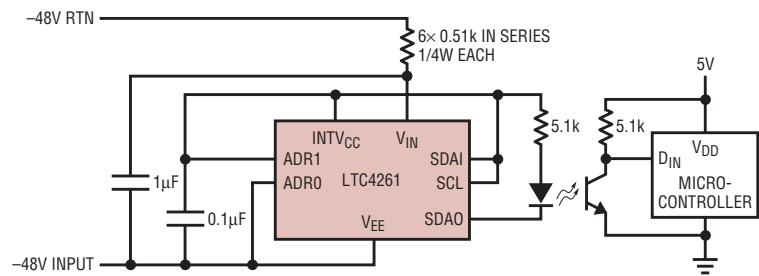consists of a start bit (STAT), a dummy bit (DMY), two bits of ADC channel labeling (CH1 and CH0), ten bits of ADC data (ADC9:0), three fault bits (OC, UV, OV) and a parity bit (PRTY). The data are encoded with an internal clock in a way similar to Manchester encoding that can be easily decoded by a microcontroller.

Figure 7. The LTC4261 in single-wire broadcast mode reports ADC data and fault information using a single optoisolator and the SDAO signal.
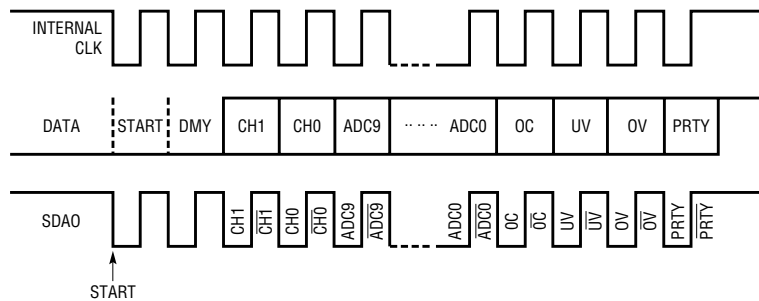

Figure 8. Data format of the single-wire broadcast mode

Which of the Four Fuses is Open?

Some high availability systems such as AdvancedTCA require dual feeds on both –48V and RTN lines and a fuse on each feed, resulting in four fuses. Since the plug-in card is designed to operate without interruption even if one of the fuses is open, it can be dif-
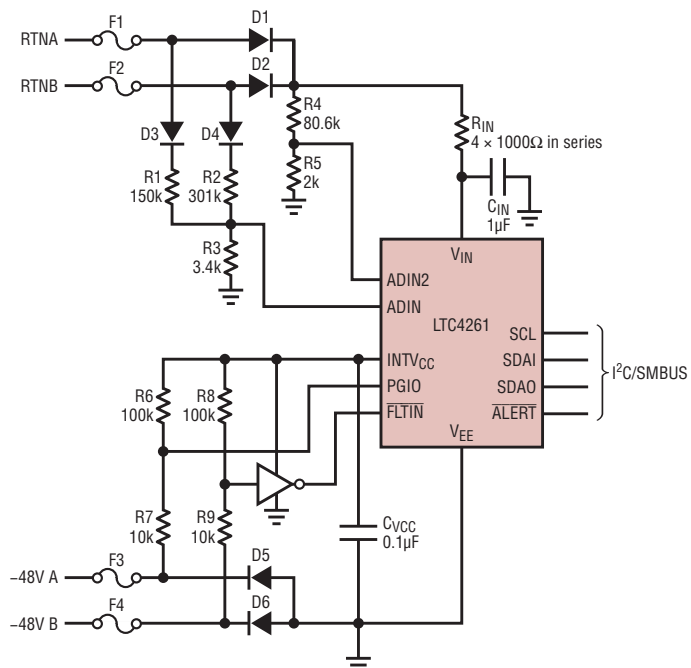

Figure 9. LTC4261 makes it possible to determine which of the four fuses is open in an AdvancedTCA system.

Table 2. The voltages at ADIN and ADIN2 (referred to V_{EE}) indicate which RTN fuse is open in the 4-fuse monitor in Figure 9

$V_{ADIN} = V_{ADIN2} = 0V$	Both F1 and F2 are open
$0.25 \bullet V_{ADIN2} \leq V_{ADIN} < 0.7 \bullet V_{ADIN2}$	F1 is open
$0.7 \bullet V_{ADIN2} \leq V_{ADIN} < 1.1 \bullet V_{ADIN2}$	F2 is open
$V_{ADIN} > 1.1 \bullet V_{ADIN2}$	Normal Operation

ficult, without direct fuse monitoring, to detect a single open fuse.

The integrated ADC, I^{2}C monitoring, and general-purpose pins of the LTC4261 make it possible to monitor the individual fuses, as shown in Figure 9. Fuses on the RTN side are sensed using resistors R1, R2 and R3 with the output measured by the ADC at the ADIN pin. At the same time, the input voltage after the ORing diodes is sensed using R4 and R5 and measured at the ADIN2 pin. Diodes D3 and D4 are used to compensate the ORing

diodes. Table 2 shows how the voltages at ADIN and ADIN2 indicate which fuse on the RTN side is open.

Using the input voltage as the reference ensures valid detection in the full operating range.

Fuse monitoring on the –48V side is more straightforward using the INTV$_{CC}$ pin along with two logic input pins, PGIO (when configured as input) and $\overline{FLTIN}$ as shown in Figure 9. Fuse F3 is sensed with R6 and R7 at PGIO, and fuse F4 is sensed with R8 and R9 at $\overline{FLTIN}$ with inverted input. If F3

is open, PGIO is pulled high and the PGIO input bit in the FAULT register is set. If F4 is open, $\overline{FLTIN}$ is pulled low and the FLTIN bit is set. In the latter case, if the corresponding bit in the $\overline{ALERT}$ register is also set, the LTC4261 interrupts the host using the $\overline{ALERT}$ pin.

Conclusion

The LTC4261 is a full-featured, intelligent Hot Swap controller that enhances the reliability and durability of high availability –48V power systems. The internal 10-bit ADC, I^{2}C/SMBus and registers make it easy to monitor faults and real-time power and communicate with the system host. Its unique inrush and overcurrent control technique minimizes stresses on the pass transistor in all operating conditions. ⏗

nection between SDAIN and SDAOUT, and SCLIN and SCLOUT is broken, isolating the problem device from the bus. $\overline{FAULT}$ pulls low indicating a stuck bus. At this time it is assumed that the MCU and the device it is communicating with are out of sync. The MCU sent out all of the clocks necessary for the transaction, but the device is still in the middle of the transaction. The device is waiting for more clocks to finish putting its data on the bus, and the last bit it put on the bus happened to be a low, hence it holds the bus low until it gets more clocks (bus is stuck). Because the connection is broken, the problem device is now isolated from the I^{2}C bus, and the rest of the system is free to resume normal operation.

After the connection is broken, the LTC4304 automatically generates up to 16 clock pulses at 8.5kHz on SCLOUT, enough clocks to clear the internal register on the problem device. The device could be cleared with one or any number of clocks (up to 16) depending on how the fault occurred. At any time, if SDAOUT and SCLOUT go high, $\overline{FAULT}$ is released to go high and the automatic clocking is stopped, and a connection is automatically enabled.

When the slave that was stuck sees a START bit after connection, it will abort the stalled communication and reset. The fault is cleared independently of the MCU. If the fault cannot be cleared, the offending circuit remains isolated from the system. Figure 2 shows an example of a stuck bus being resolved with automatic clocking.

Supply Independence and Level Translation

The LTC4304 can be the bridge between a backplane operating at one voltage and a card operating at a different voltage. Figure 3 shows some typical configurations. Notice that V$_{CC}$, the pull-up voltage on SDAIN and SCLIN and the pull-up on SDAOUT and SCLOUT are independent of each other.

The rise time accelerators must be disabled when the bus pull-up voltage is lower than V$_{CC}$. Figure 3a shows a situation where the V$_{CC}$ is higher than the pull-up voltage on SDAIN and SCLIN. In this case $\overline{ACC}$ must be floating, disabling the rise time accelerators on the inputs only. In Figure 3b, V$_{CC}$ is equal to the output side pull-up voltage, and less than input side pull-up voltage. $\overline{ACC}$ is connected to GND to

enable all four rise time accelerators. Finally, in Figure 3c, V$_{CC}$ is greater than the pull-up voltages of both sides. $\overline{ACC}$ is connected to V$_{CC}$ to disable all four accelerators.

Conclusion

The LTC4304 is a multifunctional device with an impressive number of features designed to increase the reliability of an I^{2}C bus. The flexible architecture allows the LTC4304 to be configured into almost any system. The LTC4304 isolates and resolves stuck buses independently of the MCU. Capacitance buffering, level translation, Hot Swap features and ±15kV human body ESD protection make the LTC4304 an ideal solution for any I^{2}C application.

The LTC4304 is offered in small 10 pin MSOP and DFN (3mm × 3mm) packages.

A feature-reduced version of the LTC4304 is also available. The LTC4303 provides all of the functionality of the LTC4304 with the exception of the $\overline{FAULT}$ output flag and $\overline{ACC}$ control pin. The LTC4303 is a drop in replacement for the LTC4300A-1 and its rise time accelerators are permanently enabled. ⏗