# I²C Bus Buffer Resolves Stuck Buses, Eliminates Heavy Load Limitations and Provides Level Translation

by George Humphrey

## Introduction

The I²C bus is a 2-wire bidirectional communications bus primarily used for system configuration and monitoring. A bus master, typically a microcontroller unit (MCU), polls system components for information such as supply voltage and temperature, Vital Product Data (VPD) from memories on removable cards, and system configuration. The master can also use the bus to reconfigure the system through general purpose input/output ports (GPIOs) and other programmable devices. Large-scale telecommunication and data storage systems are divided up into several peripheral cards. Each card plugs on to the I²C bus and communicates its system information to the MCU through the back plane.

Certain considerations must be addressed to ensure a high level of reliability when designing a system using the I²C bus. Primarily, systems must provide protection against a hung or stuck bus. If for any reason the bus is stuck low, there is the potential to bring the entire system down. Another consideration is dealing with heavy capacitive loads on the bus. The I²C standard specifies a 400pF limit on the bus. With systems becoming larger, this specification becomes problematic because of so many devices connected directly to the bus. Systems also need to be robust, allowing cards to

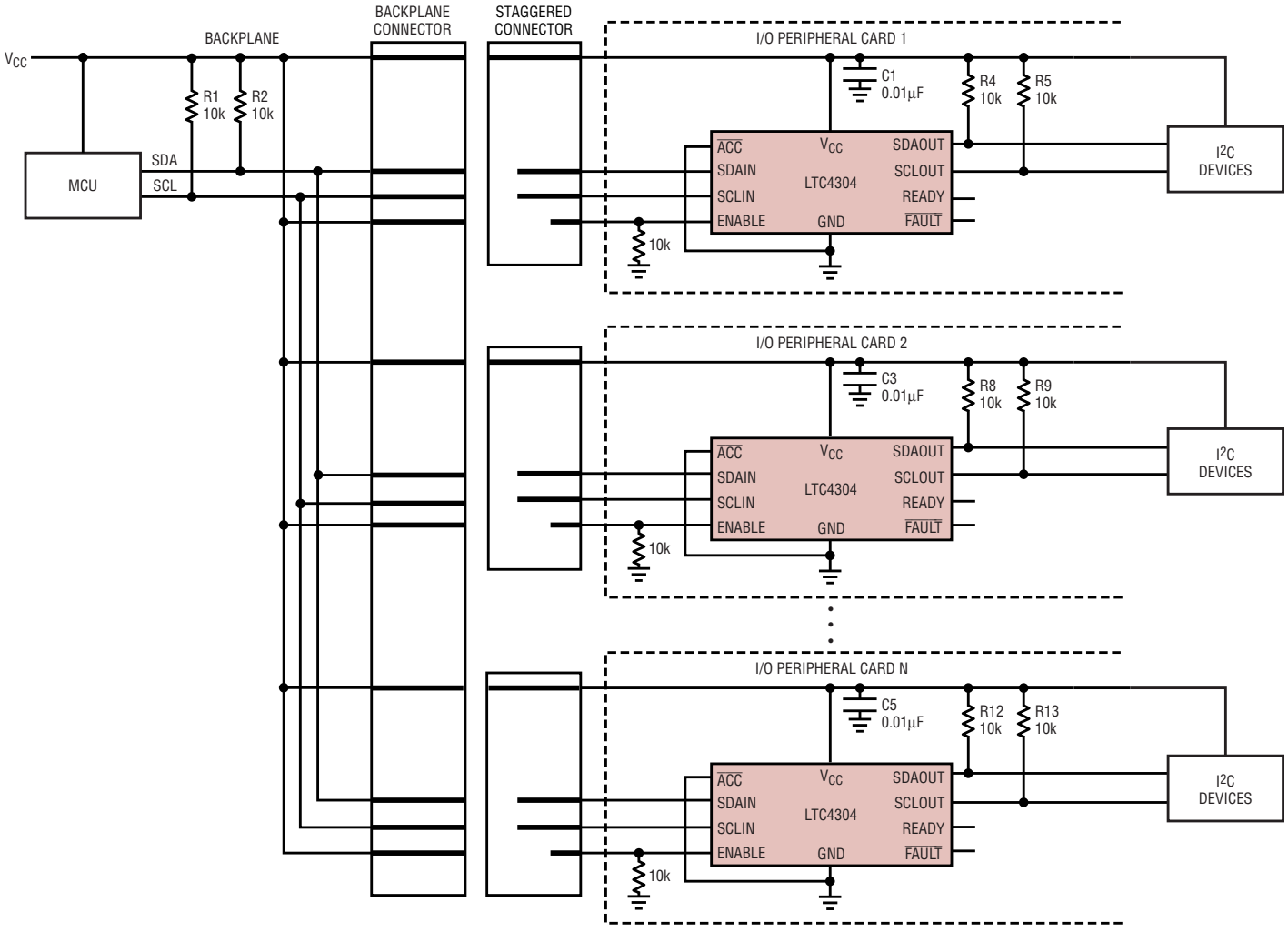


**Figure 1. Typical application of the LTC4304**

be inserted or removed from a live backplane without corruption of the $I^2C$ bus data. Finally, cards must be immune to ESD events that can occur from human handling.

The LTC4304 is a multifunctional device. It has a flexible architecture that allows it to be configured into almost any system. The LTC4304 features proprietary stuck bus protection circuitry that unburdens the MCU from the tasks of monitoring, troubleshooting and resolving stuck buses. Simplifying this task also saves PCB board space and connector pins. The LTC4304 provides bidirectional capacitance buffering, isolating the card bus from the backplane bus. Rise time accelerators help heavily capacitive-loaded buses meet $I^2C$ rise time specifications. The LTC4304 also enables cards to be inserted or removed from the system without corrupting the data on the $I^2C$ bus. Built-in ±15kV of human Body Model ESD protection provides a rugged front end for cards that typically have the SDA and SCL lines connected directly to the card connector.

## Circuit Operation

### Startup and Hot Swap

To take full advantage of the LTC4304's Hot Swap features, a staggered connector must be used: where $V_{CC}$ and GND are the longest pins, SDA and SCL pins medium length and ENABLE the shortest. After the card's $V_{CC}$ and GND connect with the live backplane, the voltage on $V_{CC}$ starts to rise. At this time, the LTC4304's precharge circuitry charges the capacitance on the SDA and SCL lines to 1V. Precharged SDA/SCL lines minimize disturbances on the bus when they connect to the backplane. The remainder of the LTC4304's circuitry is disabled until the supply voltage rises above 2.5V (typical) and the voltage on ENABLE is above 1.4V (typical). Making ENABLE the shortest pin insures that SCL and SDA are firmly seated before a connection is established on the bus. When the $V_{CC}$ supply to the LTC4304 is valid, it assumes that the card is connected to a live backplane and looks for either a stop bit or a bus idle on the backplane side on SDAIN and SCLIN. When one of these conditions is met and SDAOUT and SCLOUT are high, the connection circuitry is activated, connecting the card side bus with the backplane bus. These requirements ensure that the data on the bus is not corrupted when the card is plugged in. READY indicates the status of the connection circuitry and is high when the connection circuitry is active.

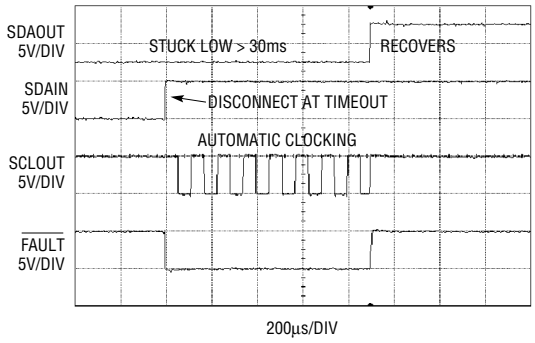


**Figure 2. Stuck bus resolved with automatic clocking**

### Bus Stuck Low Timeout

The LTC4304 monitors SDAOUT and SCLOUT on the card side of the $I^2C$ bus. When SDAOUT or SCLOUT is low, an internal timer is started, only to be reset when SDAOUT and SCLOUT are both high. If SDAOUT or SCLOUT do not go high within 30ms, the connection between the inputs and outputs is automatically disconnected, and $\overline{FAULT}$ asserts low indicating a stuck bus. The LTC4304 also detects a fault if powered up into a stuck bus condition. In either case, the LTC4304 automatically generates up to 16 clock pulses at 8.5kHz on SCLOUT. If SDAOUT and SCLOUT go high, $\overline{FAULT}$ releases and is pulled high. The LTC4304 then looks for a stop bit or a bus idle before automatically reconnecting. While there is a stuck bus condition, a connection can be forced with a rising edge on ENABLE, even if bus idle conditions are not met.

### Capacitance Buffering

The connection circuitry contains a unique patent-pending architecture that provides electrical isolation, isolating the capacitance on the card side bus from the backplane side bus, while maintaining full $I^2C$ functionality. This means that the MCU only sees the capacitance of the backplane and the low input capacitance of the LTC4304, <10pF guaranteed by design. The LTC4304 drives the capacitance of the circuitry on the card side. The LTC4304 regulates the voltage on the opposite side from which it is being driven to a slightly higher voltage. This voltage (call it $V_{OS}$) is a function of $V_{CC}$, the pull-up resistor, and an internally set constant terms given by the equation:

$$V_{OS} = \frac{V_{CC}}{R_{PULLUP}} \bullet 20 + 75mV$$

For example: For a 2.7kΩ pull-up and a $V_{CC}$ of 3.3V,

$$V_{OS} = \frac{3.3mV}{2.7k\Omega} \bullet 20 + 75mV = 99.4mV$$

### Rise Time Accelerators

Rise-time accelerators are included on all four SDA and SCL pins. Once activated, the accelerators switch in 3.5mA of current (typical at $V_{CC}$ = 2.7V) into the SDA and SCL lines to make them rise faster. This ensures that rise-time requirements are met and allows the use of larger pull-up resistors to reduce power consumption. When $\overline{ACC}$ is connected to ground, all four accelerators are ON. When $\overline{ACC}$ is connected to $V_{CC}$, all four accelerators are OFF. And when $\overline{ACC}$ is floating, only the accelerators on SDAOUT and SCLOUT are activated. Accelerators cannot be used on pins where the pull-up voltage is less than $V_{CC}$. The flexibility of the accelerators control provided by $\overline{ACC}$ allows the LTC4304

to interface with buses not common with its supply.

## Applications

### Stuck Bus Automatically Resolved Independent of the MCU

The I²C bus protocol calls for bidirectional communication between devices. A typical example is a microcontroller unit (or MCU) communicating with a slave device. As the slave device's internal register is read by the MCU, the MCU clocks the slave device to receive each bit of data. A problem occurs when the MCU is out of sync with the slave device—the slave device is waiting for another clock and the MCU thinks it has already sent out enough clocks. If the slave device happens to be holding the data line low, all further communications are prevented and the I²C bus is stuck.

Figure 1 shows a card with a resident LTC4304 that acts as the interface between the devices on the card and the I²C bus, when the card is plugged into the backplane. In normal, plugged-in operation, a connection is established between SDAIN and SDAOUT, and SCLIN and SCLOUT. Internal comparators monitor the SDAOUT and SCLOUT nodes of the circuit. When SDAOUT or SCLOUT is low, an internal timer starts. The timer is only reset when SDAOUT and SCLOUT are both high. If they don't go high within 30ms, it is determined that the bus is stuck low and the con-

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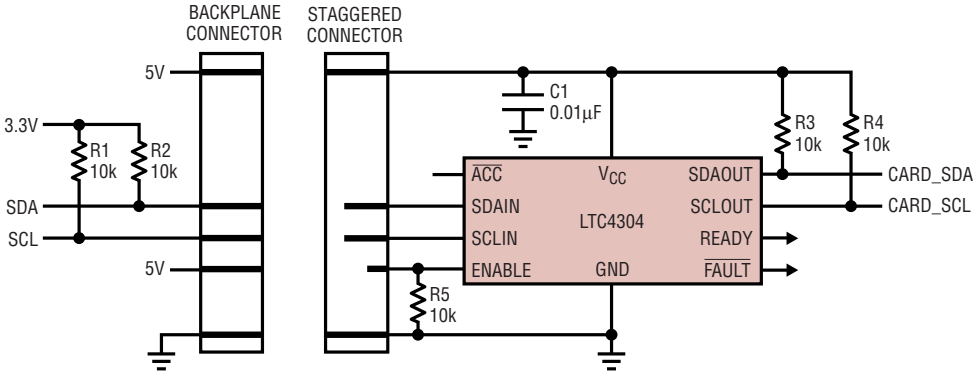
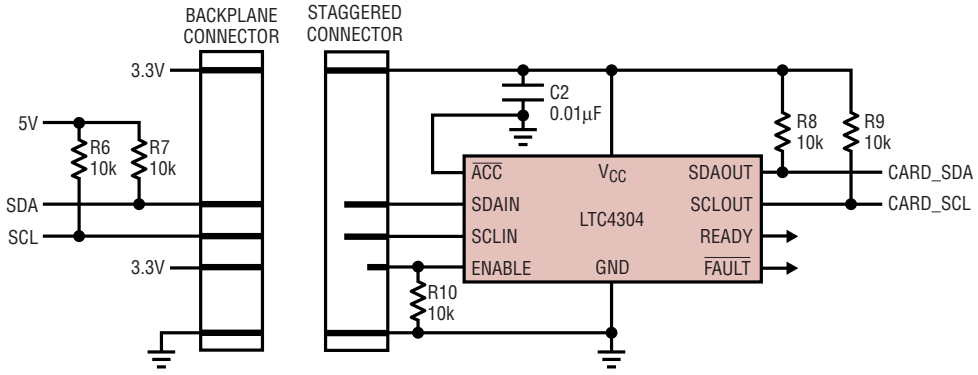
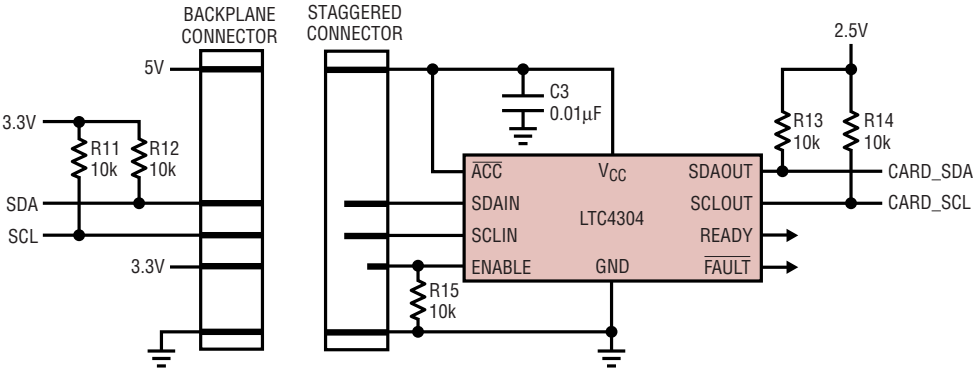



**a. $V_{CC}$ is higher than the pull-up voltage on SDAIN and SCLIN.**




**b. $V_{CC}$ is equal to the output side pull-up voltage, and less than input side pull-up voltage.**




**c. $V_{CC}$ is greater than the pull-up voltages of both sides.**

**Figure 3. The LTC4304 can be the bridge between a backplane operating at one voltage and a card operating at a different voltage. Here are three possible scenarios and appropriate configurations.**

**Table 2. The voltages at ADIN and ADIN2 (referred to $V_{EE}$) indicate which RTN fuse is open in the 4-fuse monitor in Figure 9**

| | |
|---|---|
| $V_{ADIN} = V_{ADIN2} = 0V$ | Both F1 and F2 are open |
| $0.25 \bullet V_{ADIN2} \le V_{ADIN} < 0.7 \bullet V_{ADIN2}$ | F1 is open |
| $0.7 \bullet V_{ADIN2} \le V_{ADIN} < 1.1 \bullet V_{ADIN2}$ | F2 is open |
| $V_{ADIN} > 1.1 \bullet V_{ADIN2}$ | Normal Operation |

ficult, without direct fuse monitoring, to detect a single open fuse.

The integrated ADC, I²C monitoring, and general-purpose pins of the LTC4261 make it possible to monitor the individual fuses, as shown in Figure 9. Fuses on the RTN side are sensed using resistors R1, R2 and R3 with the output measured by the ADC at the ADIN pin. At the same time, the input voltage after the ORing diodes is sensed using R4 and R5 and measured at the ADIN2 pin. Diodes D3 and D4 are used to compensate the ORing diodes. Table 2 shows how the voltages at ADIN and ADIN2 indicate which fuse on the RTN side is open.

Using the input voltage as the reference ensures valid detection in the full operating range.

Fuse monitoring on the –48V side is more straightforward using the $INTV_{CC}$ pin along with two logic input pins, PGIO (when configured as input) and $\overline{FLTIN}$ as shown in Figure 9. Fuse F3 is sensed with R6 and R7 at PGIO, and fuse F4 is sensed with R8 and R9 at $\overline{FLTIN}$ with inverted input. If F3 is open, PGIO is pulled high and the PGIO input bit in the FAULT register is set. If F4 is open, $\overline{FLTIN}$ is pulled low and the FLTIN bit is set. In the latter case, if the corresponding bit in the $\overline{ALERT}$ register is also set, the LTC4261 interrupts the host using the $\overline{ALERT}$ pin.

## Conclusion

The LTC4261 is a full-featured, intelligent Hot Swap controller that enhances the reliability and durability of high availability –48V power systems. The internal 10-bit ADC, I²C/SMBus and registers make it easy to monitor faults and real-time power and communicate with the system host. Its unique inrush and overcurrent control technique minimizes stresses on the pass transistor in all operating conditions.

*LTC4304, continued from page 12*

nection between SDAIN and SDAOUT, and SCLIN and SCLOUT is broken, isolating the problem device from the bus. $\overline{FAULT}$ pulls low indicating a stuck bus. At this time it is assumed that the MCU and the device it is communicating with are out of sync. The MCU sent out all of the clocks necessary for the transaction, but the device is still in the middle of the transaction. The device is waiting for more clocks to finish putting its data on the bus, and the last bit it put on the bus happened to be a low, hence it holds the bus low until it gets more clocks (bus is stuck). Because the connection is broken, the problem device is now isolated from the I²C bus, and the rest of the system is free to resume normal operation.

After the connection is broken, the LTC4304 automatically generates up to 16 clock pulses at 8.5kHz on SCLOUT, enough clocks to clear the internal register on the problem device. The device could be cleared with one or any number of clocks (up to 16) depending on how the fault occurred. At anytime, if SDAOUT and SCLOUT go high, $\overline{FAULT}$ is released to go high and the automatic clocking is stopped, and a connection is automatically enabled. When the slave that was stuck sees a START bit after connection, it will abort the stalled communication and reset. The fault is cleared independently of the MCU. If the fault cannot be cleared, the offending circuit remains isolated from the system. Figure 2 shows an example of a stuck bus being resolved with automatic clocking.

### Supply Independence and Level Translation

The LTC4304 can be the bridge between a backplane operating at one voltage and a card operating at a different voltage. Figure 3 shows some typical configurations. Notice that $V_{CC}$, the pull-up voltage on SDAIN and SCLIN and the pull-up on SDAOUT and SCLOUT are independent of each other.

The rise time accelerators must be disabled when the bus pull-up voltage is lower than $V_{CC}$. Figure 3a shows a situation where the $V_{CC}$ is higher than the pull-up voltage on SDAIN and SCLIN. In this case $\overline{ACC}$ must be floating, disabling the rise time accelerators on the inputs only. In Figure 3b, $V_{CC}$ is equal to the output side pull-up voltage, and less than input side pull-up voltage. $\overline{ACC}$ is connected to GND to enable all four rise time accelerators. Finally, in Figure 3c, $V_{CC}$ is greater than the pull-up voltages of both sides. $\overline{ACC}$ is connected to $V_{CC}$ to disable all four accelerators.

## Conclusion

The LTC4304 is a multifunctional device with an impressive number of features designed to increase the reliability of an I²C bus. The flexible architecture allows the LTC4304 to be configured into almost any system. The LTC4304 isolates and resolves stuck buses independently of the MCU. Capacitance buffering, level translation, Hot Swap features and ±15kV human body ESD protection make the LTC4304 an ideal solution for any I²C application.

The LTC4304 is offered in small 10 pin MSOP and DFN (3mm × 3mm) packages.

A feature-reduced version of the LTC4304 is also available. The LTC4303 provides all of the functionality of the LTC4304 with the exception of the $\overline{FAULT}$ output flag and $\overline{ACC}$ control pin. The LTC4303 is a drop in replacement for the LTC4300A-1 and its rise time accelerators are permanently enabled.