# µModule Isolation Solution for High Resolution 1Msps ADCs Reads Data at 100MHz, Serves Multiple ADCs
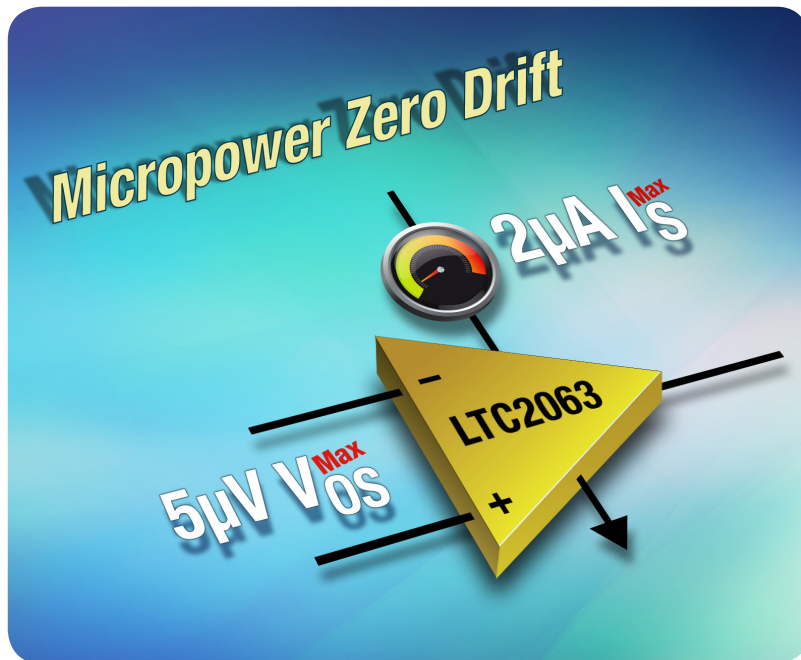Brian Jadus

The ideal isolator for an analog-to-digital converter (ADC) is one that is invisible. It manages all the control and data signals, maximizes the sampling rate and minimizes the effects of jitter on SNR performance. The LTM2893 µModule isolator achieves these goals for ADCs with SPI interfaces, in the 1Msps range, and supports a 6000V$_{RMS}$ isolation rating.



**Micropower Zero Drift**

**2µA I$_S$** Max

**LTC2063**

**5µV V$_{OS}$** Max

The LTC2063 zero-drift, 20kHz amplifier enables high resolution measurement at extremely low power levels. See page page 30.

Reading data from high resolution successive approximation register (SAR) analog-to-digital converters through a digital isolator is limited with more traditional options. When reading from a serial peripheral interface (SPI) most high speed digital isolators max out at 25MHz, with a few specialty devices operating up to 40MHz. The LTM®2893 reads data at up to 100MHz, is flexible, and handles multiple ADCs solving the timing issues and limitations of standard digital isolators interfacing to SAR ADCs.

**REASONS TO ISOLATE ADCS**

The isolation barrier allows the ADC to float to the common mode of the input signal and absorbs harsh conditions and transients. Even applications that don't require isolation can benefit from it. The LTM2893 makes it particularly easy to add a layer of isolation, improving system safety. For instance, whereas process and test equipment require isolation to protect inputs

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# General purpose digital isolators and dedicated SPI isolators can be used to isolate ADCs, but such solutions use multiple digital isolators to support signals such as conversion start or busy status signals, in addition to the 3- or 4-wire SPI port.

*(LTM2893, continued from page 1)*

from damage due to accidental misconnections or overvoltage events, an isolator can also be used as a high voltage level shifter to extend the common mode range or to reduce ground noise. The LTM2893 ignores common mode transient events up to 50kV/μs with a low capacitance isolation barrier and fully differential data communication.

## PRIOR GENERAL PURPOSE DIGITAL ISOLATORS FALL SHORT

General purpose digital isolators and dedicated SPI isolators can be used to isolate ADCs, but such solutions use multiple digital isolators to support signals such as conversion start or busy status signals, in addition to the 3- or 4-wire SPI port. Standard digital isolators are limited by the signal propagation delay in sending an SCK signal to the isolated SPI port and waiting for the return of the MISO (SDO) data before the next latching edge of the SCK signal can occur, as shown in Figure 2. This adds propagation delays in addition to the response delay

from the ADC SPI port. Adding up all the delays, a read may take up to 38ns from what initially appeared an attractive 150Mbps digital isolator. This reduces the effective SCK frequency to 25MHz or less.

## STREAMING ISOLATOR

The LTM2893 is tailored to communicate with ADCs with a dedicated master SPI function on the isolated side and a dedicated slave function with a buffer on the logic side as shown in Figure 3.

The isolated side master SPI engine monitors status signals from the ADC and fetches the data after the BUSY signal goes low. This function initiates without logic side interaction after the start of a conversion.

The logic side slave SPI engine contains a buffer register to receive data from the isolated side through the isolation barrier. During an ADC conversion operation, when the buffer register receives data from the isolated side SPI master, the logic side BUSY signal goes low indicating the SPI slave port is ready to be read.

The LTM2893 has the logic functions to fetch and buffer the data to minimize the data interaction across the isolation barrier. Data is streamed internally at 200Mbps when two ADCs are read at 100MHz.

## SAR ADC SPECIFIC SIGNAL ISOLATION

Typical SAR ADCs have a conversion start (CNV) signal to initiate resolving the input signal into a digital result, and a BUSY signal to indicate when the conversion is in progress. The LTM2893 is tailored for SAR ADCs by including a conversion start (CNV) and busy (BUSY) signals to manage communication to the ADC. The conversion start signal is transported through the LTM2893 from the CNV input to the CNV2 output on a rising edge.

The transport of the conversion start signal through the isolator has low jitter to minimize degradation to the aperture jitter of the ADC sample. The BUSY signal remains high after a rising edge of the CNV input and will go low when data
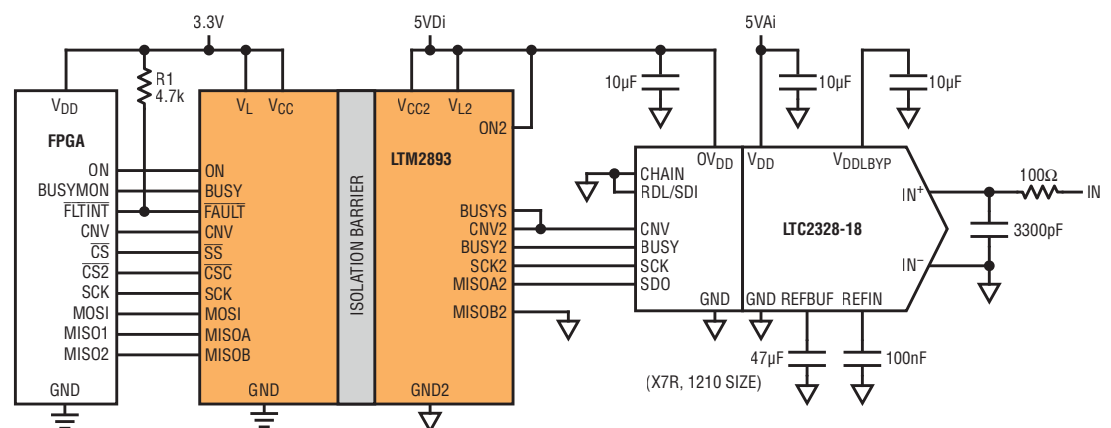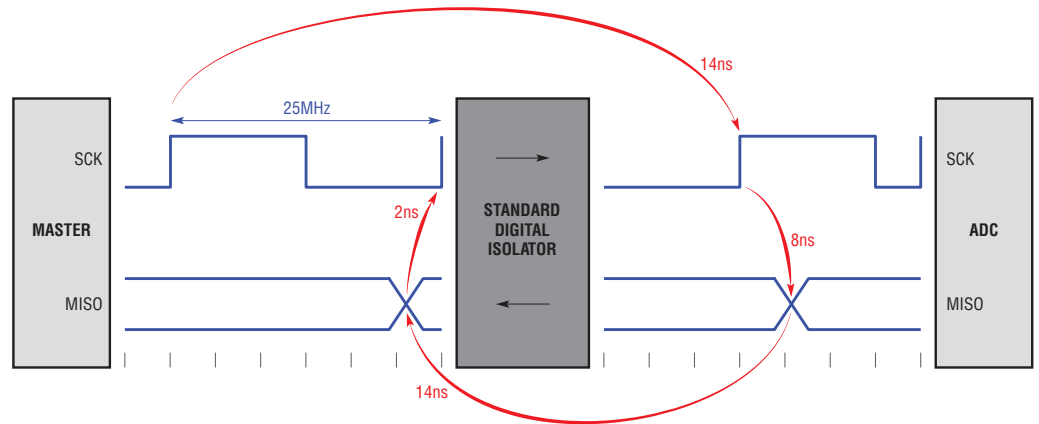
**Figure 1. Typical application**

Figure 2. Standard digital isolator SPI read delays can add up to 38ns, reducing effective SCK frequency to approximately 25MHz.

has been received in a local SPI buffer from the isolated side. Once the BUSY signal goes low the local SPI port is ready to be read. ADCs without conversion start and busy signals are also compatible with the LTM2893, by connecting the CNV2 and BUSY2 pins together.

## AUXILIARY CHANNELS FOR MULTIPLEXER CONTROL SIGNALS

The LTM2893 provides three signals for controlling functions across the isolation barrier in either direction. The signals are ideal for controlling devices such as an analog multiplexer (Figure 4), a programmable gain amplifier, or control signals on an ADC such as power down or resets. The select signals cannot be used at the beginning or during a conversion, but are ideal
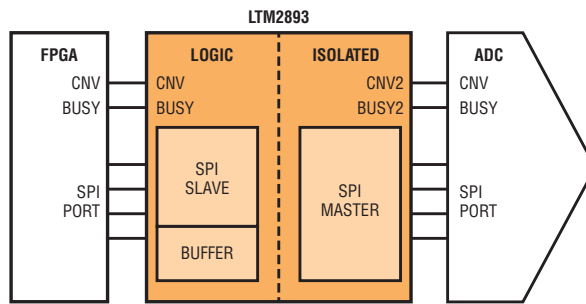


Figure 3. ADC streaming isolator can effectively read ADCs at 100MHz

for changing settings or making selections prior to starting a conversion. A configuration register allows individual adjustment in the direction of the three select signals.

## FLEXIBILITY

The factory sets the LTM2893 SPI port to an SCK2 frequency of 100MHz, with a 24-bit data word length, and a single word

count, which is selected to operate directly with the LTC2338, LTC2328, and LTC2378 ADCs. The SCK2 frequency setting is the serial clock frequency used to read data from the ADC. The logic side SPI port can be operated down to 1/128 of the SCK2 frequency setting. The second chip select (CSC) enables writing to two configuration
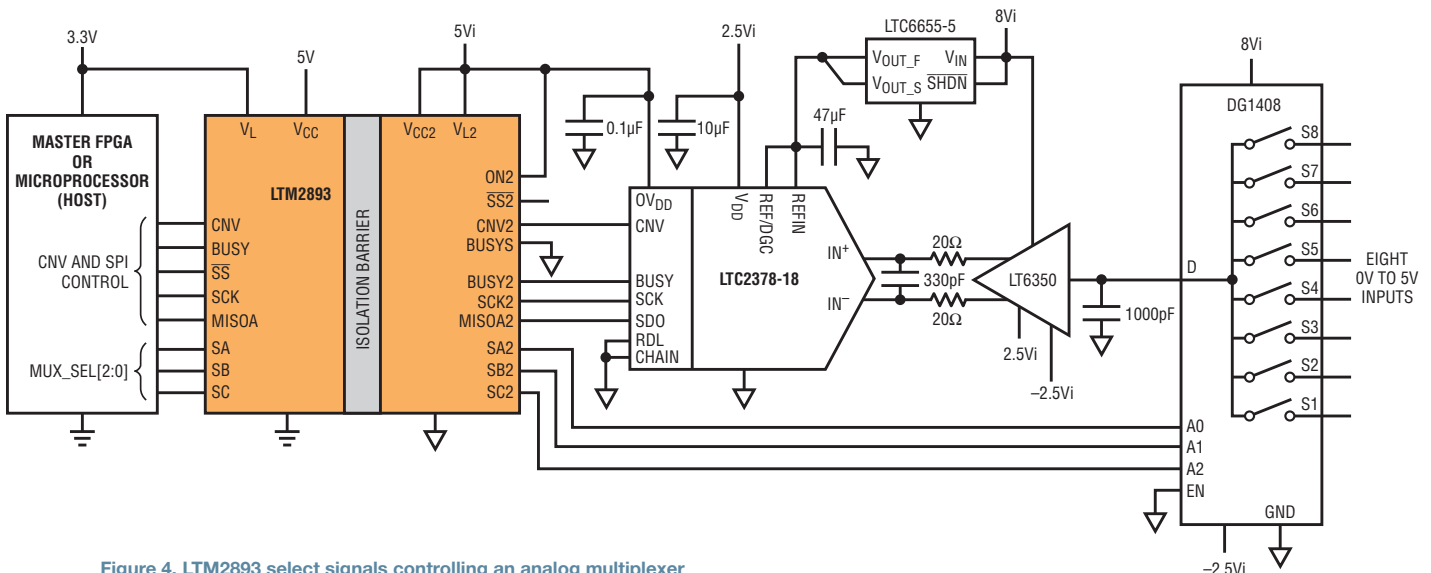


Figure 4. LTM2893 select signals controlling an analog multiplexer

The LTM2893 has a dual read port (MISOA, MISOB) that allows two ADC results to be read simultaneously. Two ADCs can be connected to the isolated side of the LTM2893 and share the CNV2 and SCK2 signals; the BUSYS and BUSY2 signals independently connect to each ADC, while the SDO outputs of the ADCs connect MISOA and MISOB, respectively.
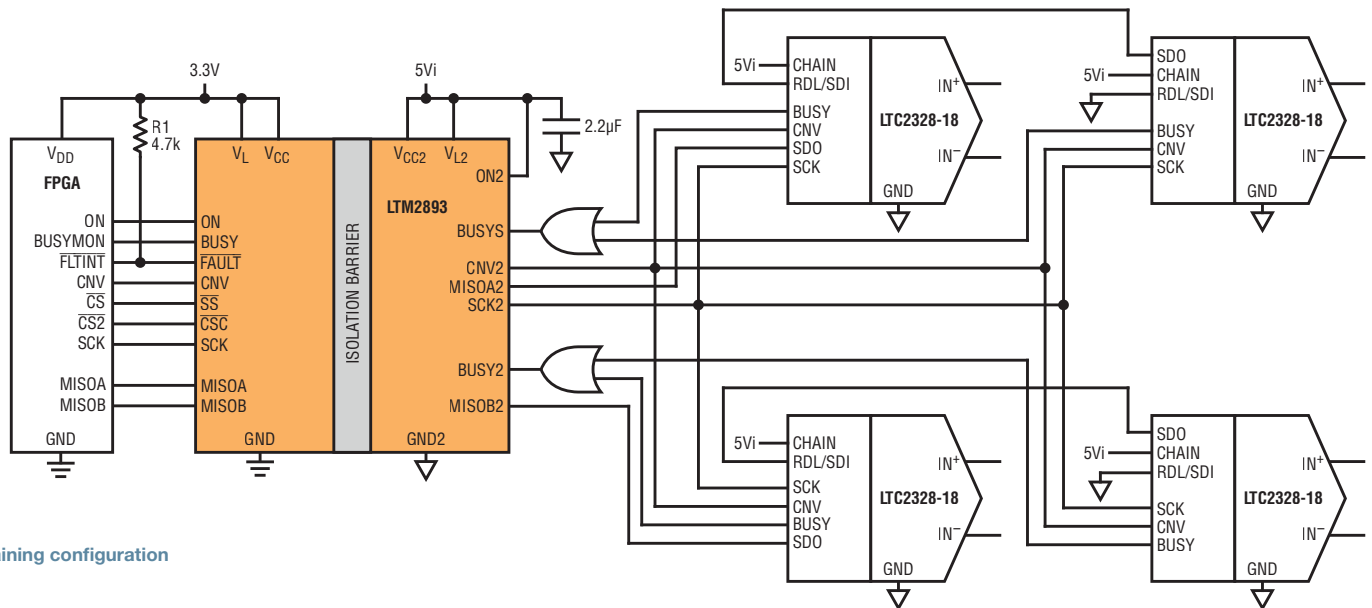


Figure 5. Chaining configuration

registers in the LTM2893 selecting SPI clock speeds, word lengths, and word counts.

The SCK2 frequency has eight selections in the configuration register supporting ADC SPI ports from 100MHz to 6.25MHz.

The 24-bit data word length setting works for a number of our general purpose SAR ADCs with 16-bit to 24-bit results and 1Msps performance. This word length setting defines the number of bits the

isolated side SPI master retrieves from the ADC and stores in the logic side buffer. Reading the data from the logic side SPI port does not require reading the full word length. The word length can be optimized in the configuration register for the parameters of the ADC to reduce sampling time or reduce power with eight settings from 32 bits to 8 bits. The word count setting selects how many multiple words are read in a single conversion cycle.
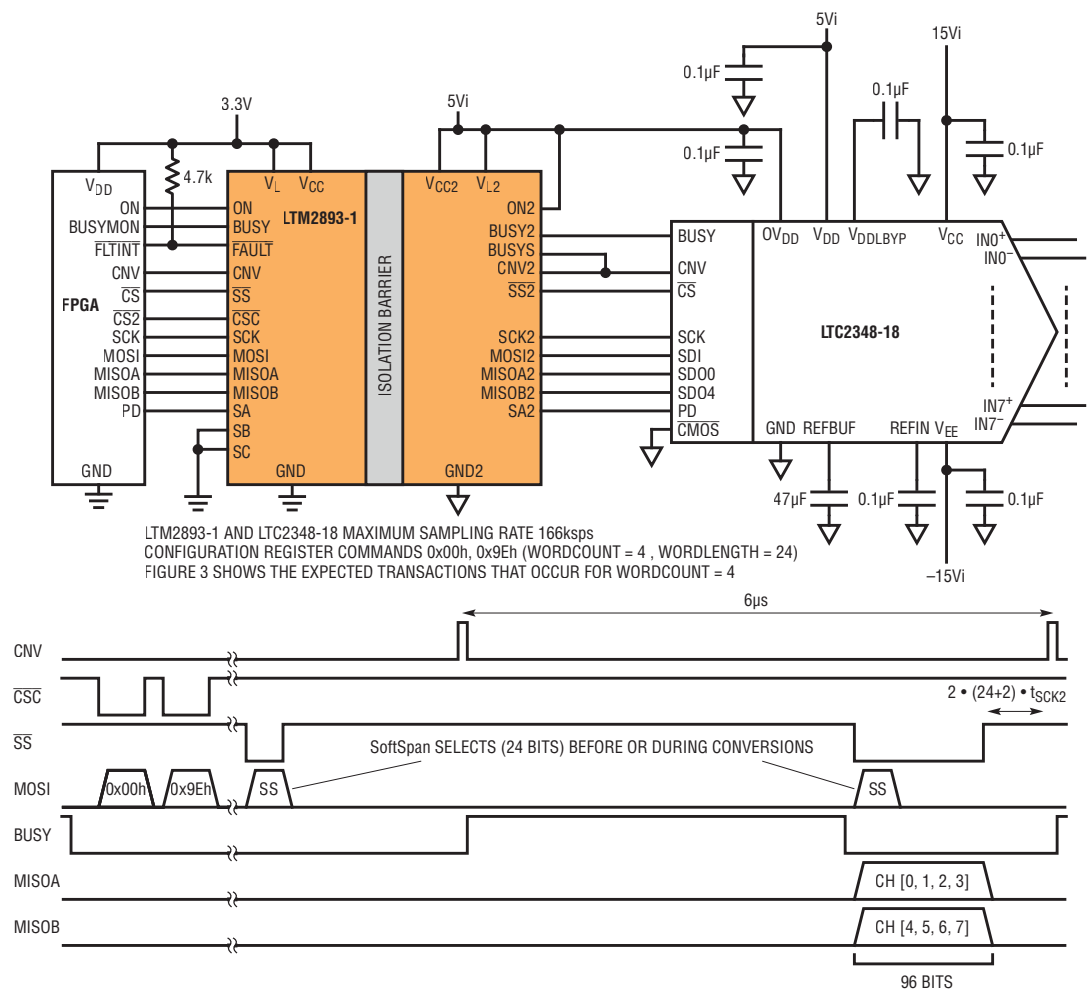
**ISOLATING MULTIPLE ADCs**

The LTM2893 has a dual read port (MISOA, MISOB) enabling two ADC results to be read simultaneously. Two ADCs can be connected to the isolated side of the LTM2893 and share the CNV2 and SCK2 signals; the BUSYS and BUSY2 signals independently connect to each ADC, while the SDO outputs of the ADCs connect MISOA and MISOB, respectively.

**Digital isolators for ADCs and DACs**

| | LTM2893 | LTM2893-1 | LTM2895 |
|---|---|---|---|
| Function | SAR ADC interface | SAR ADC interface with configuration | DAC or general purpose SPI interface |
| SPI communication | read only | read/write for LTC2348/LTC2358 ADC family | write with readback |
| Maximum SCK frequency | 100MHz | 100MHz | 100MHz |
| Effective number of communicated signals | 9 (4 SPI, 5 control) | 10 (5 SPI, 5 control) | 9 (5 SPI, 4 control) |

The LTM2893-1 read and write SPI ADC isolator enables configuring the SoftSpan register and reading all the multiplexed data results from an LTC2348. The LTC2348 ADC family has eight analog inputs that are simultaneously sampled, sequentially converted, and accessed through an 8-output SPI port.

**Figure 6. LTM2893-1 and the LTC2348-18**



LTM2893-1 AND LTC2348-18 MAXIMUM SAMPLING RATE 166ksps
CONFIGURATION REGISTER COMMANDS 0x00h, 0x9Eh (WORDCOUNT = 4 , WORDLENGTH = 24)
FIGURE 3 SHOWS THE EXPECTED TRANSACTIONS THAT OCCUR FOR WORDCOUNT = 4

Additionally, with ADCs that support chaining (Figure 5), up to eight ADCs can be connected to a single LTM2893. Reading more than two parallel ADCs requires a write to the configuration register in the LTM2893 to select the number of devices. The configuration register allows the selection of two, four, six or eight devices to be accessed through the two MISOA and MISOB SPI outputs.

## ISOLATE THE LTC2348 MULTIPLEXED ADC WITH THE LTM2893-1

Most ADCs require only a read-capable SPI port. The LTM2893 is dedicated to reading ADCs with a read-only SPI port. The LTM2893-1 is dedicated to ADCs with configuration registers such as the LTC2348 simultaneous sampling ADC family, shown in Figure 6.

The LTM2893-1 read and write SPI ADC isolator enables configuring the SoftSpan™

register and reading all the multiplexed data results from an LTC2348. The LTC2348 ADC family has eight analog inputs that are simultaneously sampled, sequentially converted, and accessed through an 8-output SPI port. Connecting ports 0 and 4 to the MISOA2 and MISOB2 inputs of the LTM2893-1 and setting the LTM2893-1 configuration register to a word length of 24 and a device count of 8 shifts two channels of four results per conversion. Adding an isolator to the LTC2348 has a

The addition of any digital isolator can introduce timing jitter resulting in performance degradation. The LTM2893 is designed with a low jitter path for the conversion start signal to minimize degradation in signal-to-noise performance. The system performance of the LTM2893 with a LTC2328-18 is similar to the standalone performance of the LTC2328-18.
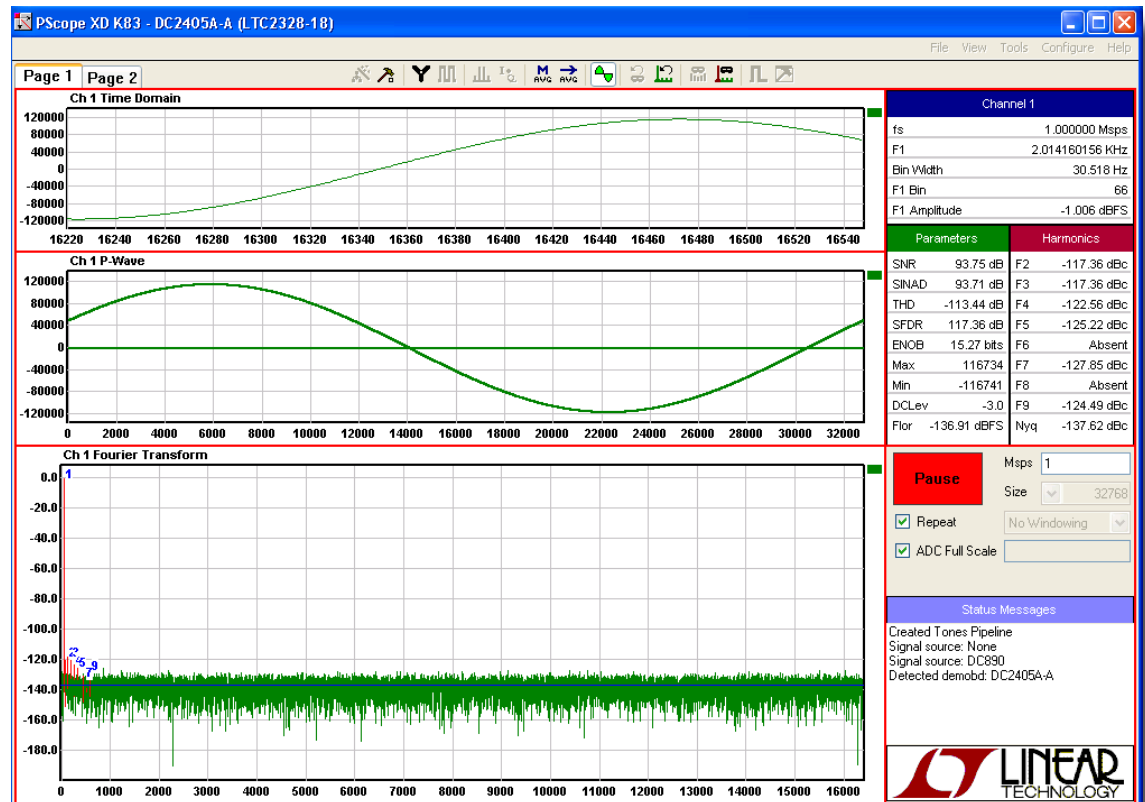


**Figure 7. PScope plot of the DC2405A demonstration circuit**

small penalty on sampling rate, reducing the ideal speed of 200ksps to 166ksps.

### SYSTEM PERFORMANCE

The addition of any digital isolator can introduce timing jitter resulting in performance degradation. The LTM2893 is designed with a low jitter path for the conversion start signal to minimize degradation in signal-to-noise performance. The system performance of the LTM2893 with a LTC2328-18 is similar to the standalone performance of the LTC2328-18. To illustrate this performance, Figure 7 shows a plot of the DC2405A

demo board capturing a 2kHz input at −1dBFS with our PScope™ application.

### CONCLUSION

The LTM2893 is a fully integrated isolation solution specifically designed for ADC applications. The LTM2893 handles all the necessary signals for accessing ADCs through an isolation barrier with minimal performance degradation. The LTM2893 meets 100MHz SPI operation when interfaced with ADCs. In contrast, other, piecemeal isolated solutions must reduce the clock frequency to overcome propagation delays. The LTM2893's flexible

interface allows it to isolate multiple ADCs, reducing overall component count and system complexity, compared to other SPI isolation solutions. Because it is optimized for ADCs, designers can easily add it to any solution requiring a robust interface. ■