I²C Programmable Multichannel Voltage Supervisors with EEPROM

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The LTC2933 and LTC2936 are 6-channel, I²C/SMBus programmable voltage supervisors with EEPROM. Table 1 shows Linear Technology's broad line of programmable voltage supervisors and Power System Managers. The LTC2933 and LTC2936 are well suited for multirail systems that require accurate power supply overvoltage (OV) and undervoltage (UV) detection.

UNMATCHED VERSATILITY

The following features can be configured, read, modified, and stored in the onboard EEPROM via the I²C/SMBus interface:

- Two voltage thresholds for each of the six inputs
- Comparator polarity and mapping to GPIO pins
- GPIO mode, polarity, and delay
- GPI mode, polarity, and mapping to GPIO pins
- Comparator output mapping to dedicated comparator output pins (LTC2936 only)
- I²C/SMBus write protection
- First fault snapshot

The threshold settings for each channel are programmable over multiple voltage ranges and feature 256 settings per range (see Tables 2 and 3). Programmability eliminates the need to qualify, source or stock unique parts for different threshold voltages or other feature combinations.

A snapshot of the first fault to occur after power-up is stored in the EEPROM, which can be used for debugging power failures in complex systems. These devices also record subsequent faults in the volatile memory. Both the instantaneous status and the fault history can be accessed remotely through the I²C/SMBus interface.

Various combinations of faults and input signals can be mapped to any general purpose input-output (GPIO) pin, providing flexibility in application design. The GPIO pins can also be programmed to act as SMBus $\overline{\text{ALERT}}$ outputs. The

Table 1. Feature comparison of Linear's programmable voltage supervisors

	LTC2933	LTC2936	LTC2970	LTC2974	LTC2975	LTC2977	LTC2978	LTM®2987
Sequence				✓	✓	✓	✓	✓
Trim and Margin			✓	✓	✓	✓	✓	✓
Supervise	✓	✓	✓	✓	✓	✓	✓	✓
Monitor Telemetry			✓	✓	✓	✓	✓	✓
Manage Faults			✓	✓	✓	✓	✓	✓
Create Fault logs	✓	✓		✓	✓	✓	✓	✓
Number of Channels	6	6	2	4	4	8	8	16
Autonomous Operation	✓	✓		✓	✓	✓	✓	✓
LTpowerPlay GUI Support	✓	✓		✓	✓	✓	✓	✓
PMBus Compliant Command Set				✓	✓	✓	✓	✓
Package	5×4 DFN	4×5 QFN	4×5 QFN	9×9 QFN	9×9 QFN	9×9 QFN	9×9 QFN	15×15 BGA

The threshold settings for each channel are programmable over multiple voltage ranges and feature 256 steps per range (see Tables 1 and 2). Programmability eliminates the need to qualify, source or stock unique parts for different threshold voltages or other feature combinations.

LTC2936 has six dedicated comparator outputs (CMP*n*), which can be used in simple sequencing applications.

An additional pair of auxiliary comparators, on the general purpose input (GPI*n*) pins, are available with 500mV preset thresholds and programmable polarities. The outputs of these auxiliary comparators can be mapped to any of the GPIO*n* pins, allowing the device to supervise up to eight inputs. The GPI*n* pins can also be configured to mask any UV faults ($\overline{\text{UVDIS}}$), mask both UV and OV faults ($\overline{\text{MARG}}$), act as a manual reset input ($\overline{\text{MR}}$) or write protect the part ($\overline{\text{WP}}$, LTC2936 only). Masking of the OV and UV faults can be used for sequencing or power supply margining purposes.

An accurate linear regulator output (3.3V ± 2.5%) can be used as a reference voltage for level shifting negative power supply rails into a range where they can be supervised by the device. The high input impedance Precision Range enables this capability with an input current less than 10nA. This mode is available on V5 and V6 of the LTC2933 and all inputs of the LTC2936.

The LTC2933 automatically selects the highest voltage applied on channels V1–V4 as the supply voltage. This increases system reliability when multiple power rails might fail in a multirail system. The LTC2936 uses a dedicated power supply input. This input can be driven by an external 3.3V regulator, or from a 3.4V to 13.9V power supply.

Table 2. LTC2933 voltage threshold summary

	V1		V2–V6		
Range	High	Medium	Medium	Low	Precision
Limits	2.5V–13.9V	1V–5.8V	1V–5.8V	0.5V–3V	0.2V–1.2V
Step Size	50mV	20mV	20mV	10mV	4mV

Table 3. LTC2936 voltage threshold summary

	V1–V6		
Range	Medium	Low	Precision
Limits	1V–5.8V	0.5V–3V	0.2V–1.2V
Step Size	20mV	10mV	4mV

THRESHOLD ACCURACY

In most applications, the supply voltages must be maintained within relatively narrow tolerances. The effective tolerance a supervisor can guarantee is a function of both the threshold setting resolution and the comparator accuracy. The LTC2933 and LTC2936 provide multiple threshold ranges, each with 256 threshold settings. By selecting the smallest range that encompasses the expected variation of the supply voltage being supervised, the error due to the threshold setting resolution can be minimized. The devices are also guaranteed to have less than 1% threshold error across a broad range of threshold settings.

PREVENTING FALSE ALARMS

False triggering of a supervisor can happen when excessive noise is present on the voltage rail being supervised. To handle this noise, the LTC2933 and

Figure 1. Typical application

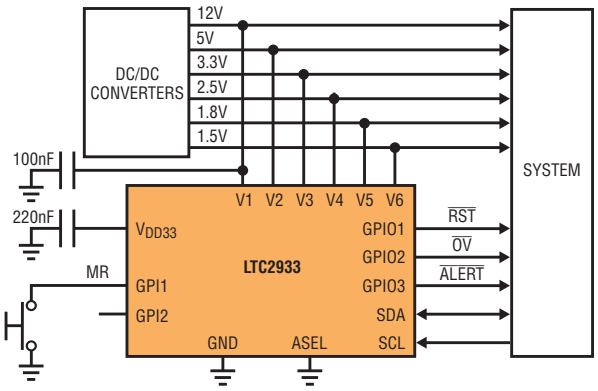


Table 4. LTC2933 slave addresses

ASEL	0	HI-Z	1
7-Bit Address	0x1C	0x1D	0x1E
8-Bit Address	0x38	0x3A	0x3C

Table 5. LTC2936 slave addresses

ASEL0	0	Hi-Z	1	0	Hi-Z	1	0	Hi-Z	1
ASEL1	0	0	0	Hi-Z	Hi-Z	Hi-Z	1	1	1
7-Bit Address	0x50	0x51	0x52	0x53	0x54	0x55	0x58	0x59	0x5A
8-Bit Address	0xA0	0xA2	0xA4	0xA6	0xA8	0xAA	0xB0	0xB2	0xB4

LTC2936 internally filter these transients. Additionally, the GPIO*n* pins can be configured to have an output delay of up to 1.6s, which can also be used to mask transients on the supply.

CONNECTING MULTIPLE OPEN-DRAIN OUTPUTS

The GPIO*n* outputs of the LTC2933 and LTC2936 can be configured to address the needs of a wide variety of applications. The factory default output type is an active low, open-drain output. Multiple devices can pull the line low, in a wired-OR configuration, allowing a single line to communicate fault information from multiple supervisors.

If configured as an $\overline{\text{ALERT}}$ output, this feature can be used to allow the SMBus master to determine which device triggered an alert by accessing all slave devices using the Alert Response Address (ARA) protocol. Only a slave device that asserted $\overline{\text{ALERT}}$ acknowledges the ARA by sending its address to the SMBus master and releasing the $\overline{\text{ALERT}}$ line. When multiple devices assert $\overline{\text{ALERT}}$ at the same time, arbitration of the returned address occurs, with the lowest address winning arbitration. By reading the ARA address until the $\overline{\text{ALERT}}$ line is released by all devices, a list of device addresses can be obtained and the SMBus master can take further action.

MANUAL RESET

Any GPI*n* pin can be programmed as an active low, manual reset input. This input can be mapped to any GPIO*n* pin to force a reset or trigger an interrupt. Programmable output delay times can be used to guarantee a minimum reset pulse width.

The manual reset input can also be configured to clear the fault history in volatile memory and re-enable the fault snapshot in EEPROM. This allows for a full pushbutton system reset.

MARGINING

Designing a robust system typically involves some form of power supply margining. The LTC2933 and LTC2936 have modes that allow the power supply voltages to be margined beyond their normal tolerances, without triggering faults, by configuring a GPI*n* pin as a margin ($\overline{\text{MARG}}$) or UV disable ($\overline{\text{UVDIS}}$) input and pulling the GPI*n* pin low during system margin testing. The $\overline{\text{MARG}}$ mode ignores both OV and UV faults as detected by the comparators, while the $\overline{\text{UVDIS}}$ mode ignores only UV faults from the comparators.

WRITE PROTECTION

The LTC2933 and LTC2936 contain write-protect features that prevent accidental I²C/SMBus writes to the user configuration. By setting the lock bit, writes to any user configuration commands are ignored. To unlock the part, a user-configurable, 14-bit unlock key must be written. Additionally, the LTC2936 provides a hardware write-protect input as one of the configuration options for the GPI*n* pins.

I²C/SMBus INTERFACE

The LTC2933 and LTC2936 are I²C/SMBus transmit/receive slave-only devices. The LTC2933 can respond to one of three addresses, depending on whether the address select pin is grounded, floating, or tied to the VDD33 supply pin (Table 4). All LTC2933 parts respond to the global address 0x1B (7-bit)/0x36 (8-bit), regardless of the address select pin.

Figure 2. Negative power supply monitor

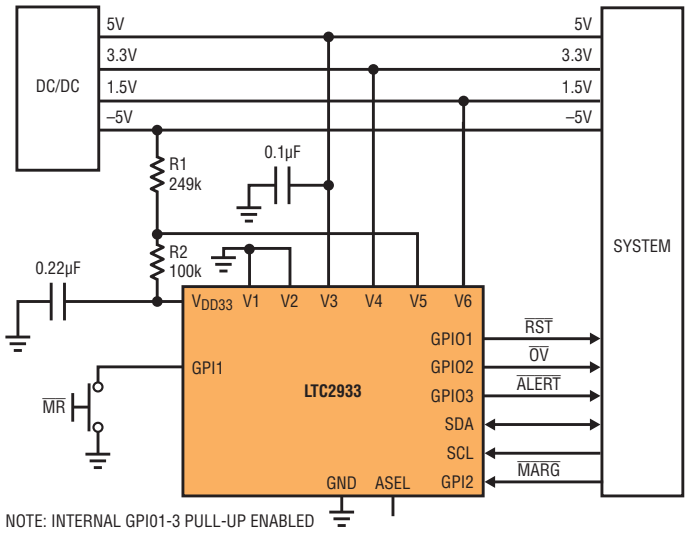
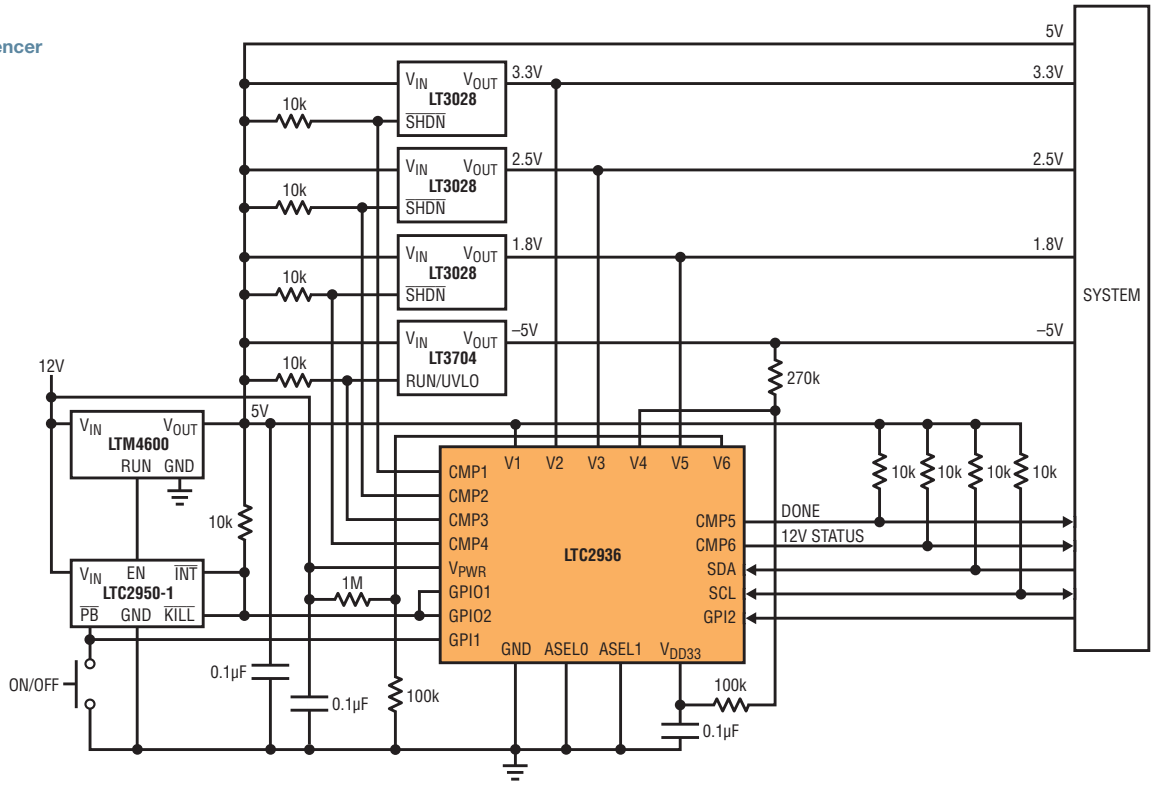


Figure 3. Five-supply power-up sequencer



The LTC2936 has two ternary address select pins, allowing it to respond to nine different addresses (Table 5). All LTC2936 parts respond to the global address 0x73 (7-bit)/0xE6 (8-bit), regardless of the address select pins.

All threshold voltages and configurations for the comparators, GPI*n* pins, and GPIO*n* pins can be programmed and read back through the I²C/SMBus interface. The interface can also be used to read the current status, read the fault snapshot, clear the volatile fault history and store and restore configuration in EEPROM.

APPLICATIONS

Negative Power Supply Monitor

Figure 2 illustrates how to configure the LTC2933 to monitor a negative supply rail. A voltage divider from VDD33 is used to level-shift the negative supply into the input range of the LTC2933. The precision input range should be used to minimize the error caused by leakage current into the V5 pin.

Five Supply Power-Up Sequencer

Figure 3 illustrates how to use the LTC2936 dedicated comparator outputs to enable DC/DC converters sequentially, at power-up. The system is powered by a 12V power source, which is also monitored.

When the pushbutton is pressed, the LTC2950-1 turns on the LTM4600 by taking its RUN pin high. The LTM4600 generates a 5V intermediate rail, which supplies the other four DC/DC converters. When the programmed UV threshold is reached on V1, the CMP1 output goes high enabling the 3.3V supply. When the programmed UV threshold is reached on V2, the CMP2 output goes high, enabling the 2.5V supply. Once all the converters have been enabled and power is good, CMP5 goes high, signaling the system that sequencing is complete. GPIO1 is configured to go high 6.4ms after CMP5, disabling the $\overline{\text{KILL}}$ input of the LTC2950-1.

If the $\overline{\text{KILL}}$ input of the LTC2950-1 does not go high within 512ms of initial power-up, the LTC2950-1 disables the supplies by pulling the LTM4600 RUN pin low. Additionally, if the external 12V supply drops below its UV threshold, as measured on V6, CMP6 and GPIO2 go low, causing the LTC2950-1 to disable the LTM4600.

CONCLUSION

The LTC2933 and LTC2936 complement Linear Technology's portfolio of voltage supervisors and Power System Managers. They are ideal for simple, yet flexible, power system monitoring and provide programmability, versatile features, and accurate supervision. ■